Si4031/32 ISM TRANSMITTER

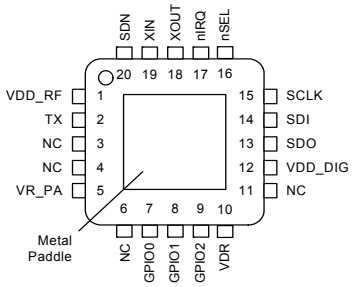
Features

- Frequency Range = 240–930 MHz
- Output Power Range
  - +11 to +20 dBm (Si4032)
  - –8 to +13 dBm (Si4030/31)
- Low Power Consumption
  - (Si4032)
    80 mA @ +20 dBm
    27 mA @ +11 dBm
  - (Si4031)
    28 mA @ +13 dBm
    16 mA @ +1 dBm
- Data Rate = 1 to 128 kbps
- Power Supply = 1.8 to 3.6 V
- Ultra low power shutdown mode
- Wake Up Timer
- Integrated 32 kHz RC or 32 kHz XTAL
- Integrated voltage regulators
- Configurable packet structure
- TX 64 byte FIFO
- Low battery detector
- Temperature sensor and 8-bit ADC
- –40 to +85 °C temperature range
- Integrated voltage regulators
- Frequency hopping capability
- On-chip crystal tuning
- 20-Pin QFN package
- FSK, GFSK, and OOK modulation
- Low BOM
- Power-on-reset (POR)

Ordering Information:
See page 112.

Pin Assignments

Si4031/32



Patents pending

Applications

- Remote control
- Home security & alarm
- Telemetry
- Personal data logging
- Toy control
- Wireless PC peripherals
- Remote meter reading
- Remote keyless entry
- Home automation
- Industrial control
- Sensor networks
- Health monitors

Description

Silicon Laboratories' Si4031/32 highly integrated, single chip wireless ISM transmitter is part of the EZRadioPRO™ family. The EZRadioPRO family includes a complete line of transmitters, receivers, and transceivers allowing the RF system designer to choose the optimal wireless part for their application.

The Si4031/32 offers advanced radio features including continuous frequency coverage from 240–930 MHz with adjustable power output levels of –8 to +13 dBm on the Si4030/31 and +11 to +20 dBm on the Si4032. Power adjustments are made in 3 dB steps. The Si4031/32's high level of integration offers reduced BOM cost while simplifying the overall system design. The Si4032's Industry leading +20 dBm output power ensures extended range and improved link performance.

Additional system features such as an automatic wake-up timer, low battery detector, 64 byte TX FIFO, and automatic packet handling reduce overall current consumption and allow the use of lower-cost system MCUs. An integrated temperature sensor, general purpose ADC, power-on-reset (POR), and GPIOs further reduce overall system cost and size.

The direct digital transmit modulation and automatic PA power ramping ensure precise transmit modulation and reduced spectral spreading ensuring compliance with FCC and ETSI regulations.

Functional Block Diagram

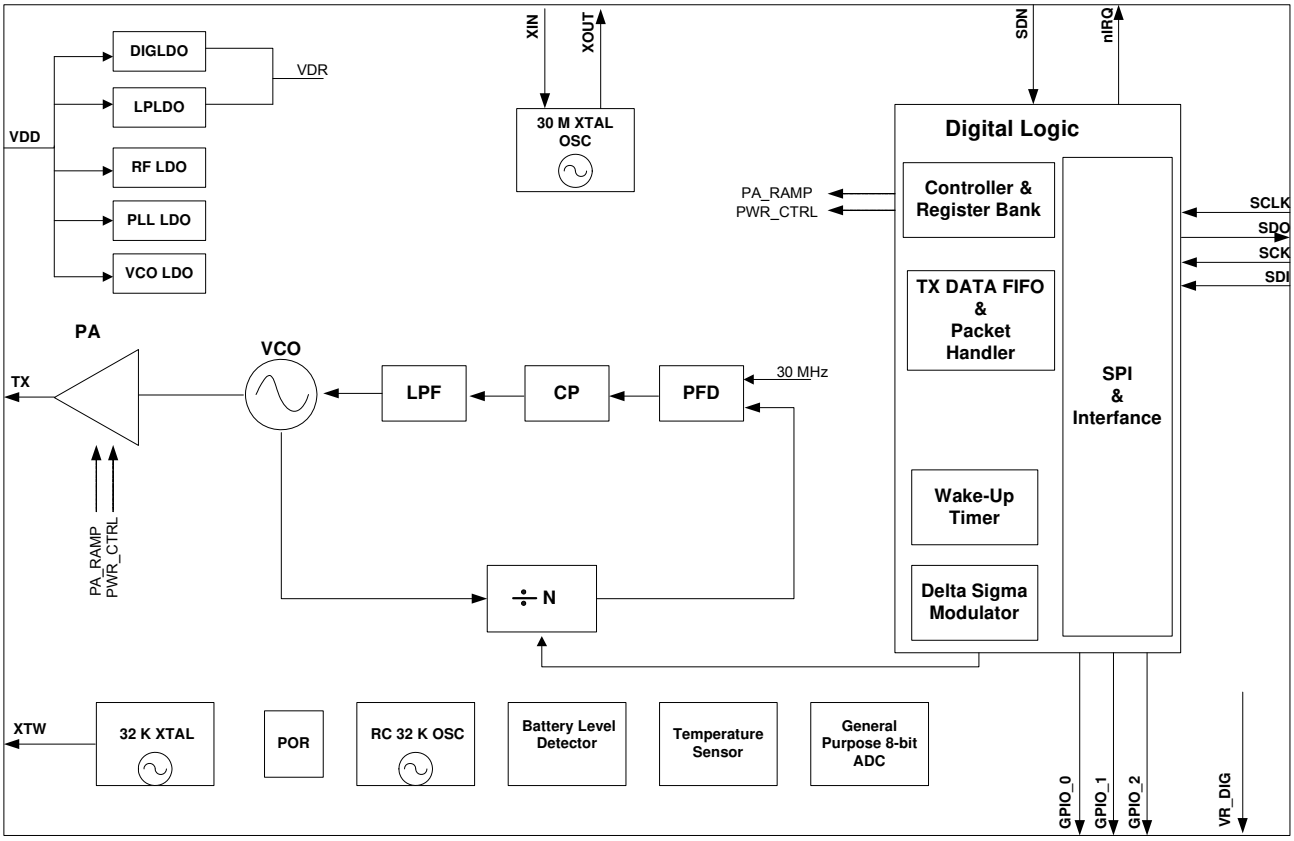


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Table 1. DC Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Supply Voltage Range	V_{dd}		1.8	3.0	3.6	V
Power Saving Modes	$I_{Shutdown}$	RC Oscillator, Main Digital Regulator, and Low Power Digital Regulator OFF[2]	—	10	TBD	nA
	$I_{Standby}$	Low Power Digital Regulator ON (Register values retained) and Main Digital Regulator, and RC Oscillator OFF[1]	—	400	—	nA
	I_{Sleep}	RC Oscillator and Low Power Digital Regulator ON (Register values retained) and Main Digital Regulator OFF[1]	—	800	—	nA
	$I_{Sensor-LBD}$	Main Digital Regulator and Low Battery Detector ON, Crystal Oscillator and all other blocks OFF[2]	—	1	—	µA
	$I_{Sensor-TS}$	Main Digital Regulator and Temperature Sensor ON, Crystal Oscillator and all other blocks OFF[2]	—	1	—	µA
	I_{Ready}	Crystal Oscillator and Main Digital Regulator ON, all other blocks OFF. Crystal Oscillator buffer disabled[1]	—	600	—	µA
TUNE Mode Current	I_{Tune}	Synthesizer and regulators enabled	—	9.5	—	mA
TX Mode Current for Si4032	I_{TX_+20}	txpow[2:0] = 011 (+20 dBm), VDD = 3.3 V	—	80	—	mA
	I_{TX_+11}	txpow[2:0] = 000 (+11 dBm), VDD = 3.3 V	—	27	—	mA
TX Mode Current for Si4031	I_{TX_+13}	txpow[2:0] = 111 (+13 dBm), VDD = 3.3 V	—	28	—	mA
	I_{TX_+1}	txpow[2:0] = 100 (+1 dBm), VDD = 3.3 V	—	16	—	mA

Notes:
1. All specification guaranteed by production test unless otherwise noted.
2. Guaranteed by qualification.

Table 2. Synthesizer AC Electrical Characteristics[1]

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Synthesizer Frequency Range	$F_{SYNTH-LB}$	Low Band	240	—	480	MHz
	$F_{SYNTH-HB}$	High Band	480	—	930	MHz
Synthesizer Frequency Resolution[2]	F_{RES-LB}	Low Band	—	156.25	—	Hz
	F_{RES-HB}	High Band	—	312.5	—	Hz
Reference Frequency	f_{REF}	$f_{crystal}$ / 3	—	10	—	MHz
Reference Frequency Input Level[2]	f_{REF_LV}	When using reference frequency instead of crystal. Measured peak-to-peak (V_{PP})	0.7	—	1.6	V
Synthesizer Settling Time[2]	t_{LOCK}	Measured from leaving Ready mode with XOSC running to any frequency including VCO Calibration	—	200	—	µs
Residual FM[2]	ΔF_{RMS}	Integrated over ±250 kHz bandwidth (500 Hz lower bound of integration)	—	2	4	kHz_{RMS}
Phase Noise[2]	$L\phi(f_M)$	ΔF = 10 kHz	—	–80	—	dBc/Hz
		ΔF = 100 kHz	—	–90	—	dBc/Hz
		ΔF = 1 MHz	—	–115	—	dBc/Hz
		ΔF = 10 MHz	—	–130	—	dBc/Hz

Notes:
1. All specification guaranteed by production test unless otherwise noted.
2. Guaranteed by qualification.

Table 3. Transmitter AC Electrical Characteristics[1]

Parameter	Symbol	Conditions	Min	Typ	Max	Units
TX Frequency Range[1]	$F_{SYNTH-LB}$	Low Band	240	—	480	MHz
	$F_{SYNTH-HB}$	High Band	480	—	930	
FSK Modulation Data Rate[2]	DR_{FSK}		1	—	128	kbps
OOK Modulation Data Rate[2]	DR_{OOK}		1.2	—	40	kbps
Modulation Deviation[1]	Δf	Production tests maximum limit of 320 kHz	±0.625		±320	kHz
Modulation Deviation Resolution	Δf_{RES}		—	0.625	—	kHz
Output Power Range[1](Si4031)	P_{TX}	Power control by txpow[2:0] Register Production test at txpow[2:0] = 11 Tested at 915 MHz	–8	—	+13	dBm
Output Power Range[1](Si4032)	P_{TX}	Power control by txpow[2:0] Register Production test at txpow[2:0] = 11 Tested at 915 MHz	+11	—	+20	dBm
TX RF Output Steps[2]	ΔP_{RF_OUT}	controlled by txpow[2:0] Register	—	3	—	dB
TX RF Output Level Variation vs. Voltage[2]	ΔP_{RF_V}	Measured from VDD=3.6 V to VDD=1.8 V	—	2	—	dB
TX RF Output Level[2] Variation vs. Temperature	ΔP_{RF_TEMP}	–40 to +85 °C	—	2	—	dB
TX RF Output Level Variation vs. Frequency[2]	ΔP_{RF_FREQ}	Measured across any one frequency band	—	1	—	dB
Transmit Modulation Filtering[2]	B*T	Gaussian Filtering Bandwith Time Product	—	0.5	—	
Spurious Emissions[2]	P_{OB-TX1}	P_{OUT} = 11 dBm, Frequencies <1 GHz	—	—	–54	dBm
	P_{OB-TX2}	1–12.75 GHz, excluding harmonics	—	—	–54	dBm
Harmonics[2]	P_{2HARM}	Using Reference Design TX Matching Network and Filter with Max Output Power (+13 dBm). Harmonics reduce linearly with output power	—	—	–42	dBm
	P_{3HARM}		—	—	–42	dBm

Notes:
1. All specification guaranteed by production test unless otherwise noted.
2. Guaranteed by qualification.

Table 4. Auxiliary Block Specifications[1]

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Temperature Sensor Accuracy[2]	TS_A	When calibrated using temp sensor offset register	—	0.5	—	°C
Temperature Sensor Sensitivity[2]	TS_S		—	5	—	mV/°C
Low Battery Detector Resolution[2]	LBD_{RES}		—	50	—	mV
Low Battery Detector Conversion Time[2]	LBD_{CT}		—	250	—	µs
Microcontroller Clock Output Frequency	MC	Configurable to 30 MHz, 15 MHz, 10 MHz, 4 MHz, 3 MHz, 2 MHz, 1 MHz, or 32.768 kHz	32.768K	—	30M	Hz
General Purpose ADC Accuracy[2]	ADC_{ENB}		—	8	—	bit
General Purpose ADC Resolution[2]	ADC_{RES}		—	4	—	mV
Temp Sensor & General Purpose ADC Conversion Time[2]	ADC_{CT}		—	305	—	µsec
30 MHz XTAL Start-Up time	t_{30M}		—	1	—	ms
30 MHz XTAL Cap Resolution[2]	$30M_{RES}$		—	97	—	fF
32 kHz XTAL Start-Up Time[2]	t_{32k}		—	6	—	sec
32 kHz XTAL Accuracy[2]	$32K_{RES}$		—	100	—	ppm
32 kHz RC OSC Accuracy[2]	$32KRC_{RES}$		—	2500	—	ppm
POR Reset Time	t_{POR}		—	16	—	ms
Software Reset Time[2]	t_{soft}		—	100	—	µs

Notes:
1. All specification guaranteed by production test unless otherwise noted.
2. Guaranteed by qualification.

Table 5. Digital IO Specifications (SDO, SDI, SCLK, nSEL, and nIRQ)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Rise Time	T_{RISE}	0.1 x V_{DD} to 0.9 x V_{DD}, C_L= 5 pF	—	—	8	ns
Fall Time	T_{FALL}	0.9 x V_{DD} to 0.1 x V_{DD}, C_L= 5 pF	—	—	8	ns
Input Capacitance	C_{IN}		—	—	1	pF
Logic High Level Input Voltage	V_{IH}		V_{DD} – 0.6	—	—	V
Logic Low Level Input Voltage	V_{IL}			—	0.6	V
Input Current	I_{IN}	0<V_{IN}< V_{DD}	–100	—	100	nA
Logic High Level Output Voltage	V_{OH}	I_{OH}<1 mA source, V_{DD}=1.8 V	V_{DD} – 0.6	—	—	V
Logic Low Level Output Voltage	V_{OL}	I_{OL}<1 mA sink, V_{DD}=1.8 V	—	—	0.6	V
Note: All specification guaranteed by production test unless otherwise noted.						

Table 6. GPIO Specifications (GPIO_0, GPIO_1, and GPIO_2)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Rise Time	T_{RISE}	0.1 x V_{DD} to 0.9 x V_{DD}, C_L= 10 pF, DRV<1:0>=HH	—	—	8	ns
Fall Time	T_{FALL}	0.9 x V_{DD} to 0.1 x V_{DD}, C_L= 10 pF, DRV<1:0>=HH	—	—	8	ns
Input Capacitance	C_{IN}		—	—	1	pF
Logic High Level Input Voltage	V_{IH}		V_{DD} – 0.6	—		V
Logic Low Level Input Voltage	V_{IL}		—	—	0.6	V
Input Current	I_{IN}	0<V_{IN}< V_{DD}	–100	—	100	nA
Input Current If Pullup is Activated	I_{INP}	V_{IL}=0 V	5	—	25	µA
Maximum Output Current	I_{OmaxLL}	DRV<1:0>=LL	0.1	0.5	0.8	mA
	I_{OmaxLH}	DRV<1:0>=LH	0.9	2.3	3.5	mA
	I_{OmaxHL}	DRV<1:0>=HL	1.5	3.1	4.8	mA
	I_{OmaxHH}	DRV<1:0>=HH	1.8	3.6	5.4	mA
Logic High Level Output Voltage	V_{OH}	I_{OH}< I_{Omax} source, V_{DD}=1.8 V	V_{DD} – 0.6	—	—	V
Logic Low Level Output Voltage	V_{OL}	I_{OL}< I_{Omax} sink, V_{DD}=1.8 V	—	—	0.6	V
Note: All specification guaranteed by production test unless otherwise noted.						

Table 7. Absolute Maximum Ratings

Parameter	Value	Unit
V_{DD} to GND	–0.3, +3.6	V
V_{DD} to GND on TX Output Pin	–0.3, +8.0	V
Voltage on Digital Control Inputs	–0.3, V_{DD} + 0.3	V
Voltage on Analog Inputs	–0.3, V_{DD} + 0.3	V
Operating Ambient Temperature Range T_A	–40 to +85	°C
Thermal Impedance θ_{JA}	30	°C/W
Junction Temperature T_J	+125	°C
Storage Temperature Range T_{STG}	–55 to +125	°C

Note: Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at or beyond these ratings in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Caution: ESD sensitive device.
Power Amplifier may be damaged if switched on without proper load or termination connected.

1.1. Definition of Test Conditions

Production Test Conditions:

T_A = +25 °C

V_{DD} = +3.3 VDC

External reference signal (XIN) = 1.0 V_{PP} at 30 MHz, centered around 0.8 VDC

Production test schematic (unless noted otherwise)

All RF input and output levels referred to the pins of the Si4031/32 (not the RF module)

Extreme Test Conditions:

T_A = –40 to +85 °C

V_{DD} = +1.8 to +3.6 VDC

External reference signal (XIN) = 0.7 to 1.6 V_{PP} at 30 MHz centered around 0.8 VDC

Production test schematic (unless noted otherwise)

All RF input and output levels referred to the pins of the Si4031/32 (not the RF module)

Test Notes:

All electrical parameters with Min/Max values are guaranteed by one (or more) of the following test methods. Electrical parameters shown with only Typical values are not guaranteed.

- Guaranteed by design and/or simulation but not tested.
- Guaranteed by Engineering Qualification testing at Extreme Test Conditions.
- Guaranteed by 100% Production Test Screening at Production Test Conditions.

2. Functional Description

The Si4031/32 is a 100% CMOS ISM wireless transmitter with continuous frequency tuning over the complete 240–930 MHz band. The wide operating voltage range of 1.8–3.6 V and low current consumption makes the Si4031/32 and ideal solution for battery powered applications.

A high precision local oscillator (LO) is used for transmit mode. The LO is generated by an integrated VCO and ΔΣ Fractional-N PLL synthesizer. The synthesizer is designed to support configurable data rates, output frequency, frequency deviation, and Gaussian filtering at any frequency between 240–930 MHz. The transmit FSK data is modulated directly into the ΔΣ data stream and can be shaped by a Gaussian low-pass filter to reduce unwanted spectral content.

The Si4032's PA output power can be configured between +11 and +20 dBm in 3 dB steps, while the Si4031's PA output power can be configured between –8 and +13 dBm in 3 dB steps. The PA is single-ended to allow for easy antenna matching and low BOM cost. The PA incorporates automatic ramp-up and ramp-down control to reduce unwanted spectral spreading.

The Si4031/32 is designed to work with a microcontroller, crystal, and a few passives to create a very low cost system. Voltage regulators are integrated on-chip which allow for a wide range of operating supply voltage conditions from +1.8 to +3.6 V. A standard 4-pin SPI bus is used to communicate with the microcontroller. Three configurable general purpose I/Os are available for use to tailor towards the needs of the system. A more complete list of the available GPIO functions is shown in "7. Auxiliary Functions" on page 37 but just to name a few, microcontroller clock output, POR, and specific interrupts. A limited number of passive components are needed to match the PA. Refer to Figure 20, “Si4031 Reference Design Schematic,” on page 48.

2.1. Operating Modes

The Si4031/32 provides several modes of operation which can be used to optimize the power consumption of the device application.

Table 8 summarizes the modes of operation of the Si4031/32. In general, any given mode of operation may be classified as an Active mode or a Power Saving mode. The table indicates which block(s) are enabled (active) in each corresponding mode. With the exception the Shutdown mode, all can be dynamically selected by sending the appropriate commands over the SPI in order to optimize the average current consumption. An “X” in any cell means that, in the given mode of operation, that block can be independently programmed to be either ON or OFF, without noticeably affecting the current consumption. The SPI circuit block includes the SPI interface and the register space. The 32 kHz OSC circuit block includes the 32.768 kHz RC oscillator or 32.768 kHz crystal oscillator, and wake-up timer. AUX (Auxiliary Blocks) includes the temperature sensor, general purpose ADC, and low-battery detector.

Table 8. Operating Modes

Mode Name	Circuit Blocks							
	Digital LDO	SPI	32 kHz OSC	AUX	30 MHz XTAL	PLL	PA	I_{VDD}
Shutdown	OFF (Register contents lost)	OFF	OFF	OFF	OFF	OFF	OFF	10 nA
Standby	ON (Register contents retained)	ON	OFF	OFF	OFF	OFF	OFF	400 nA
Sleep		ON	ON	X	OFF	OFF	OFF	800 nA
Sensor		ON	X	ON	OFF	OFF	OFF	1 µA
Ready		ON	X	X	ON	OFF	OFF	600 µA
Tuning		ON	X	X	ON	ON	OFF	9.5 mA
Transmit		ON	X	X	ON	ON	ON	28 mA*

***Note:** 28 mA at +3 dBm (Si4031).

3. Controller Interface

3.1. Serial Peripheral Interface (SPI)

The Si4031/32 communicates with the host MCU over a 3 wire SPI interface: SCLK, SDI, and nSEL. The host MCU can also read data from internal registers on the SDO output pin. A SPI transaction is a 16-bit sequence which consists of a Read-Write ($\overline{R}$/W) select bit, followed by a 7-bit address field (ADDR), and an 8-bit data field (DATA), as demonstrated in Figure 1. The 7-bit address field supports reading from or writing to one of the 128, 8-bit control registers. The $\overline{R}$/W select bit determines whether the SPI transaction is a write or read transaction. If $\overline{R}$/W = 1, it signifies a WRITE transaction, while $\overline{R}$/W = 0 signifies a READ transaction. The contents (ADDR or DATA) are latched into the Si4031/32 every eight clock cycles. The timing parameters for the SPI interface are shown in Table 9. The SCLK rate is flexible with a maximum rate of 10 MHz.

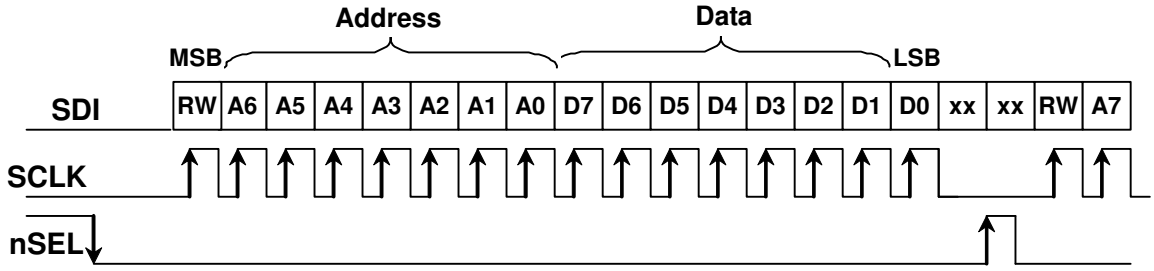
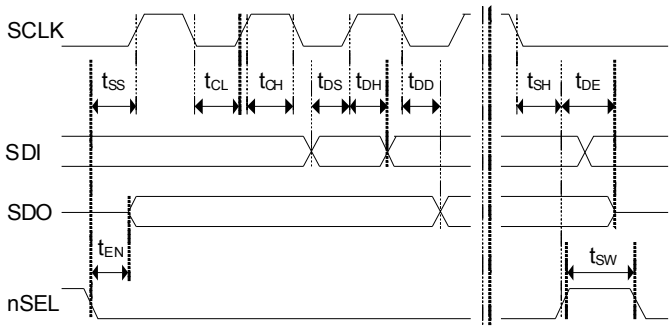


Figure 1. SPI Timing

Table 9. Serial Interface Timing Parameters

Symbol	Parameter	Min (nsec)	Diagram
t_{CH}	Clock high time	40	
t_{CL}	Clock low time	40	
t_{DS}	Data setup time	20	
t_{DH}	Data hold time	20	
t_{DD}	Output data delay time	20	
t_{EN}	Output enable time	20	
t_{DE}	Output disable time	50	
t_{SS}	Select setup time	20	
t_{SH}	Select hold time	50	
t_{SW}	Select high period	80	

To read back data from the Si4031/32, the $\overline{R}$/W bit must be set to 0 followed by the 7-bit address of the register from which to read. The 8 bit DATA field following the 7-bit ADDR field is ignored when $\overline{R}$/W = 0. The next eight negative edge transitions of the SCLK signal will clock out the contents of the selected register. The data read from the selected register will be available on the SDO output pin. The READ function is shown in Figure 2. After the READ function is completed the SDO pin will remain at either a logic 1 or logic 0 state depending on the last data bit clocked out (D0). When nSEL goes high the SDO output pin will be pulled high by internal pullup.

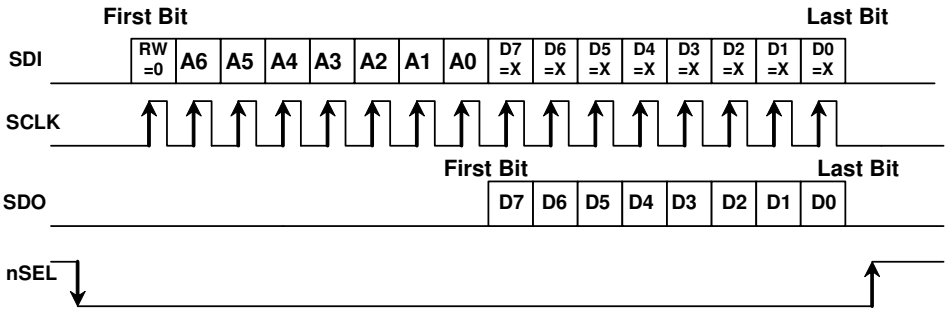


Figure 2. SPI Timing—READ Mode

The SPI interface contains a burst read/write mode which will allows for reading/writing sequential registers without having to re-send the SPI address. When the nSEL bit is held low while continuing to send SCLK pulses, the SPI interface will automatically increment the ADDR and read from/write to the next address. An SPI burst write transaction is demonstrated in Figure 3 and burst read in Figure 2. As long as nSEL is held low, input data will be latched into the Si4031/32 every eight SCLK cycles. A burst read transaction is also demonstrated in Figure 4.

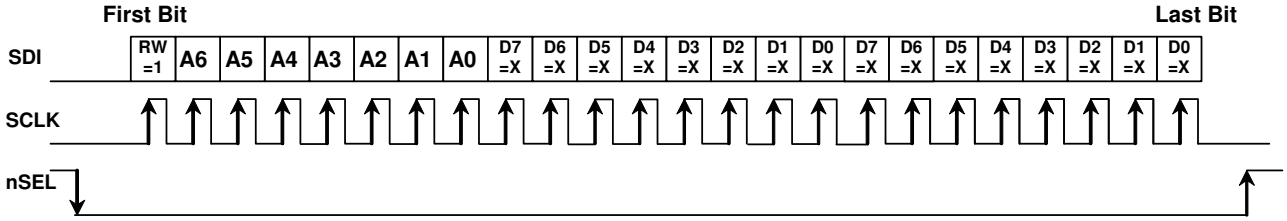


Figure 3. SPI Timing—Burst Write Mode

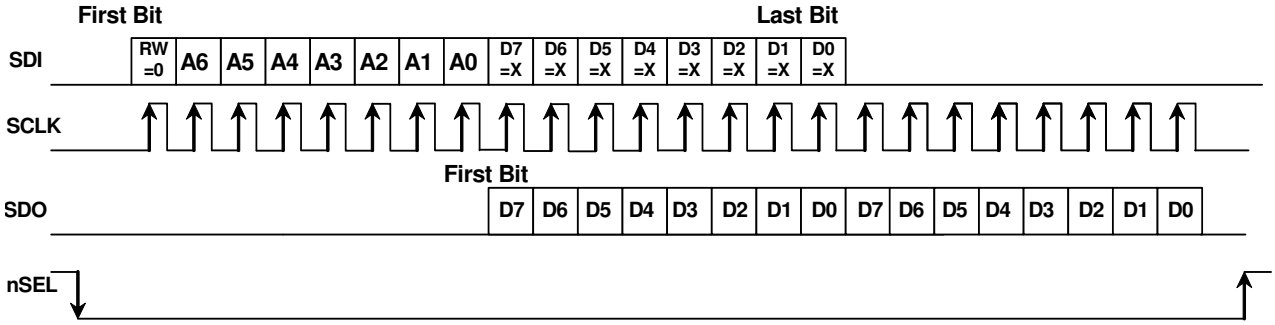


Figure 4. SPI Timing—Burst Read Mode

3.2. Operating Mode Control

There are three primary states in the Si4031/32 radio state machine: SHUTDOWN, IDLE, and TX (see Figure 5). The SHUTDOWN state completely shuts down the radio to minimize current consumption. There are five different configurations/options for the IDLE state which can be selected to optimize the chip to the applications needs. "Register 07h. Operating Mode and Function Control 1" controls which operating mode/state is selected. The TX state may be reached automatically from any of the IDLE states by setting the txon bit in "Register 07h. Operating Mode and Function Control 1". Table 10 shows each of the operating modes with the time required to reach TX mode as well as the current consumption of each mode.

The output of the LPLDO is internally connected in parallel to the output of the main digital regulator (and is available externally at the VR_DIG pin); this common digital supply voltage is connected to all digital circuit blocks, including the digital modem, crystal oscillator, and SPI and register space. The LPLDO has extremely low quiescent current consumption but limited current supply capability; it is used only in the IDLE-STANDBY and IDLE-SLEEP modes.

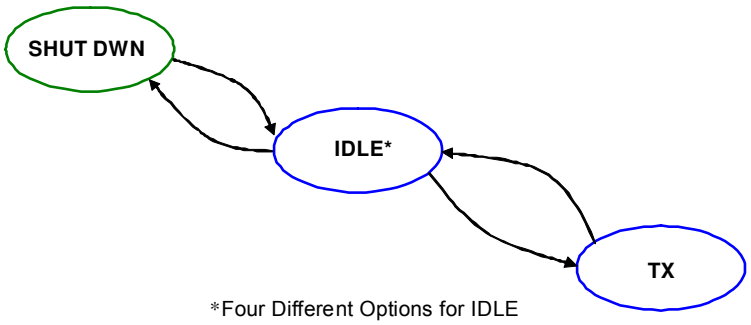


Figure 5. State Machine Diagram

Table 10. Operating Modes

State/Mode	xtal	pll	wt	LBD or TS	Response Time to TX	Current in State /Mode [µA]
Shut Down State	X	X	X	X	16.21 ms	10 nA
Idle States:						
Standby Mode	0	0	0	0	1.21 ms	400 nA
Sleep Mode	0	0	1	0		800 nA
Sensor Mode	0	0	X	1		1 µA
Ready Mode	1	0	X	X	210 µs	600 µA
Tune Mode	1	1	X	X	200 µs	9.5 mA
TX State	1	1	X	X	200 µs	Si4032: 80 mA @ +20 dBm, 27 mA @ +11 dBm Si4031 28 mA @ +13 dBm, 16 mA @ +1 dBm

3.2.1. Shutdown State

The shutdown state is the lowest current consumption state of the device with nominally less than 10 nA of current consumption. The shutdown state may be entered by driving the SDN pin (Pin 20) high. The SDN pin should be held low in all states except the SHUTDOWN state. In the SHUTDOWN state, the contents of the registers are lost and there is no SPI access.

When the chip is connected to the power supply, a POR will be initiated after the falling edge of SDN.

3.2.2. Idle State

There are four different modes in the IDLE state which may be selected by "Register 07h. Operating Mode and Function Control 1". All modes have a tradeoff between current consumption and response time to TX mode. This tradeoff is shown in Table 10. After the POR event, SWRESET, or exiting from the SHUTDOWN state the chip will default to the IDLE-READY mode. After a POR event the interrupt registers must be read to properly enter the SLEEP, SENSOR, or STANDBY mode and to control the 32 kHz clock correctly.

3.2.2.1. STANDBY Mode

STANDBY mode has the lowest current consumption possible with only the LPLDO enabled to maintain the register values. In this mode the registers can be accessed in both read and write mode. The standby mode can be entered by writing 0h to "Register 07h. Operating Mode and Function Control 1". If an interrupt has occurred (i.e., the nIRQ pin = 0) the interrupt registers must be read to achieve the minimum current consumption. Additionally, the ADC should not be selected as an input to the GPIO in this mode as it will cause excess current consumption.

3.2.2.2. SLEEP Mode

In SLEEP mode the LPLDO is enabled along with the Wake-Up-Timer, which can be used to accurately wake-up the radio at specified intervals. See "7.6. Wake-Up Timer" on page 45 for more information on the Wake-Up-Timer. Sleep mode is entered by setting enwt = 1 (40h) in "Register 07h. Operating Mode and Function Control 1". If an interrupt has occurred (i.e., the nIRQ pin = 0) the interrupt registers must be read to achieve the minimum current consumption. Also, the ADC should not be selected as an input to the GPIO in this mode as it will cause excess current consumption.

3.2.2.3. SENSOR Mode

In SENSOR Mode either the Low Battery Detector, Temperature Sensor, or both may be enabled in addition to the LPLDO and Wake-Up-Timer. The Low Battery Detector can be enabled by setting enlbd = 1 and the temperature sensor can be enabled by setting ents = 1 in "Register 07h. Operating Mode and Function Control 1". See "7.4. Temperature Sensor" on page 42 and "7.5. Low Battery Detector" on page 44 for more information on these features. If an interrupt has occurred (i.e., the nIRQ pin = 0) the interrupt registers must be read to achieve the minimum current consumption.

3.2.2.4. READY Mode

READY Mode is designed to give a fast transition time to TX mode with reasonable current consumption. In this mode the Crystal oscillator remains enabled reducing the time required to switch to the TX mode by eliminating the crystal start-up time. Ready mode is entered by setting xton = 1 in "Register 07h. Operating Mode and Function Control 1". To achieve the lowest current consumption state the crystal oscillator buffer should be disabled. This is done by setting "Register 62h. Crystal Oscillator/Power-on-Reset Control" to a value of 02h. To exit ready mode, bufovr (bit 1) of this register must be set back to 0.

3.2.2.5. TUNE Mode

In TUNE Mode the PLL remains enabled in addition to the other blocks enabled in the IDLE modes. This will give the fastest response to TX mode as the PLL will remain locked but it results in the highest current consumption. This mode of operation is designed for Frequency Hopping Systems (FHS). Tune mode is entered by setting pllon = 1 in "Register 07h. Operating Mode and Function Control 1". It is not necessary to set xton to 1 for this mode, the internal state machine automatically enables the crystal oscillator.

3.2.3. TX State

The TX state may be entered from any of the IDLE modes when the txon bit is set to 1 in "Register 07h. Operating Mode and Function Control 1". A built-in sequencer takes care of all the actions required to transition between states from enabling the crystal oscillator to ramping up the PA to prevent unwanted spectral splatter. The following sequence of events will occur automatically when going from STANDBY mode to TX mode by setting the txon bit.

1. Enable the Main Digital LDO and the Analog LDOs.
2. Start up crystal oscillator and wait until ready (controlled by timer).
3. Enable PLL.
4. Calibrate VCO (this action is skipped when the vcocal bit is “0”, default value is “1”).
5. Wait until PLL settles to required transmit frequency (controlled by timer).
6. Activate Power Amplifier and wait until power ramping is completed (controlled by timer).
7. Transmit Packet.

The first few steps may be eliminated depending on which IDLE mode the chip is configured to prior to setting the txon bit. By default, the VCO and PLL are calibrated every time the PLL is enabled. If the ambient temperature is constant and the same frequency band is being used these functions may be skipped by setting the appropriate bits in "Register 55h. Calibration Control".

3.2.4. Device Status

Add	R/W	Function/Description	D7	D6	D5	D4	D3	D2	D1	D0	POR Def.
02	R	Device Status	ffovfl	ffunfl	Reserved	Reserved			cps[1]	cps[0]	—

The operational status of the chip can be read from "Register 02h. Device Status".

3.3. Interrupts

The Si4031/32 is capable of generating an interrupt signal when certain events occur. The chip notifies the microcontroller that an interrupt event has been detected by setting the nIRQ output pin LOW = 0. This interrupt signal will be generated when any one (or more) of the interrupt events (corresponding to the Interrupt Status bits) shown below occur. The nIRQ pin will remain low until the microcontroller reads the Interrupt Status Register(s) (Registers 03h–04h) containing the active Interrupt Status bit; the nIRQ output signal will then be reset until the next change in status is detected. All of the interrupts must be enabled by the corresponding enable bit in the Interrupt Enable Registers (Registers 05h–06h). All enabled interrupt bits will be cleared when the microcontroller reads the interrupt status register. If the interrupt is not enabled when the event occurs inside of the chip it will not trigger the nIRQ pin, but the status may still be read correctly at anytime in the Interrupt Status registers.

Add	R/W	Function/Description	D7	D6	D5	D4	D3	D2	D1	D0	POR Def.
03	R	Interrupt Status 1	ifferr	itxffafull	itxffaem	Reserved	iext	ipksent	Reserved	Reserved	—
04	R	Interrupt Status 2	Reserved	Reserved	Reserved	Reserved	iwut	ilbd	ichiprdy	ipor	—
05	R/W	Interrupt Enable 1	enfferr	entxffafull	entxffaem	Reserved	enext	enpksent	Reserved	Reserved	00h
06	R/W	Interrupt Enable 2	Reserved	Reserved	Reserved	Reserved	enwut	enlbd	enchiprdy	enpor	01h

See “Register 03h. Interrupt/Status 1,” on page 60 and “Register 04h. Interrupt/Status 2,” on page 62 for a complete list of interrupts.

3.4. Device Code

The device version code is readable from "Register 01h. Version Code (VC)". This is a read only register.

Add	R/W	Function/Description	D7	D6	D5	D4	D3	D2	D1	D0	POR Def.	Notes
01	R	Device Version	0	0	0	vc[4]	vc[3]	vc[2]	vc[1]	vc[0]	00h	DV

3.5. System Timing

The system timing for TX mode is shown in Figure 6. The timing is shown transitioning from STANDBY mode to TX mode and going automatically through the built-in sequencer of required steps. If a small range of frequencies is being used and the temperature range is fairly constant a calibration may only be needed at the initial power up of the device. The relevant system timing registers are shown below.

Add	R/W	Function/Description	D7	D6	D5	D4	D3	D2	D1	D0	POR Def.
53	R/W	PLL Tune Time	pllts[4:0]					pllt0[2:0]			45h
54	R/W	Reserved 1	X	X	X	X	X	X	X	X	00h
55	R/W	Calibration Control		xtal-starthalf	adccal-done	enrcfcal	rccal	vco-caldp	vcocal	skip-vco	04h

The VCO will automatically calibrate at every frequency change or power up. The VCO CAL may also be forced by setting the vcocal bit. The 32.768 kHz RC oscillator is also automatically calibrated but the calibration may also be forced. The enrcfcal will enable the RC Fine Calibration which will occur every 30 seconds. The rccal bit will force a complete calibration of the RC oscillator which will take approximately 2 ms. The PLL T0 time is to allow for bias settling of the VCO, the default for this should be adequate. The PLL TS time is for the settling time of the PLL, which has a default setting of 200 µs. This setting should be adequate for most applications but may be reduced if small frequency jumps are used. For more information on the PLL register configuration options, see “Register 53h. PLL Tune Time,” on page 89 and “Register 55h. Calibration Control,” on page 90.

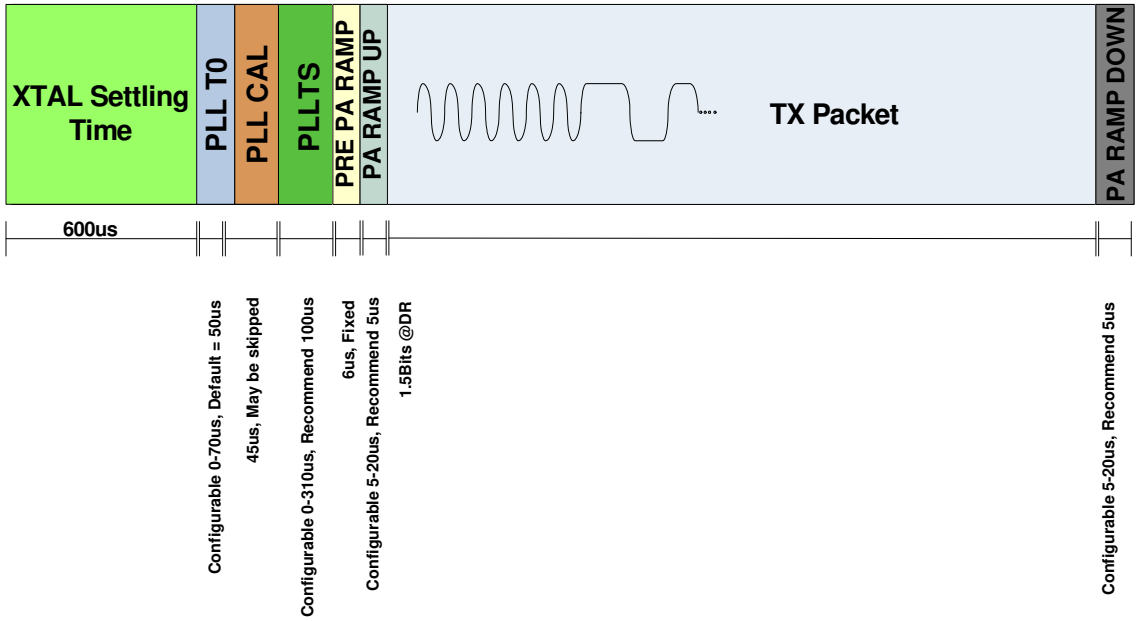


Figure 6. TX Timing

3.6. Frequency Control

For calculating the necessary frequency register settings it is recommended that customers use the easy control window in Silicon Labs' Wireless Design Suite (WDS) or the Excel Calculator available on the product website. These methods offer a simple method to quickly determine the correct settings based on the application requirements. The following information can be used to calculated these values manually.

3.6.1. Frequency Programming

In order to transmit an RF signal, the desired channel frequency, fcarrier, must be programmed into the Si4031/32. Note that this frequency is the center frequency of the desired channel and not an LO frequency. The carrier frequency is generated by a Fractional-N Synthesizer, using 10 MHz both as the reference frequency and the clock of the (3rd order) ΔΣ modulator. This modulator uses modulo 64000 accumulators. This design was made to obtain the desired frequency resolution of the synthesizer. The overall division ratio of the feedback loop consist of an integer part (N) and a fractional part (F).In a generic sense, the output frequency of the synthesizer is:

$$f_{OUT} = 10MHz \times (N + F)$$

The fractional part (F) is determined by three different values, Carrier Frequency (fc[15:0]), Frequency Offset (fo[8:0]), and Frequency Modulation (fd[7:0]). Due to the fine resolution and high loop bandwidth of the synthesizer, FSK modulation is applied inside the loop and is done by varying F according to the incoming data; this is discussed further in "3.6.4. Frequency Deviation" on page 24. Also, a fixed offset can be added to fine-tune the carrier frequency and counteract crystal tolerance errors. For simplicity assume that only the fc[15:0] register will determine the fractional component. The equation for selection of the carrier frequency is shown below:

$$f_{carrier} = 10MHz \times (hbsel + 1) \times (N + F)$$

$$f_{TX} = 10MHz * (hbsel + 1) * (fb[4:0] + 24 + \frac{fc[15:0]}{64000})$$

Add	R/W	Function/Description	D7	D6	D5	D4	D3	D2	D1	D0	POR Def.
73	R/W	Frequency Offset 1	fo[7]	fo[6]	fo[5]	fo[4]	fo[3]	fo[2]	fo[1]	fo[0]	00h
74	R/W	Frequency Offset 2							fo[9]	fo[8]	00h
75	R/W	Frequency Band Select		sbsel	hbsel	fb[4]	fb[3]	fb[2]	fb[1]	fb[0]	35h
76	R/W	Nominal Carrier Frequency 1	fc[15]	fc[14]	fc[13]	fc[12]	fc[11]	fc[10]	fc[9]	fc[8]	BBh
77	R/W	Nominal Carrier Frequency 0	fc[7]	fc[6]	fc[5]	fc[4]	fc[3]	fc[2]	fc[1]	fc[0]	80h

The integer part (N) is determined by fb[4:0]. Additionally, the output frequency can be halved by connecting a ÷2 divider to the output. This divider is not inside the loop and is controlled by the hbsel bit in "Register 75h. Frequency Band Select". This effectively partitions the entire 240–930 MHz frequency range into two separate bands: High Band (HB) for hbsel = 1, and Low Band (LB) for hbsel = 0. The valid range of fb[4:0] is from 0 to 23. If a higher value is written into the register, it will default to a value of 23. The integer part has a fixed offset of 24 added to it as shown in the formula above. Table 11 demonstrates the selection of fb[4:0] for the corresponding frequency band.

After selection of the fb (N) the fractional component may be solved with the following equation:

$$fc[15:0] = \left(\frac{f_{TX}}{10MHz * (hbsel + 1)} - fb[4:0] - 24 \right) * 64000$$

fb and fc are the actual numbers stored in the corresponding registers.

Table 11. Frequency Band Selection

fb[4:0] Value	N	Frequency Band	
		hbsel=0	hbsel=1
0	24	240–249.9 MHz	480–499.9 MHz
1	25	250–259.9 MHz	500–519.9 MHz
2	26	260–269.9 MHz	520–539.9 MHz
3	27	270–279.9 MHz	540–559.9 MHz
4	28	280–289.9 MHz	560–579.9 MHz
5	29	290–299.9 MHz	580–599.9 MHz
6	30	300–309.9 MHz	600–619.9 MHz
7	31	310–319.9 MHz	620–639.9 MHz
8	32	320–329.9 MHz	640–659.9 MHz
9	33	330–339.9 MHz	660–679.9 MHz
10	34	340–349.9 MHz	680–699.9 MHz
11	35	350–359.9 MHz	700–719.9 MHz
12	36	360–369.9 MHz	720–739.9 MHz
13	37	370–379.9 MHz	740–759.9 MHz
14	38	380–389.9 MHz	760–779.9 MHz
15	39	390–399.9 MHz	780–799.9 MHz
16	40	400–409.9 MHz	800–819.9 MHz
17	41	410–419.9 MHz	820–839.9 MHz
18	42	420–429.9 MHz	840–859.9 MHz
19	43	430–439.9 MHz	860–879.9 MHz
20	44	440–449.9 MHz	880–899.9 MHz
21	45	450–459.9 MHz	900–919.9 MHz
22	46	460–469.9 MHz	920–930.0 MHz
23	47	470–479.9 MHz	—

The chip will automatically shift the frequency of the Synthesizer down by 937.5 kHz (30 MHz ÷ 32) to achieve the correct Intermediate Frequency (IF).

3.6.2. Easy Frequency Programming for FHSS

While Registers 73h–77h may be used to program the carrier frequency of the Si4031/32, it is often easier to think in terms of “channels” or “channel numbers” rather than an absolute frequency value in Hz. Also, there may be some timing-critical applications (such as for Frequency Hopping Systems) in which it is desirable to change frequency by programming a single register. Once the channel step size is set, the frequency may be changed by a single register corresponding to the channel number. A nominal frequency is first set using Registers 73h–77h, as described above. Registers 79h and 7Ah are then used to set a channel step size and channel number, relative to the nominal setting. The Frequency Hopping Step Size (fhs[7:0]) is set in increments of 10 kHz with a maximum channel step size of 2.56 MHz. The Frequency Hopping Channel Select Register then selects channels based on multiples of the step size.

$$F_{carrier} = Fnom + fhs[7:0] \times (fhch[7:0] \times 10kHz)$$

For example: if the nominal frequency is set to 900 MHz using Registers 73h–77h and the channel step size is set to 1 MHz using "Register 7Ah. Frequency Hopping Step Size". For example, if the "Register 79h. Frequency Hopping Channel Select" is set to 5d, the resulting carrier frequency would be 905 MHz. Once the nominal frequency and channel step size are programmed in the registers, it is only necessary to program the fhch[7:0] register in order to change the frequency.

Add	R/W	Function/Description	D7	D6	D5	D4	D3	D2	D1	D0	POR Def.
79	R/W	Frequency Hopping Channel Select	fhch[7]	fhch[6]	fhch[5]	fhch[4]	fhch[3]	fhch[2]	fhch[1]	fhch[0]	00h
7A	R/W	Frequency Hopping Step Size	fhs[7]	fhs[6]	fhs[5]	fhs[4]	fhs[3]	fhs[2]	fhs[1]	fhs[0]	00h

3.6.3. Automatic Frequency Change

If registers 79h or 7Ah are changed in TX mode, the state machine will automatically transition the chip back to tune and change the frequency. This feature is useful to reduce the number of SPI commands required in a Frequency Hopping System. This in turn reduces microcontroller activity, reducing current consumption.

3.6.4. Frequency Deviation

The peak frequency deviation is configurable from ±1 to ±320 kHz. The Frequency Deviation (Δf) is controlled by the Frequency Deviation Register (fd), address 71 and 72h, and is independent of the carrier frequency setting. When enabled, regardless of the setting of the hbsel bit (high band or low band), the resolution of the frequency deviation will remain in increments of 625 Hz. When using frequency modulation the carrier frequency will deviate from the nominal center channel carrier frequency by ±Δf:

$$\Delta f = fd[8:0] \times 625Hz$$

$$fd[8:0] = \frac{\Delta f}{625Hz} \quad \Delta f = \text{peak deviation}$$

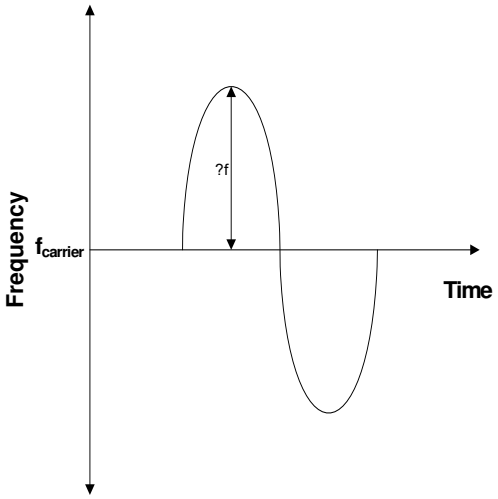


Figure 7. Frequency Deviation

The previous equation should be used to calculate the desired frequency deviation. If desired, frequency modulation may also be disabled in order to obtain an unmodulated carrier signal at the channel center frequency; see "4.1. Modulation Type" on page 27 for further details.

Add	R/W	Function/Description	D7	D6	D5	D4	D3	D2	D1	D0	POR Def.
71	R/W	Modulation Mode Control 2	trclk[1]	trclk[0]	dtmod[1]	dtmod[0]	eninv	fd[8]	modtyp[1]	modtyp[0]	00h
72	R/W	Frequency Deviation	fd[7]	fd[6]	fd[5]	fd[4]	fd[3]	fd[2]	fd[1]	fd[0]	43h

3.6.5. Frequency Offset Adjustment

A frequency offset can be adjusted manually by fo[9:0] in registers 73h and 74h. The frequency offset adjustment is implemented by shifting the Synthesizer Local Oscillator frequency. This register is a signed register so in order to get a negative offset you will need to take the twos complement of the positive offset number. The offset can be calculated by the following:

$$DesiredOffset = 156.25Hz \times (hbsel + 1) \times fo[9:0]$$

$$fo[9:0] = \frac{DesiredOffset}{156.25Hz \times (hbsel + 1)}$$

The adjustment range in high band is: ±160 kHz, and adjustment range in low band is: ±80 kHz. For example to compute an offset of +50 kHz in high band mode fo[9:0] should be set to 0A0h. For an offset of –50 kHz in high band mode the fo[9:0] register should be set to 360h.

Add	R/W	Function/Description	D7	D6	D5	D4	D3	D2	D1	D0	POR Def.	Notes
73	R/W	Frequency Offset	fo[7]	fo[6]	fo[5]	fo[4]	fo[3]	fo[2]	fo[1]	fo[0]	00h	73
74	R/W	Frequency Offset							fo[9]	fo[8]	00h	

3.6.6. TX Data Rate Generator

The data rate is configurable between 1–128 kbps. For data rates below 30 kbps the"txdtrtscale" bit in register 70h should be set to 1. When higher data rates are used this bit should be set to 0**.**

The TX date rate is determined by the following formula:

$$DR\_TX = \frac{txdr[15:0] \times 1MHz}{2^{16+5 \cdot txdtrtscale}}$$

$$txdr[15:0] = \frac{DR\_TX \times 2^{16+5 \cdot txdtrtscale}}{1MHz}$$

The txdr register may be found in the following registers.

Add	R/W	Function/Description	D7	D6	D5	D4	D3	D2	D1	D0	POR Def.
6E	R/W	TX Data Rate 1	txdr[15]	txdr[14]	txdr[13]	txdr[12]	txdr[11]	txdr[10]	txdr[9]	txdr[8]	0Ah
6F	R/W	TX Data Rate 0	txdr[7]	txdr[6]	txdr[5]	txdr[4]	txdr[3]	txdr[2]	txdr[1]	txdr[0]	AAh

4. Modulation Options

4.1. Modulation Type

The Si4031/32 supports three different modulation options: Gaussian Frequency Shift Keying (GFSK), Frequency Shift Keying (FSK), and On-Off Keying (OOK). GFSK is the recommended modulation type as it provides the best performance and cleanest modulation spectrum. Figure 8 demonstrates the difference between FSK and GFSK for a Data Rate of 64 kbps. The time domain plots demonstrate the effects of the Gaussian filtering. The frequency domain plots demonstrate the spectral benefit of GFSK over FSK. The type of modulation is selected with the modtyp[1:0] bits in "Register 71h. Modulation Mode Control 2". Note that it is also possible to obtain an unmodulated carrier signal by setting modtyp[1:0] = 00.

modtyp[1:0]	Modulation Source
00	Unmodulated Carrier
01	OOK
10	FSK
11	GFSK (enable TX Data CLK when direct mode is used)

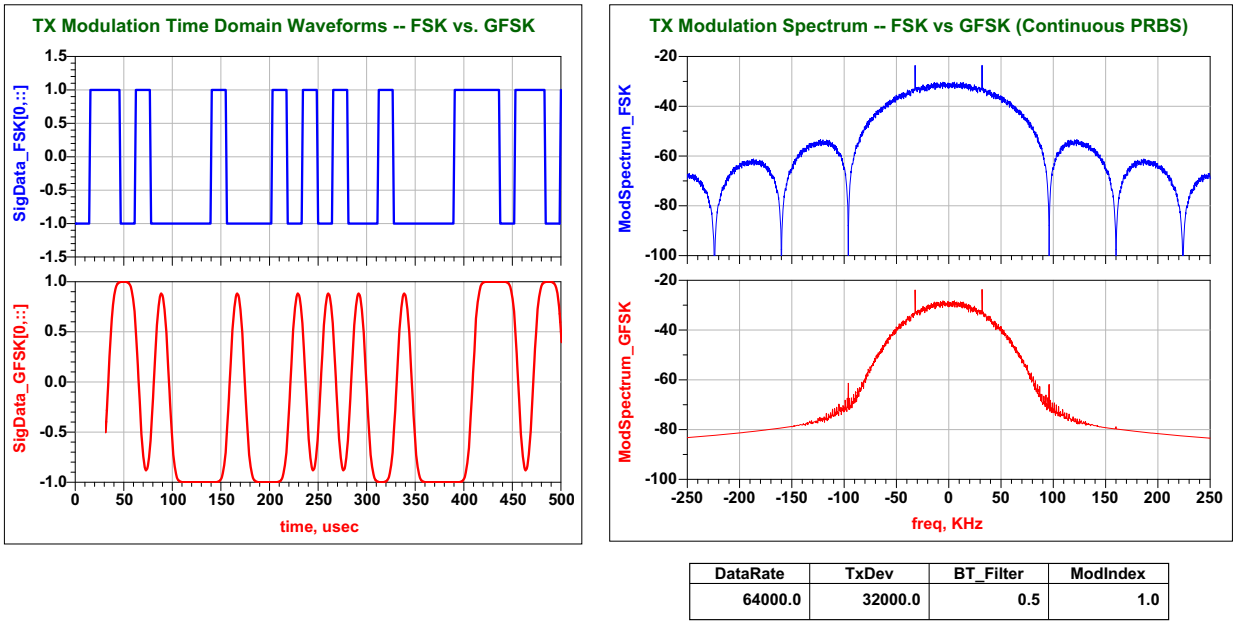


Figure 8. FSK vs GFSK Spectrums

4.2. Modulation Data Source

The Si4031/32 may be configured to obtain its modulation data from one of three different sources: FIFO mode, Direct Mode, and from a PN9 mode. Furthermore, in Direct Mode, the TX modulation data may be obtained from several different input pins. These options are set through the dtmod[1:0] field in "Register 71h. Modulation Mode Control 2".

Add	R/W	Function/Description	D7	D6	D5	D4	D3	D2	D1	D0	POR Def.
71	R/W	Modulation Mode Control 2	trclk[1]	trclk[0]	dtmod[1]	dtmod[0]	eninv	fd[8]	modtyp[1]	modtyp[0]	23h

dtmod[1:0]	Modulation Source
00	Direct Mode using TX_Data via GPIO pin (GPIO needs programming accordingly also)
01	Direct Mode using TX_Data via SDI pin (only when nSEL is high)
10	FIFO Mode
11	PN9 (internally generated)

4.3. FIFO Mode

In FIFO mode, the integrated FIFO is used to transmit the data. The FIFO is accessed via "Register 7Fh. FIFO Access" with burst write capability. The FIFO may be configured specific to the application packet size, etc. (see "6. Data Handling and Packet Handler" on page 33 for further information).

When in FIFO mode the chip will automatically exit the TX State when the *ipksent* interrupt occurs. The chip will return to any of the other states based on the settings in "Register 07h. Operating Mode and Function Control 1". For instance, if both the txon and pllon bits are set, the chip will transmit all of the contents of the FIFO and the ipksent interrupt will occur. When this event occurs the chip will clear the txon bit and return to pllon or Tune Mode. If no other bits are set in register 07h besides txon initially then the chip will return to the Idle state.

4.4. Direct Mode

For legacy systems that have packet handling within an MCU or other baseband chip, it may not be desirable to use the FIFO. For this scenario, a Direct Mode is provided which bypasses the FIFOs entirely. In Direct Mode, the TX modulation data is applied to an input pin of the chip and processed in “real time” (i.e., not stored in a register for transmission at a later time). There are various configurations for choosing which pin is used for the TX Data. Furthermore, an additional input pin is required for the TX Data Clock if GFSK modulation is desired (only the TX Data input pin is required for FSK). Two options for the source of the TX Data are available in the dtmod[1:0] field, and various configurations for the source of the TX Data Clock may be selected through the trclk[1:0] field.

trclk[1:0]	TX Data Clock Configuration
00	No TX Clock (only for FSK)
01	TX Data Clock is available via GPIO (GPIO needs programming accordingly as well)
10	TX Data Clock is available via SDO pin (only when nSEL is high)
11	TX Data Clock is available via the nIRQ pin

The eninv bit in Address 71h will invert the TX Data for testing purposes.

4.5. PN9 Mode

In this mode the TX Data is generated internally using a pseudorandom (PN9 sequence) bit generator. The primary purpose of this mode is for use as a test mode to observe the modulated spectrum without having to load/provide data.

4.6. Synchronous vs. Asynchronous

In Asynchronous mode no clock is used to synchronize the data to the internal modulator. This mode can only be used with FSK. The advantage of this mode that it saves a microcontroller pin because no data clock is required. The disadvantage is that you don't get the clean spectrum and limited BW of GFSK. If Asynchronous FSK is used the TX_DR register should be set to its maximum value.

5. Internal Functional Blocks

This section provides an overview some of the key blocks of the internal radio architecture.

5.1. Synthesizer

An integrated Sigma Delta (ΣΔ) Fractional-N PLL synthesizer capable of operating from 240–930 MHz is provided on-chip. Using a ΣΔ synthesizer has many advantages; it provides large amounts of flexibility in choosing data rate, deviation, channel frequency, and channel spacing. The transmit modulation is applied directly to the loop in the digital domain through the fractional divider which results in very precise accuracy and control over the transmit deviation.

The PLL and Δ-Σ modulator scheme is designed to support any desired frequency and channel spacing in the range from 240–930 MHz with a frequency resolution of 156.25 Hz (Low band) or 312.5 Hz (High band). The transmit data rate can be programmed between 1–128 kbps, and the frequency deviation can be programmed between ±1–160 kHz. These parameters may be adjusted via registers as shown in "3.6. Frequency Control" on page 22.

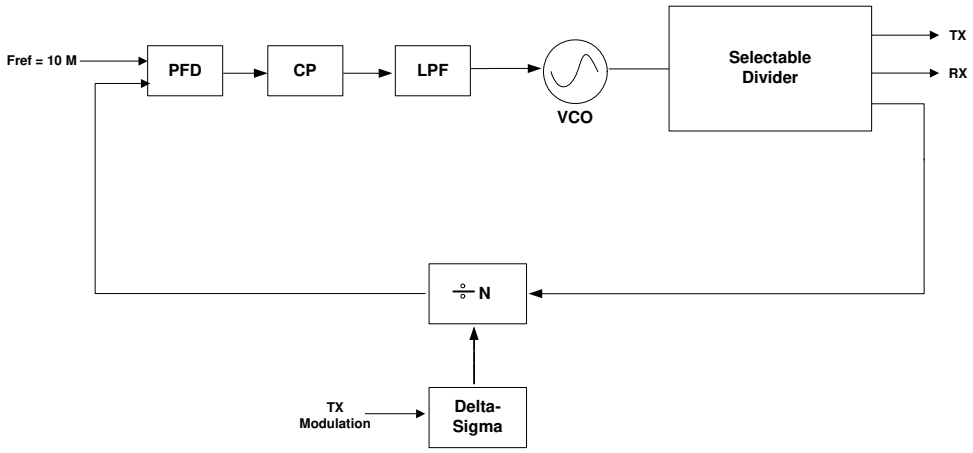


Figure 9. PLL Synthesizer Block Diagram

The reference frequency to the PLL is 10 MHz. The PLL utilizes a differential L-C VCO, with integrated on-chip spiral inductors. The output of the VCO is followed by a configurable divider which will divide down the signal to the desired output frequency band. The modulus of this divider stage is controlled dynamically by the output from the Δ-Σ modulator. The tuning resolution of the Δ-Σ modulator is determined largely by the over-sampling rate and the number of bits carried internally. The tuning resolution is sufficient to tune to the commanded frequency with a maximum accuracy of 312.5 Hz anywhere in the range between 240–930 MHz.

5.1.1. VCO

The output of the VCO is automatically divided down to the correct output frequency depending on the hbsel and fb[4:0] fields in "Register 75h. Frequency Band Select". A 2X VCO is utilized to help avoid problems due to frequency pulling, especially when turning on the integrated Power Amplifier. In receive mode, the LO frequency is automatically shifted downwards (without reprogramming) by the IF frequency of 937.5 kHz, allowing transmit operation on the same frequency. The VCO integrates the resonator inductor, tuning varactor, so no external VCO components are required.

The VCO uses capacitance bank to cover the wide frequency range specified. The capacitance bank will automatically be calibrated every time the synthesizer is enabled. In certain fast hopping applications this might not be desirable so the VCO calibration may be skipped by setting the appropriate register.

5.2. Power Amplifier

The Si4032 contains an internal integrated power amplifier (PA) capable of transmitting at output levels between +11 to +20 dBm. The output power is programmable in 3 dB steps through the txpow[2:0] field in "Register 6Dh. TX Power".

The Si4031 contains a PA which is capable of transmitting output levels between –8 to +13 dBm.

The PA design is single-ended and is implemented as a two stage class CE amplifier with efficiency in the range of 45–50% while transmitting at maximum power. The efficiency drops to approximately 20% when operating at the lowest power steps. Due to the high efficiency a simple filter is required on the board to filter the harmonics. The PA output is ramped up and down to prevent unwanted spectral splatter.

5.2.1. Output Power Selection

With the Si4032, the output power is configurable in 3 dB steps from +11 to +20 dBm with the txpow[2:0] field in "Register 6Dh. TX Power". The PA output is ramped up and down to prevent unwanted spectral splatter.

Extra output power can allow use of a cheaper, smaller antenna reducing the overall BOM cost. The higher power setting of the chip achieves maximum possible range, but of course comes at the cost of higher TX current consumption. However, depending on the duty cycle of the system, the effect on battery life may be insignificant. Contact Silicon Labs Support for help in evaluating this tradeoff.

The +13 dBm output power of the Si4031 is targeted at systems that require lower output power. The PA still offers high efficency and a range of output power from –8 to +13 dBm.

Add	R/W	Function/Description	D7	D6	D5	D4	D3	D2	D1	D0	POR Def.
6D	R/W	TX Power						txpow[2]	txpow[1]	txpow[0]	07h

txpow[1:0]	Si4032 Output Power
00	+11 dBm
01	+14 dBm
10	+17 dBm
11	+20 dBm

txpow[2:0]	Si4031 Output Power
000	–8 dBm
001	–5 dBm
010	–2 dBm
011	+1 dBm
100	+4 dBm
101	+7 dBm
110	+10 dBm
111	+13 dBm

5.3. Crystal Oscillator

The Si4031/32 includes an integrated 30 MHz crystal oscillator with a fast start-up time of less than 600 µs when a suitable parallel resonant crystal is used. The design is differential with the required crystal load capacitance integrated on-chip to minimize the number of external components. By default, all that is required off-chip is the 30 MHz crystal blank.

The crystal load capacitance can be digitally programmed to accommodate crystals with various load capacitance requirements and to slightly adjust the frequency of the crystal oscillator. The tuning of the crystal load capacitance is programmed through the xlc[6:0] field of "Register 09h. 30 MHz Crystal Oscillator Load Capacitance". The total internal capacitance is 12.5 pF and is adjustable in approximately 127 steps (97fF/step). The xtalshift bit is a course shift in frequency but is not binary with xlc[6:0].

The crystal load capacitance can be digitally programmed to accommodate crystals with various load capacitance requirements and to slightly adjust the frequency of the crystal oscillator. This latter function can be used to compensate for crystal production tolerances. Utilizing the on-chip temperature sensor and suitable control software even the temperature dependency of the crystal can be canceled.

The crystal load capacitance is programmed using register 09h. The typical value of the total on-chip (internal) capacitance Cint can be calculated as follows:

Cint = 1.8 pF + 0.085 pF x xlc[6:0] + 3.7 pF x xtalshift

Note that the course shift bit xtalshift is not binary with xlc[6:0]. The total load capacitance Cload seen by the crystal can be calculated by adding the sum of all external parasitic PCB capacitances Cext to Cint. If the maximum value of Cint (16.3 pF) is not sufficient, an external capacitor can be added for exact tuning. See more on this, calculating Cext and crystal selection guidelines in "10. Application Notes" on page 55.

If AFC is disabled then the synthesizer frequency may be further adjusted by programming the Frequency Offset field fo[9:0]in "Register 73h. Frequency Offset 1" and "Register 74h. Frequency Offset 2", as discussed in "3.6. Frequency Control" on page 22.

The crystal oscillator frequency is divided down internally and may be output to the microcontroller through one of the GPIO pins for use as the System Clock. In this fashion, only one crystal oscillator is required for the entire system and the BOM cost is reduced. The available clock frequencies (i.e., internal division ratios) and the GPIO configuration are discussed further in "7.2. Microcontroller Clock" on page 38.

The Si4031/32 may also be driven with an external 30 MHz clock signal through the XIN pin.

Add	R/W	Function/Description	D7	D6	D5	D4	D3	D2	D1	D0	POR Def.
09	R/W	Crystal Oscillator Load Capacitance	xtalshift	xlc[6]	xlc[5]	xlc[4]	xlc[3]	xlc[2]	xlc[1]	xlc[0]	40h

5.4. Regulators

There are a total of six regulators integrated onto the Si4031/32. With the exception of the IF and Digital all regulators are designed to operate with only internal decoupling. The IF and Digital regulators both require an external 1 µF decoupling capacitor. All of the regulators are designed to operate with an input supply voltage from +1.8 to +3.6 V, and produce a nominal regulated output voltage of +1.7 V ±5%. The internal circuitry nominally operates from this regulated +1.7 V supply. The output stage of the of PA is not connected internally to a regulator and is connected directly to the battery voltage.

A supply voltage should only be connected to the VDD pins. No voltage should be forced on the IF or DIG regulator outputs.

6. Data Handling and Packet Handler

6.1. TX FIFO

A 64 byte FIFO is integrated into the chip for TX, as shown in Figure 10. "Register 7Fh. FIFO Access" is used to access the FIFO. A burst write, as described in "3.1. Serial Peripheral Interface (SPI)" on page 15, to address 7Fh will write data to the TX FIFO.

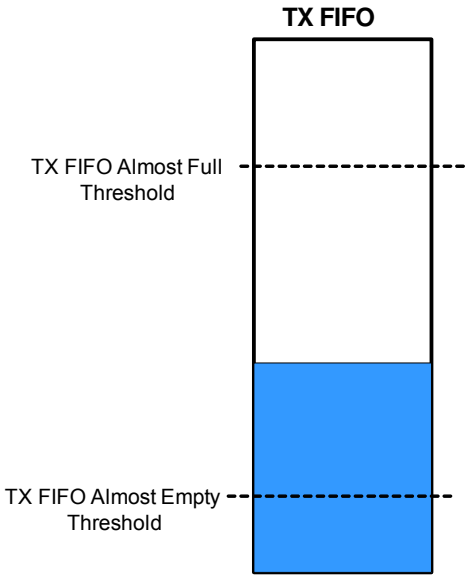


Figure 10. FIFO Threshold

The TX FIFO has two programmable thresholds. An interrupt event occurs when the data in the TX FIFO reaches these thresholds. The first threshold is the FIFO Almost Full threshold, txafthr[5:0]. The value in this register corresponds to the desired threshold value in number of bytes. When the data being filled into the TX FIFO reaches this threshold limit, an interrupt to the microcontroller is generated so the chip can enter TX mode to transmit the contents of the TX FIFO. The second threshold for TX is the FIFO Almost Empty Threshold, txaethr[5:0]. When the data being shifted out of the TX FIFO reaches the Almost Empty threshold an interrupt will be generated. The microcontroller will need to switch out of TX mode or fill more data into the TX FIFO. The Transmitter may be configured so that when the TX FIFO is empty the chip will automatically move to the Ready state. In this mode the TX FIFO Almost Empty Threshold may not be useful. This functionality is set by the ffidle bit in “Register 08h. Operating Mode and Function Control 2,” on page 67.

Add	R/W	Function/Description	D7	D6	D5	D4	D3	D2	D1	D0	POR Def.
08	R/W	Operating & Function Control 2	Reserved	Reserved	Reserved	Reserved	autotx	Reserved	Reserved	ffclrtx	00h
7C	R/W	TX FIFO Control 1			txafthr[5]	txafthr[4]	txafthr[3]	txafthr[2]	txafthr[1]	txafthr[0]	37h
7D	R/W	TX FIFO Control 2			txaethr[5]	txaethr[4]	txaethr[3]	txaethr[2]	txaethr[1]	txaethr[0]	04h

The TX FIFO may be cleared or reset with the ffclrtx bit in “Register 08h. Operating Mode and Function Control 2,” on page 67. All interrupts may be enabled by setting the Interrupt Enabled bits in "Register 05h. Interrupt Enable 1" and “Register 06h. Interrupt Enable 2,” on page 65. If the interrupts are not enabled the function will not generate an interrupt on the nIRQ pin but the bits will still be read correctly in the Interrupt Status registers.

6.2. Packet Configuration

When using the FIFO, automatic packet handling may be enabled for the TX mode. "Register 30h. Data Access Control" through “Register 3Eh. Packet Length,” on page 85 control the configuration for Packet Handling. The usual fields for network communication (such as preamble, synchronization word, headers, packet length, and CRC) can be configured to be automatically added to the data payload. The fields needed for packet generation normally change infrequently and can therefore be stored in registers. Automatically adding these fields to the data payload greatly reduces the amount of communication between the microcontroller and the Si4031/32 and therefore also reduces the required computational power of the microcontroller.

The general packet structure is shown in Figure 11. The length of each field is shown below the field. The preamble pattern is always a series of alternating ones and zeroes, starting with a one. All the fields have programmable lengths to accommodate different applications. The most common CRC polynominals are available for selection.

Figure 11. Packet Structure

An overview of the packet handler configuration registers is shown in Table 12. A complete register description can be found in “11.1. Complete Register Table and Descriptions”.

6.3. Packet Handler TX Mode

If the TX packet length is set the packet handler will send the number of bytes in the packet length field before returning to ready mode and asserting the packet sent interrupt. To resume sending data from the FIFO the microcontroller needs to command the chip to re-enter TX mode Figure 12 provides an example transaction where the packet length is set to three bytes.

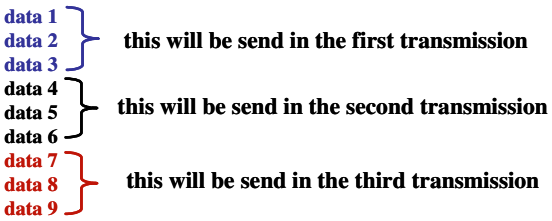


Figure 12. Multiple Packets in TX Packet Handler

Table 12. Packet Handler Registers

Add	R/W	Function/Description	D7	D6	D5	D4	D3	D2	D1	D0	POR Def.
30	R/W	Data Access Control	enpacrx	lsbfrst	crcdonly	*	enpactx	encrc	crc[1]	crc[0]	1Dh
31	R	EzMAC status	0	Reserved	Reserved	Reserved	Reserved	Reserved	pktx	pksent	—
32	R/W	Header Control 1	bcen[3]	enbcast[2]	enbcast[1]	enbcast[0]	Reserved	Reserved	Reserved	Reserved	0Ch
33	R/W	Header Control 2	Reserved	hdlen[2]	hdlen[1]	hdlen[0]	fixpklen	synclen[1]	synclen[0]	prealen[8]	22h
34	R/W	Preamble Length	prealen[7]	prealen[6]	prealen[5]	prealen[4]	prealen[3]	prealen[2]	prealen[1]	prealen[0]	07h
35	R/W	Preamble Detection Control	preath[4]	preath[3]	preath[2]	preath[1]	preath[0]	Reserved	Reserved	Reserved	20h
36	R/W	Sync Word 3	sync[31]	sync[30]	sync[29]	sync[28]	sync[27]	sync[26]	sync[25]	sync[24]	2Dh
37	R/W	Sync Word 2	sync[23]	sync[22]	sync[21]	sync[20]	sync[19]	sync[18]	sync[17]	sync[16]	D4h
38	R/W	Sync Word 1	sync[15]	sync[14]	sync[13]	sync[12]	sync[11]	sync[10]	sync[9]	sync[8]	00h
39	R/W	Sync Word 0	sync[7]	sync[6]	sync[5]	sync[4]	sync[3]	sync[2]	sync[1]	sync[0]	00h
3A	R/W	Transmit Header 3	txhd[31]	txhd[30]	txhd[29]	txhd[28]	txhd[27]	txhd[26]	txhd[25]	txhd[24]	00h
3B	R/W	Transmit Header 2	txhd[23]	txhd[22]	txhd[21]	txhd[20]	txhd[19]	txhd[18]	txhd[17]	txhd[16]	00h
3C	R/W	Transmit Header 1	txhd[15]	txhd[14]	txhd[13]	txhd[12]	txhd[11]	txhd[10]	txhd[9]	txhd[8]	00h
3D	R/W	Transmit Header 0	txhd[7]	txhd[6]	txhd[5]	txhd[4]	txhd[3]	txhd[2]	txhd[1]	txhd[0]	00h
3E	R/W	Transmit Packet Length	pklen[7]	pklen[6]	pklen[5]	pklen[4]	pklen[3]	pklen[2]	pklen[1]	pklen[0]	00h

6.4. Data Whitening, Manchester Encoding, and CRC

Data whitening can be used to avoid extended sequences of 0s or 1s in the transmitted data stream to achieve a more uniform spectrum. When enabled, the payload data bits are XORed with a pseudorandom sequence output from the built-in PN9 generator. The generator is initialized at the beginning of the payload. The receiver recovers the original data by repeating this operation. Manchester encoding can be used to ensure a dc-free transmission and good synchronization properties. When Manchester encoding is used, the effective datarate is unchanged but the actual datarate (preamble length, etc.) is doubled due to the nature of the encoding. The effective datarate when using Manchester encoding is **limited to 64 kbps**. Data Whitening and Manchester encoding can be selected with "Register 70h. Modulation Mode Control 1". The CRC is configured via "Register 30h. Data Access Control".

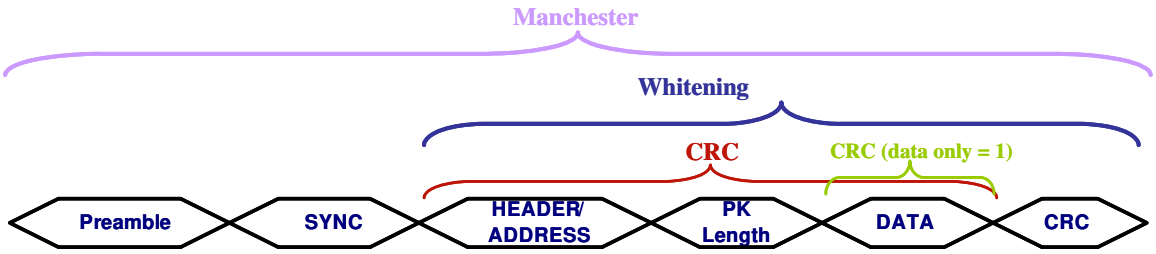


Figure 13. Operation of Data Whitening, Manchester Encoding, and CRC

6.5. TX Retransmission and Auto TX

The Si4031/32 is capable of automatically retransmitting the last packet in the FIFO if no additional packets were loaded into the TX FIFO. Automatic Retransmission is achieved by entering the TX state with the txon bit set. This feature is useful for Beacon transmission or when retransmission is required due to the absence of a valid acknowledgement. Only packets that fit completely in the TX FIFO are valid for retransmit. When it is necessary to transmit longer packets, the TX FIFO uses the circular read/write capability.

An Automatic Transmission is also available. When autotx = 1 the transceiver will enter automatically TX State when the TX FIFO is almost full. When the TX FIFO is empty the transceiver will automatically return to the IDLE State.

Add	R/W	Function/Description	D7	D6	D5	D4	D3	D2	D1	D0	POR Def.
08	R/W	Operating & Function Control 2	Reserved				autotx	Reserved		ffclrtx	00h

7. Auxiliary Functions

7.1. Smart Reset

The Si4031/32 contains an enhanced integrated SMART RESET or POR circuit. The POR circuit contains both a classic level threshold reset as well as a slope detector POR. This reset circuit was designed to produce reliable reset signal in any circumstances. Reset will be initiated if any of the following conditions occur:

- Initial power on, when VDD starts from 0V: reset is active till VDD reaches V_{RR} (see table);
- When VDD decreases below V_{LD} for any reason: reset is active till VDD reaches V_{RR} again;
- A software reset via “Register 08h. Operating Mode and Function Control 2,” on page 67: reset is active for time T_{SWRST}
- On the rising edge of a VDD glitch when the supply voltage exceeds the following time functioned limit:

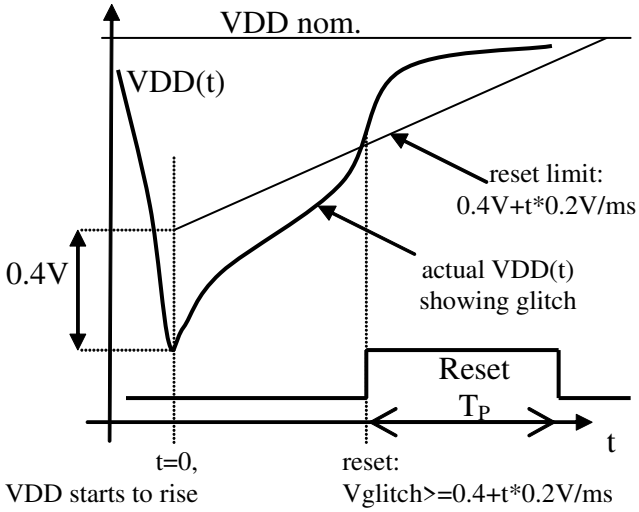


Figure 14. POR Glitch Parameters

Table 13. POR Parameters

Parameter	Symbol	Comment	Min	Typ	Max	Unit
Release Reset Voltage	VRR		0.85	1.3	1.75	V
Power-On VDD Slope	SVDD	tested VDD slope region	0.03		300	V/ms
Low VDD Limit	VLD	VLD<VRR is guaranteed	0.7	1	1.3	V
Software Reset Pulse	TSWRST		50		470	us
Threshold Voltage	VTSD			0.4		V
Reference Slope	k			0.2		V/ms
VDD Glitch Reset Pulse	TP	Also occurs after SDN, and initial power on	5	15	40	ms

The reset will initialize all registers to their default values. The reset signal is also available for output and use by the microcontroller by using the default setting for GPIO_0. The inverted reset signal is available by default on GPIO_1.

7.2. Microcontroller Clock

The crystal oscillator frequency is divided down internally and may be output to the microcontroller through GPIO2. This feature is useful to lower BOM cost by using only one crystal in the system. The system clock frequency is selectable from one of 8 options, as shown below. Except for the 32.768 kHz option, all other frequencies are derived by dividing the Crystal Oscillator frequency. The 32.768 kHz clock signal is derived from an internal RC Oscillator or an external 32 kHz Crystal, depending on which is selected. The GPIO2 default is the microcontroller clock with a 1 MHz microcontroller clock output.

Add	R/W	Function/Description	D7	D6	D5	D4	D3	D2	D1	D0	POR Def.
0A	R/W	Microcontroller Output Clock			clkt[1]	clkt[0]	enlfc	mclk[2]	mclk[1]	mclk[0]	0Bh

mclk[2:0]	Modulation Source
000	30 MHz
001	15 MHz
010	10 MHz
011	4 MHz
100	3 MHz
101	2 MHz
110	1 MHz
111	32.768 kHz

If the microcontroller clock option is being used there may be the need of a System Clock for the microcontroller while the Si4031/32 is in SLEEP mode. Since the Crystal Oscillator is disabled in SLEEP mode in order to save current, the low-power 32.768 kHz clock can be automatically switched to become the microcontroller clock. This feature is called Enable Low Frequency Clock and is enabled by the enlfc bit. When enlfc = 1 and the chip is in SLEEP mode then the 32.768 kHz clock will be provided to the microcontroller as the System Clock, regardless of the setting of mclk[2:0]. For example, if mclk[2:0] = 000, 30 MHz will be provided through the GPIO output pin to the microcontroller as the System Clock in all IDLE or TX states. When the chip is commanded to SLEEP mode, the System Clock will become 32.768 kHz.

Another available feature for the microcontroller clock is the Clock Tail, clkt[1:0]. If the Enable Low Frequency Clock feature is not enabled (enlfc = 0), then the System Clock to the microcontroller is disabled in SLEEP mode. However, it may be useful to provide a few extra cycles for the microcontroller to complete its operation prior to the shutdown of the System Clock signal. Setting the clkt[1:0] field will provide additional cycles of the System Clock before it shuts off.

clkt[1:0]	Modulation Source
00	0 cycles
01	128 cycles
10	256 cycles
11	512 cycles

If an interrupt is triggered, the microcontroller clock will remain enabled regardless of the selected mode. As soon as the interrupt is read the state machine will then move to the selected mode. For instance, if the chip is commanded to Sleep mode but an interrupt has occurred the 30 MHz XTAL will not disable until the interrupt has been cleared.

7.3. General Purpose ADC

An 8-bit SAR ADC is integrated onto the chip for general purpose use, as well as for digitizing the temperature sensor reading. “Register 0Fh. ADC Configuration,” on page 73 must be configured depending on the use of the GP ADC before use. The architecture of the ADC is demonstrated in Figure 15. First the input of the ADC must be selected by setting the ADCSEL[2:0] depending on the use of the ADC. For instance, if the ADC is going to be used to read out the internal temperature sensor, then ADCSEL[2:0] should be set to 000. Next, the input reference voltage to the ADC must be chosen. By default, the ADC uses the bandgap voltage as a reference so the input range of the ADC is from 0–1.02 V with an LSB resolution of 4 mV (1.02/255). Changing the ADC reference will change the LSB resolution accordingly.

Every time the ADC conversion is desired, the ADCStart bit in “Register 0Fh. ADC Configuration,” on page 73 must be set to 1. This is a self clearing bit that will be cleared at the end of the conversion cycle of the ADC. The conversion time for the ADC is 350 us. After the 350 us or when the ADCstart/busy bit is cleared, then the ADC value may be read out of "Register 11h. ADC Value". Setting the "Register 10h. ADC Sensor Amplifier Offset", ADC Sensor Amplifier Offset is only necessary when the ADC is configured to used as a Bridge Sensor as described in the following section.

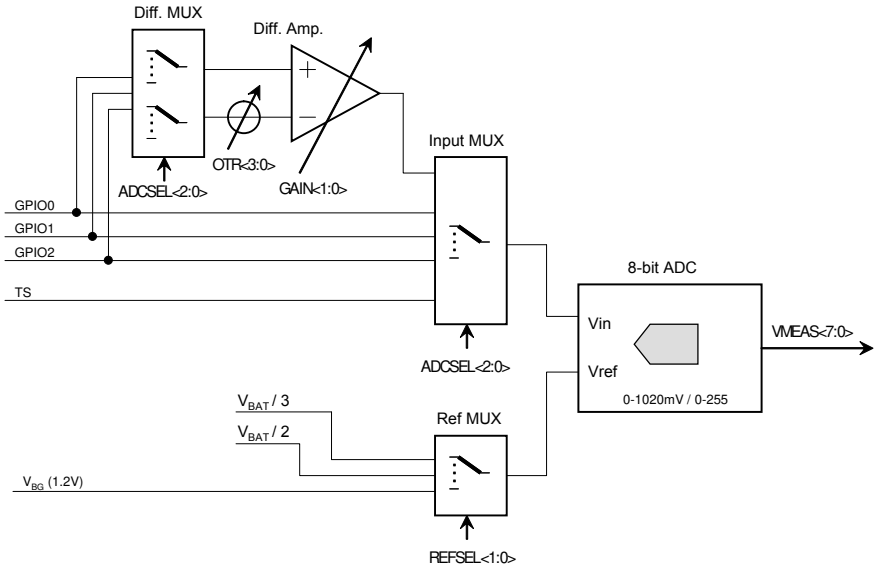


Figure 15. General Purpose ADC Architecture

Add	R/W	Function/Description	D7	D6	D5	D4	D3	D2	D1	D0	POR Def.
0F	R/W	ADC Configuration	adcstart/adcbusy	adcsel[2]	adcsel[1]	adcsel[0]	adcref[1]	adcref[0]	adcgain[1]	adcgain[0]	00h
10	R/W	ADC Sensor Amplifier Offset					adcoffs[3]	adcoffs[2]	adcoffs[1]	adcoffs[0]	00h
11	R	ADC Value	adc[7]	adc[6]	adc[5]	adc[4]	adc[3]	adc[2]	adc[1]	adc[0]	—

7.3.1. ADC Differential Input Mode—Bridge Sensor Example

The differential input mode of ADC8 is designed to directly interface any bridge-type sensor, which is demonstrated in the figure below. As seen in the figure the use of the ADC in this configuration will utilize two GPIO pins. The supply source of the bridge and chip should be the same to eliminate the measuring error caused by battery discharging. For proper operation one of the VDD dependent references (VDD/2 or VDD/3) should be selected for the reference voltage of ADC8. VDD/2 reference should be selected for VDD lower than 2.7 V, VDD/3 reference should be selected for VDD higher than 2.7 V. The differential input mode supports programmable gain to match the input range of ADC8 to the characteristic of the sensor and VDD proportional programmable offset adjustment to compensate the offset of the sensor.

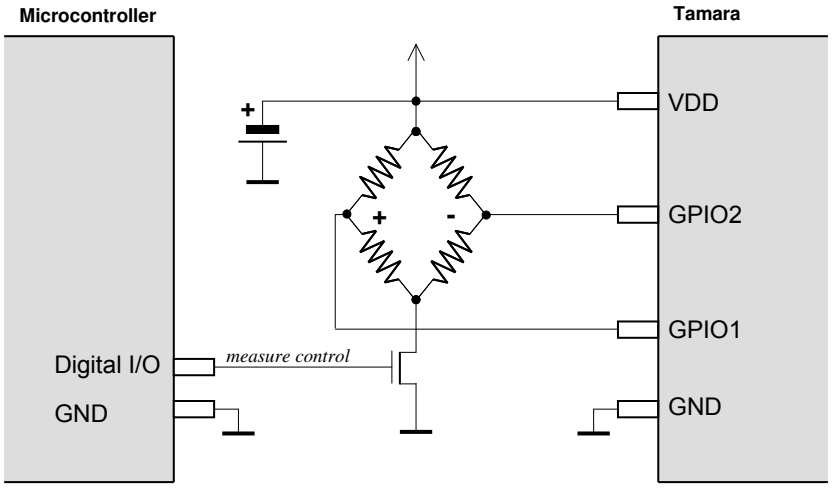


Figure 16. ADC Differential Input Example—Bridge Sensor

The adcgain[1:0] bits in "Register 0Eh. I/O Port Configuration" determine the gain of the differential/single ended amplifier. This is used to fit the input range of the ADC8 to bridge sensors having different sensitivity:

adcgain[1]	adcgain[0]	Differential Gain		Input Range (% of VDD)
		adcref[0] = 0	adcref[0] = 1	
0	0	22/13	33/13	16.7
0	1	44/13	66/13	8.4
1	0	66/13	99/13	5.6
1	1	88/13	132/13	4.2

Note: The input range is the differential voltage measured between the selected GPIO pins corresponding to the full ADC range (255).
The gain is different for different VDD dependent references so the reference change has no influence on input range and digital measured values.

The differential offset can be coarse compensated by the adcoffs[3:0] bits found in "Register 11h. ADC Value". Fine compensation should be done by the microcontroller software. The main reason for the offset compensation is to shift the negative offset voltage of the bridge sensor to the positive differential voltage range. This is essential as the differential input mode is unipolar. The offset compensation is VDD proportional, so the VDD change has no influence on the measured value.

adcoffs[3]	Input Offset (% of VDD)
0	0 if adcoffs[2:0] = 0
	–(8 – adcoffs[2:0]) x 0.12
1	adcoffs[2:0] x 0.12

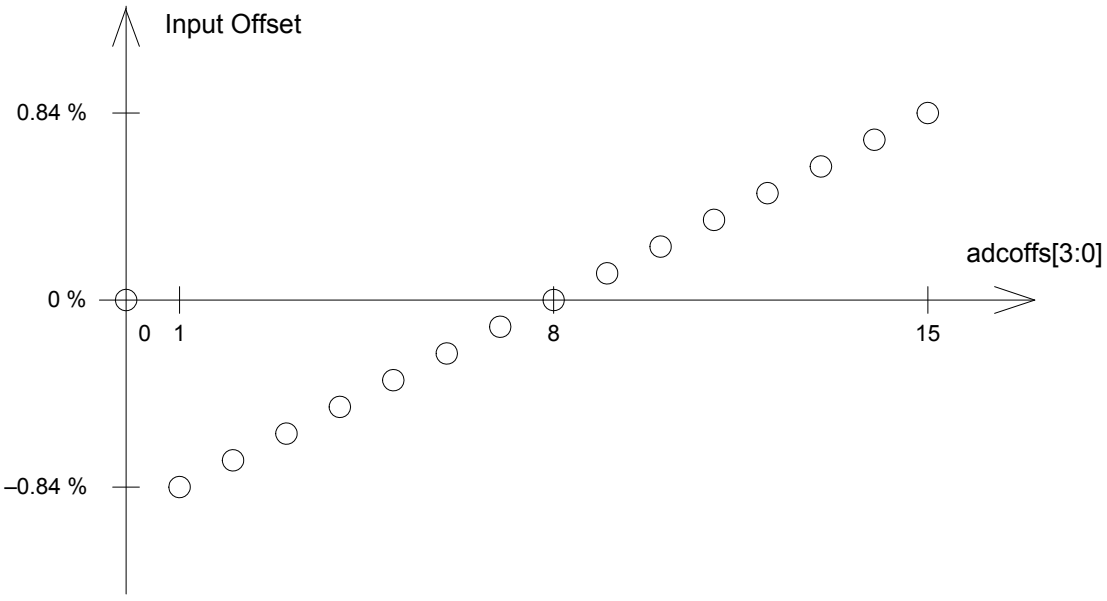


Figure 17. ADC Differential Input Offset for Sensor Offset Coarse Compensation

7.4. Temperature Sensor

An analog temperature sensor is integrated into the chip. The temperature sensor will be automatically enabled when the temperature sensor is selected as the input of the ADC or when the analog temp voltage is selected on the analog test bus. The temperature sensor value may be digitized using the general-purpose ADC and read out over the SPI through "Register 10h. ADC Sensor Amplifier Offset". The range of the temperature sensor is selectable to configure to the desired application and performance. The table below demonstrates the settings for the different temperature ranges and performance.

To use the Temp Sensor:

1. Set input for ADC to be Temperature Sensor, "Register 0Fh. ADC Configuration"—adcsel[2:0] = 000
2. Set Reference for ADC, "Register 0Fh. ADC Configuration"—adcref[1:0] = 00
3. Set Temperature Range for ADC, "Register 12h. Temperature Sensor Calibration"—tsrange[1:0]
4. Set entsoffs = 1, "Register 12h. Temperature Sensor Calibration"
5. Trigger ADC Reading, "Register 0Fh. ADC Configuration"—adcstart = 1
6. Read-out Value—Read Address in "Register 11h. ADC Value"

Add	R/W	Function/Description	D7	D6	D5	D4	D3	D2	D1	D0	POR Def.
12	R/W	Temperature Sensor Control	tsrange[1]	tsrange[0]	entsoffs	entstrim	vbgtrim[3]	vbgtrim[2]	vbgtrim[1]	vbgtrim[0]	20h
13	R/W	Temperature Value Offset	tvoffs[7]	tvoffs[6]	tvoffs[5]	tvoffs[4]	tvoffs[3]	tvoffs[2]	tvoffs[1]	tvoffs[0]	00h

Table 14. Temperature Sensor Range

entoff	tsrange[1]	tsrange[0]	Temp. range	Unit	Slope	ADC8 LSB
1	0	0	–64 … 64	°C	8 mV/°C	0.5 °C
1	0	1	–64 … 192	°C	4 mV/°C	1 °C
1	1	0	0 … 128	°C	8 mV/°C	0.5 °C
1	1	1	–40 … 216	°F	4 mV/°F	1 °F
0*	1	0	0 … 341	°K	3 mV/°K	1.333 °K
***Note:** Absolute temperature mode, no temperature shift. This mode is only for test purposes. POR value of EN_TOFF is 1.						

Control to adjust the temperature sensor accuracy is available by adjusting the bandgap voltage. By enabling the envbgcal and using the vbgcal[3:0] bits to trim the bandgap the temperature sensor accuracy may be fine tuned in the final application. The slope of the temperature sensor is very linear and monotonic but the exact accuracy or offset in temperature is difficult to control better than ±10 °C. With the vbgtrim or bandgap trim though the initial temperature offset can be easily adjusted and be better than ±3 °C.

The different ranges for the temperature sensor and ADC8 are demonstrated in Figure 18. The value of the ADC8 may be translated to a temperature reading by ADC8Value x ADC8 LSB + Lowest Temperature in Temp Range. For instance for a tsrange = 00, Temp = ADC8Value x 0.5 – 64.

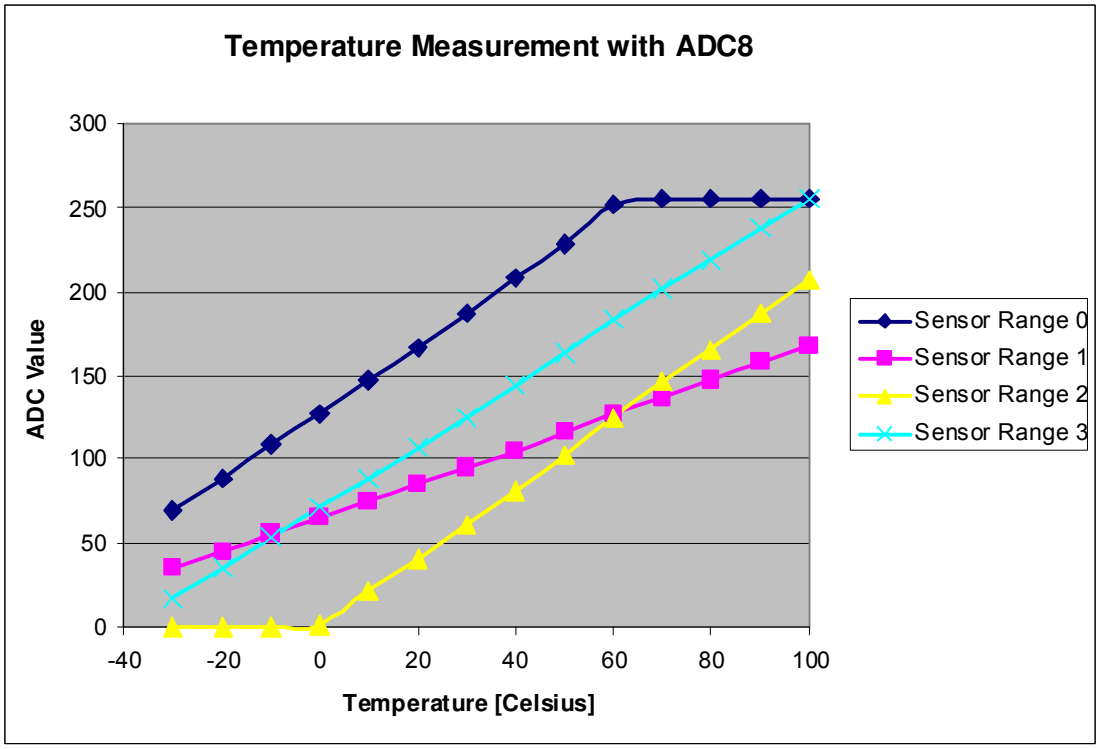


Figure 18. Temperature Ranges using ADC8

7.5. Low Battery Detector

A low battery detector (LBD) with digital read-out is integrated into the chip. A digital threshold may be programmed into the lbdt[4:0] field in "Register 1Ah. Low Battery Detector Threshold". When the digitized battery voltage reaches this threshold an interrupt will be generated on the nIRQ pin to the microcontroller. The microcontroller will then need to verify the interrupt by reading "Register 03h. Interrupt/Status 1" and “Register 04h. Interrupt/Status 2,” on page 62.

If the LBD is enabled while the chip is in SLEEP mode, it will automatically enable the RC oscillator which will periodically turn on the LBD circuit to measure the battery voltage. The battery voltage may also be read out through "Register 1Bh. Battery Voltage Level" at any time when the LBD is enabled. The Low Battery Detect function is enabled by setting enlbd=1 in "Register 07h. Operating Mode and Function Control 1".

Ad	R/W	Function/Description	D7	D6	D5	D4	D3	D2	D1	D0	POR Def.
1A	R/W	Low Battery Detector Threshold				lbdt[4]	lbdt[3]	lbdt[2]	lbdt[1]	lbdt[0]	14h
1B	R	Battery Voltage Level	0	0	0	vbat[4]	vbat[3]	vbat[2]	vbat[1]	vbat[0]	—

The LBD output is digitized by a 5-bit ADC. When the LBD function is enabled, enlbd = 1 in "Register 07h. Operating Mode and Function Control 1", the battery voltage may be read at anytime by reading "Register 1Bh. Battery Voltage Level". A Battery Voltage Threshold may be programmed to register 1Ah. When the battery voltage level drops below the battery voltage threshold an interrupt will be generated on nIRQ pin to the microcontroller if the LBD interrupt is enabled in “Register 06h. Interrupt Enable 2,” on page 65. The microcontroller will then need to verify the interrupt by reading the interrupt status register, Addresses 03 and 04H. The LSB step size for the LBD ADC is 50 mV, with the ADC range demonstrated in the table below. If the LBD is enabled the LBD and ADC will automatically be enabled every 1 s for approximately 250 µs to measure the voltage which minimizes the current consumption in Sensor mode. Before an interrupt is activated four consecutive readings are required.

$$BatteryVoltage = 1.7 + 50mV \times ADCValue$$

ADC Value	VDD Voltage [V]
0	< 1.7
1	1.7–1.75
2	1.75–1.8
…	…
29	3.1–3.15
30	3.15–3.2
31	> 3.2

7.6. Wake-Up Timer

The chip contains an integrated wake-up timer which periodically wakes the chip from SLEEP mode. The wake-up timer runs from the internal 32.768 kHz RC Oscillator. The wake-up timer can be configured to run when in SLEEP mode. If enwt = 1 in "Register 07h. Operating Mode and Function Control 1" when entering SLEEP mode, the wake-up timer will count for a time specified by the Wake-Up Timer Period in Registers 10h–12h. At the expiration of this period an interrupt will be generated on the nIRQ pin if this interrupt is enabled. The microcontroller will then need to verify the interrupt by reading the Interrupt Status Registers 03h–04h. The wake-up timer value may be read at any time by the wtv[15:0] read only registers 13h–14h.

The formula for calculating the Wake-Up Period is the following:

$$WUT = \frac{32 \times M \times 2^{R-D}}{32.768} ms$$

WUT Register	Description
wtr[3:0]	R Value in Formula
wtd[1:0]	D Value in Formula
wtm[15:0]	M Value in Formula

Use of the D variable in the formula is only necessary if finer resolution is required than the R value gives.

Add	R/W	Function/Description	D7	D6	D5	D4	D3	D2	D1	D0	POR Def.
14	R/W	Wake-Up Timer Period 1			wtr[3]	wtr[2]	wtr[1]	wtr[0]	wtd[1]	wtd[0]	00h
15	R/W	Wake-Up Timer Period 2	wtm[15]	wtm[14]	wtm[13]	wtm[12]	wtm[11]	wtm[10]	wtm[9]	wtm[8]	00h
16	R/W	Wake-Up Timer Period 3	wtm[7]	wtm[6]	wtm[5]	wtm[4]	wtm[3]	wtm[2]	wtm[1]	wtm[0]	00h
17	R	Wake-Up Timer Value 1	wtv[15]	wtv[14]	wtv[13]	wtv[12]	wtv[11]	wtv[10]	wtv[9]	wtv[8]	—
18	R	Wake-Up Timer Value 2	wtv[7]	wtv[6]	wtv[5]	wtv[4]	wtv[3]	wtv[2]	wtv[1]	wtv[0]	—

There are two different methods for utilizing the wake-up timer (WUT) depending on if the WUT interrupt is enabled in “Register 06h. Interrupt Enable 2,” on page 65. If the WUT interrupt is enabled then nIRQ pin will go low when the timer expires. The chip will also change state so that the 30 M XTAL is enabled so that the microcontroller clock output is available for the microcontroller to use process the interrupt. The other method of use is to not enable the WUT interrupt and use the WUT GPIO setting. In this mode of operation the chip will not change state until commanded by the microcontroller. The two different modes of operation of the WUT are demonstrated in Figure 19.

A 32 kHz XTAL may also be used for better timing accuracy. By setting the x32 ksel bit in 07h, GPIO0 is automatically reconfigured so that an external 32 kHz XTAL may be connected to this pin. In this mode, the GPIO0 is extremely sensitive to parasitic capacitance, so only the XTAL should be connected to this pin and the XTAL should be physically located as close to the pin as possible. Once the x32 ksel bit is set, all internal functions such as WUT, micro-controller clock, and LDC mode will use the 32 K XTAL and not the 32 kHz RC oscillator.

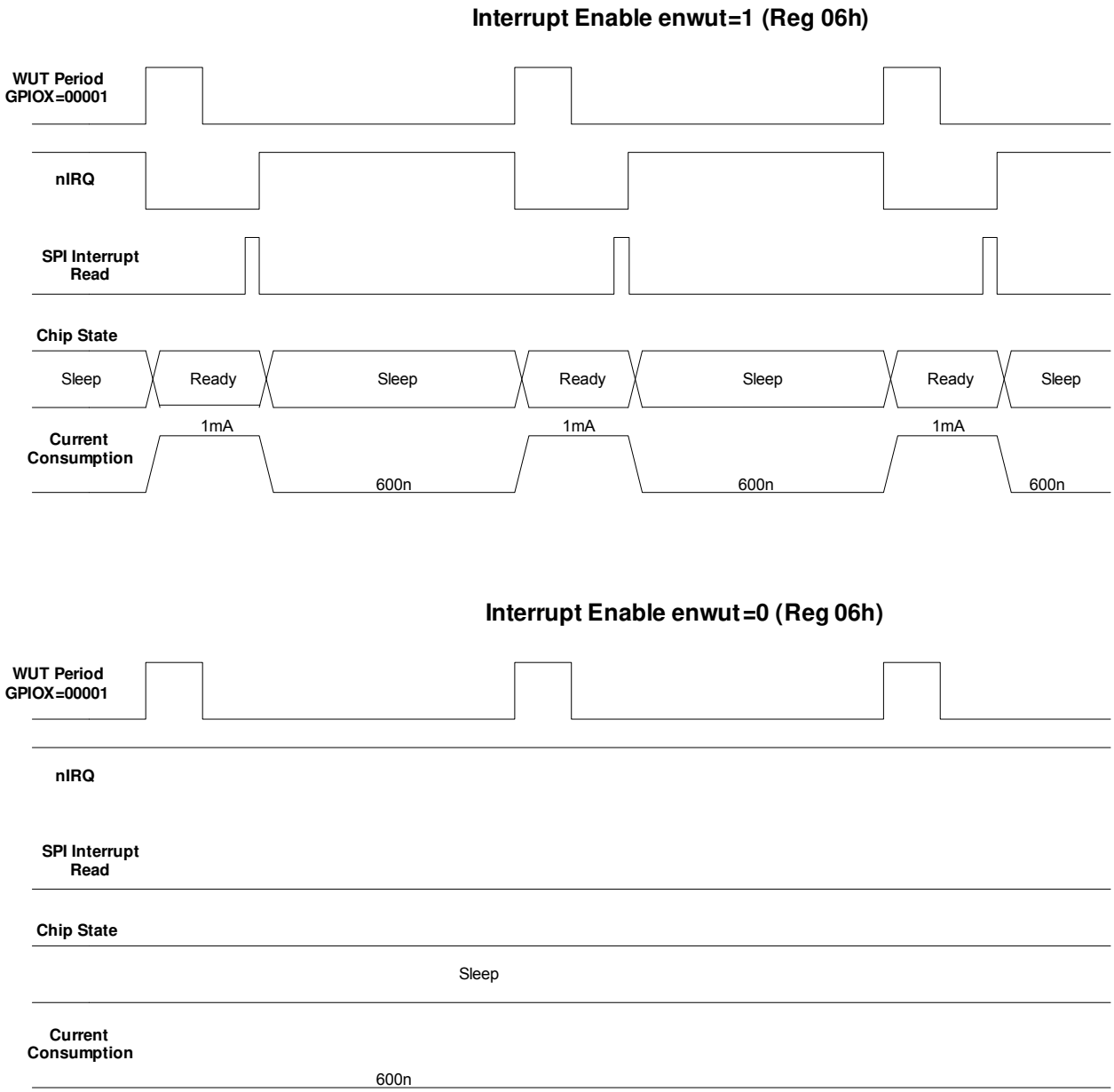


Figure 19. WUT Interrupt and WUT Operation

7.7. GPIO Configuration

Three general purpose IOs (GPIOs) are available. Numerous functions such as specific interrupts, TRSW control, Microcontroller Output, etc. can be routed to the GPIO pins as shown in the tables below. When in Shutdown mode all the GPIO pads are pulled low.

Note: The ADC should not be selected as an input to the GPIO in Standby or Sleep Modes and will cause excess current consumption.

Add	R/W	Function/Description	D7	D6	D5	D4	D3	D2	D1	D0	POR Def.
0B	R/W	GPIO0 Configuration	gpio0drv[1]	gpio0drv[0]	pup0	gpio0[4]	gpio0[3]	gpio0[2]	gpio0[1]	gpio0[0]	00h
0C	R/W	GPIO1 Configuration	gpio1drv[1]	gpio1drv[0]	pup1	gpio1[4]	gpio1[3]	gpio1[2]	gpio1[1]	gpio1[0]	00h
0D	R/W	GPIO2 Configuration	gpio2drv[1]	gpio2drv[0]	pup2	gpio2[4]	gpio2[3]	gpio2[2]	gpio2[1]	gpio2[0]	00h
0E	R/W	I/O Port Configuration		extitst[2]	extitst[1]	extitst[0]	itsdo	dio2	dio1	dio0	00h

The GPIO settings for GPIO1 and GPIO2 are the same as for GPIO0 with the exception of the 00000 default setting. The default settings for each GPIO are listed below:

GPIO	00000—Default Setting
GPIO0	POR
GPIO1	POR Inverted
GPIO2	Microcontroller Clock

The chip is configured to provide the System Clock output to the microcontroller so that only one crystal is needed in the system, therefore reducing the BOM cost. For the TX Data Source, Direct Mode is used because long packets are desired with a unique packet handling format already implemented in the microcontroller. In this configuration the TX Data Clock is configured onto GPIO0, the TX Data is configured onto GPIO1, and the Microcontroller System Clock output is configured onto GPIO2.

For a complete list of the available GPIO's see “Register 0Ch. GPIO Configuration 1,” on page 70, “Register 0Dh. GPIO Configuration 2,” on page 71, and “Register 0Eh. I/O Port Configuration,” on page 72.

8. Reference Design

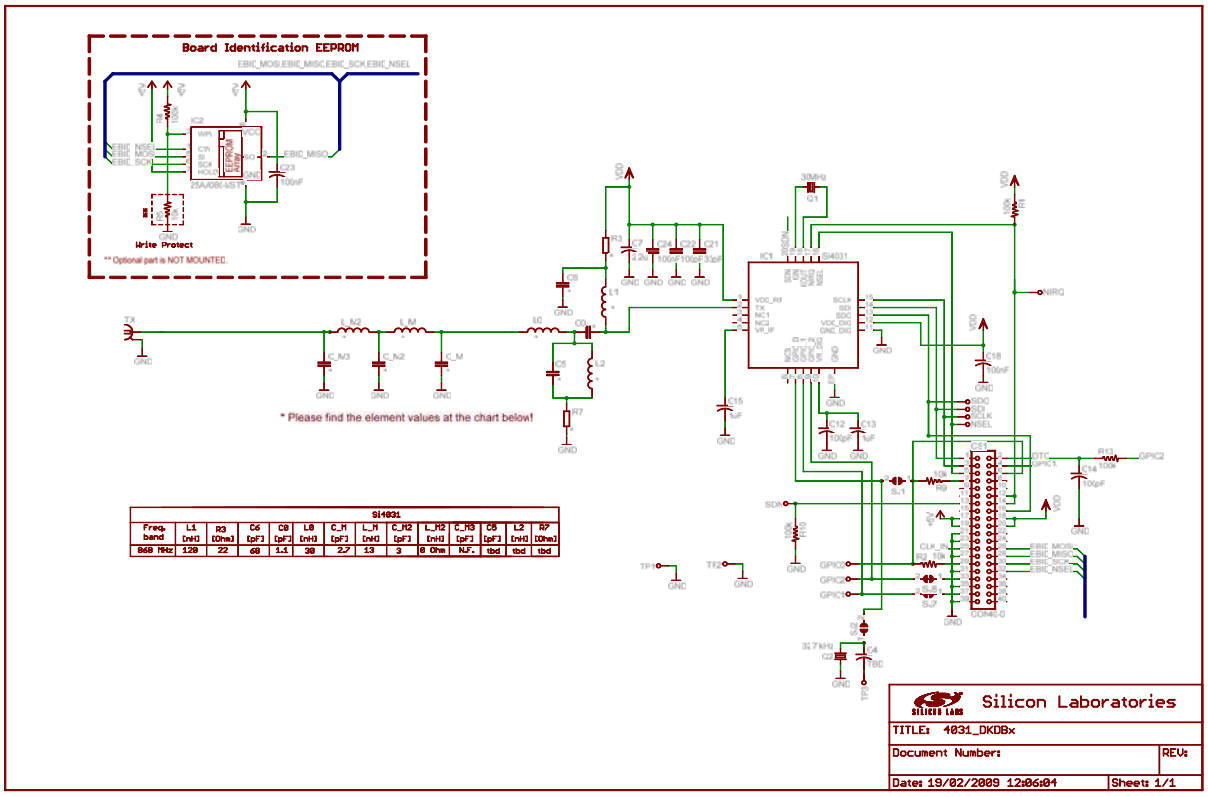


Figure 20. Si4031 Reference Design Schematic

Table 15. Reference Design Bill of Materials

Part	Value	Device	Package	Description
C0	*	C-EUC0402_SMALL	C0402_SMALL	CAPACITOR, European symbol
C1	33pF	C-EUC0402_SMALL	C0402_SMALL	CAPACITOR, European symbol
C2	100pF	C-EUC0402_SMALL	C0402_SMALL	CAPACITOR, European symbol
C3	100nF	C-EUC0402_SMALL	C0402_SMALL	CAPACITOR, European symbol
C4	TBD	C-USC0603K	C0603K	CAPACITOR, American symbol
C5	*	C-EUC0402_SMALL	C0402_SMALL	CAPACITOR, European symbol
C6	*	C-EUC0402_SMALL	C0402_SMALL	CAPACITOR, European symbol
C7	2.2u	C-USC0603K	C0603K	CAPACITOR, American symbol
C12	100pF	C-USC0603K	C0603K	CAPACITOR, American symbol
C13	1uF	C-USC0603K	C0603K	CAPACITOR, American symbol
C14	100pF	C-USC0603K	C0603K	CAPACITOR, American symbol
C15	1uF	C-USC0603K	C0603K	CAPACITOR, American symbol
C18	100nF	C-USC0603K	C0603K	CAPACITOR, American symbol
C23	100nF	C-USC0603K	C0603K	CAPACITOR, American symbol
CS1	CON40-0	CON40-0	PANDUIT-057-040-0-INTEGRATION	
C_M	*	C-EUC0402_SMALL	C0402_SMALL	CAPACITOR, European symbol
C_M2	*	C-EUC0402_SMALL	C0402_SMALL	CAPACITOR, European symbol
C_M3	*	C-EUC0402_SMALL	C0402_SMALL	CAPACITOR, European symbol

Table 15. Reference Design Bill of Materials

GPIO0	TESTPOINT39MIL	TESTPOINT39MIL	TESTPOINT1,0	
GPIO1	TESTPOINT39MIL	TESTPOINT39MIL	TESTPOINT1,0	
GPIO2	TESTPOINT39MIL	TESTPOINT39MIL	TESTPOINT1,0	
IC1	SI4031	SI4031	QFN-20	
IC2	25AA080-I/ST	25AA040ST	TSSOP8	Serial EEPROM
L0	*	L-USL0402_SMALL	L0402_SMALL	INDUCTOR, American symbol
L1	*	L-USL0402_SMALL	L0402_SMALL	INDUCTOR, American symbol
L2	*	L-USL0402_SMALL	L0402_SMALL	INDUCTOR, American symbol
L_M	*	L-USL0402_SMALL	L0402_SMALL	INDUCTOR, American symbol
L_M2	*	L-USL0402_SMALL	L0402_SMALL	INDUCTOR, American symbol
NIRQ	TESTPOINT39MIL	TESTPOINT39MIL	TESTPOINT1,0	
NSEL	TESTPOINT39MIL	TESTPOINT39MIL	TESTPOINT1,0	
Q1	30MHz	CRYSTAL-4PINSX-2520-NEW1	QUARTZ_SIWARD_2520_NEW1	
Q2	32.7 kHz	CRYSTAL32SL	SMQ32SL	
R1	100k	R-US_R0603	R0603	RESISTOR, American symbol
R2	10k	R-US_R0603	R0603	RESISTOR, American symbol
R3	*	R-EU_R0402_SMALL	R0402_SMALL	RESISTOR, European symbol
R4	100k	R-US_R0603	R0603	RESISTOR, American symbol
R5	10k	R-US_R0603	R0603	RESISTOR, American symbol
R7	*	R-EU_R0402_SMALL	R0402_SMALL	RESISTOR, European symbol
R9	10k	R-US_R0603	R0603	RESISTOR, American symbol
R10	100k	R-US_R0603	R0603	RESISTOR, American symbol
R13	100k	R-US_R0603	R0603	RESISTOR, American symbol
SCLK	TESTPOINT39MIL	TESTPOINT39MIL	TESTPOINT1,0	
SDI	TESTPOINT39MIL	TESTPOINT39MIL	TESTPOINT1,0	
SDN	TESTPOINT39MIL	TESTPOINT39MIL	TESTPOINT1,0	
SDO	TESTPOINT39MIL	TESTPOINT39MIL	TESTPOINT1,0	
SJ1		SJ	SJ	SMD solder JUMPER
SJ2		SJ	SJ	SMD solder JUMPER
SJ7		JUMPER_SMD_1	JUMPER_SMD_SJ_1	
SJ8		JUMPER_SMD_1	JUMPER_SMD_SJ_1	
TP1	TESTPOINT39MIL	TESTPOINT39MIL	TESTPOINT1,0	
TP2	TESTPOINT39MIL	TESTPOINT39MIL	TESTPOINT1,0	
TP3	TESTPOINT39MIL	TESTPOINT39MIL	TESTPOINT1,0	
TX		BU-SMA-HORIZONTAL	BU-SMA-H	

***Note:** For proper matching network values please see the chart at the schematic.

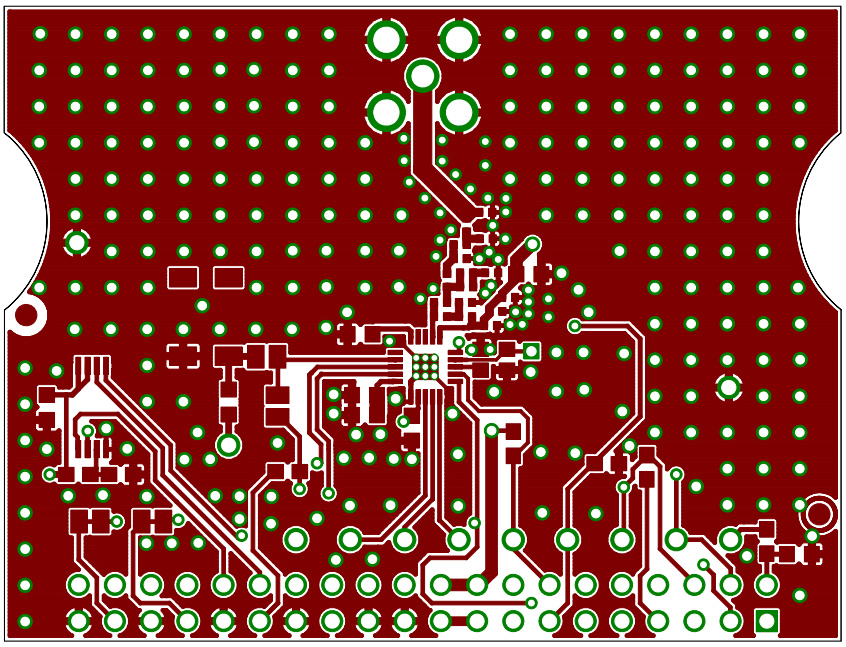


Figure 21. Si4031 Reference Design Schematic—Top

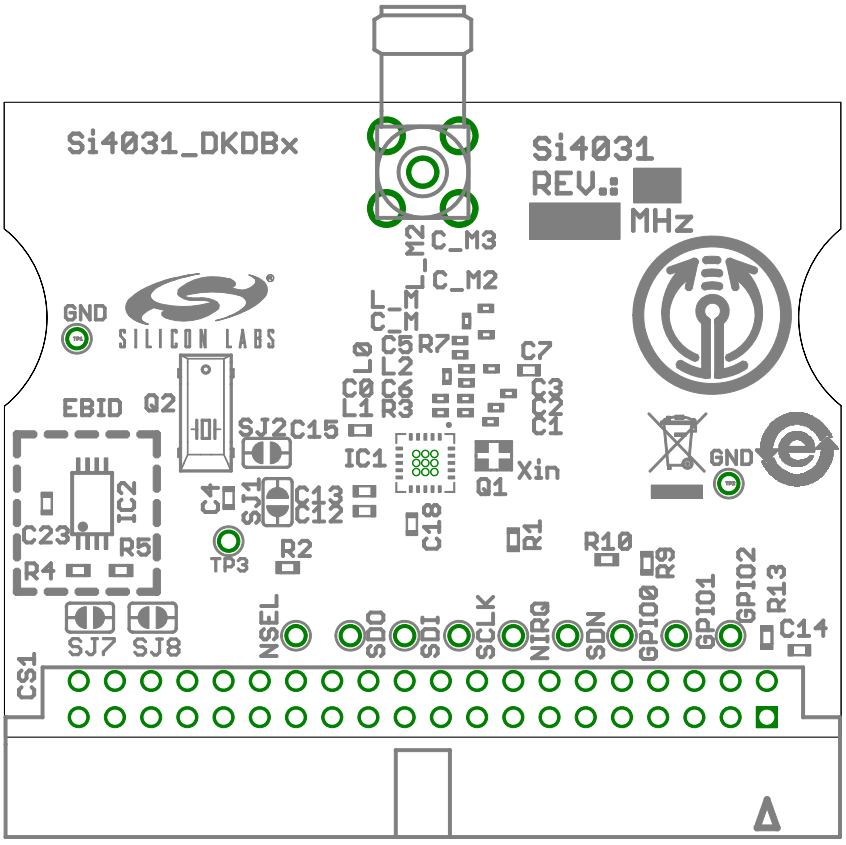


Figure 22. Si4031 Reference Design Schematic—Top Silkscreen

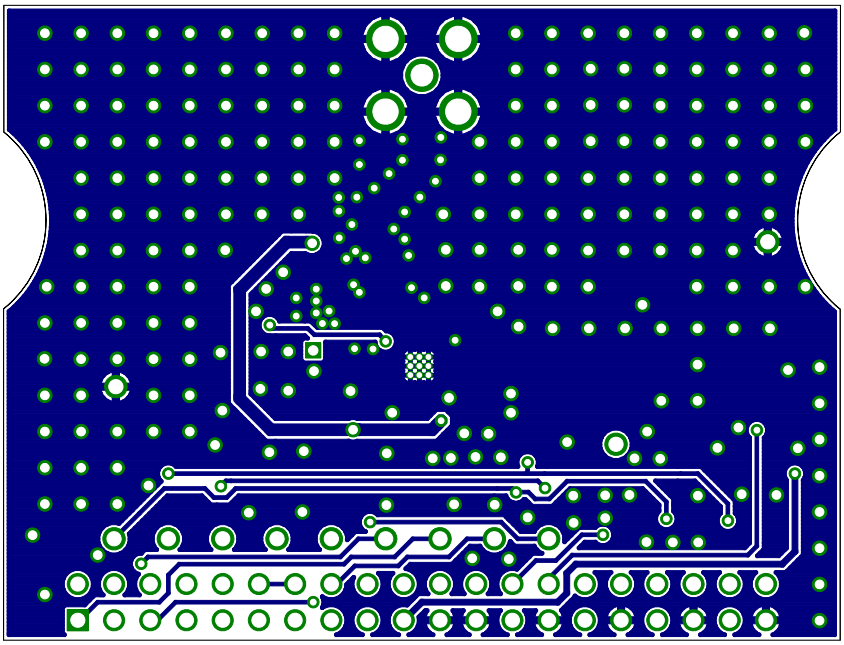


Figure 23. Si4031 Reference Design Schematic—Bottom

Note: The reference design shown above is the that of the standard testcard that may be ordered directly from Silicon Labs. Within this reference design is a EEPROM called the EBID (Evaluation Board IDentification). The EBID is used by other Silicon Labs development tools and is not required on customer designs.

9. Measurement Results

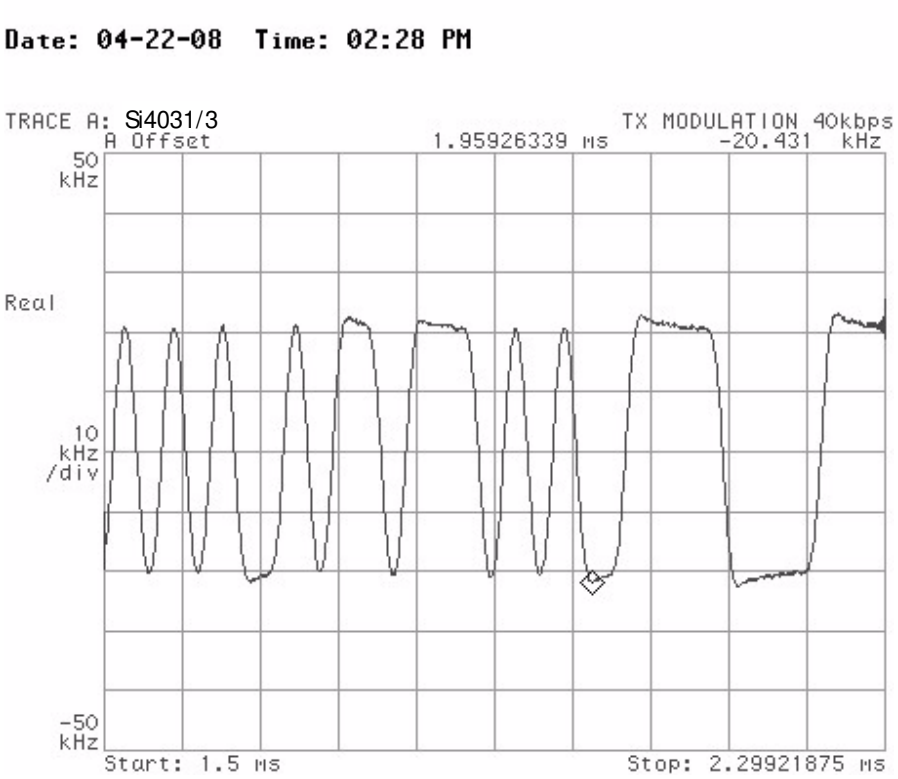


Figure 24. TX Modulation (40 kbps, 20 kHz Deviation)

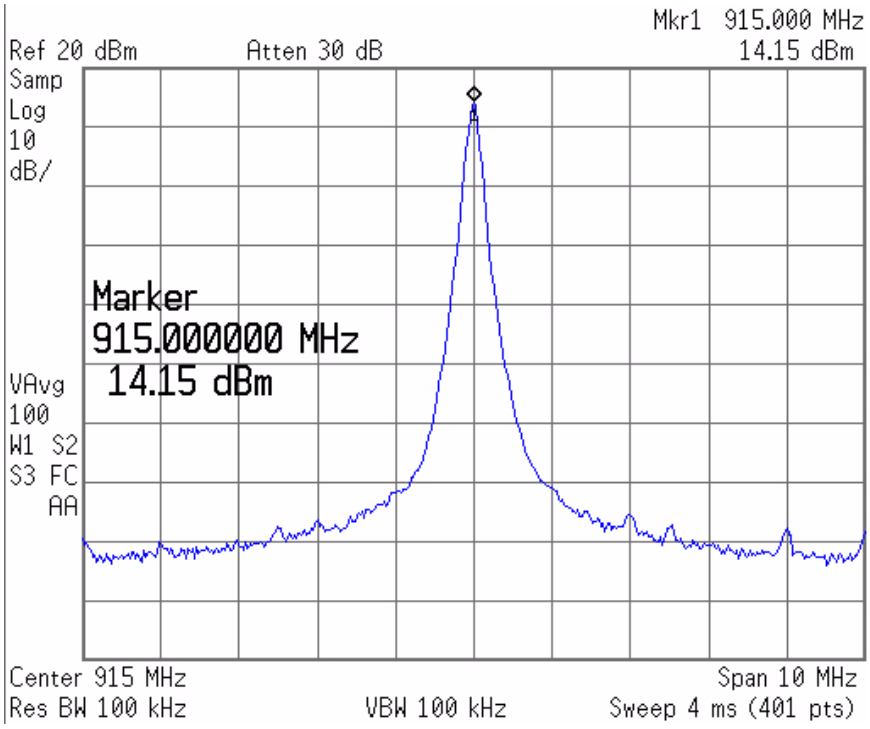


Figure 25. Si4031 TX Unmodulated Spectrum (917 MHz)

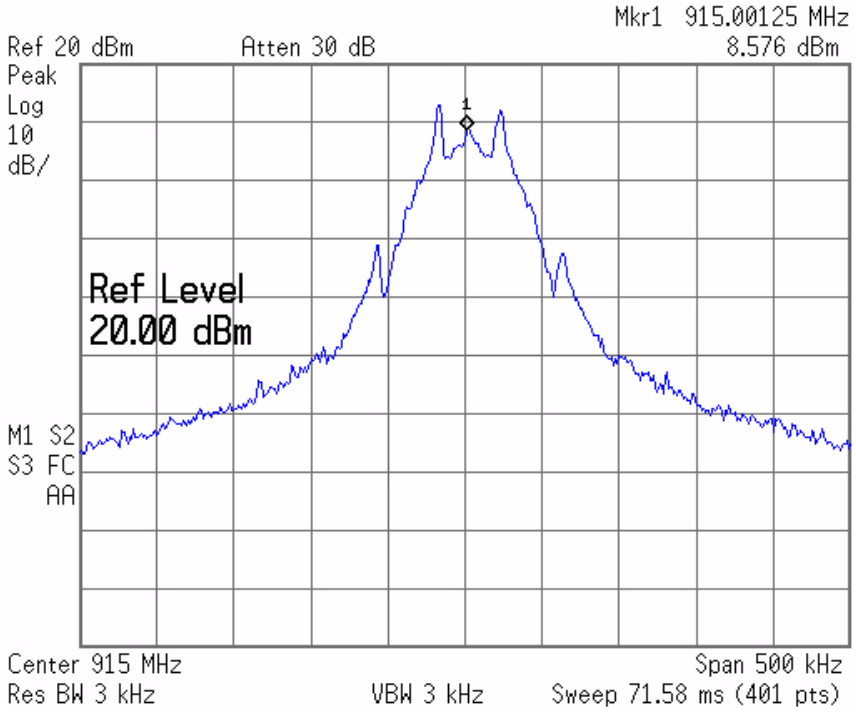


Figure 26. Si4031 TX Modulated Spectrum (917 MHz, 40 kbps, 20 kHz Deviation, GFSK)

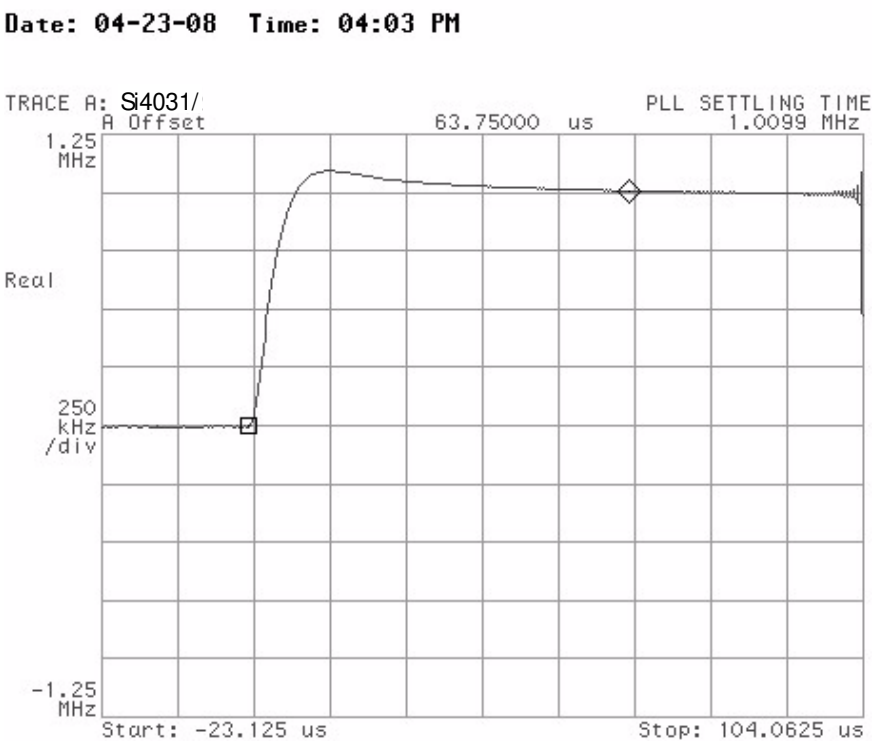


Figure 27. Synthesizer Settling Time for 1 MHz Jump Settled within 10 kHz

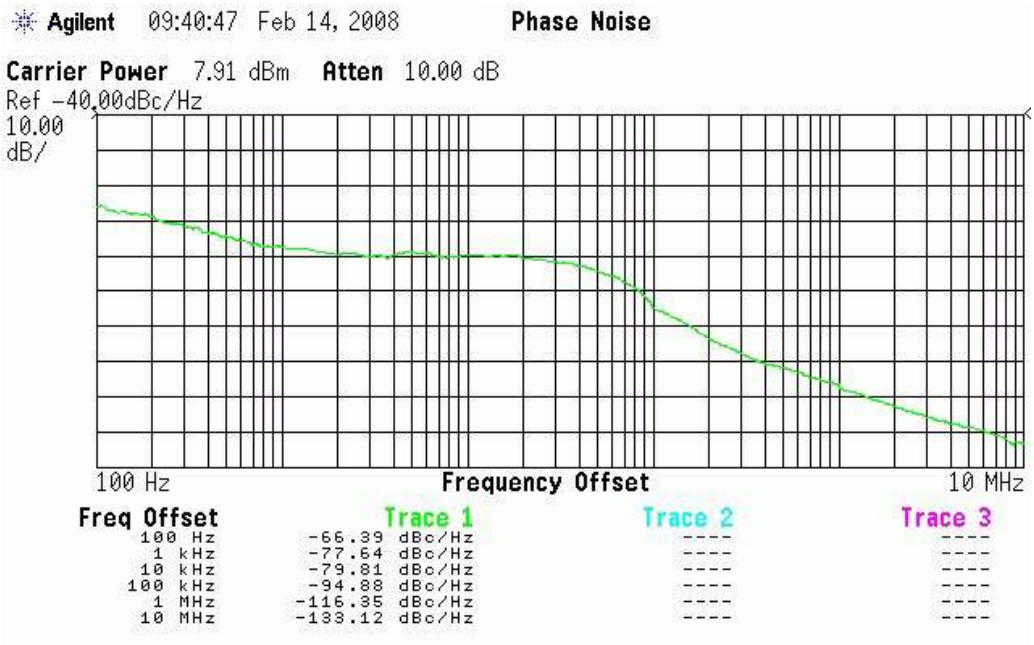


Figure 28. Synthesizer Phase Noise (VCOCURR = 11)

10. Application Notes

10.1. Crystal Selection

The recommended crystal parameters are given in Table 16.

Table 16. Recommended Crystal Parameters

Frequency	ESR	C_L	C_0	Frequency Accuracy
30 MHz	60 Ω	12 pF	5 pF	±20 ppm

The internal XTAL oscillator will work over a range for the parameters of ESR, CL, C0, and ppm accuracy. Extreme values may affect the XTAL start-up and sensitivity of the link. For questions regarding the use of a crystal parameters greatly deviating from the recommend values listed above, please contact customer support.

The crystal used for engineering evaluation and the reference design is the SIWARD –SX2520– 30.0 MHz – 12.0R. Ordering number XTL581200JIG.

10.2. Layout Practice

The following are some general best practice guidelines for PCB layout using the EZRadioPro devices:

- Bypass capacitors should be placed as close as possible to the pin.
- TX matching/layout should mimic reference as much as possible. Failing to do so may cause loss inperformance.
- A solid ground plane is required on the backside of the board under TX matching components
- Crystal should be placed as close as possible to the XIN/XOUT pins and should not have VDD traces running underneath or near it.
- The paddle on the backside of the QFN package needs solid grounding and good soldered connection
- Use GND stitch vias liberally throughout the board, especially underneath the paddle.

11. Reference Material

11.1. Complete Register Table and Descriptions

Table 17. Register Descriptions

Add	R/W	Function/Desc	Data								POR Default
			D7	D6	D5	D4	D3	D2	D1	D0	
00	R	Device Type	0	0	0	dt[4]	dt[3]	dt[2]	dt[1]	dt[0]	
01	R	Device Version	0	0	0	vc[4]	vc[3]	vc[2]	vc[1]	vc[0]	04h
02	R	Device Status	ffovfl	ffunfl		headerr	reserved	reserved	cps[1]	cps[0]	—
03	R	Interrupt Status 1	ifferr	itxffafull	itxffaem	Reserved	iext	ipksent	Reserved	Reserved	—
04	R	Interrupt Status 2	iswdet	ipreaval	ipreainval	irssi	iwut	ilbd	ichiprdy	ipor	—
05	R/W	Interrupt Enable 1	enfferr	entxffafull	entxffaem	enrxffafull	enext	enpksent	enpkvalid	encrcerror	00h
06	R/W	Interrupt Enable 2	enswdet	enpreaval	enpreainval	enrssi	enwut	enlbd	enchiprdy	enpor	03h
07	R/W	Operating & Function Control 1	swres	enlbd	enwt	x32ksel	txon	rxon	pllon	xton	01h
08	R/W	Operating & Function Control 2	antdiv[2]	antdiv[1]	antdiv[0]	rxmpk	autotx	enldm	ffclrrx	ffclrtx	00h
09	R/W	Crystal Oscillator Load Capacitance	xtalshft	xlc[6]	xlc[5]	xlc[4]	xlc[3]	xlc[2]	xlc[1]	xlc[0]	7Fh
0A	R/W	Microcontroller Output Clock	Reserved	Reserved	clkt[1]	clkt[0]	enlfc	mclk[2]	mclk[1]	mclk[0]	06h
0B	R/W	GPIO0 Configuration	gpio0drv[1]	gpio0drv[0]	pup0	gpio0[4]	gpio0[3]	gpio0[2]	gpio0[1]	gpio0[0]	00h
0C	R/W	GPIO1 Configuration	gpio1drv[1]	gpio1drv[0]	pup1	gpio1[4]	gpio1[3]	gpio1[2]	gpio1[1]	gpio1[0]	00h
0D	R/W	GPIO2 Configuration	gpio2drv[1]	gpio2drv[0]	pup2	gpio2[4]	gpio2[3]	gpio2[2]	gpio2[1]	gpio2[0]	00h
0E	R/W	I/O Port Configuration	Reserved	extitst[2]	extitst[1]	extitst[0]	itsdo	dio2	dio1	dio0	00h
0F	R/W	ADC Configuration	adcstart/*adc-done*	adcsel[2]	adcsel[1]	adcsel[0]	adcref[1]	adcref[0]	adcgain[1]	adcgain[0]	00h
10	R/W	ADC Sensor Amplifier Offset	Reserved	Reserved	Reserved	Reserved	adcoffs[3]	adcoffs[2]	adcoffs[1]	adcoffs[0]	00h
11	R	ADC Value	adc[7]	adc[6]	adc[5]	adc[4]	adc[3]	adc[2]	adc[1]	adc[0]	—
12	R/W	Temperature Sensor Control	tsrange[1]	tsrange[0]	entsoffs	entstrim	tstrim[3]	tstrim[2]	tstrim[1]	tstrim[0]	20h
13	R/W	Temperature Value Offset	tvoffs[7]	tvoffs[6]	tvoffs[5]	tvoffs[4]	tvoffs[3]	tvoffs[2]	tvoffs[1]	tvoffs[0]	00h
14	R/W	Wake-Up Timer Period 1	Reserved	Reserved	Reserved	wtr[4]	wtr[3]	wtr[2]	wtr[1]	wtr[0]	03h
15	R/W	Wake-Up Timer Period 2	wtm[15]	wtm[14]	wtm[13]	wtm[12]	wtm[11]	wtm[10]	wtm[9]	wtm[8]	00h
16	R/W	Wake-Up Timer Period 3	wtm[7]	wtm[6]	wtm[5]	wtm[4]	wtm[3]	wtm[2]	wtm[1]	wtm[0]	01h
17	R	Wake-Up Timer Value 1	wtv[15]	wtv[14]	wtv[13]	wtv[12]	wtv[11]	wtv[10]	wtv[9]	wtv[8]	—
18	R	Wake-Up Timer Value 2	wtv[7]	wtv[6]	wtv[5]	wtv[4]	wtv[3]	wtv[2]	wtv[1]	wtv[0]	—
19	R/W	Low-Duty Cycle Mode Duration	ldc[7]	ldc[6]	ldc[5]	ldc[4]	ldc[3]	ldc[2]	ldc[1]	ldc[0]	00h
1A	R/W	Low Battery Detector Threshold	Reserved	Reserved	Reserved	lbdt[4]	lbdt[3]	lbdt[2]	lbdt[1]	lbdt[0]	14h
1B	R	Battery Voltage Level	0	0	0	vbat[4]	vbat[3]	vbat[2]	vbat[1]	vbat[0]	—
1C-2F	Reserved										
30	R/W	Data Access Control	enpacrx	lsbfrst	crcdonly	Reserved	enpactx	encrc	crc[1]	crc[0]	1Dh
31	R	EzMAC status	0	rxcrc1	pksrch	pkrx	pkvalid	crcerror	pktx	pksent	—
32	Reserved										
33	R/W	Header Control 2	Reserved	hdlen[2]	hdlen[1]	hdlen[0]	fixpklen	synclen[1]	synclen[0]	prealen[8]	22h
34	R/W	Preamble Length	prealen[7]	prealen[6]	prealen[5]	prealen[4]	prealen[3]	prealen[2]	prealen[1]	prealen[0]	08h
36	R/W	Sync Word 3	sync[31]	sync[30]	sync[29]	sync[28]	sync[27]	sync[26]	sync[25]	sync[24]	2Dh
37	R/W	Sync Word 2	sync[23]	sync[22]	sync[21]	sync[20]	sync[19]	sync[18]	sync[17]	sync[16]	D4h
38	R/W	Sync Word 1	sync[15]	sync[14]	sync[13]	sync[12]	sync[11]	sync[10]	sync[9]	sync[8]	00h
39	R/W	Sync Word 0	sync[7]	sync[6]	sync[5]	sync[4]	sync[3]	sync[2]	sync[1]	sync[0]	00h
3A	R/W	Transmit Header 3	txhd[31]	txhd[30]	txhd[29]	txhd[28]	txhd[27]	txhd[26]	txhd[25]	txhd[24]	00h
3B	R/W	Transmit Header 2	txhd[23]	txhd[22]	txhd[21]	txhd[20]	txhd[19]	txhd[18]	txhd[17]	txhd[16]	00h
3C	R/W	Transmit Header 1	txhd[15]	txhd[14]	txhd[13]	txhd[12]	txhd[11]	txhd[10]	txhd[9]	txhd[8]	00h
3D	R/W	Transmit Header 0	txhd[7]	txhd[6]	txhd[5]	txhd[4]	txhd[3]	txhd[2]	txhd[1]	txhd[0]	00h
3E	R/W	Transmit Packet Length	pklen[7]	pklen[6]	pklen[5]	pklen[4]	pklen[3]	pklen[2]	pklen[1]	pklen[0]	00h
3F-50	Reserved										
51	R/W	Digital Test Bus	Reserved	ensctest	dtb[5]	dtb[4]	dtb[3]	dtb[2]	dtb[1]	dtb[0]	00h
52	R/W	TX Ramp Control	Reserved	txmod[2]	txmod[1]	txmod[0]	ldoramp[1]	ldoramp[0]	txramp[1]	txramp[0]	2Fh
53	R/W	PLL Tune Time	pllts[4]	pllts[3]	pllts[2]	pllts[1]	pllts[0]	pllt0[2]	pllt0[1]	pllt0[0]	52h
54	R/W	Invalid Preamble Threshold and PA Misc	Reserved	Reserved	inv_pre_th[3]	inv_pre_th[2]	inv_pre_th[1]	inv_pre_th[0]	ldo_pa_boost	pa_vbias_boost	14h
55	R/W	Calibration Control	Reserved	xtalstarthalf	Reserved	enrcfcal	rccal	vcocaldp	vcocal	skipvco	44h
56	R/W	Modem Test	bcrfbyp	slicfbyp	dttype	oscdeten	OOkth	refclksel	refclkinv	distogg	00h
57	R/W	Chargepump Test	pfdrst	fbdiv_rst	cpforceup	cpforcedn	cdconly	cdccur[2]	cdccur[1]	cdccur[0]	00h
58	R/W	Chargepump Current Trimming/Override	cpcurr[1]	cpcurr[0]	cpcorrov	cpcorr[4]	cpcorr[3]	cpcorr[2]	cpcorr[1]	cpcorr[0]	80h
59	R/W	Divider Current Trimming	txcorboosten	fbdivhc	d3trim[1]	d3trim[0]	d2trim[1]	d2trim[0]	d1p5trim[1]	d1p5trim[0]	40h
5A	R/W	VCO Current Trimming	txcurboosten	vcocorrov	vcocorr[3]	vcocorr[2]	vcocorr[1]	vcocorr[0]	vcocur[1]	vcocur[0]	03h
5B	R/W	VCO Calibration / Override	vcocalov/*vcdone*	vcocal[6]	vcocal[5]	vcocal[4]	vcocal[3]	vcocal[2]	vcocal[1]	vcocal[0]	00h
5C	R/W	Synthesizer Test	dsmdt	vcotype	enoloop	dsmod	dsorder[1]	dsorder[0]	dsrstmod	dsrst	0Eh
5D	R/W	Block Enable Override 1	enmix	enlna	enpga	enpa	enbf5	endv32	enbf12	enmx2	00h
5E	R/W	Block Enable Override 2	ends	enldet	enmx3	enbf4	enbf3	enbf11	enbf2	pllreset	40h
5F	R/W	Block Enable Override 3	enfrdv	endv31	endv2	endv1p5	dvbshunt	envco	encp	enbg	00h
60	R/W	Channel Filter Coefficient Address	Reserved	Reserved	Reserved	Reserved	chfiladd[3]	chfiladd[2]	chfiladd[1]	chfiladd[0]	00h
61	R/W	Channel Filter Coefficient Value	Reserved	Reserved	chfilval[5]	chfilval[4]	chfilval[3]	chfilval[2]	chfilval[1]	chfilval[0]	00h

Table 17. Register Descriptions (Continued)

Add	R/W	Function/Desc	Data								POR Default
			D7	D6	D5	D4	D3	D2	D1	D0	
62	R/W	Crystal Oscillator / Control Test	pwst[2]	pwst[1]	pwst[0]	clkhyst	enbias2x	enamp2x	bufovr	enbuf	24h
63	R/W	RC Oscillator Coarse Calibration/Override	rccov	rcc[6]	rcc[5]	rcc[4]	rcc[3]	rcc[2]	rcc[1]	rcc[0]	00h
64	R/W	RC Oscillator Fine Calibration/Override	rcfov	rcf[6]	rcf[5]	rcf[4]	rcf[3]	rcf[2]	rcf[1]	rcf[0]	00h
65	R/W	LDO Control Override	enspor	enbias	envcoldo	enifldo	enrfldo	enpllldo	endigldo	endigpwdn	81h
66	R/W	LDO Level Setting	enovr	enxtal	ents	enrc32	Reserved	diglvl[2]	diglvl[1]	diglvl[0]	02h
67-6A	Reserved										
6B	R/W	GFSK FIR Filter Coefficient Address	Reserved	Reserved	Reserved	Reserved	Reserved	firadd[2]	firadd[1]	firadd[0]	00h
6C	R/W	GFSK FIR Filter Coefficient Value	Reserved	Reserved	firval[5]	firval[4]	firval[3]	firval[2]	firval[1]	firval[0]	01h
6D	R/W	TX Power	Reserved	Reserved	Reserved	Reserved	lna_sw	txpow[2]	txpow[1]	txpow[0]	08h
6E	R/W	TX Data Rate 1	txdr[15]	txdr[14]	txdr[13]	txdr[12]	txdr[11]	txdr[10]	txdr[9]	txdr[8]	0Ah
6F	R/W	TX Data Rate 0	txdr[7]	txdr[6]	txdr[5]	txdr[4]	txdr[3]	txdr[2]	txdr[1]	txdr[0]	3Dh
70	R/W	Modulation Mode Control 1	Reserved	Reserved	txdtrtscale	enphpwdn	manppol	enmaninv	enmanch	enwhite	0Ch
71	R/W	Modulation Mode Control 2	trclk[1]	trclk[0]	dtmod[1]	dtmod[0]	eninv	fd[8]	modtyp[1]	modtyp[0]	00h
72	R/W	Frequency Deviation	fd[7]	fd[6]	fd[5]	fd[4]	fd[3]	fd[2]	fd[1]	fd[0]	20h
73	R/W	Frequency Offset 1	fo[7]	fo[6]	fo[5]	fo[4]	fo[3]	fo[2]	fo[1]	fo[0]	00h
74	R/W	Frequency Offset 2	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	fo[9]	fo[8]	00h
75	R/W	Frequency Band Select	Reserved	sbsel	hbsel	fb[4]	fb[3]	fb[2]	fb[1]	fb[0]	75h
76	R/W	Nominal Carrier Frequency 1	fc[15]	fc[14]	fc[13]	fc[12]	fc[11]	fc[10]	fc[9]	fc[8]	BBh
77	R/W	Nominal Carrier Frequency 0	fc[7]	fc[6]	fc[5]	fc[4]	fc[3]	fc[2]	fc[1]	fc[0]	80h
78	R/W	Miscellaneous Settings	Reserved	Reserved	Reserved	Reserved	Alt_PA_Seq	rcosc[2]	rcosc[1]	rcosc[0]	09h
79	R/W	Frequency Hopping Channel Select	fhch[7]	fhch[6]	fhch[5]	fhch[4]	fhch[3]	fhch[2]	fhch[1]	fhch[0]	00h
7A	R/W	Frequency Hopping Step Size	fhs[7]	fhs[6]	fhs[5]	fhs[4]	fhs[3]	fhs[2]	fhs[1]	fhs[0]	00h
7B	R/W	Turn Around and 15.4 Length Compliance	15.4 Length	Reserved	Reserved	Reserved	Reserved	turn_around_en	Phase[1]	Phase[0]	09h
7C	R/W	TX FIFO Control 1	Reserved	Reserved	txafthr[5]	txafthr[4]	txafthr[3]	txafthr[2]	txafthr[1]	txafthr[0]	37h
7D	R/W	TX FIFO Control 2	Reserved	Reserved	txaethr[5]	txaethr[4]	txaethr[3]	txaethr[2]	txaethr[1]	txaethr[0]	04h
7E	Reserved										
7F	R/W	FIFO Access	fifod[7]	fifod[6]	fifod[5]	fifod[4]	fifod[3]	fifod[2]	fifod[1]	fifod[0]	—

Register 00h. Device Type Code (DT)

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	Reserved			dt[4:0]				
Type	R			R				

Reset value = 00000111

Bit	Name	Function
7:5	Reserved	**Reserved.**
4:0	dt[4:0]	**Device Type Code.** EZRadioPRO: 01000.

Register 01h. Version Code (VC)

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	Reserved			vc[4:0]				
Type	R			R				

Reset value = xxxxxxxx

Bit	Name	Function
7:5	Reserved	**Reserved.**
4:0	vc[4:0]	**Version Code.** Code indicating the version of the chip. Rev A0: 00100 Rev V2: 00011

Register 02h. Device Status

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	ffovfl	ffunfl	Reserved	Reserved	Reserved	Reserved	cps[1:0]	
Type	R	R	R	R	R	R	R	

Reset value = xxxxxxxx

Bit	Name	Function
7	ffovfl	**TX FIFO Overflow Status.**
6	ffunfl	**TX FIFO Underflow Status.**
5:4	Reserved	**Reserved.**
3:2	Reserved	**Reserved.**
1:0	cps[1:0]	**Chip Power State.** 00: Idle State 10: TX State

Register 03h. Interrupt/Status 1

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	ifferr	itxffafull	ixtffaem	Reserved	iext	ipksent	Reserved	Reserved
Type	R	R	R	R	R	R	R	R

Reset value = xxxxxxxx

Bit	Name	Function
7	ifferr	**FIFO Underflow/Overflow Error.** When set to 1 the TX FIFO has overflowed or underflowed.
6	itxffafull	**TX FIFO Almost Full.** When set to 1 the TX FIFO has met its almost full threshold and needs to be transmitted.
5	itxffaem	**TX FIFO Almost Empty.** When set to 1 the TX FIFO is almost empty and needs to be filled.
4	Reserved	**Reserved.**
3	iext	**External Interrupt.** When set to 1 an interrupt occurred on one of the GPIO's if it is programmed so. The status can be checked in register 0Eh. See GPIOx Configuration section for the details.
2	ipksent	**Packet Sent Interrupt.** When set to1 a valid packet has been transmitted.
1:0	Reserved	**Reserved.**

When any of the Interrupt/Status 1 bits change state from 0 to 1 the device will notify the microcontroller by setting the nIRQ pin LOW if it is enabled in the Interrupt Enable 1 register. The nIRQ pin will go to HIGH and all the **enabled** interrupt bits will be cleared when the microcontroller reads this address. If any of these bits is not enabled in the Interrupt Enable 1 register then it becomes a status signal that can be read anytime in the same location and will not be cleared by reading the register.

Table 18. Interrupt or Status 1 Bit Set/Clear Description

Bit	Status Name	Set/Clear Conditions
7	ifferr	Set if there is a FIFO overflow or underflow. Cleared by applying FIFO reset.
6	itxffafull	Set when the number of bytes written to TX FIFO is greater than the Almost Full threshold. Automatically cleared at the start of transmission when the number of bytes in the FIFO is less than or equal to the threshold.
5	itxffaem	Set when the number of bytes in the TX FIFO is less than or equal to the Almost Empty threshold. Automatically cleared when the number of data bytes in the TX FIFO is above the Almost Empty threshold.
4	Reserved	**Reserved.**
3	iext	External interrupt source.
2	ipksent	Set once a packet is successfully sent (no TX abort). Cleared upon leaving FIFO mode or at the start of a new transmission.
1:0	Reserved	**Reserved.**

Table 19. When are Individual Status Bits Set/Cleared if not Enabled as Interrupts?

Bit	Status Name	Set/Clear Conditions
7	ifferr	Set if there is a FIFO Overflow or Underflow. It is cleared only by applying FIFO reset to the specific FIFO that caused the condition.
6	itxffafull	Will be set when the number of bytes written to TX FIFO is greater than the Almost Full threshold set by SPI. It is automatically cleared when we start transmitting and the FIFO data is read out and the number of bytes left in the FIFO is smaller or equal to the threshold).
5	itxffaem	Will be set when the number of bytes (not yet transmitted) in TX FIFO is smaller or equal than the Almost Empty threshold set by SPI. It is automatically cleared when we write enough data to TX FIFO so that the number of data bytes not yet transmitted is above the Almost Empty threshold.
4	Reserved	**Reserved.**
3	iext	External interrupt source
2	ipksent	Will go high once a packet is sent all the way through (no TX abort). This status will be cleaned if 1) We leave FIFO mode or 2) In FIFO mode we start a new transmission.
1:0	Reserved	**Reserved.**

Register 04h. Interrupt/Status 2

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	Reserved				iwut	ilbd	ichiprdy	ipor
Type	R				R	R	R	R

Reset value = xxxxxxxx

Bit	Name	Function
7:4	Reserved	**Reserved**
3	iwut	**Wake-Up-Timer.** On the expiration of programmed wake-up timer this bit will be set to 1.
2	ilbd	**Low Battery Detect.** When a low battery event is been detected this bit will be set to 1. This interrupt event is saved even if it is not enabled by the mask register bit and causes an interrupt after it is enabled.
1	ichiprdy	**Chip Ready (XTAL).** When a chip ready event has been detected this bit will be set to 1.
0	ipor	**Power-on-Reset (POR).** When the chip detects a Power on Reset above the desired setting this bit will be set to 1.

When any of the Interrupt/Status Register 2 bits change state from 0 to 1 the control block will notify the microcontroller by setting the nIRQ pin LOW if it is enabled in the Interrupt Enable 2 register. The nIRQ pin will go to HIGH and all the **enabled** interrupt bits will be cleared when the microcontroller reads this address. If any of these bits is not enabled in the Interrupt Enable 2 register then it becomes a status signal that can be read anytime in the same location and will not be cleared by reading the register.

Table 20. Interrupt or Status 2 Bit Set/Clear Description

Bit	Status Name	Set/Clear Conditions
7:4	Reserved	**Reserved.**
3	iwut	Wake time timer interrupt. Use as an interrupt, not as a status.
2	ilbd	Low Battery Detect. When a low battery event is been detected this bit will be set to 1. This interrupt event is saved even if it is not enabled by the mask register bit and causes an interrupt after it is enabled. Probably the status is cleared once the battery is replaced.
1	ichiprdy	Chip ready goes high once we enable the xtal, TX and a settling time for the Xtal clock elapses. The status stay high unless we go back to Idle mode.
0	ipor	Power on status.

Table 21. Detailed Description of Status Registers when not Enabled as Interrupts

Bit	Status Name	Set/Clear Conditions
7:4	Reserved	**Reserved.**
3	iwut	Wake time timer interrupt. Use as an interrupt, not as a status.
2	ilbd	Low Battery Detect. When a low battery event is been detected this bit will be set to 1. This interrupt event is saved even if it is not enabled by the mask register bit and causes an interrupt after it is enabled. Probably the status is cleared once the battery is replaced.
1	ichiprdy	Chip ready goes high once we enable the xtal, TX, and a settling time for the Xtal clock elapses. The status stay high unless we go back to Idle mode.
0	ipor	Power on status.

Register 05h. Interrupt Enable 1

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	enfferr	entxffafull	entxffaem	Reserved	enext	enpksent	Reserved	Reserved
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Reset value = 00000000

Bit	Name	Function
7	enfferr	**Enable FIFO Underflow/Overflow.** When set to 1 the FIFO Underflow/Overflow interrupt will be enabled.
6	entxffafull	**Enable TX FIFO Almost Full.** When set to 1 the TX FIFO Almost Full interrupt will be enabled.
5	entxffaem	**Enable TX FIFO Almost Empty.** When set to 1 the TX FIFO Almost Empty interrupt will be enabled.
4	Reserved	**Reserved.**
3	enext	**Enable External Interrupt.** When set to 1 the External Interrupt will be enabled.
2	enpksent	**Enable Packet Sent.** When ipksent =1 the Packet Sense Interrupt will be enabled.
1:0	Reserved	**Reserved.**

Register 06h. Interrupt Enable 2

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	Reserved				enwut	enlbd	enchiprdy	enpor
Type	R				R/W	R/W	R/W	R/W

Reset value = 00000011

Bit	Name	Function
7:4	Reserved	**Reserved.**
3	enwut	**Enable Wake-Up Timer.** When set to 1 the Wake-Up Timer interrupt will be enabled.
2	enlbd	**Enable Low Battery Detect.** When set to 1 the Low Battery Detect interrupt will be enabled.
1	enchiprdy	**Enable Chip Ready (XTAL).** When set to 1 the Chip Ready interrupt will be enabled.
0	enpor	**Enable POR.** When set to 1 the POR interrupt will be enabled.

Register 07h. Operating Mode and Function Control 1

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	swres	enlbd	enwt	x32ksel	txon	Reserved	pllon	xton
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Reset value = 00000001

Bit	Name	Function
7	swres	**Software Register Reset Bit.** This bit may be used to reset all registers simultaneously to a DEFAULT state, without the need for sequentially writing to each individual register. The RESET is accomplished by setting swres = 1. This bit will be automatically cleared.
6	enlbd	**Enable Low Battery Detect.** When this bit is set to 1 the Low Battery Detector circuit and threshold comparison will be enabled.
5	enwt	**Enable Wake-Up-Timer.** Enabled when enwt = 1. If the Wake-up-Timer function is enabled it will operate in any mode and notify the microcontroller through the GPIO interrupt when the timer expires.
4	x32ksel	**32,768 kHz Crystal Oscillator Select.** 0: RC oscillator 1: 32 kHz crystal
3	txon	**TX on in Manual Transmit Mode.** Automatically cleared in FIFO mode once the packet is sent. Transmission can be aborted during packet transmission, however, when no data has been sent yet, transmission can only be aborted after the device is programmed to “unmodulated carrier” ("Register 71h. Modulation Mode Control 2").
2	Reserved	**Reserved.**
1	pllon	**TUNE Mode (PLL is ON).** When pllon = 1 the PLL will remain enabled in Idle State. This will for faster turn-around time at the cost of increased current consumption in Idle State.
0	xton	**READY Mode (Xtal is ON).**

Register 08h. Operating Mode and Function Control 2

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	Reserved				autotx	Reserved		ffclrtx
Type	R/W				R/W	R/W		R/W

Reset value = 00000000

Bit	Name	Function
7:4	Reserved	**Reserved.**
3	autotx	**Automatic Transmission.** When autotx = 1 the transceiver will enter automatically TX State when the FIFO is almost full. When the FIFO is empty it will automatically return to the Idle State.
2:1	Reserved	**Reserved.**
0	ffclrtx	**TX FIFO Reset/Clear.** This has to be a two writes operation: Setting ffclrtx =1 followed by ffclrtx = 0 will clear the contents of the TX FIFO.

Register 09h. 30 MHz Crystal Oscillator Load Capacitance

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	xtalshft	xlc[6:0]						
Type	R/W	R/W						

Reset value = 01111111

Bit	Name	Function
7	xtalshft	Additional capacitance to course shift the frequency if xlc[6:0] is not sufficient. Not binary with xlc[6:0].
6:0	xlc[6:0]	**Tuning Capacitance for the 30 MHz XTAL.**

Register 0Ah. Microcontroller Output Clock

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	Reserved		clkt[1:0]		enlfc	mclk[2:0]		
Type	R		R/W		R/W	R/W		

Reset value = xx000110

Bit	Name	Function
7:6	Reserved	**Reserved.**
5:4	clkt[1:0]	**Clock Tail.** If enlfc = 0 then it can be useful to provide a few extra cycles for the microcontroller to complete its operation. Setting the clkt[1:0] register will provide the addition cycles of the clock before it shuts off. 00: 0 cycle 01: 128 cycles 10: 256 cycles 11: 512 cycles
3	enlfc	**Enable Low Frequency Clock.** When enlfc = 1 and the chip is in Sleep mode then the 32.768 kHz clock will be provided to the microcontroller no matter what the selection of mclk[2:0] is. For example if mclk[2:0] = '000', 30 MHz will be available through the GPIO to output to the microcontroller in all Idle or TX states. When the chip is commanded to Sleep mode the 30 MHz clock will become 32.768 kHz.
2:0	mclk[2:0]	**Microcontroller Clock.** Different clock frequencies may be selected for configurable GPIO clock output. All clock frequencies are created by dividing the XTAL except for the 32 kHz clock which comes directly from the 32 kHz RC Oscillator. The mclk[2:0] setting is only valid when xton = 1 except the 111. 000: 30 MHz 001: 15 MHz 010: 10 MHz 011: 4 MHz 100: 3 MHz 101: 2 MHz 110: 1 MHz 111: 32.768 kHz

Register 0Bh. GPIO Configuration 0

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	gpiodrv0[1:0]		pup0	gpio0[4:0]				
Type	R/W		R/W	R/W				

Reset value = 00000000

Bit	Name	Function
7:6	gpiodrv0[1:0]	**GPIO Driving Capability Setting.**
5	pup0	**Pullup Resistor Enable on GPIO0.** When set to 1 the a 200 kΩ resistor is connected internally between VDD and the pin if the GPIO is configured as a digital input.
4:0	gpio0[4:0]	**GPIO0 pin Function Select.** 00000: Power-On-Reset (output) 00001: Wake-Up Timer: 1 when WUT has expired (output) 00010: Low Battery Detect: 1 when battery is below threshold setting (output) 00011: Direct Digital Input 00100: External Interrupt, falling edge (input) 00101: External Interrupt, rising edge (input) 00110: External Interrupt, state change (input) 00111: ADC Analog Input 01000: Reserved (Analog Test N Input) 01001: Reserved (Analog Test P Input) 01010: Direct Digital Output 01011: Reserved (Digital Test Output) 01100: Reserved (Analog Test N Output) 01101: Reserved (Analog Test P Output) 01110: Reference Voltage (output) 01111: TX Data CLK output to be used in conjunction with TX Data pin (output) 10000: TX Data input for direct modulation (input) 10001: External Retransmission Request (input) 10010: TX State (output) 10011: TX FIFO Almost Full (output) 10100: Reserved 10101: Reserved 10110: Reserved 10111: Reserved 11000: Reserved 11001: Reserved 11010: Reserved 11011: Reserved 11100: Reserved 11101: VDD else : GND

Register 0Ch. GPIO Configuration 1

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	gpiodrv1[1:0]		pup1	gpio1[4:0]				
Type	R/W		R/W	R/W				

Reset value = 00000000

Bit	Name	Function
7:6	gpiodrv1[1:0]	**GPIO Driving Capability Setting.**
5	pup1	**Pullup Resistor Enable on GPIO1.** When set to 1 the a 200 kΩ resistor is connected internally between VDD and the pin if the GPIO is configured as a digital input.
4:0	gpio1[4:0]	**GPIO1 pin Function Select.** 00000: Inverted Power-On-Reset (output) 00001: Wake-Up Timer: 1 when WUT has expired (output) 00010: Low Battery Detect: 1 when battery is below threshold setting (output) 00011: Direct Digital Input 00100: External Interrupt, falling edge (input) 00101: External Interrupt, rising edge (input) 00110: External Interrupt, state change (input) 00111: ADC Analog Input 01000: Reserved (Analog Test N Input) 01001: Reserved (Analog Test P Input) 01010: Direct Digital Output 01011: Reserved (Digital Test Output) 01100: Reserved (Analog Test N Output) 01101: Reserved (Analog Test P Output) 01110: Reference Voltage (output) 01111: TX Data CLK output to be used in conjunction with TX Data pin (output) 10000: TX Data input for direct modulation (input) 10001: External Retransmission Request (input) 10010: TX State (output) 10011: TX FIFO Almost Full (output) 10100: Reserved 10101: Reserved 10110: Reserved 10111: Reserved 11000: Reserved 11001: Reserved 11010: Reserved 11011: Reserved 11100: Reserved 11101: VDD else : GND

Register 0Dh. GPIO Configuration 2

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	gpiodrv2[1:0]		pup2	gpio2[4:0]				
Type	R/W		R/W	R/W				

Reset value = 00000000

Bit	Name	Function
7:6	gpiodrv2[1:0]	**GPIO Driving Capability Setting.**
5	pup2	**Pullup Resistor Enable on GPIO2.** When set to 1 the a 200 kΩ resistor is connected internally between VDD and the pin if the GPIO is configured as a digital input.
4:0	gpio2[4:0]	**GPIO2 pin Function Select.** 00000: Microcontroller Clock 00001: Wake-Up Timer: 1 when WUT has expired (output) 00010: Low Battery Detect: 1 when battery is below threshold setting (output) 00011: Direct Digital Input 00100: External Interrupt, falling edge (input) 00101: External Interrupt, rising edge (input) 00110: External Interrupt, state change (input) 00111: ADC Analog Input 01000: Reserved (Analog Test N Input) 01001: Reserved (Analog Test P Input) 01010: Direct Digital Output 01011: Reserved (Digital Test Output) 01100: Reserved (Analog Test N Output) 01101: Reserved (Analog Test P Output) 01110: Reference Voltage (output) 01111: TX Data CLK output to be used in conjunction with TX Data pin (output) 10000: TX Data input for direct modulation (input) 10001: External Retransmission Request (input) 10010: TX State (output) 10011: TX FIFO Almost Full (output) 10100: Reserved 10101: Reserved 10110: Reserved 10111: Reserved 11000: Reserved 11001: Reserved 11010: Reserved 11011: Reserved 11100: Reserved 11101: VDD else : GND

Register 0Eh. I/O Port Configuration

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	Reserved	extitst[2]	extitst[1]	extitst[0]	itsdo	dio2	dio1	dio0
Type	R	R	R	R	R/W	R/W	R/W	R/W

Reset value = 00000000

Bit	Name	Function
7	Reserved	**Reserved.**
6	extitst[2]	**External Interrupt Status.** If the GPIO2 is programmed to be external interrupt sources then the status can be read here.
5	extitst[1]	**External Interrupt Status.** If the GPIO1 is programmed to be external interrupt sources then the status can be read here.
4	extitst[0]	**External Interrupt Status.** If the GPIO0 is programmed to be external interrupt sources then the status can be read here.
3	itsdo	**Interrupt Request Output on the SDO Pin.** nIRQ output is present on the SDO pin if this bit is set and the nSEL input is inactive (high).
2	dio2	**Direct I/O for GPIO2.** If the GPIO2 is configured to be a direct output then the value on the GPIO pin can be set here. If the GPIO2 is configured to be a direct input then the value of the pin can be read here.
1	dio1	**Direct I/O for GPIO1.** If the GPIO1 is configured to be a direct output then the value on the GPIO pin can be set here. If the GPIO1 is configured to be a direct input then the value of the pin can be read here.
0	dio0	**Direct I/O for GPIO0.** If the GPIO0 is configured to be a direct output then the value on the GPIO pin can be set here. If the GPIO0 is configured to be a direct input then the value of the pin can be read here.

Register 0Fh. ADC Configuration

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	adcstart/ adcdone	adcsel[2:0]			adcref[1:0]		adcgain[1:0]	
Type	R/W	R/W			R/W		R/W	

Reset value = 00000000

Bit	Name	Function
7	adcstart/adc-done	**ADC Measurement Start Bit.** Reading this bit gives 1 if the ADC measurement cycle has been finished.
6:4	adcsel[2:0]	**ADC Input Source Selection.** The internal 8-bit ADC input source can be selected as follows: 000: Internal Temperature Sensor 001: GPIO0, single-ended 010: GPIO1, single-ended 011: GPIO2, single-ended 100: GPIO0(+) – GPIO1(–), differential 101: GPIO1(+) – GPIO2(–), differential 110: GPIO0(+) – GPIO2(–), differential 111: GND
3:2	adcref[1:0]	**ADC Reference Voltage Selection.** The reference voltage of the internal 8-bit ADC can be selected as follows: 0X: bandgap voltage (1.2 V) 10: VDD / 3 11: VDD / 2
1:0	adcgain[1:0]	**ADC Sensor Amplifier Gain Selection.** The full scale range of the internal 8-bit ADC in differential mode (see adcsel) can be set as follows: adcref[0] = 0: adcref[0] = 1: FS = 0.014 x (adcgain[1:0] + 1) x VDD FS = 0.021 x (adcgain[1:0] + 1) x VDD

Register 10h. ADC Sensor Amplifier Offset

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	Reserved				adcoffs[3:0]			
Type	R				R/W			

Reset value = xxxx0000

Bit	Name	Function
7:4	Reserved	**Reserved.**
3:0	adcoffs[3:0]	**ADC Sensor Amplifier Offset*.**
***Note:** The offset can be calculated as Offset = adcoffs[2:0] x VDD / 1000; MSB = adcoffs[3] = Sign bit.		

Register 11h. ADC Value

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	adc[7:0]							
Type	R							

Reset value = xxxxxxxx

Bit	Name	Function
7:0	adc[7:0]	**Internal 8 bit ADC Output Value.**

Register 12h. Temperature Sensor Calibration

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	tsrange[1:0]		entsoffs	entstrim	tstrim[3:0]			
Type	R/W		R/W	R/W	R/W			

Reset value = 00100000

Bit	Name	Function
7:6	tsrange[1:0]	**Temperature Sensor Range Selection.** (FS range is 0..1024 mV) 00: –40 °C .. 64 °C (full operating range), with 0.5 °C resolution (1 LSB in the 8-bit ADC) 01: –40 °C .. 85 °C, with 1 °C resolution (1 LSB in the 8-bit ADC) 11: 0 °C .. 85 °C, with 0.5 °C resolution (1 LSB in the 8-bit ADC) 10: –40 °F .. 216 °F, with 1 °F resolution (1 LSB in the 8-bit ADC)
5	entsoffs	**Temperature Sensor Offset to Convert from K to ºC.**
4	entstrim	**Temperature Sensor Trim Enable.**
3:0	tstrim[3:0]	**Temperature Sensor Trim Value.**

Register 13h. Temperature Value Offset

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	tvoffs[7:0]							
Type	R/W							

Reset value = 00000000

Bit	Name	Function
7:0	tvoffs[7:0]	**Temperature Value Offset.** This value is added to the measured temperature value. (MSB, tvoffs[8]: sign bit)

Note: If a new configuration is needed (e.g., for the WUT or the LDC), proper functionality is required. The function must first be disabled, then the settings changed, then enabled back on.

Register 14h. Wake-Up Timer Period 1

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	Reserved			wtr[4:0]				
Type	R/W			R/W				

Reset value = xxx00011

Bit	Name	Function
7:5	Reserved	**Reserved.**
4:0	wtr[4:0]	**Wake Up Timer Exponent (R) Value*.** Maximum value for R is decimal 20. A value greater than 20 will yield a result as if 20 were written. R Value = 0 can be written here.
***Note:** The period of the wake-up timer can be calculated as $T_{WUT} = (4 \times M \times 2^R) / 32.768$ ms. R = 0 is allowed, and the maximum value for R is decimal 20. A value greater than 20 will result in the same as if 20 was written.		

Register 15h. Wake-Up Timer Period 2

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	wtm[15:8]							
Type	R/W							

Reset value = 00000000

Bit	Name	Function
7:0	wtm[15:8]	**Wake Up Timer Mantissa (M) Value*.**
***Note:** The period of the wake-up timer can be calculated as $T_{WUT} = (4 \times M \times 2^R) / 32.768$ ms.		

Register 16h. Wake-Up Timer Period 3

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	wtm[7:0]							
Type	R/W							

Reset value = 00000001

Bit	Name	Function
7:0	wtm[7:0]	**Wake Up Timer Mantissa (M) Value*.** M[7:0] = 0 is not valid here. Write at least decimal 1.
***Note:** The period of the wake-up timer can be calculated as $T_{WUT} = (4 \times M \times 2^R) / 32.768$ ms.		

Register 17h. Wake-Up Timer Value 1

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	wtm[15:8]							
Type	R							

Reset value = xxxxxxxx

Bit	Name	Function
7:0	wtm[15:8]	**Wake Up Timer Current Mantissa (M) Value*.**
***Note:** The period of the wake-up timer can be calculated as $T_{WUT} = (4 \times M \times 2^{R}) / 32.768$ ms.		

Register 18h. Wake-Up Timer Value 2

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	wtm[7:0]							
Type	R							

Reset value = xxxxxxxx

Bit	Name	Function
7:0	wtm[7:0]	**Wake Up Timer Current Mantissa (M) Value*.**
***Note:** The period of the wake-up timer can be calculated as $T_{WUT} = (4 \times M \times 2^{R}) / 32.768$ ms.		

Register 1Ah. Low Battery Detector Threshold

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	Reserved			lbdt[4:0]				
Type	R			R/W				

Reset value = xxx10100

Bit	Name	Function
7:5	Reserved	**Reserved.**
4:0	lbdt[4:0]	**Low Battery Detector Threshold.** This threshold is compared to Battery Voltage Level. If the Battery Voltage is less than the threshold the Low Battery Interrupt is set. Default = 2.7 V.*
***Note:** The threshold can be calculated as $V_{threshold}$ = 1.7 + lbdt x 50 mV.		

Register 1Bh. Battery Voltage Level

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	Reserved			vbat[4:0]				
Type	R			R				

Reset value = xxxxxxxx

Bit	Name	Function
7:5	Reserved	**Reserved.**
4:0	vbat[4:0]	**Battery Voltage Level.** The battery voltage is converted by a 5 bit ADC. In Sleep Mode the register is updated in every 1 s. In other states it measures continuously.

Register 30h. Data Access Control

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	Reserved	lsbfrst	crcdonly	Reserved	enpactx	encrc	crc[1:0]	
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

Reset value = 10001101

Bit	Name	Function
7	Reserved	**Reserved.**
6	lsbfrst	**LSB First Enable.** The LSB of the data will be transmitted first if this bit is set.
5	crcdonly	**CRC Data Only Enable.** When this bit is set to 1 the CRC is calculated on the packet data fields only.
4	Reserved	**Reserved.**
3	enpactx	**Enable Packet TX Handling.** If FIFO Mode (dtmod = 10) is being used automatic packet handling may be enabled. Setting enpactx = 1 will enable automatic packet handling in the TX path. Register 30–4D allow for various configurations of the packet structure. Setting enpactx = 0 will not do any packet handling in the TX path. It will only transmit what is loaded to the FIFO.
2	encrc	**CRC Enable.** Cyclic Redundancy Check generation is enabled if this bit is set.
1:0	crc[1:0]	**CRC Polynomial Selection.** 00: CCITT 01: CRC-16 (IBM) 10: IEC-16 11: Biacheva

Register 31h. EZMAC® Status

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	Reserved						pktx	pksent
Type	R						R	R

Reset value = 00000000

Bit	Name	Function
7:2	Reserved	**Reserved.**
1	pktx	**Packet Transmitting.** When pktx = 1 the radio is currently transmitting a packet.
0	pksent	**Packet Sent.** A pksent = 1 a packet has been sent by the radio. (Same bit as in register 03, but reading it does not reset the IRQ)

Register 33h. Header Control 2

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	Reserved	hdlen[2:0]			fixpklen	synclen[1:0]		prealen[8]
Type	R	R/W			R/W	R/W		R/W

Reset value = 00100010

Bit	Name	Function
7	Reserved	**Reserved.**
6:4	hdlen[2:0]	**Header Length.** Length of header used if packet handler is enabled for TX (enpactx). Headers are transmitted in descending order. 000: No TX header 001: Header 3 010: Header 3 and 2 011: Header 3 and 2 and 1 100: Header 3 and 2 and 1 and 0
3	fixpklen	**Fix Packet Length.** When fixpklen = 1 the packet length (pklen[7:0]) is not included in the header. When fixpklen = 0 the packet length is included in the header.
2:1	synclen[1:0]	**Synchronization Word Length.** The value in this register corresponds to the number of bytes used in the Synchronization Word. The synchronization word bytes are transmitted in descending order. 00: Synchronization Word 3 01: Synchronization Word 3 and 2 10: Synchronization Word 3 and 2 and 1 11: Synchronization Word 3 and 2 and 1 and 0
0	prealen[8]	**MSB of Preamble Length.** See register Preamble Length.

Register 34h. Preamble Length

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	prealen[7:0]							
Type	R/W							

Reset value = 00001000

Bit	Name	Function
7:0	prealen[7:0]	**Preamble Length.** The value in the prealen[8:0] register corresponds to the number of nibbles (4 bits) in the packet. For example prealen[8:0] = '000001000' corresponds to a preamble length of 32 bits (8 x 4bits) or 4 bytes. The maximum preamble length is prealen[8:0] = 111111111 which corresponds to a 255 bytes Preamble. Writing 0 will have the same result as if writing 1, which corresponds to one single nibble of preamble.

Register 36h. Synchronization Word 3

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	sync[31:24]							
Type	R/W							

Reset value = 00101101

Bit	Name	Function
7:0	sync[31:24]	**Synchronization Word 3.** 4th byte of the synchronization word.

Register 37h. Synchronization Word 2

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	sync[23:16]							
Type	R/W							

Reset value = 11010100

Bit	Name	Function
7:0	sync[23:16]	**Synchronization Word 2.** 3rd byte of the synchronization word.

Register 38h. Synchronization Word 1

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	sync[15:8]							
Type	R/W							

Reset value = 00000000

Bit	Name	Function
7:0	sync[15:8]	**Synchronization Word 1.** 2nd byte of the synchronization word.

Register 39h. Synchronization Word 0

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	sync[7:0]							
Type	R/W							

Reset value = 00000000

Bit	Name	Function
7:0	sync[7:0]	**Synchronization Word 0.** 1st byte of the synchronization word.

Register 3Ah. Transmit Header 3

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	txhd[31:24]							
Type	R/W							

Reset value = 00000000

Bit	Name	Function
7:0	txhd[31:24]	**Transmit Header 3.** 4th byte of the header to be transmitted.

Register 3Bh. Transmit Header 2

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	txhd[23:16]							
Type	R/W							

Reset value = 00000000

Bit	Name	Function
7:0	txhd[23:16]	**Transmit Header 2.** 3rd byte of the header to be transmitted.

Register 3Ch. Transmit Header 1

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	txhd[15:8]							
Type	R/W							

Reset value = 00000000

Bit	Name	Function
7:0	txhd[15:8]	**Transmit Header 1.** 2nd byte of the header to be transmitted.

Register 3Dh. Transmit Header 0

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	txhd[7:0]							
Type	R/W							

Reset value = 00000000

Bit	Name	Function
7:0	txhd[7:0]	**Transmit Header 0.** 1st byte of the header to be transmitted.

Register 3Eh. Packet Length

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	pklen[7:0]							
Type	R/W							

Reset value = 00000000

Bit	Name	Function
7:0	pklen[7:0]	**Packet Length.** The value in the pklen[7:0] register corresponds directly to the number of bytes in the Packet. For example pklen[7:0] = '00001000' corresponds to a packet length of 8 bytes. The maximum packet length is pklen[7:0] = '11111111', a 255 byte packet. Writing 0 is possible, in this case we do not send any data in the packet.

Table 22. Internal Analog Signals Available on the Analog Test Bus

atb[3:0]	TESTp	TESTn
0	NC	NC
1	PLL_Icp_Test	PLL_IBG_5u
2	PLL_VBG_Bias	VSS_VCO
3	PLL_Vctrl	PLL_Iptat_5u
4	VCO_LDO_VBG	VCO_LDO_VOUT
5	RF_LDO_VBG	RF_LDO_VOUT
6	PLL_LDO_VBG	PLL_LDO_VOUT
7	RCOSC_65kout	RCOSC_VSS
8	NC	NC
9	LBD_Comp	LBD_VBG(TS)
10	TS_VBG	TS_VTemp
11	DIG_LDO_VBG	DIG_LDO_VFB
12	PA_Ramp	NC
13	ADC_VIN	ADC_VDAC
14	NC	NC
15	NC	NC

Register 51h. Digital Test Bus Select

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	Reserved	ensctest	dtb[5:0]					
Type	R/W	R/W	R/W					

Reset value = 00000000

Bit	Name	Function
7	Reserved	**Reserved.**
6	ensctest	**Scan Test Enable.** When set to 1 then GPIO0 will be the ScanEn input.
5:0	dtb[5:0]	**Digital Test Bus.** GPIO must be configured to Digital Test Mux output.

Table 23. Internal Digital Signals Available on the Digital Test Bus

dtb[4:0]	GPIO0	Signal	GPIO1	Signal	GPIO2	Signal
0	wkup_clk_32k	wake-up 32kHz clock	rbase_en	first divided clock	clk_base	timebase clock
1	wkup_clk_32k	wake-up 32kHz clock	wake_up	wake-up event	tm1sec	1 sec timebase
2	ts_adc_en	aux. ADC enable	adc_rdy_n	aux. ADC conversion ready	adc_done	aux. ADC measurement done
3	cont_lbd	low battery continuous mode	lbd_on	low battery ON signal	lbd	unfiltered output of LBD
4	div_clk_g	gated divided clock	uc_clk	microcontroller clock	ckout_rcsel	slow clock selected
5	en_div_sync	clock divider enable (sync'ed)	en_ckout	clock out enable	en_ckout_s	clock out enable (sync'ed)
6	osc30_en	oscillator enable	osc30_bias2x	oscillator bias control	xok	chip ready
7	xok	chip ready	zero_cap	cap. load zero	osc30_buff_en	buffer enable
8	tsadc_needed	aux. ADC enable	ext_retran	ext. retransmission request	tx_mod_gpio	TX modulation input
9	gpio_0_oen_n	GPIO0 output enable	gpio_0_aen	GPIO0 analog selection	gpio_0_aden	GPIO0 ADC input line enable
10	int_ack1	interrupt acknowledge 1	int_ack2	interrupt acknowledge 2	int_store	interrupt latch closed
11	ext_int2	ext. interrupt from GPIO2	irq_bit8	combined external status	msk_bit8	combined masked ext. int.
12	sdo_aux_sel	SDO aux. function select	sdo_aux	SDO aux. signal	nirq_aux_sel	nIRQ aux. function select
13	trdata_on_sdi	TX/RX data on SDI	tx_mod	TX modulation input	tx_clk_out	TX clock output
14	start_full_sync	RC osc. full calibration start	start_fine_sync	RC osc. fine calibration start	xtal_req	crystal req. for RC osc. cal.
15	coarse_rdy	RC osc. coarse cal. ready	fine_rdy	RC osc. fine cal. ready	xtal_req_sync	sync'ed crystal request
16	vco_cal_rst_s_n	VCO calibration reset	vco_cal	VCO calibration is running	vco_cal_done	VCO calibration done
17	vco_cal_en	VCO calibration enable	en_ref_cnt	reference counter enable	en_freq_cnt_s	frequency counter enable
18	vco_cal_en	VCO calibration enable	pos_diff	positive difference to goal	en_freq_cnt_s	frequency counter enable
19	dsm_clk_mux	DSM multiplexed clock	pll_fb_clk_tst	PLL feedback clock	pll_ref_clk_tst	PLL reference clock
20	dsm[0]	delta-sigma output	dsm[1]	delta-sigma output	dsm[2]	delta-sigma output
21	dsm[3]	delta-sigma output	pll_fbdiv15		dsm_rst_s_n	delta-sigma reset
22	pll_en	PLL enable: TUNE state	pllt0_ok	PLL initial settling OK	pllts_ok	PLL soft settling OK
23	ch_freq_req	frequency change request	pllts_ok	PLL soft settling OK	vco_cal_done	VCO calibration done
24	vco_cal_en	VCO calibration enable	pll_vbias_shunt_en	VCO bias shunt enable	prog_req	frequency recalculation req.
25	bandgap_en	bandgap enable	frac_div_en	fractional divider enable	buff3_en	buffer3 enable
26	pll_pfd_up	PFD up signal	pll_pfd_down	PFD down signal	pfd_up_down	PFD output change (XOR'ed)
27	pll_lock_detect	PLL lock detect	pll_en	PLL enable: TUNE state	pllt0_ok	PLL initial settling OK
28	pll_en	PLL enable: TUNE state	pll_lock_detect	PLL lock detect	pllts_ok	PLL soft settling OK
29	pwst[0]	internal power state	pwst[1]	internal power state	pwst[2]	internal power state

Table 23. Internal Digital Signals Available on the Digital Test Bus (Continued)

dtb[4:0]	GPIO0	Signal	GPIO1	Signal	GPIO2	Signal
30	xok	chip ready: READY state	pll_en	PLL enable: TUNE state	tx_en	TX enable: TX state
31	ts_en	temperature sensor enable	auto_tx_on	automatic TX ON	tx_off	TX OFF
32	ch_freq_req	frequency change request	return_tx	return from TX	pk_sent	packet sent
33	retran_req	retransmission request	tx_ffpt_store	TX FIFO pointer store	tx_ffpt_restore	TX FIFO pointer restore
34	pa_on_trig	PA ON trigger	dly_5us_ok	5 us delay expired	mod_dly_ok	modulator delay expired
35	tx_shdwn	TX shutdown	ramp_start	modulator ramp down start	ramp_done	modulator ramp down ended
36	pk_sent_dly	delayed packet sent	tx_shdwn_done	TX shutdown done	pa_ramp_en	PA ramp enable
37	tx_en	TX enable: TX state	ldo_rf_precharge	RF LDO precharge	pa_ramp_en	PA ramp enable
38	pa_on_trig	TX enable: TX state	dp_tx_en	packet handler (TX) enable	mod_en	modulator enable
39	reg_wr_en	register write enable	reg_rd_en	register rdead enable	addr_inc	register address increment
40	dp_tx_en	packet handler (TX) enable	data_start	start of TX data	pk_sent	packet has been sent
41	data_start	start of TX data	tx_out	packet handler TX data out	pk_sent	packet has been sent
42	ramp_done	ramp is done	data_start	start of TX data	pk_tx	packet is being transmitted
43	tx_ffaf	TX FIFO almost full	tx_fifo_wr_en	TX FIFO write enable	tx_ffem_tst	internal TX FIFO empty
44	clk_mod	modulator gated 10MHz clock	tx_clk	TX clock from NCO	rd_clk_x8	read clock = tx_clk / 10
45	mod_en	modulator enable	ramp_start	start modulator ramping down	ramp_done	modulator ramp done
46	data_start	data input start from PH	ook_en	OOK modulation enable	ook (also internal PN9)	OOK modulation
47	prog_req	freq. channel update request	freq_err	wrong freq. indication	dsm_rst_s_n	dsm sync. reset
48	mod_en	modulator enable	tx_rdy	TX ready	tx_clk	TX clock from NCO
49	dp_rx_en	packet handler (RX) enable	prea_valid	valid preamble	pk_srch	packet is being searched
50	pk_srch	packet is being searched	sync_ok	sync. word has been detected	rx_data	packet handler RX data input
51	pk_rx	packet is being received	sync_ok	sync. word has been detected	pk_valid	valid packet received
52	sync_ok	sync. word has been detected	crc_error	CRC error has been detected	hdch_error	header error detected
53	direct_mode	direct mode	rx_ffaf	RX FIFO almost full	rx_fifo_rd_en	RX FIFO read enable
54	bit_clk	bit clock	prea_valid	valid preamble	rx_data	demodulator RX data output
55	prea_valid	valid preamble	prea_inval	invalid preamble	ant_div_sw	antenna switch (algorythm)
56	sync_ok	sync. word has been detected	bit_clk	bit clock	rx_data	demodulator RX data output
57	demod phase[4]	demodulator phase MSB	demod phase [3]	demodulator MSB-1	demod phase [2]	demodulator MSB-2
58	prea_valid	valid preamble	demod_tst[2]	demodulator test	demod_tst[1]	demodulator test
59	agc_smp_clk	AGC sample clock	win_h_tp	window comparator high	win_l_tp	window comparator low dly'd
60	agc_smp_clk	AGC sample clock	win_h_dly_tp	window comparator high	win_l_dly_tp	window comparator low dly'd
61	ldc_on	active low duty cycle	pll_en	PLL enable: TUNE state	rx_en	RX enable: RX state
62	ldc_on	active low duty cycle	no_sync_det	no sync word detected	prea_valid	valid preamble
63	adc_en	ADC enable	adc_refdac_en	ADC reference DAC enable	adc_rst_n	combined ADC reset

Register 52h. TX Ramp Control

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	Reserved	txmod[2:0]			ldoramp[1:0]		txramp[1:0]	
Type	R/W	R/W			R/W		R/W	

Reset value = 00101111

Bit	Name	Function
7	Reserved	**Reserved**
6:4	txmod[2:0]	**TX Modulation Delay.** The time delay between PA enable and the beginning of the TX modulation to allow for PA ramp-up. It can be set from 0 µs to 28 µs in 4 µs steps. This also works during PA ramp down.
3:2	ldoramp[1:0]	**TX LDO Ramp Time.** The RF LDO is used to help ramp the PA to prevent VCO pulling and spectral splatter. 00: 5 µs 01: 10 µs 10: 15 µs 11: 20 µs
1:0	txramp[1:0]	**TX Ramp Time.** The PA is ramped up slowly to prevent VCO pulling and spectral splatter. This register sets the time the PA is ramped up. 00: 5 µs 01: 10 µs 10: 15 µs 11: 20 µs

The total settling time (cold start) of the PLL after the calibration can be calculated as $T_{CS} = T_S + T_O$.

Register 53h. PLL Tune Time

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	pllts[4:0]					pllt0		
Type	R/W					R/W		

Reset value = 01010010

Bit	Name	Function
7:3	pllts[4:0]	**PLL Soft Settling Time (T_S).** This register will set the settling time for the PLL from a previous locked frequency in Tune mode. The value is configurable between 0 µs and 310 µs, in 10 µs intervals. The default plltime corresponds to 100 µs. See formula above.
2:0	pllt0	**PLL Settling Time (T_O).** This register will set the time allowed for PLL settling after the calibrations are completed. The value is configurable between 0 µs and 70 µs, in 10 µs steps. The default pllt0 corresponds to 20 µs. See formula above.

Register 54h. PA Boost

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	Reserved[7:6]		inv_pre_th				ldo_pa_boost	pa_vbias_boost
Type	R/W		R/W				R/W	R/W

Reset value = 01010100

Bit	Name	Function
7:6	Reserved[7:6]	**Reserved.**
5:2	inv_pre_th[5:2]	**Invalid Preamble Threshold.**
1	ldo_pa_boost	**LDO PA Boost.**
0	pa_vbias_boost	**PA VBIAS Boost.**

Invalid preamble will be evaluated during this period: (invalid_preamble_Threshold x 4) x Bit Rate period.

Register 55h. Calibration Control

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	Reserved	xtalstarthalf	Reserved	enrcfcal	rccal	vcocaldp	vcocal	skipvco
Type	R	R/W	R	R/W	R/W	R/W	R/W	R/W

Reset value = x1x00100

Bit	Name	Function
7	Reserved	**Reserved.**
6	xtalstarthalf	**If Set, the Xtal Wake Time Period is Halved.**
5	Reserved	**Reserved.**
4	enrcfcal	**RC Oscillator Fine Calibration Enable.** If this bit is set to 1 then the RC oscillator performs fine calibration in every app. 30 s.
3	rccal	**RC Calibration Force.** If setting rccal = 1 will automatically perform a forced calibration of the 32 kHz RC Oscillator. The RC OSC will automatically be calibrated if the Wake-Up-Timer is enabled. The calibration takes 2 ms. The 32 kHz RC oscillator must be enabled to perform a calibration. Setting this signal from a 0 to 1 will initiate the calibration. This bit is cleared automatically.
2	vcocaldp	**VCO Calibration Double Precision Enable.** When this bit is set to 1 then the VCO calibration measures longer thus calibrates more precisely.
1	vcocal	**VCO Calibration Force.** If in Idle Mode and pllon = 1, setting vcocal = 1 will force a one time calibration of the synthesizer VCO. This bit is cleared automatically.
0	skipvco	**Skip VCO Calibration.** Setting skipvco = 1 will skip the VCO calibration when going from the Idle state to theTX state.

Register 56h. Modem Test

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	bcrfbyp	slicfbyp	dttype	oscdeten	ookth	refclksel	refclkinv	distogg
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Reset value = 00000000

Bit	Name	Function
7	bcrfbyp	**If set, BCR phase compensation will be bypassed.**
6	slicfbyp	**If set, slicer phase compensation will be bypassed.**
5	dttype	**Dithering Type.** If low and dither enabled, we add +1/0, otherwise if high and dithering enabled, we add ±1.
4	oscdeten	If low, the ADC Oscillation Detection mechanism is allowed to work. If set, we disable the function.
3	ookth	If set, in OOK mode, the slicer threshold will be estimated by 8 bits of preamble. By default, this bit is low and the demod estimate the threshold after 4 bits.
2	refclksel	**Delta-Sigma Reference Clock Source Selection** 1: 10 MHz 0: PLL
1	refclkinv	**Delta-Sigma Reference Clock Inversion Enable.**
0	distogg	If reset, the discriminator toggling is disabled.

Register 57h. Charge Pump Test

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	pfdrst	fbdiv_rst	cpforceup	cpforcedn	cdonly	cdcurr[2:0]		
Type	R/W	R/W	R/W	R/W	R/W	R/W		

Reset value = 00000000

Bit	Name	Function
7	pfdrst	**Direct Control to Analog.**
6	fbdiv_rst	**Direct Control to Analog.**
5	cpforceup	**Charge Pump Force Up.**
4	cpforcedn	**Charge Pump Force Down.**
3	cdconly	**Charge Pump DC Offset Only.**
2:0	cdcurr[2:0]	**Charge Pump DC Current Selection.**

Register 58h. Charge Pump Current Trimming/Override

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	cpcurr[1:0]		cpcorrov	cporr[4:0]				
Type	R/W		R/W	R/W				

Reset value = 100xxxxx

Bit	Name	Function
7:6	cpcurr[1:0]	**Charge Pump Current (Gain Setting).** Changing these bits will change the BW of the PLL. The default setting is adequate for all data rates.
5	cpcorrov	**Charge Pump Correction Override Enable.**
4:0	cpcorr[4:0]	**Charge Pump Correction Value.** During read, you read what the Charge Pump sees. If cpcorrov = 1, then the value you write will go to the Charge Pump, and will also be the value you read. By default, cpcorr[4:0] wakes up as all Zeros.

Register 59h. Divider Current Trimming/Delta-Sigma Test

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	txcorboosten	fbdivhc	d3trim[1:0]		d2trim[1:0]		d1p5trim[1:0]	
Type	R/W	R/W	R/W		R/W		R/W	

Reset value = 10000000

Bit	Name	Function
7	txcorboosten	**If this is Set, then vcocorr (reg 5A[5:2]) = 1111 during TX Mode and VCO CAL followed by TX.**
6	fbdivhc	**Feedback (fractional) Divider High Current Enable (+5 µA).**
5:4	d3trim[1:0]	**Divider 3 Current Trim Value.**
3:2	d2trim[1:0]	**Divider 2 Current Trim Value.**
1:0	d1p5trim[1:0]	**Divider 1.5 (div-by-1.5) Current Trim Value.**

Register 5Ah. VCO Current Trimming

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	txcurboosten	vcocorrov	vcocorr[3:0]				vcocur[1:0]	
Type	R/W	R/W	R/W				R/W	

Reset value = 00000011

Bit	Name	Function
7	txcurboosten	**If this is Set, then vcocur = 11 during TX Mode and VCO CAL followed by TX.**
6	vcocorrov	**VCO Current Correction Override.**
5:2	vcocorr[3:0]	**VCO Current Correction Value.**
1:0	vcocur[1:0]	**VCO Current Trim Value.**

Register 5Bh. VCO Calibration/Override

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	vcocalov/vcdone	vcocal[6:0]						
Type	R/W	R/W						

Reset value = 00000000

Bit	Name	Function
7	vco-calov/vcdone	**VCO Calibration Override/Done.** When vcocalov = 0 the internal VCO calibration results may be viewed by reading the vcocal register. When vcocalov = 1 the VCO results may be overridden externally through the SPI by writing to the vcocal register. Reading this bit gives 1 if the calibration process has been finished.
6:0	vcocal[6:0]	**VCO Calibration Results.**

Register 5Ch. Synthesizer Test

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	dsmdt	vcotype	enoloop	dsmod	dsorder[1:0]		dsrstmode	dsrst
Type	R/W	R	R/W	R/W	R/W		R/W	R/W

Reset value = 0x001110

Bit	Name	Function
7	dsmdt	**Enable DSM Dithering.** If low, dithering is disabled.
6	vcotype	**VCO Type.** 0: basic, constant K 1: single varactor, changing K
5	enoloop	**Open Loop Mode Enable.**
4	dsmod	**Delta-Sigma Modulus.** 0: 64 000 1: 65 536
3:2	dsorder[1:0]	**Delta-Sigma Order.** 00: 0 order 01: 1st order 10: 2nd order 11: Mash 111
1	dsrstmode	**Delta-Sigma Reset Mode.**
0	dsrst	**Delta-Sigma Reset.**

Register 5Dh. Block Enable Override 1

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	enmix	enina	enpga	enpa	enbf5	endv32	enbf12	enmx2
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Reset value = 00000000

Bit	Name	Function
7	enmix	**Mixer Enable Override.**
6	enlna	**LNA Enable Override.**
5	enpga	**PGA Enable Override.**
4	enpa	**Power Amplifier Enable Override.**
3	enbf5	**Buffer 5 Enable Override.**
2	endv32	**Divider 3_2 Enable Override.**
1	enbf12	**Buffer 1_2 Enable Override.**
0	enmx2	**Multiplexer 2 Enable Override.**

Register 5Eh. Block Enable Override 2

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	ends	enldet	enmx3	enbf4	enbf3	enbf11	enbf2	pllreset
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Reset value = 01000000

Bit	Name	Function
7	ends	**Delta-Sigma Enable Override.**
6	enldet	**Lock Detect Enable.** (direct control, does not need override!)
5	enmx3	**Multiplexer 3 Enable Override.**
4	enbf4	**Buffer 4 Enable Override.**
3	enbf3	**Buffer 3 Enable Override.**
2	enbf11	**Buffer 1_1 Enable Override.**
1	enbf2	**Buffer 2 Enable Override.**
0	pllreset	**PLL Reset Enable Override.**

Register 5Fh. Block Enable Override 3

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	enfrdv	endv31	endv2	endv1p5	dvbshunt	envco	encp	enbg
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Reset value = 00000000

Bit	Name	Function
7	enfrdv	**Fractional Divider Enable Override.**
6	endv31	**Divider 3_1 Enable Override.**
5	endv2	**Divider 2 Enable Override.**
4	endv1p5	**Divider 1.5 (div-by-1.5) Enable Override.**
3	dvbshunt	**VCO Bias Shunt Enable Override Mode.**
2	envco	**VCO Enable Override.**
1	encp	**Charge Pump Enable Override.**
0	enbg	**Bandgap Enable Override.**

Register 62h. Crystal Oscillator/Power-on-Reset Control

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	pwst[2:0]			clkhyst	enbias2x	enamp2x	bufovr	enbuf
Type	R			R/W	R/W	R/W	R/W	R/W

Reset value = xxx00100

Bit	Name	Function
7:5	pwst[2:0]	**Internal Power States of the Chip.** LP: 000 RDY: 001 Tune: 011 TX: 010
4	clkhyst	**Clock Hysteresis Setting.**
3	enbias2x	**2 Times Higher Bias Current Enable.**
2	enamp2x	**2 Times Higher Amplification Enable.**
1	bufovr	**Output Buffer Enable Override.** If set to 1 then the enbuf bit controls the output buffer. 0: output buffer is controlled by the state machine. 1: output buffer is controlled by the enbuf bit.
0	enbuf	**Output Buffer Enable.** This bit is active only if the bufovr bit is set to 1.

Register 63h. RC Oscillator Coarse Calibration/Override

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	rccov	rcc[6:0]						
Type	R/W	R/W						

Reset value = 00000000

Bit	Name	Function
7	rccov	**RC Oscillator Coarse Calibration Override.** When rccov = 0 the internal Coarse Calibration results may be viewed by reading the rcccal register. When rccov = 1 the Coarse results may be overridden externally through the SPI by writing to the rcccal register.
6:0	rcc[6:0]	**RC Oscillator Coarse Calibration Override Value/Results.**

Register 64h. RC Oscillator Fine Calibration/Override

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	rcfov	rcf[6:0]						
Type	R/W	R/W						

Reset value = 00000000

Bit	Name	Function
7	rcfov	**RC Oscillator Fine Calibration Override.** When rcfov = 0 the internal Fine Calibration results may be viewed by reading the rcfcal register. When rcfov = 1 the Fine results may be overridden externally through the SPI by writing to the rcfcal register.
6:0	rcf[6:0]	**RC Oscillator Fine Calibration Override Value/Results.**

Register 65h. LDO Control Override

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	enspor	enbias	envcoldo	enifldo	enrfldo	enpllldo	endigldo	endigpwdn
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Reset value = 10000001

Bit	Name	Function
7	enspor	**Smart POR Enable.**
6	enbias	**Bias Enable.**
5	envcoldo	**VCO LDO Enable.**
4	enifldo	**IF LDO Enable.**
3	enrfldo	**RF LDO Enable.**
2	enpllldo	**PLL LDO Enable.**
1	endigldo	**Digital LDO Enable.**
0	endigpwdn	**Digital Power Domain Powerdown Enable in Idle Mode.**

Register 66h. LDO Level Settings

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	enovr	enxtal	ents	enrc32	Reserved	diglvl		
Type	R/W	R/W	R/W	R/W	R	R/W		

Reset value = 00000011

Bit	Name	Function
7	enovr	**Enable Overrides.** If high, ovr values are output to the blocks and can enable or disable them, if low, some ovr value can only enable the blocks.
6	enxtal	**Xtal Override Enable Value.**
5	ents	**Temperature Sensor Enable.**
4	enrc32	**32K Oscillator Enable.**
3	Reserved	**Reserved.**
2:0	diglvl	**Digital LDO Level Setting.**

Register 6Bh. GFSK FIR Filter Coefficient Address

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	Reserved					firadd[2:0]		
Type	R					R/W		

Reset value = xxxxx000

Bit	Name	Function
7:3	Reserved	**Reserved.**
2:0	firadd[2:0]	**GFSK FIR Filter Coefficient Look-up Table Address.** The address for Gaussian filter coefficients used in the TX path. The default GFSK setting is for BT = 0.5. It is not needed to change or load the GFSK Coefficients if BT = 0.5 is satisfactory for the system. 000: i_coe0 (Default = d1) 001: i_coe1 (Default = d3) 010: i_coe2 (Default = d6) 011: i_coe3 (Default = d10) 100: i_coe4 (Default = d15) 101: i_coe5 (Default = d19) 110: i_coe6 (Default = d20)

Register 6Ch. GFSK FIR Filter Coefficient Value

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	Reserved		firval[5:0]					
Type	R/W		R/W					

Reset value = xxxxx000

Bit	Name	Function
7:6	Reserved	**Reserved.**
5:0	firval[5:0]	**FIR Coefficient Value in the lOok-up Table Addressed by the firadd[2:0].** The default coefficient can be read or modified.

Register 6Dh. TX Power

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	Reserved				lna_sw	txpow[2:0]		
Type	R				R/W	R/W		

Reset value = xxxx1000

Bit	Name	Function
7:4	Reserved	**Reserved.**
3	lna_sw	**LNA Switch Controller.** If set, lna_sw control from the digital will go high during TX modes, and low during other times. If reset, the digital control signal is low at all times.
2:0	txpow[2:0]	**TX Output Power.** The output power is configurable in ~3 dBm steps.

Register 6Eh. TX Data Rate 1

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	txdr[15:8]							
Type	R/W							

Reset value = 00001010

Bit	Name	Function
7:0	txdr[15:8]	**Data Rate Upper Byte.** See formula above.

The data rate can be calculated as: TX_DR = 10^3 x txdr[15:0] / 2^{16} [kbps] (if address 70[5] = 0) **or**
The data rate can be calculated as: TX_DR = 10^3 x txdr[15:0] / 2^{21} [kbps] (if address 70[5] = 1)

Register 6Fh. TX Data Rate 0

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	txdr[7:0]							
Type	R/W							

Reset value = 00111101

Bit	Name	Function
7:0	txdr[7:0]	**Data Rate Lower Byte.** See formula above. Defaults = 40 kbps.

Register 70h. Modulation Mode Control 1

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	Reserved		txdtrtscale	enphpwdn	manppol	enmaninv	enmanch	enwhite
Type	R		R/W	R/W	R/W	R/W	R/W	R/W

Reset value = 00001100

Bit	Name	Function
7:6	Reserved	**Reserved.**
5	txdtrtscale	**This bit should be set for Data Rates below 30 kbps.**
4	enphpwdn	**If set, the Packet Handler will be powered down when chip is in low power mode.**
3	manppol	**Manchester Preamble Polarity (will transmit a series of 1 if set, or series of 0 if reset).** This bit affects ONLY the transmitter side, not the receiver. This is valid ONLY if Manchester Mode is enabled.
2	enmaninv	**Manchester Data Inversion is Enabled if this bit is set.**
1	enmanch	**Manchester Coding is Enabled if this bit is set.**
0	enwhite	**Data Whitening is Enabled if this bit is set.**

Register 71h. Modulation Mode Control 2

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	trclk[1:0]		dtmod[1:0]		eninv	fd[8]	modtyp[1:0]	
Type	R/W		R/W		R/W	R/W	R/W	

Reset value = 00000000

Bit	Name	Function
7:6	trclk[1:0]	**TX Data Clock Configuration.** 00: No TX Data CLK is available (asynchronous mode – Can only work with modulations FSK or OOK). 01: TX Data CLK is available via the GPIO (one of the GPIO's should be programmed as well). 10: TX Data CLK is available via the SDO pin. 11: TX Data CLK is available via the nIRQ pin.
5:4	dtmod[1:0]	**Modulation Source.** 00: Direct Mode using TX_Data function via the GPIO pin (one of the GPIO's should be programmed accordingly as well) 01: Direct Mode using TX_Data function via the SDI pin (only when nSEL is high) 10: FIFO Mode 11: PN9 (internally generated)
3	eninv	**TX Data.**
2	fd[8]	**MSB of Frequency Deviation Setting, see "Register 72h. Frequency Deviation".**
1:0	modtyp[1:0]	**Modulation Type.** 00: Unmodulated carrier 01: OOK 10: FSK 11: GFSK (enable TX Data CLK (trclk[1:0]) when direct mode is used)

The frequency deviation can be calculated: Fd = 625 Hz x fd[8:0].

Register 72h. Frequency Deviation

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	fd[7:0]							
Type	R/W							

Reset value = 00100000

Bit	Name	Function
7:0	fd[7:0]	**Frequency Deviation Setting.** See formula above.

Note: It's recommended to use modulation index of 1 or higher (maximum allowable modulation index is 32). The modulation index is defined by $2F_N/F_R$ were F_D is the deviation and R_B is the data rate. When Manchester coding is enabled the modulation index is defined by F_D/R_B.

Register 73h. Frequency Offset 1

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	fo[7:0]							
Type	R/W							

Reset value = 00000000

Bit	Name	Function
7:0	fo[7:0]	**Frequency Offset Setting.** The frequency offset can be calculated as Offset = 156.25 Hz x (hbsel + 1) x fo[7:0]. fo[9:0] is a twos complement value.

Register 74h. Frequency Offset 2

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	Reserved						fo[9:8]	
Type	R						R/W	

Reset value = 00000000

Bit	Name	Function
7:2	Reserved	**Reserved.**
1:0	fo[9:8]	**Upper Bits of the Frequency Offset Setting.** fo[9] is the sign bit. The frequency offset can be calculated as Offset = 156.25 Hz x (hbsel + 1) x fo[7:0]. fo[9:0] is a twos complement value.

Register 75h. Frequency Band Select

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	Reserved	sbsel	hbsel	fb[4:0]				
Type	R	R/W	R/W	R/W				

Reset value = 01110101

Bit	Name	Function
7	Reserved	**Reserved.**
6	sbsel	**Side Band Select.**
5	hbsel	**High Band Select.** Setting hbsel = 1 will choose the frequency range from 480–930 MHz (high bands). Setting hbsel = 0 will choose the frequency range from 240–479.9 MHz (low bands).
4:0	fb[4:0]	**Frequency Band Select.** Every increment corresponds to a 10 MHz Band for the Low Bands and a 20 MHz Band for the High Bands. Setting fb[4:0] = 00000 corresponds to the 240–250 MHz Band for hbsel = 0 and the 480–500 MHz Band for hbsel = 1. Setting fb[4:0] = 00001 corresponds to the 250–260 MHz Band for hbsel = 0 and the 500–520 MHz Band for hbsel = 1.

The RF carrier frequency can be calculated as follows:

$f_{carrier} = (f_b+24+(f_c+f_o) / 64000) \times 10000 \times (hbsel+1) + (f_{hch} \times f_{hs} \times 10)$ [kHz],

where parameters f_c, f_o, f_b and hb_sel come from registers 73h–77h. Parameters f_{hch} and f_{hs} come from register 79h and 7Ah.

Register 76h. Nominal Carrier Frequency

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	fc[15:8]							
Type	R/W							

Reset value = 10111011

Bit	Name	Function
7:0	fc[15:8]	**Nominal Carrier Frequency Setting.** See formula above.

Register 77h. Nominal Carrier Frequency

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	fc[7:0]							
Type	R/W							

Reset value = 10000000

Bit	Name	Function
7:0	fc[7:0]	**Nominal Carrier Frequency Setting.** See formula above.

Register 78h. Miscellaneous Settings

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	Reserved[7:4]				Alt_PA_Seq	rcosc_cal[2:0]		
Type	R/W				R/W	R/W		

Reset value = 01111000

Bit	Name	Function
7:4	Reserved[7:4]	**Reserved.**
3	Alt_PA_Seq	**Alternative PA sequencing.** If set, we will enable the alternative PA sequence. By default, this is not enabled.
2:0	rcosc_cal[2:0]	**rcosc_cal[2:0].** Fine changes on the RC OSC Calibration target frequency, to help compensate for “calibration biases.” **This register should not be changed by costumers.**

Register 79h. Frequency Hopping Channel Select

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	fhch[7:0]							
Type	R/W							

Reset value = 00000000

Bit	Name	Function
7:0	fhch[7:0]	**Frequency Hopping Channel Number.**

Register 7Ah. Frequency Hopping Step Size

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	fhs[7:0]							
Type	R/W							

Reset value = 00000000

Bit	Name	Function
7:0	fhs[7:0]	**Frequency Hopping Step Size in 10 kHz Increments.** See formula for the nominal carrier frequency at "Register 76h. Nominal Carrier Frequency".

Register 7Bh. Turn Around and 15.4 Length Compliance

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	15.4 Length	Reserved[6:3]				turn_around_en	phase[1:0]	
Type	R/W	R/W				R/W	R/W	

Reset value = 01111011

Bit	Name	Function
7	15.4 Length	**15.4 Packet Length Compliance.** If set, then PK Length definition for both TX and RX will also include the CRC bytes, If reset, then the Length refers ONLY to the DATA payload. For example, writing “9” to this register when it is set, means we are sending/expecting “7” bytes of DATA, and the other “2” should be the CRC (CRC should be enabled separately).
6:3	Reserved[6:3]	**Reserved.**
2	turn_around_en	**Turn Around Enable.** Enabling for the turn around functionality.
1:0	phase[1:0]	**Turn Around Phase.** The RX to TX and vice-versa change in frequency will happen (if bit [2] is set) at the last byte, and these two registers set the bit position in which the frequency shifts should occur. Make sure it does not happen to early otherwise the last bits will be missed.

Register 7Ch. TX FIFO Control 1

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	Reserved		txafthr[5:0]					
Type	R/W		R/W					

Reset value = 00110111

Bit	Name	Function
7:6	Reserved	**Reserved.**
5:0	txafthr[5:0]	**TX FIFO Almost Full Threshold.**

Register 7Dh. TX FIFO Control 2

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	Reserved		txfaethr[5:0]					
Type	R/W		R/W					

Reset value = 00000100

Bit	Name	Function
7:6	Reserved	**Reserved.**
5:0	txfaethr[5:0]	**TX FIFO Almost Empty Threshold.**

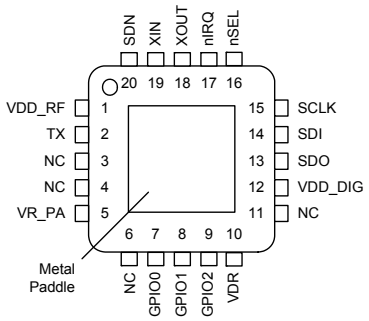
Register 7Fh. FIFO Access

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	fifod[7:0]							
Type	R/W							

Reset value = NA

Bit	Name	Function
7:0	fifod[7:0]	**FIFO Data.** A Write (R/W = 1) to this Address will begin a Burst Write to the TX FIFO. The FIFO will be loaded in the same manner as a Burst SPI Write but the SPI address will not be incremented. To conclude the TX FIFO Write the SEL pin should be brought HIGH, in the same manner.

12. Pin Descriptions: Si4031/32



Pin	Pin Name	I/O	Description
1	VDD_RF	VDD	+1.8 to +3.6 V supply voltage input to all analog +1.7 V regulators. The recommended V_{DD} supply voltage is +3.3 V.
2	TX	O	Transmit output pin. The PA output is an open-drain connection so the L-C match must supply VDD (+3.3 VDC nominal) to this pin.
3	NC	—	No Connect.
4	NC	—	No Connect.
5	VR_PA	I	Voltage Reference Power Amplifier.
6	NC	—	No Connect.
7	GPIO_0	I/O	General Purpose Digital I/O that may be configured through the registers to perform various functions including: Microcontroller Clock Output, FIFO status, POR, Wake-Up timer, Low Battery Detect, TRSW, AntDiversity control, etc. See the SPI GPIO Configuration Registers, Address 0Bh, 0Ch, and 0Dh for more information.
8	GPIO_1	I/O	
9	GPIO_2	I/O	
10	VDR	O	Regulated Output Voltage of the Digital 1.7 V Regulator. A 1 µF decoupling capacito is required.
11	NC	—	No Connect.
12	VDD_DIG	VDD	+1.8 to +3.6 V supply voltage input to the Digital +1.7 V Regulator. The recommended V_{DD} supply voltage is +3.3 V.
13	SDO	O	0–V_{DD} V digital output that provides a serial readback function of the internal control registers.
20	SDI	I	Serial Data input. 0–V_{DD} V digital input. This pin provides the serial data stream for the 4-line serial data bus.
21	SCLK	I	Serial Clock input. 0–V_{DD} V digital input. This pin provides the serial data clock function for the 4-line serial data bus. Data is clocked into the Si4031/32 on positive edge transitions.
22	nSEL	I	Serial Interface Select input. 0– V_{DD} V digital input. This pin provides the Select/Enable function for the 4-line serial data bus. The signal is also used to signify burst read/write mode.
23	nIRQ	O	General Microcontroller Interrupt Status output. When the Si4031/32 exhibits anyone of the Interrupt Events the nIRQ pin will be set low=0. Please see the Control Logic registers section for more information on the Interrupt Events. The Microcontroller can then determine the state of the interrupt by reading a corresponding SPI Interrupt Status Registers, Address 03h and 04h.
24	XOUT	O	Crystal Oscillator Output. Connect to an external 30 MHz crystal or leave floating if driving the Xin pin with an external signal source.
25	XIN	I	Crystal Oscillator Input. Connect to an external 30 MHz crystal or to an external source. If using an external clock source with no crystal, dc coupling with a nominal 0.8 VDC level is recommended with a minimum ac amplitude of 700 mVpp.
26	SDN	I	Shutdown input pin. 0–V_{DD} V digital input. SDN should be = 0 in all modes except Shutdown mode. When SDN =1 the chip will be completely shutdown and the contents of the registers will be lost.
PKG	PADDLE_GND	GND	The exposed metal paddle on the bottom of the Si4031/32 supplies the RF and circuit ground(s) for the entire chip. It is very important that a good solder connection is made between this exposed metal paddle and the ground plane of the PCB underlying the Si4031/32.

13. Ordering Information

Part Number*	Description	Package Type	Operating Temperature
Si4031-A0-FM Si4032-V2-FM	ISM EZRadioPRO Transmitter	QFN-20 Pb-free	–40 to 85 °C
***Note:** Add an “(R)” at the end of the device part number to denote tape and reel option; 2500 quantity per reel.			

14. Package Information

Figure 29 illustrates the package details for the Si4031/32.

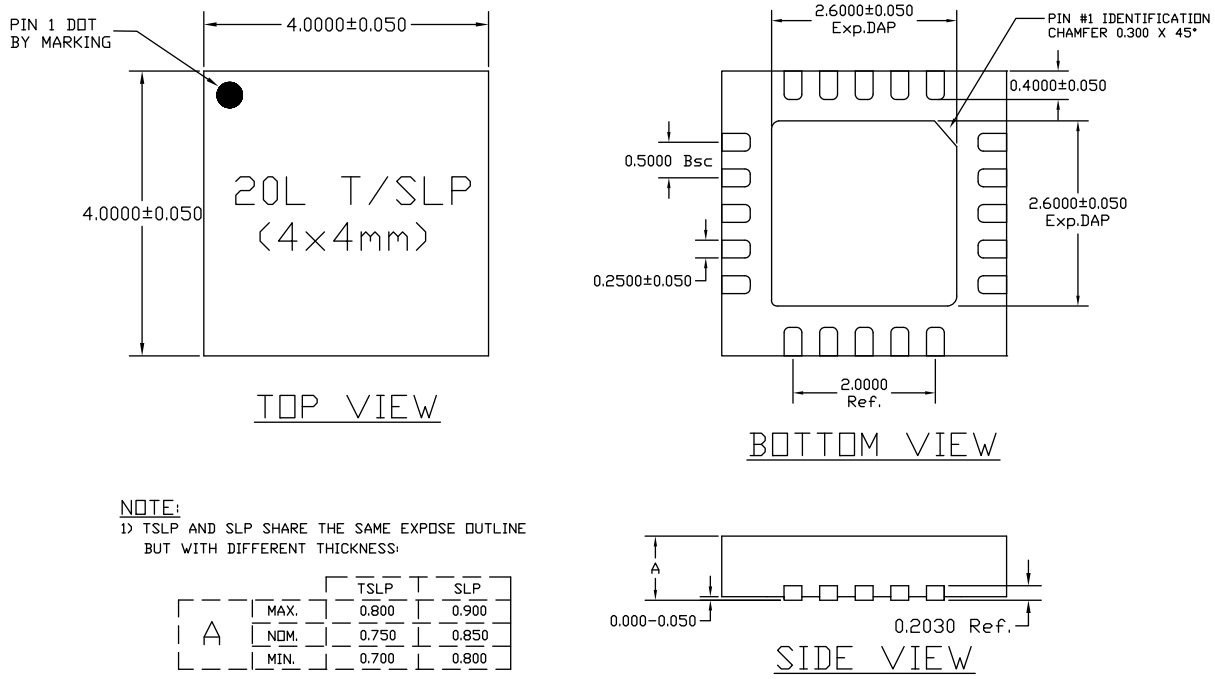


Figure 29. QFN-20 Package Dimensions

DOCUMENT CHANGE LIST

Revision 0.1 to Revision 0.2

- Updated package to QFN20 for consistency across product family

NOTES:

CONTACT INFORMATION

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