



# PJQ4463AP

## 60V P-Channel Enhancement Mode MOSFET

**Voltage** -60 V **Current** -4.2 A

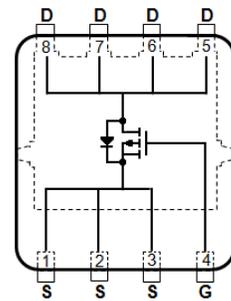
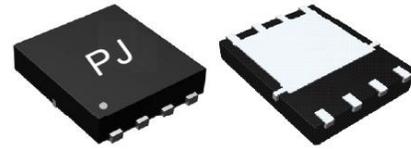
### Features

- $R_{DS(ON)}$ ,  $V_{GS}@-10V$ ,  $I_D@-6A < 68m\Omega$
- $R_{DS(ON)}$ ,  $V_{GS}@-4.5V$ ,  $I_D@-3A < 85m\Omega$
- Advanced Trench Process Technology
- High density cell design for ultra low on-resistance
- Lead free in compliance with EU RoHS 2.0
- Green molding compound as per IEC 61249 standard

### Mechanical Data

- Case : DFN3333-8L Package
- Terminals : Solderable per MIL-STD-750, Method 2026
- Approx. Weight : 0.001 ounces, 0.03 grams

DFN3333-8L



### Maximum Ratings and Thermal Characteristics ( $T_A=25^\circ\text{C}$ unless otherwise noted)

PARAMETER		SYMBOL	LIMIT	UNITS
Drain-Source Voltage		$V_{DS}$	-60	V
Gate-Source Voltage		$V_{GS}$	$\pm 20$	V
Continuous Drain Current	$T_A=25^\circ\text{C}$	$I_D$	-4.2	A
	$T_A=70^\circ\text{C}$		-3.4	
Pulsed Drain Current <sup>(Note 1)</sup>		$I_{DM}$	-16.8	
Power Dissipation	$T_A=25^\circ\text{C}$	$P_D$	2.1	W
	$T_A=70^\circ\text{C}$		1.3	
Operating Junction and Storage Temperature Range		$T_J, T_{STG}$	-55~150	$^\circ\text{C}$
Typical Thermal Resistance Junction to Ambient, $t \leq 10s$ <sup>(Note 5)</sup>		$R_{\theta JA}$	59.5	$^\circ\text{C/W}$

- Limited only By Maximum Junction Temperature



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## Electrical Characteristics (T<sub>A</sub>=25°C unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNITS
<b>Static</b>						
Drain-Source Breakdown Voltage	BV <sub>DSS</sub>	V <sub>GS</sub> =0V, I <sub>D</sub> =-250μA	-60	-	-	V
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =-250μA	-1	-1.53	-2.5	
Drain-Source On-State Resistance	R <sub>DS(on)</sub>	V <sub>GS</sub> =-10V, I <sub>D</sub> =-6A	-	55	68	mΩ
		V <sub>GS</sub> =-4.5V, I <sub>D</sub> =-3A	-	71	85	
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> =-60V, V <sub>GS</sub> =0V	-	-	-1	μA
Gate-Source Leakage Current	I <sub>GSS</sub>	V <sub>GS</sub> =±20V, V <sub>DS</sub> =0V	-	-	±100	nA
<b>Dynamic</b> (Note 6)						
Total Gate Charge	Q <sub>g</sub>	V <sub>DS</sub> =-30V, I <sub>D</sub> =-6A, V <sub>GS</sub> =-10V (Note 3)	-	17	-	nC
Gate-Source Charge	Q <sub>gs</sub>		-	2.8	-	
Gate-Drain Charge	Q <sub>gd</sub>		-	3.6	-	
Input Capacitance	C <sub>iss</sub>	V <sub>DS</sub> =-30V, V <sub>GS</sub> =0V, f=1.0MHZ	-	879	-	pF
Output Capacitance	C <sub>oss</sub>		-	70	-	
Reverse Transfer Capacitance	C <sub>rss</sub>		-	47	-	
Turn-On Delay Time	t <sub>d(on)</sub>	V <sub>DD</sub> =-30V, I <sub>D</sub> =-1A, V <sub>GS</sub> =-10V, R <sub>G</sub> =6Ω (Note 3)	-	8.4	-	ns
Turn-On Rise Time	t <sub>r</sub>		-	30	-	
Turn-Off Delay Time	t <sub>d(off)</sub>		-	52	-	
Turn-Off Fall Time	t <sub>f</sub>		-	16	-	
<b>Drain-Source Diode</b>						
Maximum Continuous Drain-Source Diode Forward Current	I <sub>S</sub>	---	-	-	-4.2	A
Diode Forward Voltage	V <sub>SD</sub>	I <sub>S</sub> =-1A, V <sub>GS</sub> =0V	-	-0.73	-1	V

NOTES :

1. Pulse width ≤ 300μs, Duty cycle ≤ 2%
2. Essentially independent of operating temperature typical characteristics
3. Repetitive rating, pulse width limited by junction temperature T<sub>J(MAX)</sub>=150°C. Ratings are based on low frequency and duty cycles to keep initial T<sub>J</sub> = 25°C.
4. The maximum current rating is package limited
5. R<sub>θJA</sub> is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. Mounted on a 1 inch<sup>2</sup> with 2oz.square pad of copper
6. Guaranteed by design, not subject to production testing.



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## TYPICAL CHARACTERISTIC CURVES

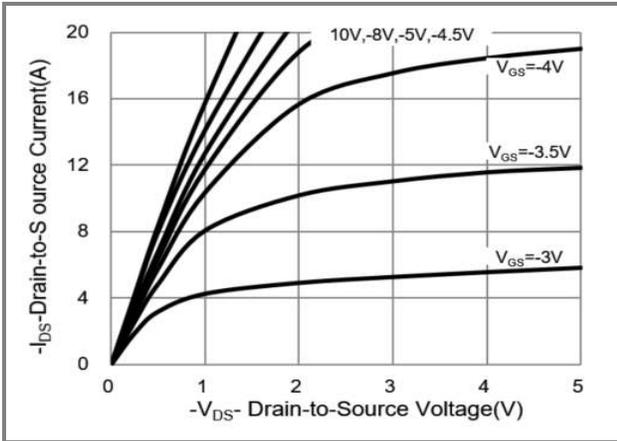


Fig.1 On-Region Characteristics

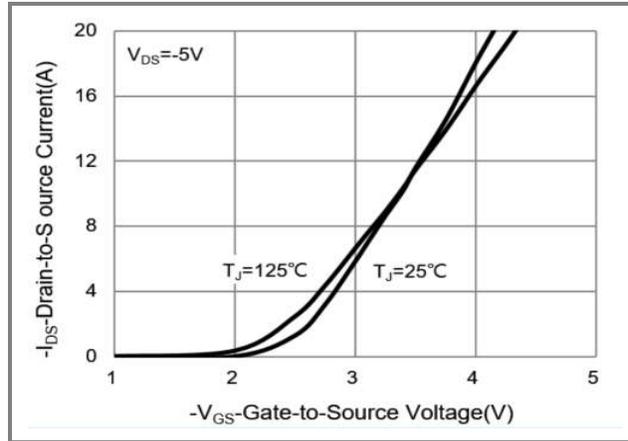


Fig.2 Transfer Characteristics

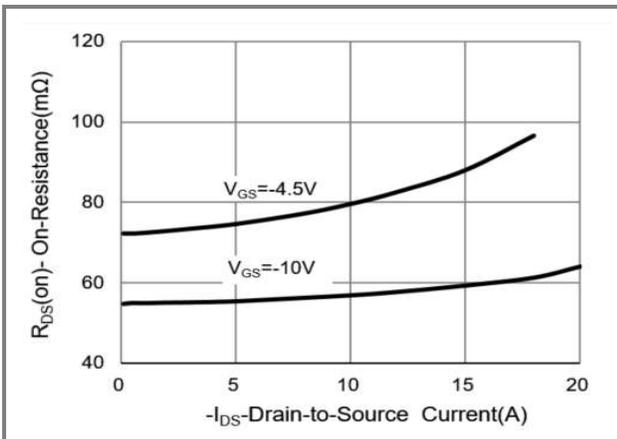


Fig.3 On-Resistance vs. Drain Current

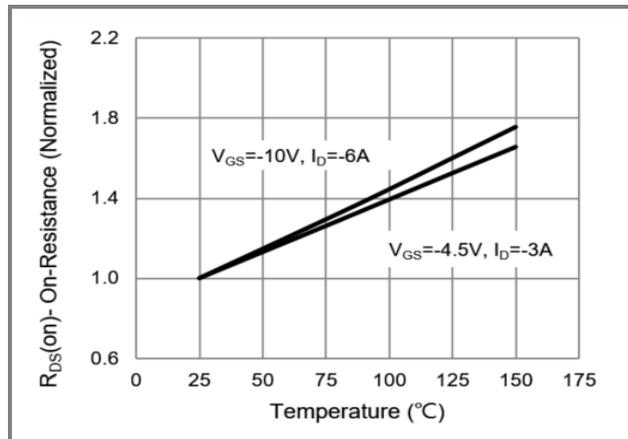


Fig.4 On-Resistance vs. Junction temperature

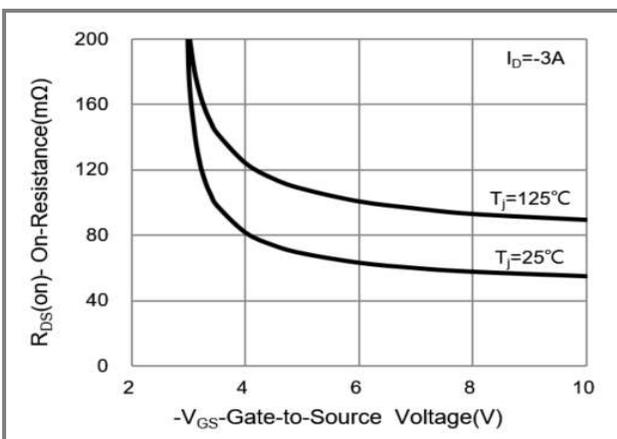


Fig.5 On-Resistance Variation with VGS.

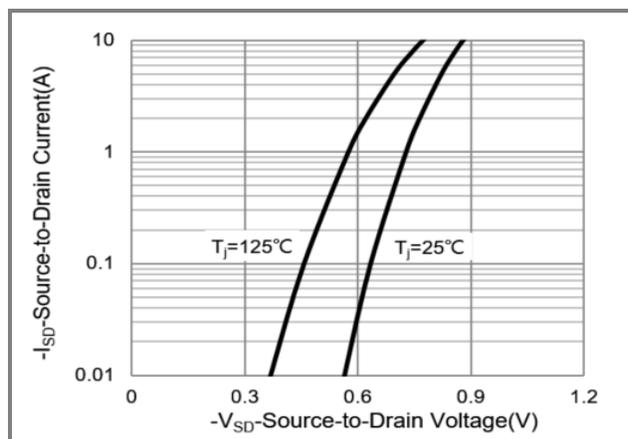


Fig.6 Source-Drain Diode Forward Voltage



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## TYPICAL CHARACTERISTIC CURVES

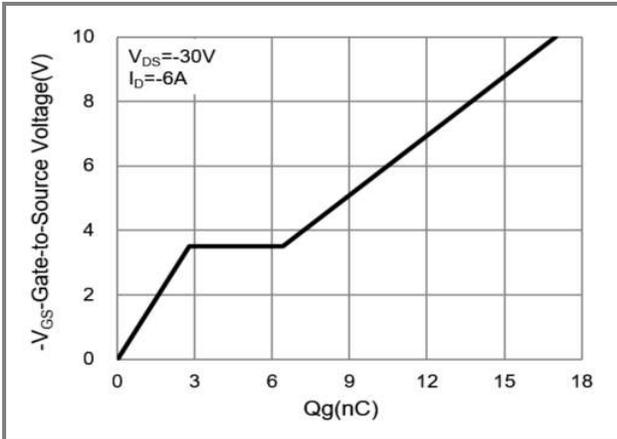


Fig.7 Gate-Charge Characteristics

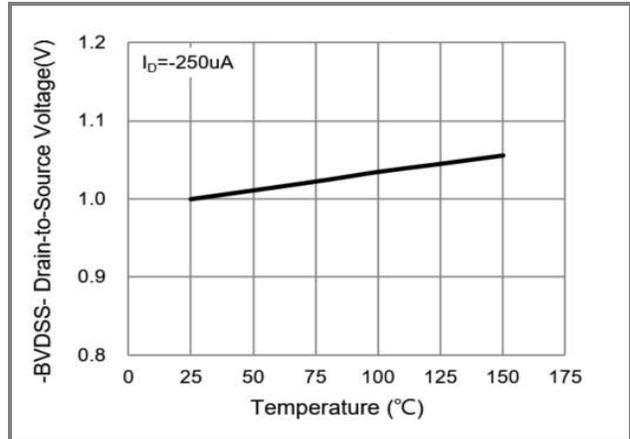


Fig.8 Breakdown Voltage Variation vs. Temperature.

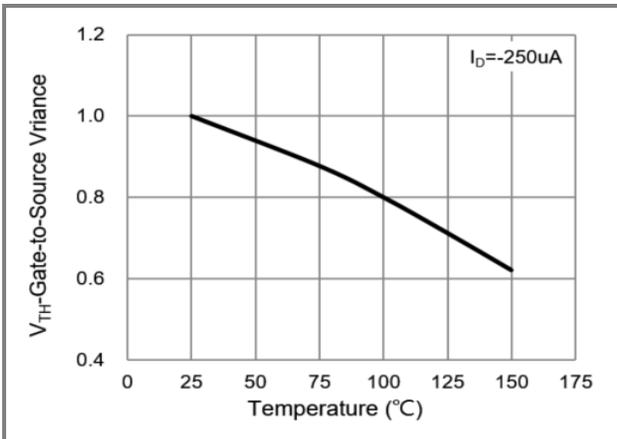


Fig.9 Threshold Voltage Variation with Temperature

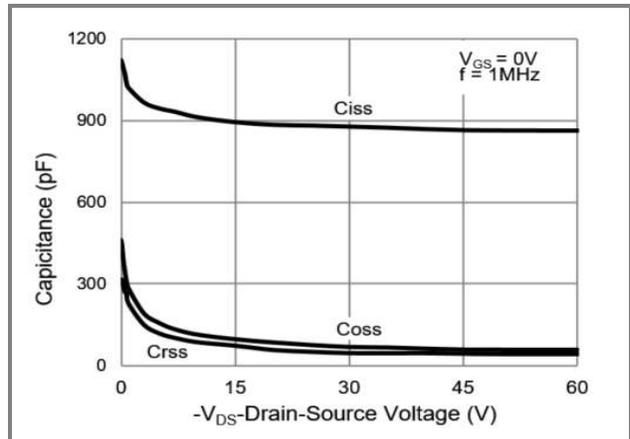


Fig.10 Capacitance vs. Drain-Source Voltage

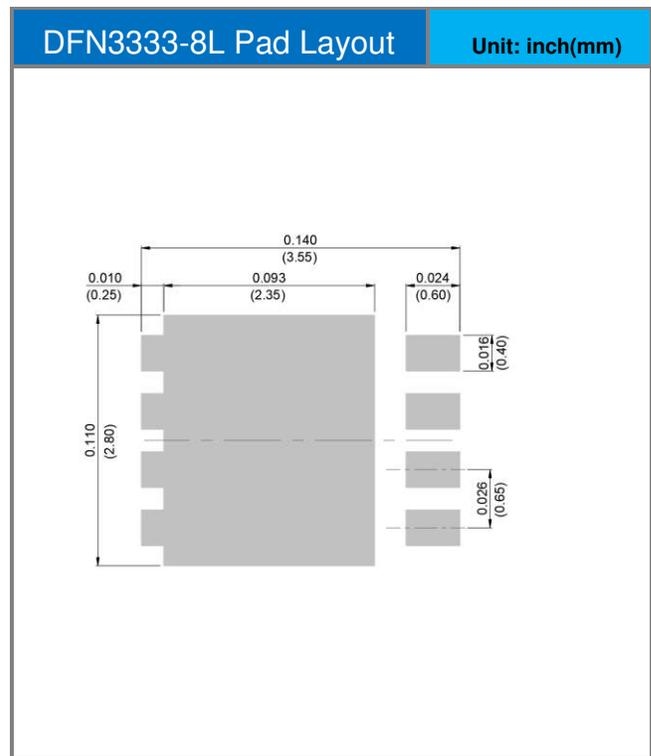
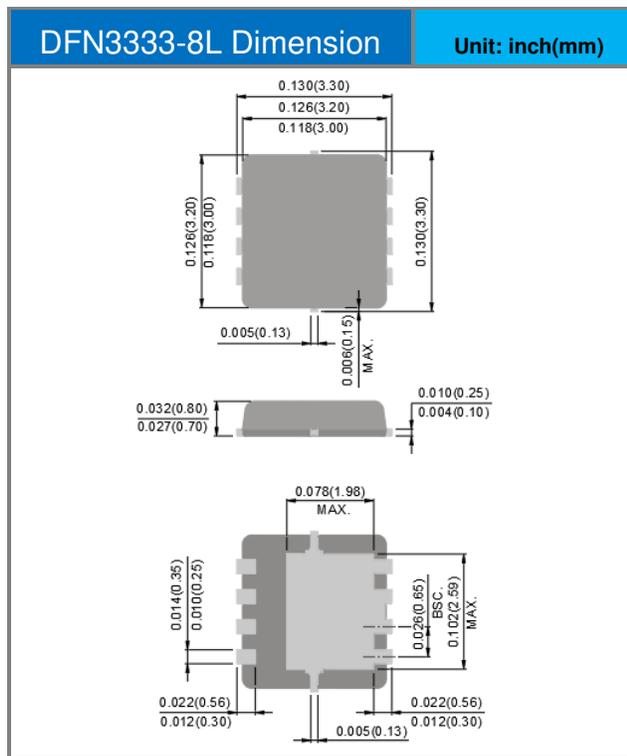


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## PART NO. PACKING CODE VERSION

Part No. Packing Code	Package Type	Packing Type	Marking	Version
PJQ4463AP_R2_00001	DFN3333-8L	5K pcs / 13" reel	4463	Halogen free RoHS compliant

## Packaging Information & Mounting Pad Layout





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