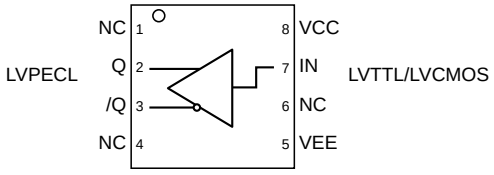
Features

- **Guaranteed AC performance over temp and voltage:**
  - **DC-to-800MHz f_{MAX}**
  - **<100ps IN-to-OUT t_{pd}**
- **Ultra-low jitter design:**
  - **<1ps$_{RMS}$ random jitter**
  - **<10ps$_{PP}$ deterministic jitter**
  - **<1ps$_{RMS}$ cycle-to-cycle jitter**
  - **<1ps$_{PP}$ total jitter (clock)**
- **Differential LVPECL output**
- **I_{CC} max. 20mA**
- **Q output will default HIGH with inputs open**
- **Power supply 3.3V ±10% or 5.0V ±10%**
- **–40°C to +85°C temperature range**
- **Available in ultra-small 8-pin (2mm × 2mm) MLF™ package**

Applications

- **High-speed logic**
- **Data communications systems**
- **Wireless communications systems**
- **Telecom systems**



8-Pin MLF™ (2mm × 2mm)

Precision Edge®

General Description

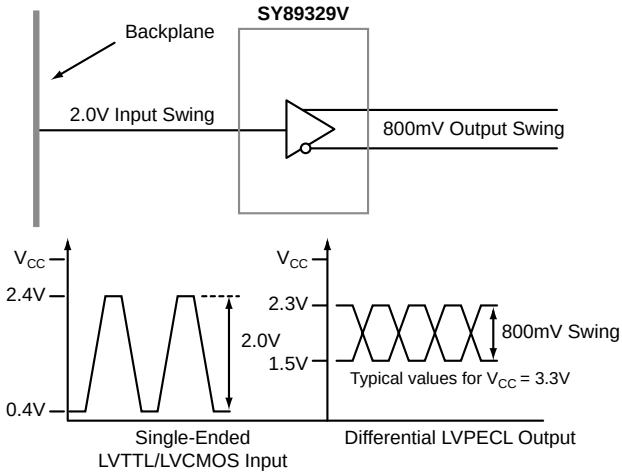
The SY89329V is a TTL/CMOS-to-differential PECL translator. Capable of running from a 3.3V or 5V supply, the part can be used in either LVTTL/LVCMOS/LVPECL or TTL/CMOS/PECL systems.

The device requires only a single positive supply of 3.3V or 5V; no negative supply is required.

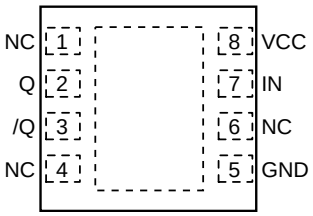
The ultra-small 8-pin MLF™ package of the SY89329V makes it ideal for applications where space, performance, and low power are at a premium. For applications that require a dual translator in this same ultra-small MLF™ package, consider the SY89322V.

All support documentation can be found on Micrel's web site at www.micrel.com.

Functional Block Diagram



Precision Edge is a registered trademark of Micrel, Inc.
*Micro*LeadFrame and MLF are trademarks of Amkor Technology, Inc.



8-Pin MLF™

Ordering Information

Part Number	Package Type	Operating Range	Package Marking	Lead Finish
SY89329VMITR	MLF-8	Industrial	329	Sn-Pb
SY89329VMGTR	MLF-8	Industrial	329 with Pb-Free bar-line indicator	Pb-Free NiPdAu

Pin Number	Pin Name	Pin Function
7	IN	Single-ended input: This is the LVTTL/LVCMOS input to the device. Input switching threshold is $V_{CC}/2$. If left floating, Q output will default HIGH.
8	VCC	Positive power supply. Bypass with 0.1µF||0.01µF low ESR capacitors.
2, 3	Q, /Q	Differential LVPECL output: This output is the output of the device. Terminate with 50Ω to V_{CC}–2V. See “Output Interface Applications” section. Defaults HIGH if IN is floating.
5	GND, Exposed Pad	Ground: Ground pin and exposed pad must be connected to the same ground plane.
1, 4, 6	NC	No connect.

Absolute Maximum Ratings[1]

Supply Voltage (V_{CC}) ..... –0.5V to + 4.0V
Input Voltage (V_{IN}) ..... –0.5V to V_{CC}
LVPECL Output Voltage (V_{OUT}) .... V_{CC}–1.0V to V_{CC}+0.5V
LVPECL Output Current (I_{OUT})
  Continuous 50mA
  Surge 100mA
Input Current
  Source or sink current on IN ..... ±50mA
Lead Temperature (soldering, 20 sec.) ..... +260°C
Storage Temperature (T_S) ..... –65°C to +150°C

Operating Ratings[2]

Supply Voltage (V_{CC}) ..... 3.0V to 3.3V
  ..... 4.5V to 5.5V
Ambient Temperature (T_A) ..... –40°C to +85°C
Package Thermal Resistance[3]
MLF™ (θ_{JA})
  Still-Air ..... 93°C/W
  500lfpm ..... 87°C/W
MLF™ (Ψ_{JB})
  Junction-to-board ..... 32°C/W

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{CC}	Power Supply		3.0	3.3	3.6	V
			4.5	5.0	5.5	V
I_{CC}	Power Supply Current	No load, max. V_{CC}.			20	mA

T_A= –40°C to +85°C; Unless otherwise stated.

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{IH}	Input HIGH Voltage (IN, /IN)		2.0			V
V_{IL}	Input LOW Voltage (IN, /IN)				0.8	V
I_{IH}	Input HIGH Current	V_{IN} = 2.7V			20	µA
		V_{IN} = V_{CC}			100	µA
I_{IL}	Input LOW Current	V_{IN} = 0.5V			–0.2	mA
V_{IK}	Input Clamp Voltage	I_{IN} = –18mA			–1.2	V

V_{CC} = 3.3V ±10% or 5V ±10%; T_A = –40°C to +85°C; R_L = 50Ω to V_{CC}–2V, or equivalent, unless otherwise stated.

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{OH}	Output HIGH Voltage Q, /Q	**Note 2**	V_{CC}–1.080		V_{CC} –0.880	V
V_{OL}	Output LOW Voltage Q, /Q		V_{CC}–1.830		V_{CC} –1.550	V
V_{OUT}	Output Voltage Swing Q, /Q	See Figure 1a.	600	800		mV
$V_{DIFF-OUT}$	Differential Output Voltage Swing Q, /Q	See Figure 1b.	1200	1600		mV

Notes:

1. Permanent device damage may occur if the “Absolute Maximum Ratings” are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to the absolute maximum ratings conditions for extended periods may affect device reliability.
2. The data sheet limits are not guaranteed if the device is operated beyond the operating ratings.
3. Package Thermal Resistance assumes exposed pad is soldered (or equivalent) to the devices most negative potential on the PCB. Ψ_{JB} uses 4-layer θ_{JA} in still-air unless otherwise stated.
4. The circuit is designed to meet the DC specifications shown in the above table after thermal equilibrium has been established.

V_{CC} = 3.3V ±10% or 5.0V ±10%; T_A = –40°C to +85°C, unless otherwise stated.

Symbol	Parameter	Condition	Min	Typ	Max	Units
f_{MAX}	Maximum Operating Frequency	$V_{OUT} \geq 350mV$			800	MHz
t_{pd}	Propagation Delay IN-to-Q, /IN-to-/Q		100		600	ps
t_{JITTER}	Random Jitter (RJ)	**Note 6**			1	ps_{RMS}
	Deterministic Jitter (DJ)	**Note 7**			10	ps_{PP}
	Cycle-to-Cycle Jitter	**Note 8**			1	ps_{RMS}
	Total Jitter (TJ)	**Note 9**			25	ps_{PP}
t_r, t_f	Rise / Fall Time (20% to 80%) Q, /Q	At full output swing.	200		500	ps

Notes:

5. Measured with outputs loaded with 50Ω to V_{CC} –2V unless otherwise stated. See "Timing Diagrams" section for definition of parameters. High-frequency AC-parameters are guaranteed by design and characterization.
6. RJ is measured with a K28.7 comma detect character pattern, measured at f_{MAX}.
7. DJ is measured at f_{MAX}, with both K28.5 and 2^{23}-1 PRBS pattern
8. Cycle-to-cycle jitter definition: the variation of periods between adjacent cycles, Tn–Tn–1 where T is the time between rising edges of the output signal.
9. Total jitter definition: with an ideal clock input of frequency ≤ f_{MAX}, no more than one output edge in 10^{12} output edges will deviate by more than the specified peak-to-peak jitter value.

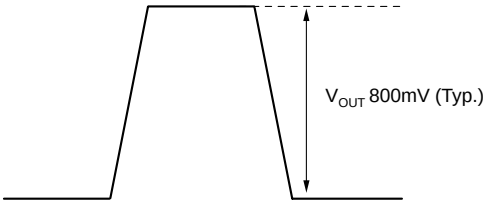


Figure 1a. Single-Ended Voltage Swing

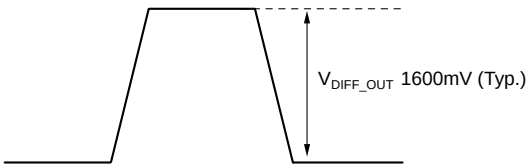


Figure 1b. Differential Voltage Swing

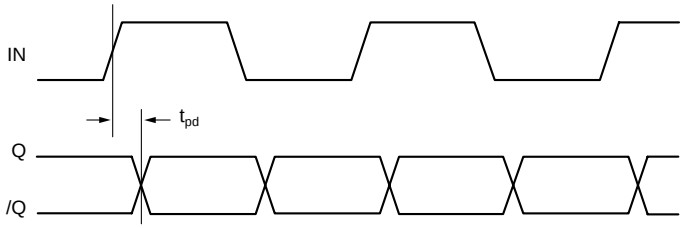


Figure 2. Timing Diagram

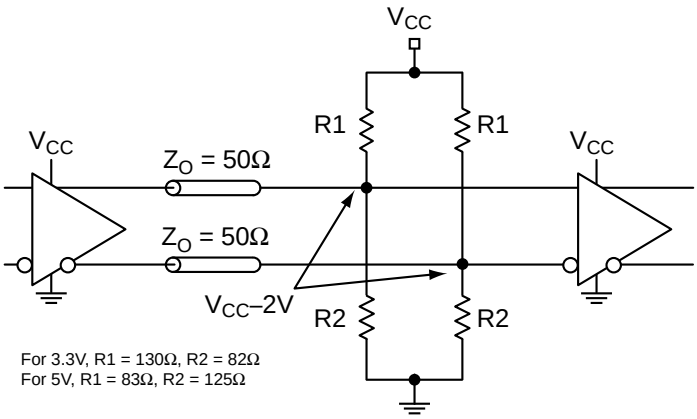


Figure 3a. Parallel Thevenin-Equivalent Termination

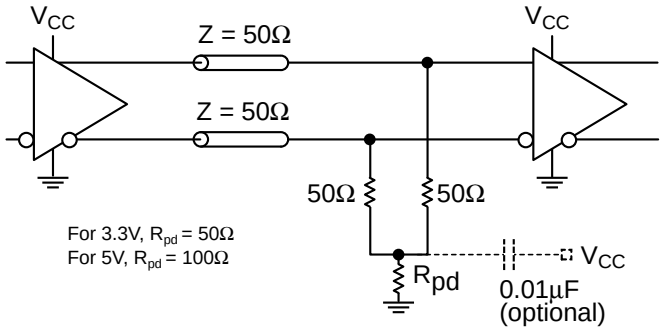


Figure 3b. Three-Resistor Termination

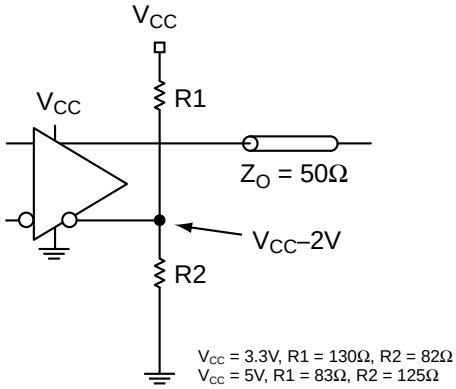
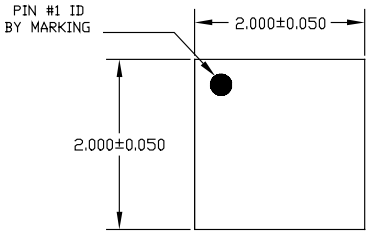
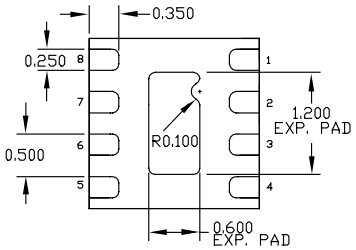


Figure 3c. Terminating Unused I/O

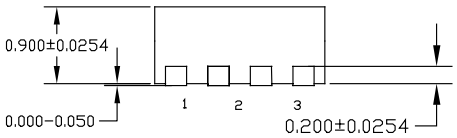
Part Number	Function	Data Sheet Link
SY89322V	3.3V/5V Dual LVTTL/LVCMOS-to-Differential LVPECL Translator	www.micrel.com/product-info/products/sy89322v.shtml
	MLF™ Application Note	www.amkor.com/products/notes_papers/MLF_AppNote_0902.pdf
HBW Solutions	New Products and Applications	www.micrel.com/product-info/products/solutions.shtml



TOP VIEW



BOTTOM VIEW



SIDE VIEW

NOTE:
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. MAX. PACKAGE WARPAGE IS 0.05 mm.
3. MAXIMUM ALLOWABE BURRS IS 0.076 mm IN ALL DIRECTIONS.
4. PIN #1 ID ON TOP WILL BE LASER/INK MARKED.

MICREL, INC. 2180 FORTUNE DRIVE SAN JOSE, CA 95131 USA

TEL + 1 (408) 944-0800 FAX + 1 (408) 474-1000 WEB http://www.micrel.com