

**Advantech**

**AQD-D4U4GE21-SG**

**Datasheet**

Rev. 1.0  
2015-03-16

## Description

DDR4 ECC U-DIMMs are high-speed and low power memory modules that use 512Mx8bits DDR4 SDRAM in FBGA package and a 4K-bit serial EEPROM on a 288-pin printed circuit board. DDR4 ECC U-DIMMs are dual In-Line memory modules and are intended for mounting into 288-pin edge connector sockets.

The synchronous design allows precise cycle control with the use of system clock. Data I/O transactions are possible on both edges of DQS. The large range of operation frequencies and programmable latencies allow the same device to be useful for a variety of high bandwidth and high performance memory system applications.

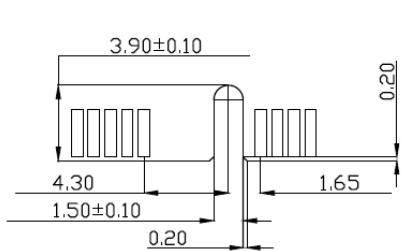
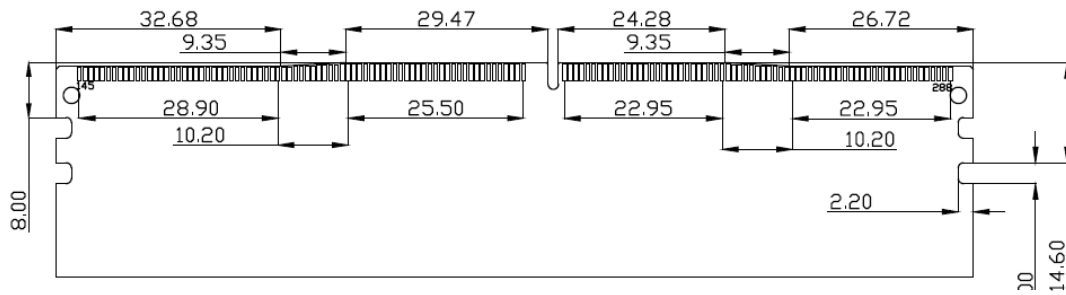
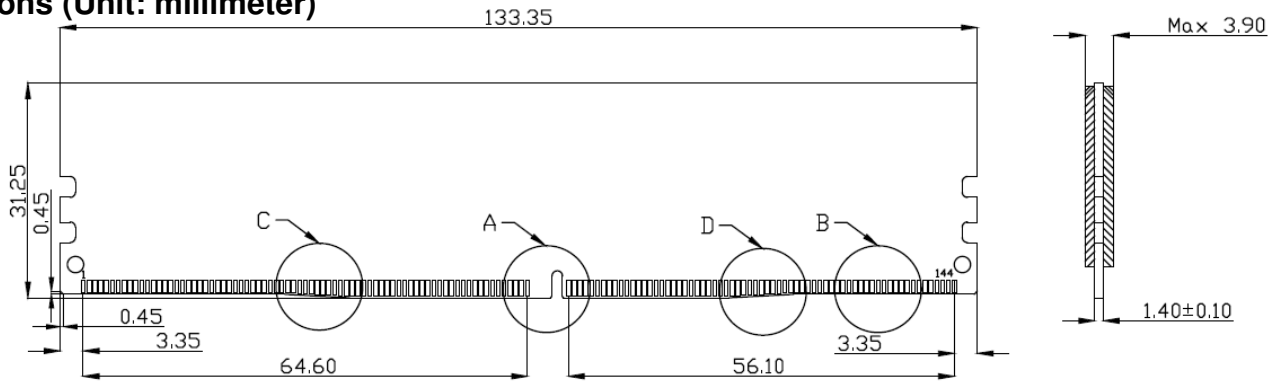
## Features

- RoHS compliant
- JEDEC standard 1.2V  $\pm$  0.06V power supply
- VDDQ=1.2V  $\pm$  0.06V
- Clock Freq: 1067MHZ for 2133Mb/s/Pin.
- Programmable CAS Latency: 10,11,12,13,14,15,16
- Programmable Additive Latency (Posted /CAS):  
0,CL-2 or CL-1 clock
- Programmable /CAS Write Latency (CWL)  
= 11, 14(DDR4-2133)
- 8 bit pre-fetch
- Burst Length: 4, 8
- Bi-directional Differential Data-Strobe
- On Die Termination with ODT pin
- Serial presence detect with EEPROM
- On DIMM Thermal Sensor
- Asynchronous reset

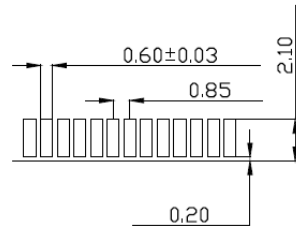
## Pin Identification

Symbol	Function
A0–A14	SDRAM address bus
BA0, BA1	SDRAM bank select
BG0, BG1	SDRAM bank group select
RAS <sub>n</sub>	SDRAM row address strobe
CAS <sub>n</sub>	SDRAM column address strobe
WE <sub>n</sub>	SDRAM write enable
CS0 <sub>n</sub> , CS1 <sub>n</sub>	DIMM Rank Select Lines
CKE0, CKE1	SDRAM clock enable lines
ODT0, ODT1	SDRAM on-die termination control lines
ACT <sub>n</sub>	SDRAM activate
DQ0–DQ63	DIMM memory data bus
CB0–CB7	DIMM ECC check bits
DM <sub>n</sub> /DBI <sub>n</sub> /	Input data mask and data bus inversion
DQS0 <sub>t</sub> –DQS8 <sub>t</sub>	SDRAM data strobes (positive line of differential pair)
DQS0 <sub>c</sub> –DQS8 <sub>c</sub>	SDRAM data strobes (negative line of differential pair)
CK0 <sub>t</sub> , CK1 <sub>t</sub>	SDRAM clocks (positive line of differential pair)
CK0 <sub>c</sub> , CK1 <sub>c</sub>	SDRAM clocks (negative line of differential pair)
PARITY	SDRAM parity input
VDD	SDRAM I/O and core power supply
VREFCA	SDRAM command/address reference supply
VSS	Power supply return (ground)
VDDSPD	Serial SPD EEPROM positive power supply
SCL	I <sup>2</sup> C serial bus clock for EEPROM
SDA	I <sup>2</sup> C serial bus data line for EEPROM
SA0–SA2	I <sup>2</sup> C slave address select for EEPROM
ALERT <sub>n</sub>	SDRAM ALERT <sub>n</sub>
VPP	SDRAM Supply
RESET <sub>n</sub>	Set DRAMs to a Known State
EVENT <sub>n</sub>	SPD signals a thermal event has occurred
VTT	SDRAM I/O termination supply
RFU	Reserved for future use
NC	No Connection

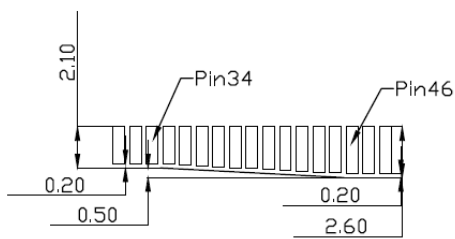
**Dimensions (Unit: millimeter)**



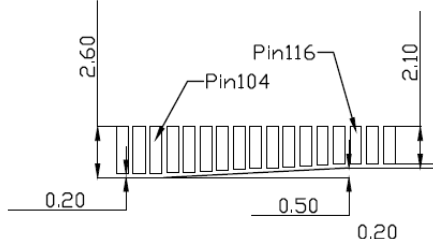
Detail A



Detail B



Detail C



Detail D

**Note:**

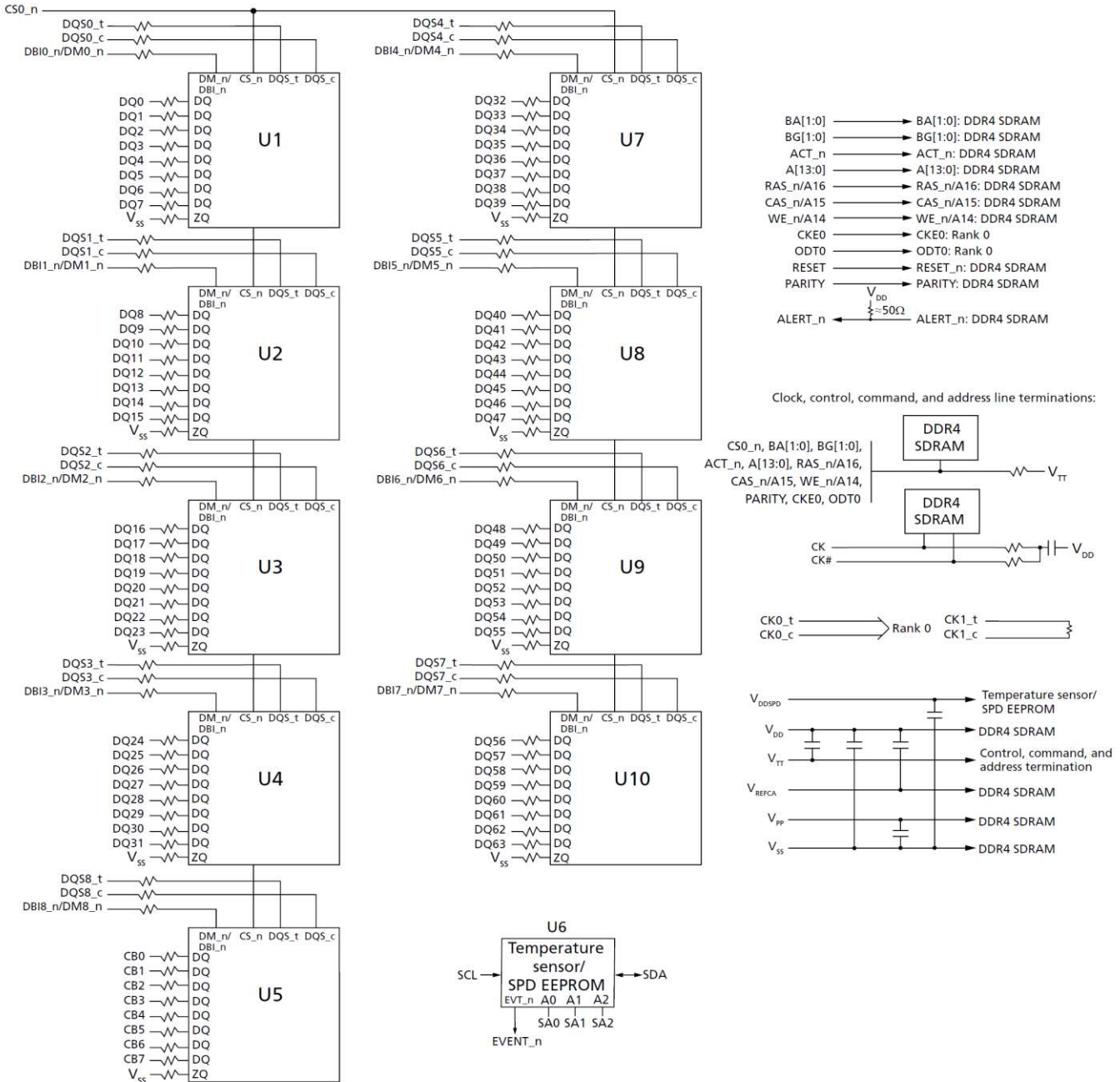
1. Tolerances on all dimensions +/-0.15mm unless otherwise specified.

### Pin Assignments

Pin No	Pin Name	Pin No	Pin Name	Pin No	Pin Name	Pin No	Pin Name	Pin No	Pin Name	Pin No	Pin Name	Pin No	Pin Name	Pin No	Pin Name
01	NC	37	VSS	73	VDD	109	VSS	145	NC	181	DQ29	217	VDD	253	DQ41
02	VSS	38	DQ24	74	CK0_t	110	DM5_n/ DBI5_n, NC	146	VREFCA	182	VSS	218	CK1_t	254	VSS
03	DQ4	39	VSS	75	CK0_c	111	NC	147	VSS	183	DQ25	219	CK1_c	255	DQS5_c
04	VSS	40	DM3_n/ DBI3_n, NC	76	VDD	112	VSS	148	DQ5	184	VSS	220	VDD	256	DQS5_t
05	DQ0	41	NC	77	VTT	113	DQ46	149	VSS	185	DQS3_c	221	VTT	257	VSS
06	VSS	42	VSS	78	EVENT_n	114	VSS	150	DQ1	186	DQS3_t	222	PARITY	258	DQ47
07	DM0_n/ DBI0_n, NC	43	DQ30	79	A0	115	DQ42	151	VSS	187	VSS	223	VDD	259	VSS
08	NC	44	VSS	80	VDD	116	VSS	152	DQS0_c	188	DQ31	224	BA1	260	DQ43
09	VSS	45	DQ26	81	BA0	117	DQ52	153	DQS0_t	189	VSS	225	A10/AP	261	VSS
10	DQ6	46	VSS	82	RAS_n/A16	118	VSS	154	VSS	190	DQ27	226	VDD	262	DQ53
11	VSS	47	CB4/ NC	83	VDD	119	DQ48	155	DQ7	191	VSS	227	RFU	263	VSS
12	DQ2	48	VSS	84	CS0_n	120	VSS	156	VSS	192	CB5, NC	228	WE_n/A14	264	DQ49
13	VSS	49	CB0/ NC	85	VDD	121	DM6_n/ DBI6_n, NC	157	DQ3	193	VSS	229	VDD	265	VSS
14	DQ12	50	VSS	86	CAS_n/A15	122	NC	158	VSS	194	CB1, NC	230	NC	266	DQS6_c
15	VSS	51	DM8_n/ DBI8_n, NC	87	ODT0	123	VSS	159	DQ13	195	VSS	231	VDD	267	DQS6_t
16	DQ8	52	NC	88	VDD	124	DQ54	160	VSS	196	DQS8_c	232	A13	268	VSS
17	VSS	53	VSS	89	CS1_n	125	VSS	161	DQ9	197	DQS8_t	233	VDD	269	DQS5
18	DMI_n/ DBI1_n, NC	54	CB6/ DBI8_n, NC	90	VDD	126	DQ50	162	VSS	198	VSS	234	NC	270	VSS
19	NC	55	VSS	91	ODT1	127	VSS	163	DQS1_c	199	CB7, NC	235	NC	271	DQ51
20	VSS	56	CB2/ NC	92	VDD	128	DQ60	164	DQS1_t	200	VSS	236	VDD	272	VSS
21	DQ14	57	VSS	93	NC	129	VSS	165	VSS	201	CB3, NC	237	NC	273	DQ61
22	VSS	58	RESET_n	94	VSS	130	DQ56	166	DQ15	202	VSS	238	SA2	274	VSS
23	DQ10	59	VDD	95	DQ36	131	VSS	167	VSS	203	CKE1	239	VSS	275	DQ57
24	VSS	60	CKE0	96	VSS	132	DM7_n/ DBI7_n, NC	168	DQ11	204	VDD	240	DQ37	276	VSS
25	DQ20	61	VDD	97	DQ32	133	NC	169	VSS	205	RFU	241	VSS	277	DQS7_c
26	VSS	62	ACT_n	98	VSS	134	VSS	170	DQ21	206	VDD	242	DQ33	278	DQS7_t
27	DQ16	63	BG0	99	DM4_n/ DBI4_n, NC	135	DQ62	171	VSS	207	BG1	243	VSS	279	VSS
28	VSS	64	VDD	100	NC	136	VSS	172	DQ17	208	ALERT_n	244	DQS4_c	280	DQ63
29	DM2_n/ DBI2_n, NC	65	A12/BC_n	101	VSS	137	DQ58	173	VSS	209	VDD	245	DQS4_t	281	VSS
30	NC	66	A9	102	DQ38	138	VSS	174	DQS2_c	210	A11	246	VSS	282	DQ59
31	VSS	67	VDD	103	VSS	139	SA0	175	DQS2_t	211	A7	247	DQ39	283	VSS
32	DQ22	68	A8	104	DQ34	140	SA1	176	VSS	212	VDD	248	VSS	284	VDDSPD
33	VSS	69	A6	105	VSS	141	SCL	177	DQ23	213	A5	249	DQ35	285	SDA
34	DQ18	70	VDD	106	DQ44	142	VPP	178	VSS	214	A4	250	VSS	286	VPP
35	VSS	71	A3	107	VSS	143	VPP	179	DQ19	215	VDD	251	DQ45	287	VPP
36	DQ28	72	A1	108	DQ40	144	RFU	180	VSS	216	A2	252	VSS	288	VPP

- Note:
1. VPP is 2.5V DC.
  2. Pin 230 is defined as NC for UDIMMs, RDIMMs and LRDIMMs. Pin 230 is defined as SAVE\_n for NVDIMMs.
  3. Pins 1 and 145 are defined as NC for UDIMMs, RDIMMs and LRDIMMs. Pins 1 and 145 are defined as 12V for Hybrid /NVDIMM
  4. The 5th VPP is required on all modules and DIMMs.

## Block Diagram 4GB, 512Mx72 Module(1Rank x8)



Note: 1. The ZQ ball on each DDR4 component is connected to an external 240Ω ±1% resistor that is tied to ground. It is used for the calibration of the component's ODT and output driver.

This technical information is based on industry standard data and tests believed to be reliable. However, Transcend makes no warranties, either This technical information is based on industry standard data and tests believed to be reliable. However, Transcend makes no warranties, either expressed or implied, as to its accuracy and assume no liability in connection with the use of this product. Transcend reserves the right to make changes in specifications at any time without prior notice.

## Operating Temperature Condition

Parameter	Symbol	Rating	Unit	Note
Operating Temperature	TOPER	0 to 85	°C	1,2

Note: Operating Temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JESD51-2 standard.  
At 0 - 85°C, operation temperature range is the temperature which all DRAM specification will be supported.

## Absolute Maximum DC Ratings

Parameter	Symbol	Value	Unit	Note
Voltage on VDD relative to Vss	VDD	-0.3 ~ 1.5	V	1
Voltage on VDDQ pin relative to Vss	VDDQ	-0.3 ~ 1.5	V	1
Voltage on VPP pin relative to Vss	VPP	-0.3 ~ 3.0	V	3
Voltage on any pin relative to Vss	VIN, VOUT	-0.3 ~ 1.5	V	1
Storage temperature	TSTG	-55~+100	°C	1,2

Note: Stress greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.  
Storage Temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JESD51-2 standard.  
VPP must be equal or greater than VDD/VDDQ at all times.

## AC & DC Operating Conditions

### Recommended DC operating conditions (SSTL –1.5)

Parameter	Symbol	Rating			Unit	Notes
		Min	Typ.	Max		
Supply voltage	VDD	1.14	1.2	1.26	V	1, 2
Supply voltage for Output	VDDQ	1.14	1.2	1.26	V	1, 2
Wordline supply voltage	VPP	2.375	2.5	2.75	V	3

Note: Under all conditions VDDQ must be less than or equal to VDD.  
VDDQ tracks with VDD, AC parameters are measured with VDD and VDDQ tied together.  
DC bandwidth is limited to 20MHz

### Single-ended AC & DC input levels for Command and Address

Parameter	Symbol	DDR4-1600/1866/2133		Unit	Note
		Min	Max		
I/O Reference Voltage (CMD/ADD)	VREFCA(DC)	0.49*VDDQ	0.51*VDDQ	V	1,2
DC Input Logic High	VIH(DC)	VREF+0.075	VDD	V	
DC Input Logic Low	VIL(DC)	VSS	VREF-0.075	V	
AC Input Logic High	VIH(AC)	VREF+0.1	Note 1	V	
AC Input Logic Low	VIL(AC)	Note 1	VREF-0.1	V	

Note: The AC peak noise on VREFCA may not allow VREFCA to deviate from VREFCA(DC) by more than  $\pm 1\%$  VDD (for reference: approx.  $\pm 12\text{mV}$ )  
For reference: approx.  $VDD/2 \pm 12\text{mV}$

**Differential AC and DC Input Levels**

Parameter	Symbol	DDR4-1600/1866/2133		Unit	Note
		Min	Max		
differential input high DC	VIHdiff(DC)	+0.150	NOTE 3	V	1
differential input low DC	VILdiff(DC)	NOTE 3	-0.150	V	1
differential input high AC	VIHdiff(AC)	2 x (VIH(AC) - VREF)	NOTE 3	V	2
differential input low AC	VILdiff(AC)	NOTE 3	2 x (VIL(AC) - VREF)	V	2

Note: Used to define a differential signal slew-rate.  
 For CK<sub>t</sub> - CK<sub>c</sub> use VIH.CA/VIL.CA(AC) of ADD/CMD and VREFCA;  
 These values are not defined; however, the differential signals CK<sub>t</sub> - CK<sub>c</sub>, need to be within the respective limits (VIH.CA(DC) max, VIL.CA(DC)min) for single-ended signals as well as the limitations for overshoot and undershoot.

**Single-ended AC & DC output levels**

Parameter	Symbol	DDR4-1600/1866/2133	Unit	Note
DC output high measurement level	VOH(DC)	1.1 x VDDQ	V	
DC output mid measurement level	VOM(DC)	0.8 x VDDQ	V	
DC output low measurement level	VOL(DC)	0.5 x VDDQ	V	
AC output high measurement level	VOH(AC)	(0.7 + 0.15) x VDDQ	V	1
AC output low measurement level	VOL(AC)	(0.7 - 0.15) x VDDQ	V	1

Note: The swing of  $\pm 0.15 \times VDDQ$  is based on approximately 50% of the static single-ended output peak-to-peak swing with a driver impedance of RZQ/7 $\Omega$  and an effective test load of 50 $\Omega$  to VTT = VDDQ.

**Differential AC & DC output levels**

Parameter	Symbol	DDR4-1600/1866/2133	Unit	Note
AC differential output high measurement level	VOHdiff(AC)	+0.3 x VDDQ	V	1
AC differential output low measurement level	VOLdiff(AC)	-0.3 x VDDQ	V	1

Note: The swing of  $\pm 0.3 \times VDDQ$  is based on approximately 50% of the static differential output peak-to-peak swing with a driver impedance of RZQ/7 $\Omega$  and an effective test load of 50 $\Omega$  to VTT = VDDQ at each of the differential outputs.

### IDD Specification parameters Definition

(IDD values are for full operating range of Voltage and Temperature)

#### 4GB, 512Mx72 Module (1 Rank x8)

Parameter	Symbol	DDR4 2133 CL15	Unit
<b>Operating One bank Active-Precharge current;</b> tCK = tCK(IDD), tRC = tRC(IDD), tRAS = tRASmin(IDD); CKE is HIGH, /CS is HIGH between valid commands; Address bus inputs are SWITCHING; Data bus inputs are SWITCHING	IDD0	540	mA
<b>Operating One bank Active-read-Precharge current;</b> IOU <sub>T</sub> = 0mA; BL = 8, CL = CL(IDD), AL = 0; tCK = tCK(IDD), tRC = tRC(IDD), tRAS = tRASmin(IDD), tRCD = tRCD(IDD); CKE is HIGH, /CS is HIGH between valid commands; Address bus inputs are SWITCHING; Data pattern is same as IDD4W	IDD1	585	mA
<b>Precharge power-down current;</b> All banks idle; tCK = tCK(IDD); CKE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING	IDD2P	270	mA
<b>Precharge quiet standby current;</b> All banks idle; tCK = tCK(IDD); CKE is HIGH, /CS is HIGH; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING	IDD2Q	351	mA
<b>Precharge standby current;</b> All banks idle; tCK = tCK(IDD); CKE is HIGH, /CS is HIGH; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING	IDD2N	414	mA
<b>Active power - down current;</b> All banks open; tCK = tCK(IDD); CKE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING	IDD3P	396	mA
<b>Active standby current;</b> All banks open; tCK = tCK(IDD), tRAS = tRASmax(IDD), tRP = tRP(IDD); CKE is HIGH, /CS is HIGH between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING	IDD3N	567	mA
<b>Operating burst read current;</b> All banks open, Continuous burst reads, IOU <sub>T</sub> = 0mA; BL = 4, CL = CL(IDD), AL = 0; tCK = tCK(IDD), tRAS = tRASmax(IDD), tRP = tRP(IDD); CKE is HIGH, /CS is HIGH between valid commands; Address bus inputs are SWITCHING; Data pattern is same as IDD4W	IDD4R	1350	mA
<b>Operating burst write current;</b> All banks open, Continuous burst writes; BL = 8, CL = CL(IDD), AL = 0; tCK = tCK(IDD), tRAS = tRASmax(IDD), tRP = tRP(IDD); CKE is HIGH, /CS is HIGH between valid commands; Address bus inputs are SWITCHING; Data bus inputs are SWITCHING IDD4R	IDD4W	1440	mA
<b>Burst refresh current;</b> tCK = tCK(IDD); Refresh command at every tRFC(IDD) interval; CKE is HIGH, /CS is HIGH between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING	IDD5	1710	mA
<b>Self refresh current;</b> CK and /CK at 0V; CKE = 0.2V; Other control and address bus inputs are FLOATING; Data bus inputs are FLOATING	IDD6	180	mA
<b>Operating bank interleave read current;</b> All bank interleaving reads, IOU <sub>T</sub> = 0mA; BL = 8, CL = CL(IDD), AL = tRCD(IDD)-1*tCK(IDD); tCK = tCK(IDD), Trc = tRC(IDD), tRRD = tRRD(IDD), tRCD = 1*tCK(IDD); CKE is HIGH, CS is HIGH between valid commands; Address bus inputs are STABLE during DESELECTs; Data pattern is same as IDD4R;	IDD7	1665	mA

Note: Module IDD was calculated on the specific brand DRAM(2Xnm) component IDD and can be differently measured according to DQ loading capacitor.



### Timing Parameters & Specifications

Speed		DDR4 2133		Unit
Parameter	Symbol	Min	Max	
Average Clock Period	tCK	0.938	<1.071	ns
CK high-level width	tCH	0.48	0.52	tCK
CK low-level width	tCL	0.48	0.52	tCK
DQS_t,DQS_c to DQ skew, per group, per access	tDQSQ	-	TBD	tCK/2
DQS_t,DQS_c to DQ Skew deterministic, per group, per access	tDQSQ	-	TBD	tCK/2
DQ output hold time from DQS_t,DQS_c	tQH	TBD	-	tCK/2
DQ output hold time deterministic from DQS_t, DQS_c	tQH	TBD	-	UI
DQS_t,DQS_c to DQ Skew total, per group, per access; DBI enabled	tDQSQ	-	TBD	UI
DQ output hold time total from DQS_t, DQS_c; DBI enabled	tQH	TBD	-	UI
DQ to DQ offset , per group, per access referenced to DQS_t, DQS_c	tDQSQ	TBD	TBD	UI
DQS_t, DQS_c differential READ Preamble (2 clock preamble)	tRPRE	0.9	TBD	tCK
DQS_t, DQS_c differential READ Postamble	tRPST	TBD	TBD	tCK
DQS_t, DQS_c differential WRITE Preamble	tWPRE	0.9	-	tCK
DQS_t, DQS_c differential WRITE Postamble	tWPST	TBD	TBD	tCK
DQS_t and DQS_c low-impedance time (Referenced from RL-1)	tLZ(DQS)	-360	180	ps
DQS_t and DQS_c high-impedance time (Referenced from RL+BL/2)	tHZ(DQS)	-	180	ps
DQS_t, DQS_c differential input low pulse width	tDQSL	0.46	0.54	tCK
DQS_t, DQS_c differential input high pulse width	tDQSH	0.46	0.54	tCK
DQS_t, DQS_c rising edge to CK_t, CK_c rising edge (1 clock preamble)	tDQSS	-0.27	0.27	tCK
DQS_t, DQS_c falling edge setup time to CK_t, CK_c rising edge	tDSS	0.18	-	tCK
DQS_t, DQS_c falling edge hold time from CK_t, CK_c rising edge	tDSH	0.18	-	tCK
Delay from start of internal write transaction to internal read command for different bank group	tWTR_S	Max(2nCK, 2.5ns)	-	
Delay from start of internal write transaction to internal read command for same bank group	tWTR_L	Max(4nCK,7.5ns)	-	
WRITE recovery time	tWR	15	-	ns
Mode Register Set command cycle time	tMRD	8	-	nCK
CAS_n to CAS_n command delay for same bank group	tCCD_L	6	-	nCK

Speed		DDR4 2133		Unit
Parameter	Symbol	Min	Max	
CAS_n to CAS_n command delay for different bank group	tCCD_S	4	-	nCK
Auto precharge write recovery + precharge time	tDAL	tWR+tRP/tCK		nCK
ACTIVATE to ACTIVATE Command delay to different bank group for 2KB page size	tRRD_S(2K)	Max(4nCK,5.3ns)	-	nCK
ACTIVATE to ACTIVATE Command delay to different bank group for 1KB page size	tRRD_S(1K)	Max(4nCK,3.7ns)	-	nCK
ACTIVATE to ACTIVATE Command delay to different bank group for 1/ 2KB page size	tRRD_S (1/ 2K)	Max(4nCK,3.7ns)	-	nCK
ACTIVATE to ACTIVATE Command delay to same bank group for 2KB page size	tRRD_L(2K)	Max(4nCK,6.4ns)	-	nCK
ACTIVATE to ACTIVATE Command delay to same bank group for 1KB page size	tRRD_L(1K)	Max(4nCK,5.3ns)	-	nCK
ACTIVATE to ACTIVATE Command delay to same bank group for 1/2KB page size	tRRD_L (1/ 2K)	Max(4nCK,5.3ns)	-	nCK
Four activate window for 2KB page size	tFAW_2K	Max(28nCK, 30ns)	-	ns
Four activate window for 1KB page size	tFAW_1K	Max(20nCK, 21ns)	-	ns
Four activate window for 1/2KB page size	tFAW_1/2K	Max(16nCK, 15ns)	-	ns
Power-up and RESET calibration time	tZQinit	1024	-	nCK
Normal operation Full calibration time	tZQoper	512	-	nCK
Normal operation short calibration time	tZQCS	128	-	nCK
Exit Self Refresh to commands not re-quiring a locked DLL	tXS	tRFC(min)+ 10ns	-	
Exit Self Refresh to commands requir-ing a locked DLL	tXSDLL	tDLLK(min)	-	
Internal READ Command to PRE-CHARGE Command delay	tRTP	Max(4nCK,7.5ns)	-	
Minimum CKE low width for Self re-fresh entry to exit timing	tCKESR	tCKE(min)+1nCK	-	
Exit Power Down with DLL on to any valid command;Exit Precharge Power Down with DLL frozen to commands not requiring a locked DLL	tXP	Max (4nCK,6ns)	-	
CKE minimum pulse width	tCKE	Max (3nCK,5ns)	-	
Asynchronous RTT turn-on delay (Power-Down with DLL frozen)	tAONAS	1.0	9.0	ns
Asynchronous RTT turn-off delay (Power-Down with DLL frozen)	tAOFAS	1.0	9.0	ns
RTT dynamic change skew	tADC	0.3	0.7	tCK

**SERIAL PRESENCE DETECT SPECIFICATION**

AQD-D4U4GE21-SG Serial Presence Detect			
Byte No.	Function Described	Standard Specification	Vendor Part
0	Number of Bytes Used / Number of Bytes in SPD Device / CRC Coverage	CRC:0-255Byte SPD Byte use: 512Byte SPD Byte total: 512Byte	24
1	SPD Revision	-	-
2	Key Byte / DRAM Device Type	DDR4 SDRAM	0C
3	Key Byte / Module Type	ECC U-DIMM	02
4	SDRAM Density and Banks	4Gb, 16banks	84
5	SDRAM Addressing	ROW:15, Column:10	19
6	SDRAM Package Type	-	-
7	SDRAM Optional Features	-	-
8	SDRAM Thermal and Refresh Options	-	-
9	Other SDRAM Optional Features	-	-
10	Reserved	-	00
11	Module Nominal Voltage, VDD	1.2V	03
12	Module Organization	1Rank, 8bits	01
13	Module Memory Bus Width	ECC, 72bits	0B
14	Module Thermal Sensor	Support	80
15-16	Reserved	-	00
17	Timebases	-	00
18	SDRAM Minimum Cycle Time (tCKAVGmin)	0.938ns	08
19	SDRAM Maximum Cycle Time (tCKAVGmax)	1.5ns	0C
20-23	CAS Latencies Supported	10, 11, 12, 13, 14, 15, 16	-
24	Minimum CAS Latency Time (tAmin)	13.5ns	6C
25	Minimum RAS to CAS Delay Time (tRCDmin)	13.5ns	6C
26	Minimum Row Precharge Delay Time (tRPmin)	13.5ns	6C
27	Upper Nibbles for tRASmin and tRCmin	-	11
28	Minimum Active to Precharge Delay Time (tRASmin), Least Significant Byte	33ns	08
29	Minimum Active to Active/Refresh Delay Time (tRCmin), Least Significant Byte	46.5ns	74
30-31	Minimum Refresh Recovery Delay Time (tRFC1min)	260ns	20,08
32-33	Minimum Refresh Recovery Delay Time (tRFC2min)	160ns	00,05
34-35	Minimum Refresh Recovery Delay Time (tRFC4min)	110ns	70,03
36-37	Minimum Four Activate Window Delay Time (tFAWmin)	21ns	00,A8
38	Minimum Activate to Activate Delay Time (tRRD_Smin), different bank group	3.7ns	1E
39	Minimum Activate to Activate Delay Time (tRRD_Lmin), same bank group	5.3ns	2B
40	Minimum CAS to CAS Delay Time (tCCD_Lmin), same bank group	5.355ns	2B
41-59	Reserved	-	00
60-77	Connector to SDRAM Bit Mapping	-	-

78-116	Reserved	-	00				
117	Fine Offset for Minimum CAS to CAS Delay Time (tCCD_Lmin), same bank group	-	83				
118	Fine Offset for Minimum Activate to Activate Delay Time (tRRD_Lmin), same bank group	-	B5				
119	Fine Offset for Minimum Activate to Activate Delay Time (tRRD_Smin), different bank group	-	CE				
120	Fine Offset for Minimum Active to Active/Refresh Delay Time (tRCmin)	-	00				
121	Fine Offset for Minimum Row Precharge Delay Time (tRPmin)	-	00				
122	Fine Offset for Minimum RAS to CAS Delay Time (tRCDmin)	-	00				
123	Fine Offset for Minimum CAS Latency Time (tAamin)	-	00				
124	Fine Offset for SDRAM Maximum Cycle Time (tCKAVGmax)	-	00				
125	Fine Offset for SDRAM Minimum Cycle Time (tCKAVGmin)	-	C2				
126-127	Cyclical Redundancy Code	-	-				
128	Raw Card Extension, Module Nominal Height	31.25mm	11				
129	Module Maximum Thickness	Planar Single Sides	01				
130	Reference Raw Card Used	Revision 0, Raw card D	03				
131	Address Mapping from Edge Connector to DRAM	Standard	00				
132-253	Reserved	-	00				
254-255	Cyclical Redundancy Code (CRC)	-	-				
256-319	Reserved	-	00				
320-321	Module Manufacturer ID Code	Transcend	01,4F				
322	Module Manufacturing Location	Taipei	54				
323-324	Module Manufacturing Date	-	00				
325-328	Module Serial Number	-	00				
329-348	Module Part Number	AQD-D4U4GE21-SG	41	51	44	2D	44
			34	55	34	47	45
			32	31	2D	53	47
			20	20	20	20	20
349	Module Revision Code	-	00				
350-351	DRAM Manufacturer ID Code	By Manufacturer	Variable				
352	DRAM Stepping	-	00				
353-381	Manufacturer Specific Data	By Manufacturer	Variable				
382-383	Reserved	-	00				
384-551	End User Programmable	-	-				