

PRODUCT OVERVIEW

The D1U86T-W-800-12-HxxC is a very high efficiency 800 watt, power factor corrected front end power module with a 12Vdc (Main) output and a 12Vdc (2.5A) standby output. The power module has active current sharing and up to 4 supplies may be operated in parallel. The power module may be hot plugged; auto-recovers from overtemperature faults and possesses a single bi-colour status LED on the front panel. In addition logic and PMBus™ status and command signals are provided. The low profile 1U package and 19.5W/cubic inch power density it ideal for delivering reliable, efficient power to servers, storage systems and other 12V distributed power architectures. The power module also is able to operate as an element of a "Cold Redundant" system architecture.

ORDERING GUIDE

Model Number	Power Output (90-264Vac)	Main Output	Standby Output	Airflow
D1U86T-W-800-12-HB4C	800W	12Vdc	12Vdc	Back to Front

INPUT CHARACTERISTICS

Parameter	Conditions	Min.	Nom.	Max.	Units
Input Voltage Operating Range ; AC	Low Line	90	100-120	132	Vac
	High Line	180	200-240	264	
Input Frequency		47	50/60	63	Hz
Turn-on Input Voltage – AC	Ramp up	81	85	89	Vac
Turn-off Input Voltage – AC	Ramp down	69	74	79	
Maximum input current;	800W; Vin 100Vac			9	Arms
Input Voltage Operating Range; DC		180	192-288	300	Vdc
	Turn-on Input Voltage – DC	Ramp up	152	162	
Turn-off Input Voltage – DC	Ramp down	140	149		
Inrush Current	Cold start between 0 to 200msec			35	Apk
Power Factor	At 230Vac, 10% load	0.90			W/VA
	At 230Vac, 20% load	0.96			
	At 230Vac, 50% load	0.98			
	At 230Vac, 100% load	0.99			
Efficiency (230Vac) excluding fan load	10% load	90			%
	20% load	94			
	50% load	96			
	100% load	91			
		N/A			
Efficiency (115Vac) excluding fan load	10% load	92			%
	20% load	94			
	50% load	94			
	100% load	90			
Offline/Cold Redundant Power Consumption	Full Line Range			5	W
Touch (Leakage) Current	264Vac; 50Hz			0.85	mArms

FEATURES

- 800W max continuous output power
- Cold Redundant Compliant
- Certified to meet 80Plus Titanium efficiency
- 12V Main Output
- 12V Standby Output
- 1U height:
86.3mm x 196.5mm x 39.5mm
(3.40" x 7.74" x 1.56")
- 19.5Watts per cubic inch power density
- N+1 redundancy capable,
■ including hot plugging
- Active current sharing on 12V main output; ORING
FET isolation
- Overvoltage, overcurrent, overtemperature
protection
- Internal cooling fan (variable speed)
- PMBus™ Revision 1.2 via SMBus/I²C interface
- Single Bi-Colour LED
- RoHS compliant
- Two-year warranty

OUTPUT VOLTAGE CHARACTERISTICS

Nominal Output Voltage	Parameter	Conditions	Min.	Typ.	Max.	Units
12V V1 (Main)	Nominal Output Voltage			12.0		Vdc
	Line and Load Regulation & Output Set Point Accuracy	Full Line Range; 0-100% Full Load	-5.0		+5.0	%
	Ripple Voltage & Noise ¹	20MHz Bandwidth			120	mV p-p
	Output Current (100/240Vac)	780W max continuous	1		65	A
	Peak Power	Up to 20s; 78A 15ms; 91A, 5% duty cycle			936	W
	Load Capacitance		2200		50000	µF
12VSB	Nominal Output Voltage			12.0		Vdc
	Line and Load Regulation & Output Set Point Accuracy	Full Line Range; 0-100% Full Load	-5.0		+5.0	%
	Ripple Voltage & Noise ¹	20MHz Bandwidth			120	mV p-p
	Output Current	30W max continuous	0.1		2.5	A
	Peak Power	Up to 20s; 3A 15ms; 3.5 A, 5% duty cycle			36	W
	Load Capacitance		100		3100	µF

¹Ripple and noise are measured with 0.1 µF of ceramic capacitance and 10 µF of tantalum capacitance on each of the power supply outputs. A short coaxial cable with 50Ω scope termination is used.

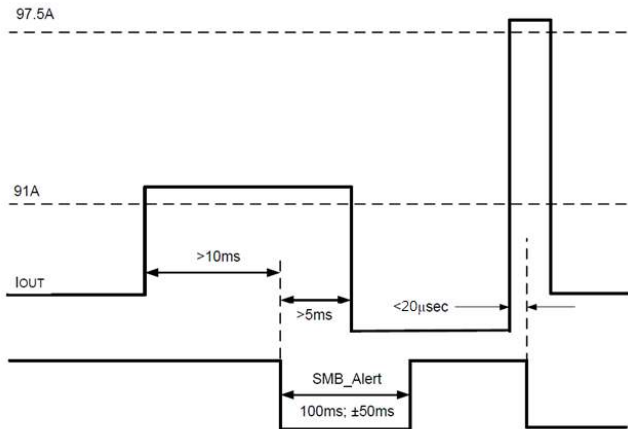


OUTPUT CHARACTERISTICS					
Parameter	Conditions	Min.	Typ	Max.	Units
Startup Time	From application of AC to 90% (10.8Vdc) of V1 (Main) 12Vdc			2	s
Transient Response	12V, 60% load step within range of 20% to 100%; 2.5A/μs di/dt; 2200μF load capacitance			600	mV
	12VSB, 50% load step within range of 20% to 100%; 2.5A/μs di/dt, 100μF load capacitance			600	
V1 (Main) 12Vdc Output Current sharing accuracy (module to module deviation); up to 4 power modules in parallel	Load Range 20-50% per module load capability (13A – 32.5A)			±10	%
	Load Range >50% per module load capability (>32.5A)			±5	
Hot Swap Transients	All outputs remain within in regulation band			±5	%
Holdup Time	100% load; V1 (Main) 12Vdc > 11.4Vdc	16			ms

ENVIRONMENTAL CHARACTERISTICS					
Parameter	Conditions	Min.	Typ	Max.	Units
Storage Temperature Range		-40		70	°C
Operating Temperature Range	Altitude of 3000m (9843 ft)	0		55	
Operating Humidity	Noncondensing	5		85	%
Storage Humidity	Noncondensing	5		95	
System Back Pressure Tolerance (Target; module P-Q Curves to be confirmed by physical testing to be provided)		1.0/250			in-H ₂ O/Pa
Shock	30G non-operating				
Operational Vibration	Sine sweep; 5-150Hz, 2G; random vibration, 5-500Hz, 1.11G				
MTBF	Per Telcordia SR-332 Issue 3 M1C3; 50°C	398K			hrs
Safety Approval Standards – Planned Submissions	CAN/CSA C22.2 No 60950-1-07, Am.1:2011, Am2:2014 UL 60950-1-2014, 2nd Ed. TÜV IEC60950-1:2005+A1: +A2 TÜV EN 60950-1 :2006+A11+A1+A12+A2 CCC GB17625.1-2012;GB4943.1-2011 ;GB/T9254-2008(Class A) BSMI CNS13438 (095/ 06/ 01) , CNS14336-1 (099 / 09 / 30) , CNS 156635 -102				
Input Fuse	12.5A/420V fast blow fuse on the AC Live/HVDC.				
Weight - Target	<1.1kg				

PROTECTION CHARACTERISTICS						
Output Voltage	Parameter	Conditions	Min.	Typ.	Max.	Units
---	Overtemperature (intake)	Autorestart;10° hysteresis is provided		65		°C
---	Fan Fail	Fan fail warning will be issued after fan failure for 5 secs, unit shutdown after another 5 secs	---	---	---	---
V1 (Main) 12V	Overtoltage	Latching; recycle the incoming AC source or toggle PS_ON to reset.	13.5		15	V
	Undervoltage		10		11	
	Overcurrent (Overload or S/C)	In line with peak load requirements see #Peak Loading Tables				
12VSB	Overtoltage	Hiccup; non latching	13.5		15	V
	Undervoltage		10		11	
	Overcurrent (Overload or S/C)	Hiccup; auto recovery once condition is removed. Response time 5-20ms for >3.5A, >20S for 3-3.5A	3.5		4.5	A

PEAK LOADING CAPABILITY DIAGRAM



Max Power = 1170W; 97.5A for 100µs with added 2200µF system buffer capacitance.
Output Voltage Regulation is maintained at ±5% during this condition.

OC condition	Minimum	SMBAlert Delay	PSU Fault Delay
12V - OCW	69A	20 sec	None
12V - OCP1	78A	20 sec	>20Sec +100mS
12V - OCP2	91A	10-15mSec	>20mSec
12V - OCP3	97.5A	<20uSec	>100uSec
12V - SCP	>160% load	<20uSec	immediately
12VSB - OCP1	3A	None	>20 sec
12VSB - OCP2	3.5A	None	>15mS

[#Return to Protection Characteristics](#)

ISOLATION CHARACTERISTICS

Parameter	Conditions	Min.	Typ.	Max.	Units
Insulation Safety Rating / Test Voltage	Input to Output - Reinforced	3000			Vrms
	Input to Chassis - Basic	1500			Vrms

STATUS INDICATORS

LED Colour	LED STATE/OPERATION	DESCRIPTION
Green	Solid	Power Module operating normally: <ul style="list-style-type: none"> V1 (Main) 12Vdc output correct PWOK asserted
N/A	OFF (Not Illuminated)	Power Module unpowered; no AC/HVDC source present
Green	Blinking Green (0.5Hz)	AC/HVDC applied; VSB operational; PS_ON in disable (high) condition
Green	Blinking Green (2Hz)	Sleep mode (Cold Redundant or offline mode)
N/A	OFF(Not Illuminated)	VSB has failed: <ul style="list-style-type: none"> OCP (Overload or S/C) OVP/UVP Normal operation resumes when the abnormal (fault) condition is removed.
Amber	Solid Amber	Power module fault detected: <ul style="list-style-type: none"> OCP (Overload or S/C) OVP/UVP OTP Fan Fault

SLAVE DEVICE ADDRESSES

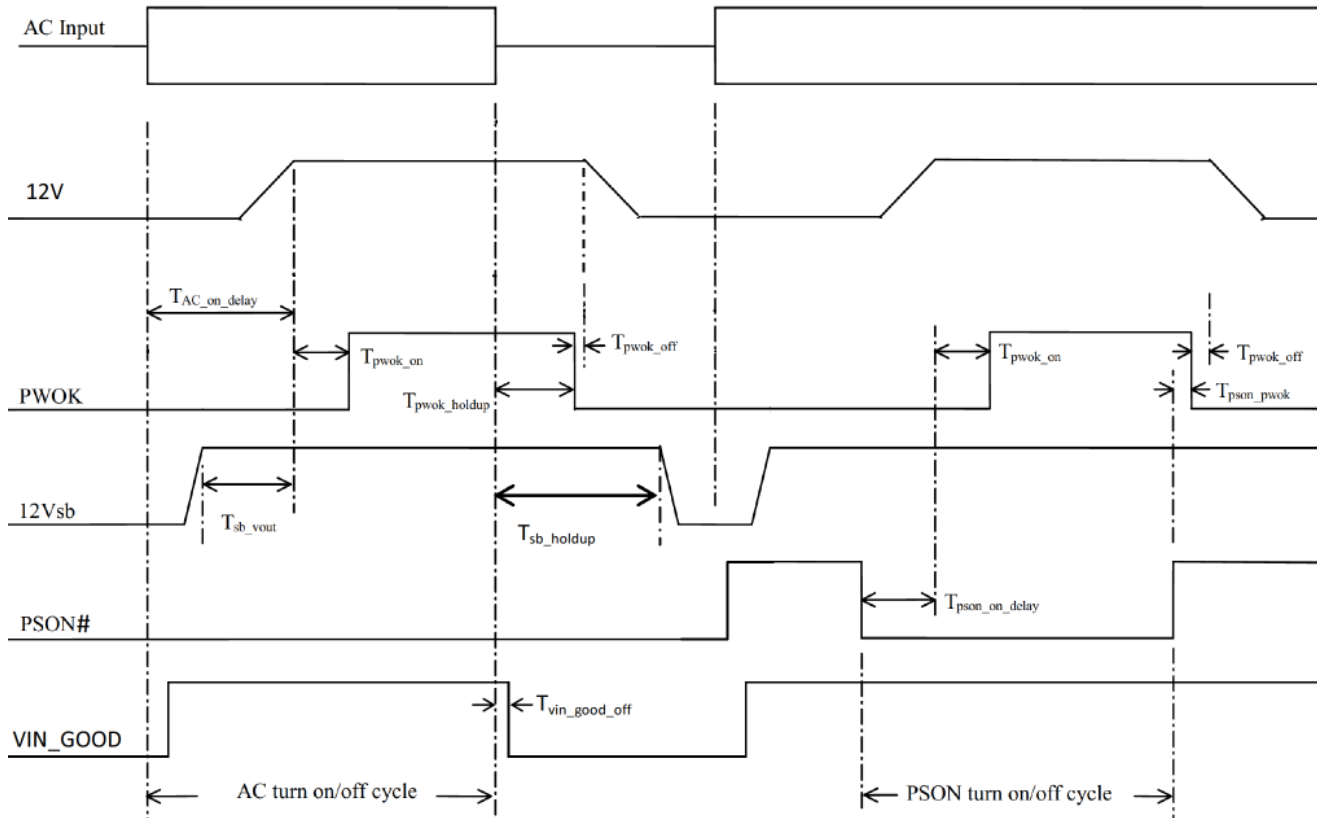
Slave Address (hex)	Slave Address (bin)	A0 Pin Status
0xB0	1011 0000	Low
0xB2	1011 0010	High

Note: Pin **A0** bit shown in bold; note that the address assumes that the R/W bit (LSB of the eight bit word) is assumed to be "0" (i.e. configured for "write")

STATUS AND CONTROL SIGNALS			
Signal Name	I/O	Description	Interface Details
VIN_GOOD (AC or HVDC Input Source present & correct)	Output	The signal output is an active output that requires an internal pull up resistor. It is driven high when input source is available and within acceptable operational limits. The output is driven low to indicate loss of input power.	Pulled up via 1K to internal 3.3VDC A logic high >2.4Vdc A logic low <0.4Vdc
PWOK (V1 (Main 12Vdc and VSB "OK"))	Output	The signal output is an active output that requires an internal pull up resistor. It is driven high, by the power module to indicate that all outputs are valid and within their operational limits. The output is driven low to indicate that the outputs are outside of their limit of regulation.	Pulled up via 1K to internal 3.3VDC A logic high >2.4Vdc A logic low <0.4Vdc
SMB_ALERT# (FAULT/ WARNING)	Output	The signal output is driven low to indicate that the power module has detected a warning or event and is intended to alert the system accordingly. This output must be driven high when the power is operating correctly (within specified limits). The signal will revert to a high level when the warning/fault stimulus (that caused the alert) is removed.	Pulled up via 10K to internal 3.3VDC A logic high >2.4Vdc A logic low <0.4Vdc
PRESENT (Power Supply Presence)	Output	The signal is used to detect the presence (installation) of a power module within the host system. The signal is connected to PSU logic SGND within the power module.	Passive connection via 100ohms to RETURN/GND. A logic low <0.8Vdc
PS_ON# (Power Supply Enable/Disable)	Input	This signal is pulled up internally to the internal housekeeping supply (within the power module). The power module main 12Vdc output will be enabled when this signal is pulled low to Signal_Return. The 12Vdc output will be disabled when the input is driven higher than 2.0V, or open circuited. Cycling this signal shall clear latched fault conditions.	Pulled up via 10K to internal 3.3VDC A logic high >2.0Vdc A logic low <1.0Vdc
PSKILL	Input	This signal is used during hot swap to disable the main output during hot swap extraction. The input is pulled up internally to the internal housekeeping supply (within the power module). The signal is provided on a short (lagging pin) and should be connected to Signal Return to "enable" the power module.	Pulled up via 10K to internal 3.3VDC A logic low <0.8Vdc
SCL (Serial Clock)	Both	A serial clock line compatible with PMBus™ Power Systems Management Protocol Part 1 – General Requirements Rev 1.2. This signal is pulled up internally to the internal housekeeping supply (within the power module). The pull-up resistor must be diode isolated to prevent an unpowered/ faulted supply from loading the signal.	Pulled up via 5.9K to internal 3.3VDC A logic high >2.1Vdc A logic low <0.8Vdc
SDA (Serial Data)	Both	A serial clock line compatible with PMBus™ Power Systems Management Protocol Part 1 – General Requirements Rev 1.2. This signal is pulled up internally to the internal housekeeping supply (within the power module). The pull-up resistor must be diode isolated to prevent an unpowered/ faulted supply from loading the signal.	Pulled up via 5.9K to internal 3.3VDC A logic high >2.1Vdc A logic low <0.8Vdc
+VSENSE -VSENSE (return)	Input	Remote sense connections intended to be connected at and sense the voltage at the point of load. The voltage sense will interact with the internal module regulation loop to compensate for voltage drops due to connection resistance between the output connector and the load. When one or more remote sense lines are opened, regulation measured at the power supply output connector is maintained within regulation defined, plus or minus an additional 0.2V.	Compensation for up to 0.2Vdc total connection drop (output and return connections).
PS_A0	Input	LSB of PMBus™ slave device address structure	Pulled up via 10K to internal 3.3VDC A logic high >2.4Vdc A logic low <0.4Vdc
I_SHARE	Bi-Dir. Analog Bus	The current sharing signal is connected between sharing units (forming an ISHARE bus). It is an input and/or an output (bi-directional analog bus) as the voltage on the line controls the current share between sharing units. A power module will respond to a change in this voltage but a power module can also change the voltage depending on the load drawn from it. On a single unit the voltage on the pin (and the common ISHARE bus would read 8VDC at 100% load (module capability). For two identical units sharing the same 100% load this would read 4VDC for perfect current sharing (i.e. 50% module load capability per unit).	Analogue voltage: +8Vnominal for 100% load capability per module; <ul style="list-style-type: none"> Sink Current capability; 0.5mA max Source Current capability; 4.0mA min
CR_BUS#	Bi-Dir. Digital Bus	Cold Redundancy is a technique for optimizing efficiency of power delivery by multiple units connected in an N+1 load-sharing configuration to a common system load. The objective is to ensure that the "optimum" numbers of units are "active" to service the system load while providing the highest overall efficiency. This element is the "cold redundant" signal bus between parallel load-sharing units for the system power bus. The CR_BUS# operates in conjunction with specific PMBus™ commands provided to the power module to control the cold redundant "status of the power module. It operates between two levels: <ul style="list-style-type: none"> Logic level "low"; this is the "normal" operating state of the power module and the state of the "CR_Bus" accordingly Logic level "high"; the bus is driven "high" if the master unit lose their incoming AC (or DC) source or develop a "fault". Refer to ACAN-85 and ACAN-100 for PMBus command detail	A logic high >2.4Vdc A logic low <0.4Vdc

TIMING SPECIFICATIONS

Turn-On Delay & Output Rise Time:



ITEM	DESCRIPTION	MIN	MAX	UNITS
T _{sb_vout}	Delay from 12VSB within regulation to 12V within regulation	7	520	ms
T _{rise}	12VDC / 12VSB rise time	2	20	ms
T _{pwok_on}	Delay from 12V within regulation to PWOK asserted at turn on	100	500	ms
T _{pwok_off}	Delay from PWOK desertion to 12V dropping out of regulation	1		ms
T _{sb_holdup}	Delay from AC loss to 12VSB turned off	22		ms
T _{pwok_holdup}	Delay from AC loss to PWOK desertion	16		ms
T _{AC_on_delay}	Delay from AC on to 12V within regulation		2000	ms
T _{pson_pwok}	Delay from PSON# desertion to PWOK		2	ms
T _{pson_on_delay}	Delay from PSON# assertion to 12V within regulation		350	ms
T _{vin_good_off}	Delay from AC loss to VIN_GOOD desertion & SMBAlert# assertion		2	ms

EMISSIONS AND IMMUNITY

Characteristic	Standard	Compliance
Input Current Harmonics	IEC/EN 61000-3-2	Complies with Class Limits
Voltage Fluctuation and Flicker	IEC/EN 61000-3-3	Complies
Conducted Emissions	FCC 47 CFR Part 15/CISPR 22/EN55022	Class A with 6dB margin
ESD Immunity	IEC/EN 61000-4-2	Level 4 criteria A
Radiated Field Immunity	IEC/EN 61000-4-3	Level 3 criteria B
Electrical Fast Transients/Burst Immunity	IEC/EN 61000-4-4	1kV criteria A
Surge Immunity	IEC/EN 61000-4-5	Level 4 criteria A
RF Conducted Immunity	IEC/EN 61000-4-6	Level 3 criteria A
Magnetic Field Immunity	IEC/EN 61000-4-8	3 A/m criteria B
Voltage Dips, Interruptions	IEC/EN 61000-4-11	230Vin, 100% load, Phase 0°, Dip 100% Duration 10ms (A) 230Vin, 50% load, Phase 0°, Dip 100% Duration 20ms (VSB:A, V1:B) 230Vin, 100% load, Phase 0°, Dip 100% Duration > 20ms (VSB, V1:B)

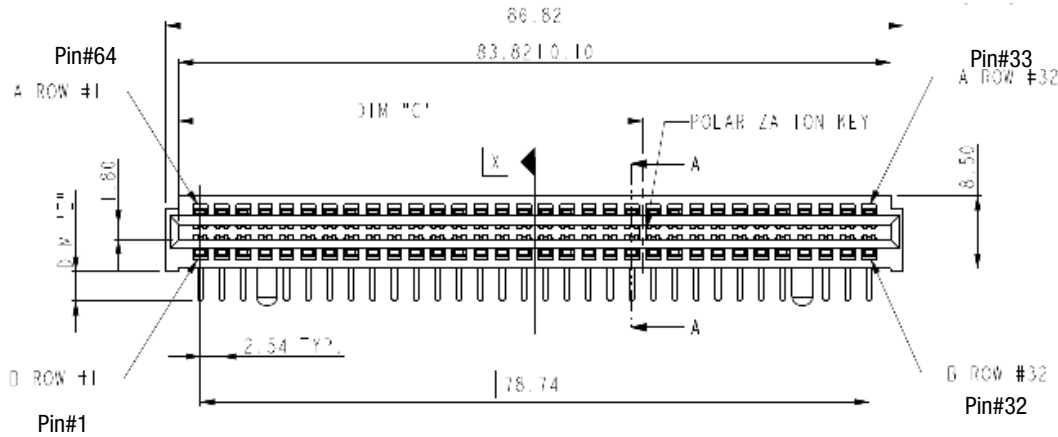
OUTPUT & SIGNAL INTERFACE; PIN ASSIGNMENT; CARD EDGE GOLD FINGERS

PCB TOP (COMPONENT) SIDE				PCB BOTTOM (SOLDER) SIDE			
PIN#	Length	NAME/FUNCTION	DESCRIPTION	PIN#	Length	NAME/FUNCTION	DESCRIPTION
53-64	Standard	V1 (MAIN) 12Vdc	12Vdc Main Output	1-12	Standard	V1 (MAIN) 12Vdc	12Vdc Main Output
41-52	Long	PWR RTN	12V Main & 12VSB Output RTN/GND	13-24	Long	PWR RTN	12V Main & 12VSB Output RTN/GND
40	Standard	+VSENSE	12V Main Output +VE Sense	25	Standard	CR_BUS#	Cold Redundant Status Signal
39	Standard	12VSB	Standby Output	26	Standard	-VSENSE	12Vdc Main Output -VE Sense
38	Standard	PS_A0	I2C Address LSB	27	Standard	VIN_GOOD	Incoming Source Status Signal
37	Standard	PWOK	Power OK Signal	28	Standard	I_SHARE	Analogue current share line/bus
36	Long	Signal Return	Standby/Signal Return	29	Standard	PSON#	Power Module Enable/Disable Signal
35	Short	SCL	I2C Serial Clock Line	30	Short	PSKILL	Rapid Enable/Disable for hotswap
34	Short	PRESENT	Power Module Present Signal	31	Short	Not Used	No User Connection
33	Short	SDA	I2C Serial Data Line	32	Short	SMBALERT#	SMBus_Alert signal

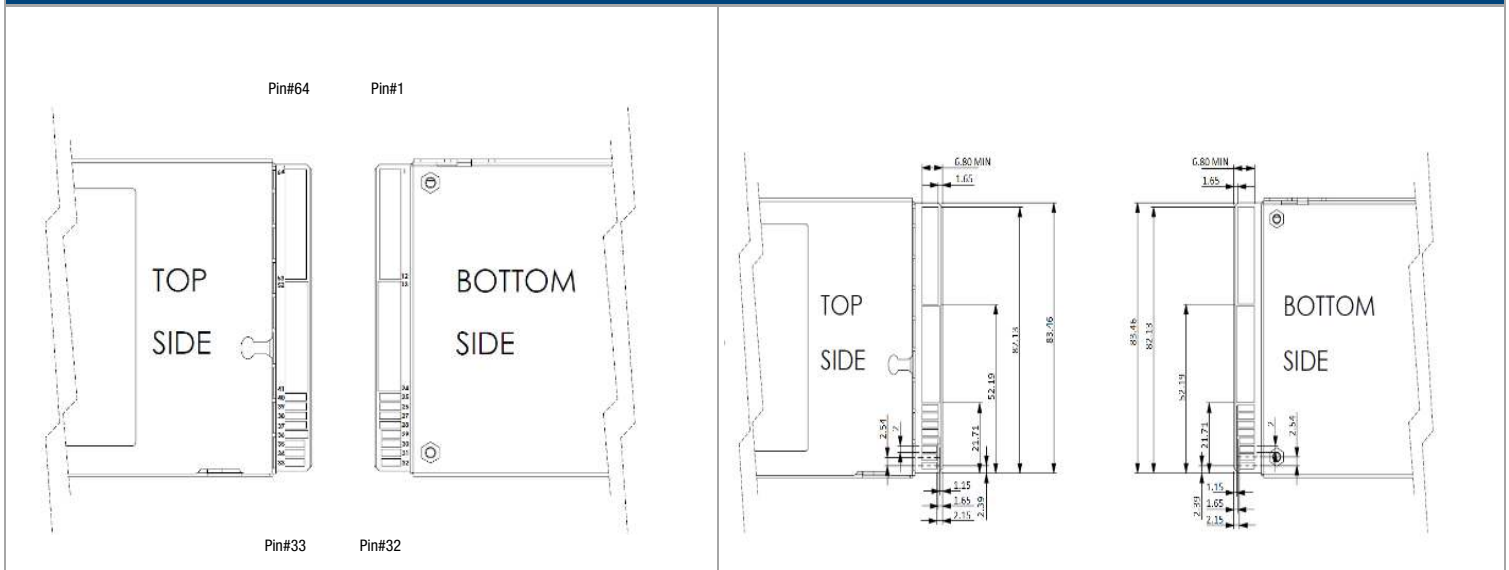
DC OUTPUT & SIGNAL INTERFACE MATING CONNECTOR; FCI PN 51939-768LF

Part Number	Description
FCI 10053363-200LF	Right Angle (Without key)
FCI 10046971-001LF	Vertical

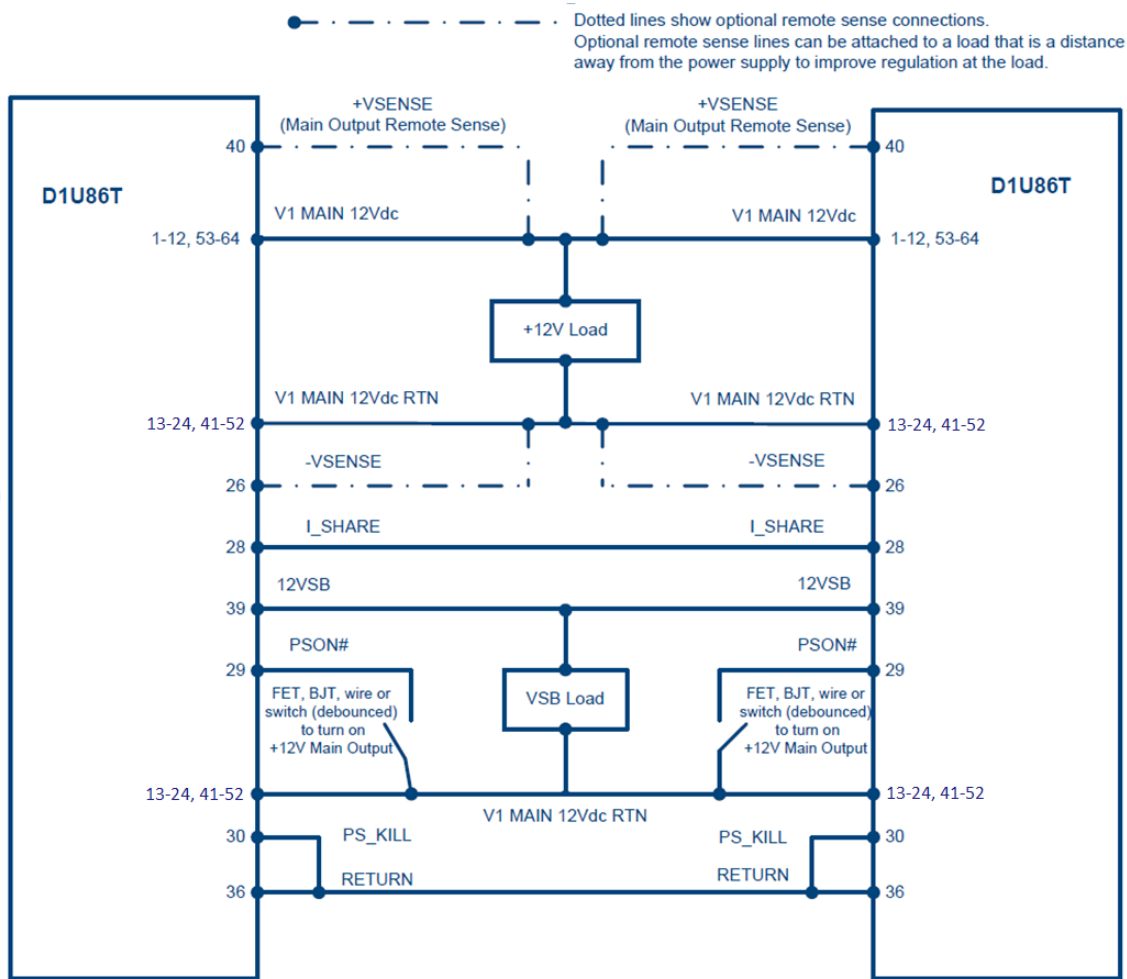
Right Angle 10053363-200LF



OUTPUT CONNECTOR AND SIGNAL SPECIFICATION OUTPUT & SIGNAL INTERFACE; PIN CONFIGURATION



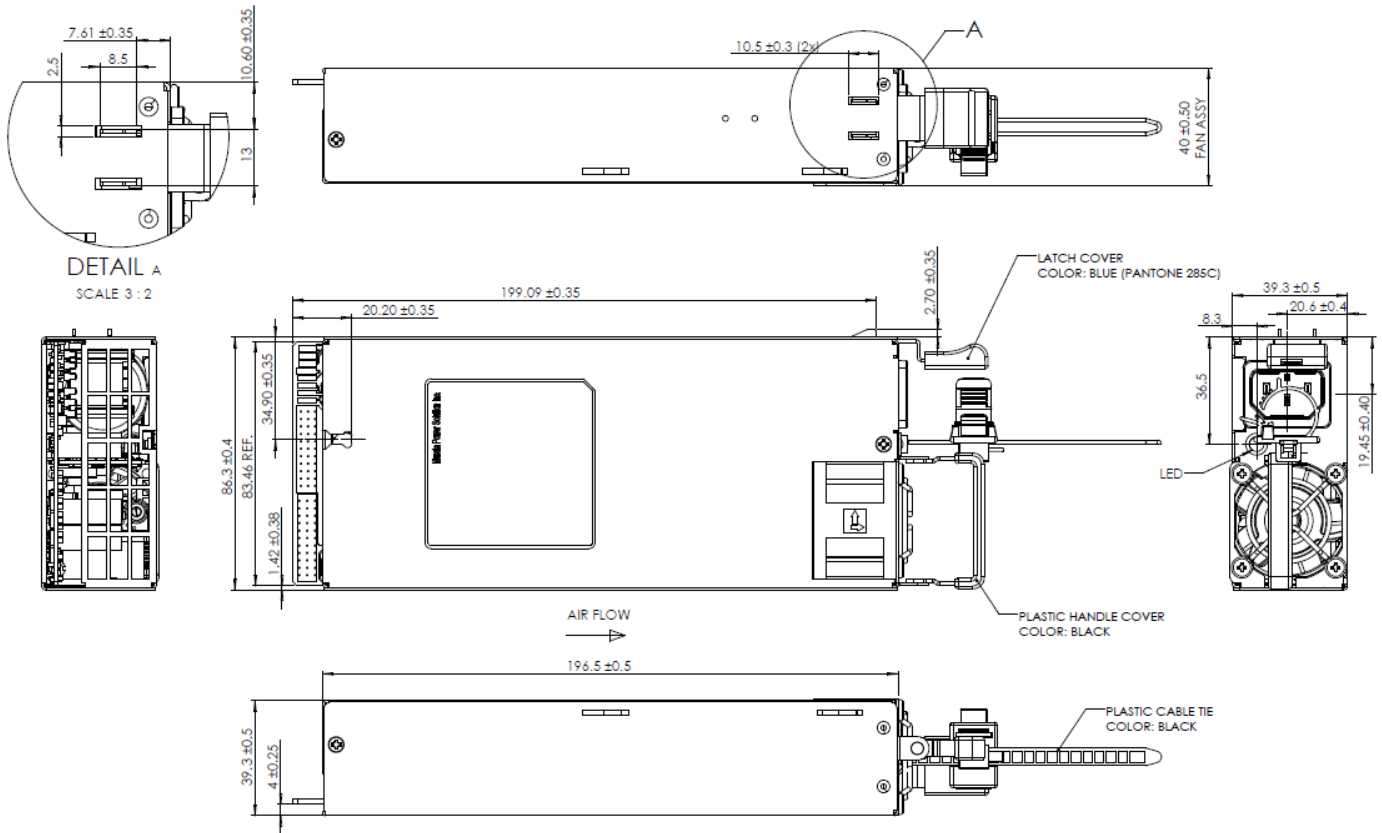
WIRING DIAGRAM



CURRENT SHARING NOTES:

1. V1 (Main) 12Vdc output current sharing is achieved using the active current share method. (See wiring diagram for connection details.)
2. The current share (I_SHARE) pin 28 is a direct connection between the sharing units. It is an input and/or output as the voltage on the line controls the current share ratio. A power module will respond to a change in this voltage to contribute additional or less current to the current share power bus. However, a power module can also modify the ISHARE bus voltage depending on the load drawn from it. On a single unit the ISHARE bus signal would read 8V at 100% output load (65A) capability. For two units sharing this common load then the ISHARE bus should read 4V for perfect (50/50) current sharing and ideally each unit would contribute 32.5A to the common load.
3. Up to 4units can be paralleled together. Please consult your Murata sales representative if operation with more than 4 units in parallel is required.
4. 12VSB outputs can be tied together for redundancy with a total combined output current provided of at least 4A. The 12VSB output has an internal ORing MOSFET for additional redundancy / internal short protection.

MECHANICAL DIMENSIONS



Nominal Dimensions: 86.3mm x 196.5mm x 39.3mm (3.40" x 7.74" x 1.56")

OPTIONAL ACCESSORIES

Description	Part Number
12V D1U86T Output Connector Card	D1U86T-12-CONC

APPLICATION NOTES

Document Number	Description	Link
ACAN-84	D1U86T Output Connector Card	http://power.murata.com/datasheet?/data/apnotes/acan-84.pdf
ACAN-85	D1U86T Communication Protocol	http://power.murata.com/datasheet?/data/apnotes/acan-85.pdf
ACAN-100	Cold Redundant Application Note	http://power.murata.com/datasheet?/data/apnotes/acan-100.pdf

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