

N-channel 100 V, 15 mΩ logic level MOSFET in LFPAK56 4 November 2016 Product data sheet

### 1. General description

Logic level N-channel MOSFET in an LFPAK56 (Power SO8) package using TrenchMOS technology. This product has been designed and qualified to AEC Q101 standard for use in high performance automotive applications.

### 2. Features and benefits

- Q101 compliant
- Repetitive avalanche rated
- Suitable for thermally demanding environments due to 175 °C rating
- True logic level gate with V<sub>GS(th)</sub> rating of greater than 0.5 V at 175 °C

### 3. Applications

- 12 V, 24 V and 48 V Automotive systems
- Motors, lamps and solenoid control
- Transmission control
- Ultra high performance power switching

### 4. Quick reference data

Table 1. Qui	ck reference data					
Symbol	Parameter	Conditions	Min	Тур	Max	Unit
V <sub>DS</sub>	drain-source voltage	25 °C ≤ T <sub>j</sub> ≤ 175 °C	-	-	100	V
I <sub>D</sub>	drain current	V <sub>GS</sub> = 5 V; T <sub>mb</sub> = 25 °C; <u>Fig.</u>	-	-	69	А
P <sub>tot</sub>	total power dissipation	T <sub>mb</sub> = 25 °C; <u>Fig. 1</u>	-	-	195	W
Static characte	eristics					
R <sub>DSon</sub>	drain-source on-state resistance	V <sub>GS</sub> = 5 V; I <sub>D</sub> = 20 A; T <sub>j</sub> = 25 °C; <u>Fig. 11</u>	-	12.1	15	mΩ
Dynamic chara	acteristics					
Q <sub>GD</sub>	gate-drain charge	I <sub>D</sub> = 20 A; V <sub>DS</sub> = 80 V; V <sub>GS</sub> = 5 V; Fig. 13; Fig. 14	-	16	-	nC

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### 5. Pinning information

Table 2.	Pinning	information		
Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S	source	mb	D
2	S	source		
3	S	source	q	G-UFA
4	G	gate	មុច្ចមុ	mbb076 S
mb	D	mounting base; connected to drain	1 2 3 4 LFPAK56; Power- SO8 (SOT669)	

# 6. Ordering information

Table 3. Ordering information							
Type number	Package	ckage					
	Name	Description	Version				
BUK9Y15-100E	LFPAK56; Power-SO8	Plastic single-ended surface-mounted package (LFPAK56; Power-SO8); 4 leads	SOT669				

# 7. Marking

Table 4. Marking codes	
Type number	Marking code
BUK9Y15-100E	91510E

# 8. Limiting values

#### Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V <sub>DS</sub>	drain-source voltage	25 °C ≤ T <sub>j</sub> ≤ 175 °C		-	100	V
V <sub>DGR</sub>	drain-gate voltage	R <sub>GS</sub> = 20 kΩ		-	100	V
V <sub>GS</sub>	gate-source voltage	DC; T <sub>j</sub> ≤ 175 °C		-10	10	V
		Pulsed; T <sub>j</sub> ≤ 175 °C	[1][2]	-15	15	V
P <sub>tot</sub>	total power dissipation	T <sub>mb</sub> = 25 °C; <u>Fig. 1</u>		-	195	W
I <sub>D</sub>	drain current	V <sub>GS</sub> = 5 V; T <sub>mb</sub> = 25 °C; <u>Fig. 2</u>		-	69	А
		V <sub>GS</sub> = 5 V; T <sub>mb</sub> = 100 °C; <u>Fig. 2</u>		-	49	А
I <sub>DM</sub>	peak drain current	pulsed; $t_p \le 10 \ \mu s$ ; $T_{mb} = 25 \ ^\circ C$ ; Fig. 3		-	274	А

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Symbol	Parameter	Conditions		Min	Max	Unit
T <sub>stg</sub>	storage temperature			-55	175	°C
Tj	junction temperature			-55	175	°C
Source-drai	in diode					
l <sub>S</sub>	source current	T <sub>mb</sub> = 25 °C		-	69	А
I <sub>SM</sub>	peak source current	pulsed; $t_p \le 10 \ \mu s$ ; $T_{mb} = 25 \ ^\circ C$		-	274	А
Avalanche r	ruggedness					
E <sub>DS(AL)S</sub>	non-repetitive drain-source avalanche energy	$\label{eq:ID} \begin{split} I_D &= 69 \text{ A};  \text{V}_{\text{sup}} \leq 100  \text{V};  \text{R}_{\text{GS}} = 50  \Omega; \\  \text{V}_{\text{GS}} &= 5  \text{V};  \text{T}_{j(\text{init})} = 25 ^{\circ}\text{C}; \text{ unclamped}; \\ \hline \text{Fig. 4} \end{split}$	[3][4]	-	110	mJ

- Accumulated pulse duration up to 50 hours delivers zero defect ppm Significantly longer life times are achieved by lowering  $\rm T_{j}$  and or  $\rm V_{GS}$ [1]
- [2]
- Single-pulse avalanche rating limited by maximum junction temperature of 175 °C. [3]
- Refer to application note AN10273 for further information. [4]

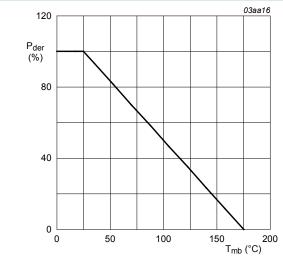


Fig. 1. Normalized total power dissipation as a function of mounting base temperature \_

$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}C)}} \times 100\%$$

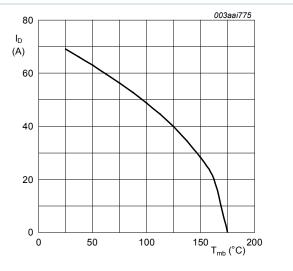
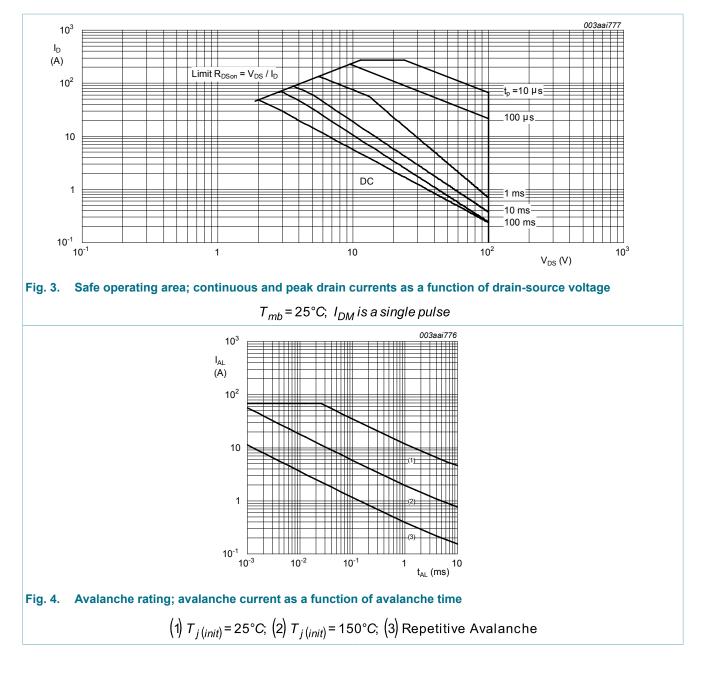


Fig. 2. Continuous drain current as a function of mounting base temperature

 $V_{GS} \ge 5V$ 

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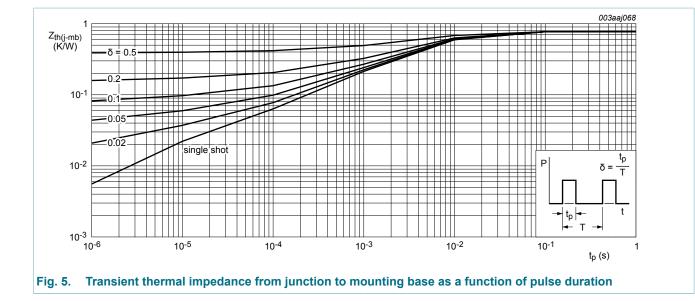


### 9. Thermal characteristics

Fable 6. Thermal characteristics								
Symbol	Parameter	Conditions		Min	Тур	Max	Unit	
R <sub>th(j-mb)</sub>	thermal resistance from junction to mounting base	<u>Fig. 5</u>		-	-	0.77	K/W	

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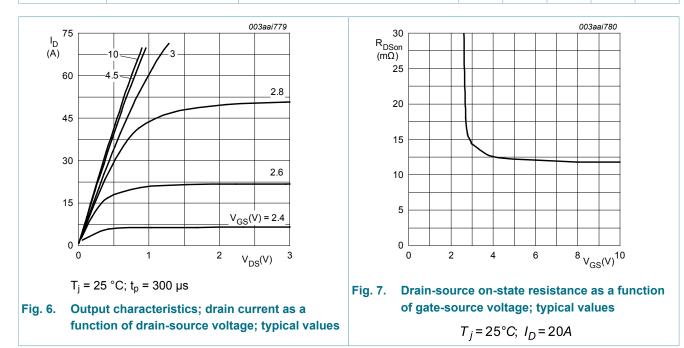
## **10. Characteristics**

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
Static chara	acteristics		I			
V <sub>(BR)DSS</sub>	drain-source	$I_D$ = 250 µA; $V_{GS}$ = 0 V; $T_j$ = 25 °C	100	-	-	V
	breakdown voltage	I <sub>D</sub> = 250 μA; V <sub>GS</sub> = 0 V; T <sub>j</sub> = -55 °C	90	-	-	V
()	gate-source threshold voltage	I <sub>D</sub> = 1 mA; V <sub>DS</sub> =V <sub>GS</sub> ; T <sub>j</sub> = 25 °C; <u>Fig. 9;</u> Fig. 10	1.4	1.7	2.1	V
		I <sub>D</sub> = 1 mA; V <sub>DS</sub> =V <sub>GS</sub> ; T <sub>j</sub> = -55 °C; <u>Fig. 9</u>	-	-	2.45	V
		I <sub>D</sub> = 1 mA; V <sub>DS</sub> =V <sub>GS</sub> ; T <sub>j</sub> = 175 °C; <u>Fig. 9</u>	0.5	-	-	V
I <sub>DSS</sub> drain leakage cur	drain leakage current	V <sub>DS</sub> = 100 V; V <sub>GS</sub> = 0 V; T <sub>j</sub> = 25 °C	-	0.11	10	μA
		V <sub>DS</sub> = 100 V; V <sub>GS</sub> = 0 V; T <sub>j</sub> = 175 °C	-	-	500	μA
I <sub>GSS</sub>	gate leakage current	$V_{GS}$ = 10 V; $V_{DS}$ = 0 V; $T_j$ = 25 °C	-	2	100	nA
		$V_{GS}$ = -10 V; $V_{DS}$ = 0 V; $T_j$ = 25 °C	-	2	100	nA
R <sub>DSon</sub>	drain-source on-state	V <sub>GS</sub> = 5 V; I <sub>D</sub> = 20 A; T <sub>j</sub> = 25 °C; <u>Fig. 11</u>	-	12.1	15	mΩ
	resistance	V <sub>GS</sub> = 10 V; I <sub>D</sub> = 20 A; T <sub>j</sub> = 25 °C; Fig. 11	-	11.6	14.7	mΩ
		V <sub>GS</sub> = 5 V; I <sub>D</sub> = 20 A; T <sub>j</sub> = 175 °C; Fig. 12; Fig. 11	-	-	41.4	mΩ
Dynamic ch	aracteristics					
Q <sub>G(tot)</sub>	total gate charge	I <sub>D</sub> = 20 A; V <sub>DS</sub> = 80 V; V <sub>GS</sub> = 5 V;	-	45.8	-	nC
Q <sub>GS</sub>	gate-source charge	Fig. 13; Fig. 14	-	11	-	nC
Q <sub>GD</sub>	gate-drain charge		-	16	-	nC

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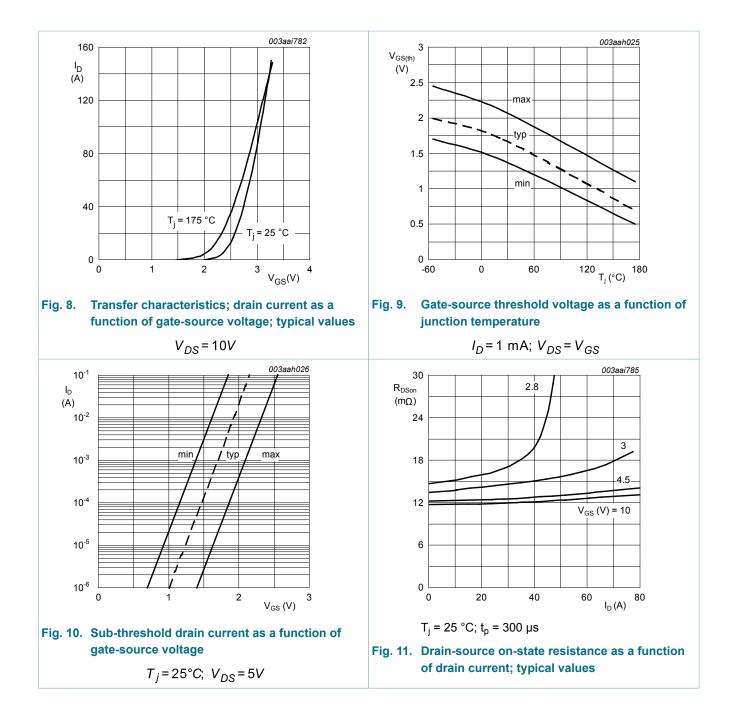
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Symbol	Parameter	Conditions		Min	Тур	Мах	Unit
C <sub>iss</sub>	input capacitance	$V_{DS}$ = 25 V; $V_{GS}$ = 0 V; f = 1 MHz;		-	4604	6139	pF
C <sub>oss</sub>	output capacitance	T <sub>j</sub> = 25 °C; <u>Fig. 15</u>		-	269	323	pF
C <sub>rss</sub>	reverse transfer capacitance	$V_{DD} = 80 \text{ V}^{2} \text{ B}_{1} = 4 \text{ O}^{2} \text{ V}_{DD} = 5 \text{ V}^{2}$		-	156	213	pF
t <sub>d(on)</sub>	turn-on delay time	$V_{DS} = 80 \text{ V}; \text{ R}_{L} = 4 \Omega; \text{ V}_{GS} = 5 \text{ V};$ $\text{R}_{G(ext)} = 5 \Omega$		-	21	-	ns
t <sub>r</sub>	rise time			-	32	-	ns
t <sub>d(off)</sub>	turn-off delay time			-	85	-	ns
t <sub>f</sub>	fall time			-	59	-	ns
Source-dra	ain diode	-	I	1	1		
V <sub>SD</sub>	source-drain voltage	$I_{S}$ = 20 A; $V_{GS}$ = 0 V; $T_{j}$ = 25 °C; <u>Fig. 16</u>		-	0.8	1.2	V
t <sub>rr</sub>	reverse recovery time	I <sub>S</sub> = 20 A; dI <sub>S</sub> /dt = -100 A/µs; V <sub>GS</sub> = 0 V;		-	44	-	ns
Q <sub>r</sub>	recovered charge	V <sub>DS</sub> = 25 V		-	79	-	nC



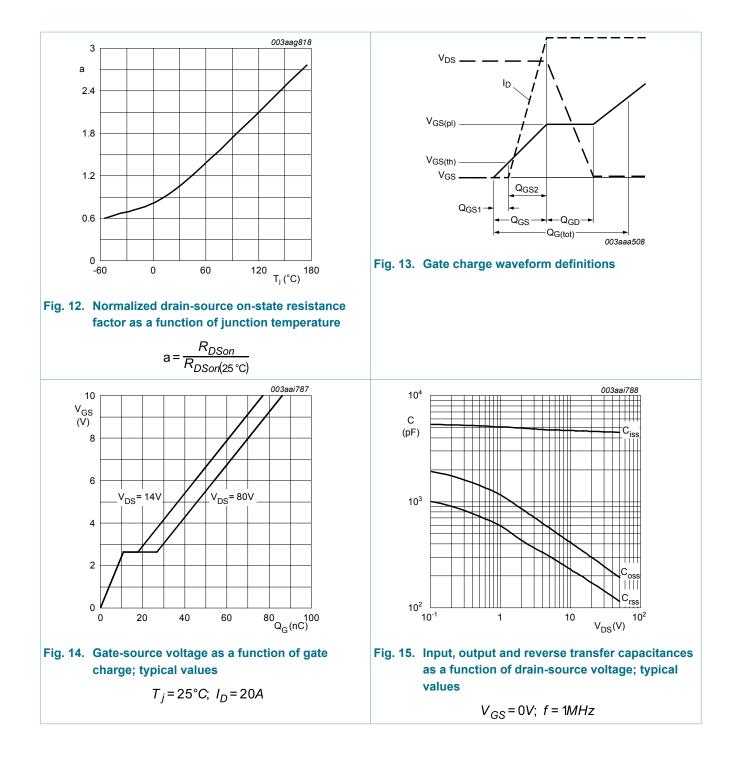
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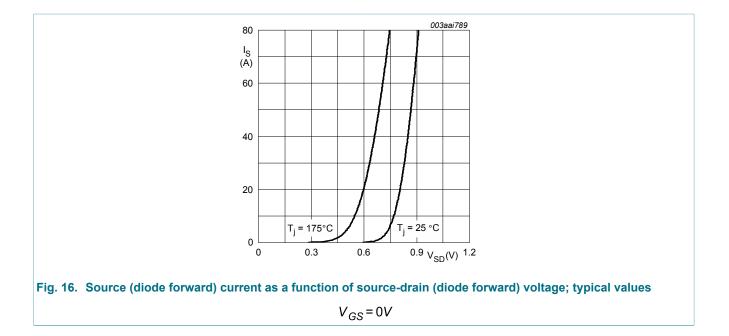
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#### N-channel 100 V, 15 mΩ logic level MOSFET in LFPAK56



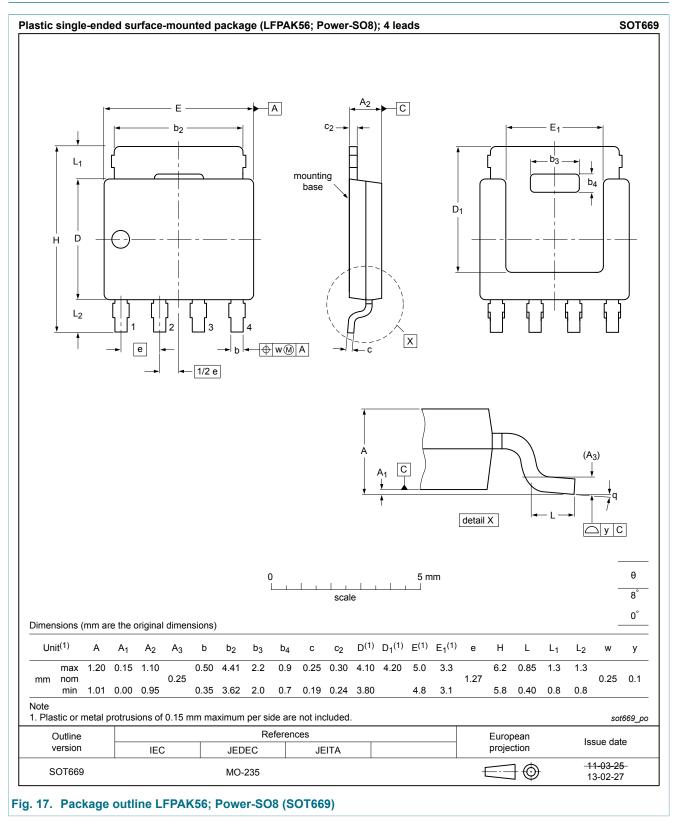
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#### N-channel 100 V, 15 mΩ logic level MOSFET in LFPAK56



#### N-channel 100 V, 15 m logic level MOSFET in LFPAK56

### **11. Package outline**



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#### N-channel 100 V, 15 mΩ logic level MOSFET in LFPAK56

### 12. Legal information

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Document status [1][2]	Product status [ <u>3]</u>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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#### N-channel 100 V, 15 mΩ logic level MOSFET in LFPAK56

### 13. Contents

1	General description	1
2	Features and benefits	1
3	Applications	1
4	Quick reference data	1
5	Pinning information	2
6	Ordering information	2
7	Marking	2
8	Limiting values	2
9	Thermal characteristics	4
10	Characteristics	5
11	Package outline	10
12	Legal information	11
12.1	Data sheet status	11
12.2	Definitions	11
12.3	Disclaimers	11
12.4	Trademarks	12

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