ADVANCED MULTI-CHEMISTRY AND MULTI-CELL SYNCHRONOUS SWITCH-MODE CHARGER AND SYSTEM POWER SELECTOR

FEATURES

- **High Efficiency:**
  - **– NMOS-NMOS Synchronous Buck Converter With Fixed 300 kHz Frequency**
  - **– Enhanced 6-V Drive Supply Voltage and 99.5% Max Duty Cycle**
- **High Voltage and Current Regulation Accuracy (0°C-85°C):**
  - **– 0.4% Charge Voltage Regulation Accuracy**
  - **– 4% Charge Current Regulation Accuracy**
  - **– 4% Adapter Current Regulation Accuracy Dynamic Power Management (DPM)**
- **3-Cell or 4-Cell Li-Ion Battery Voltage Select**
- **Programmable Battery Charge Current, and AC Adapter Current via Resistor**
- **2% Accurate Current Sense Amplifiers for Both Input Current and Charge Current (0°C-125°C)**
- **Input Current Sense Amplifier Can Be Enabled with No Adapter to Sense Battery Discharge Current**
- **Regulates Charge Current Down to 0-V Battery Voltage**
- **AC Adapter Operating Range 8 V–24 V**
- **Internal Soft Start**
- **Status Indicators:**
  - **– AC Adapter Present**
  - **– Low Battery Indicator**
  - **– DPM Regulation Loop Active Indicator**
- **Reverse Battery to Adapter Discharge Protection**
- **Battery/Adapter to System Power Selector Function**
- **Charge Overcurrent Protection**
- **Available in 40-Pin 5x7mm QFN Package**

APPLICATIONS

- **Portable Notebook Computers**
- **Portable DVD Players**
- **Webpads, PC Tablets**

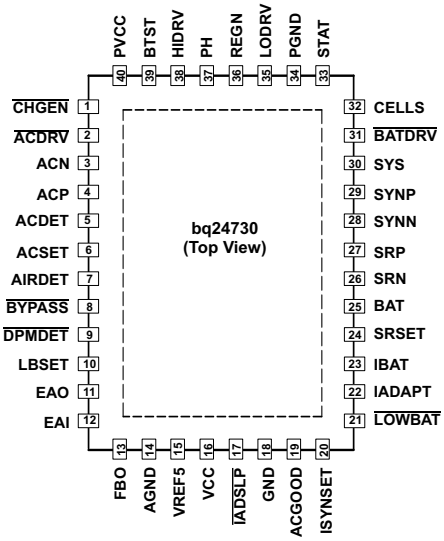
DESCRIPTION

The bq24730 is a high efficiency synchronous battery pack charger with high level of integration for portable applications. This device implements a high performance analog front-end that interfaces to the system power management micro-controller through a hardware interface.

The dynamic power management (DPM) function modifies the charge current depending on system load conditions, avoiding ac adapter overload.

High accuracy current sense amplifiers enable accurate measurement of either the charge current or the ac adapter current, allowing termination of nonsmart packs and monitoring of overall system power. The input current sense amplifier can be enabled with no adapter to sense battery discharge current.

Integrated features such as charger soft start, charge overcurrent protection, and IC temperature monitoring provide a second level of protection, in addition to pack and system protection functions.



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ORDERING INFORMATION

PART NO.	PACKAGE	BATTERY SHORTED (VERY LOW BATTERY VOLTAGE) OPERATION	ORDERING NUMBER (TAPE AND REEL)	QUANTITY
bq24730	40 PIN 5 x 7 mm QFN	Charge Current Down to BAT = 0 V	bq24730RGFR	3000
			bq24730RGFT	250

PACKAGE THERMAL DATA

PACKAGE(1)	θ_{JA}	TA ≤ 40°C POWER RATING	DERATING FACTOR ABOVE T_A = 25°C
RGF(2)	36°C/W	2.36 W	0.028 W/°C

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI Web site at www.ti.com.
(2) This data is based on using the JEDEC High-K board and the exposed die pad is connected to a copper pad on the board. This is connected to the ground plane by a 2×3 via matrix.

DEVICE INFORMATION

TERMINAL FUNCTIONS

TERMINAL		DESCRIPTION
NO.	NAME	
1	$\overline{\text{CHGEN}}$	Charge enable logic level low input. Logic High (HI) on the $\overline{\text{CHGEN}}$ pin disables the charger. Logic Low (LO) on the $\overline{\text{CHGEN}}$ pin enables the charger.
2	$\overline{\text{ACDRV}}$	AC adapter to system switch driver output. Connect directly to the gate of the ACFET PMOS power FET. Connect the FET source to the PVCC node and negative side of the input current-sense resistor. Connect the FET drain to the system load side. Recommend placing a 10-kΩ resistor from the gate to the source of the AC FET to keep the FET off when there is no power to the IC. If needed, an optional capacitor from gate to source of the ACFET is used to help slow down the ON and OFF times. The internal gate drive is asymmetrical allowing a quick turn-off and slower turn-off in addition to the internal break-before-make logic with respect to the $\overline{\text{BATDRV}}$.
3	ACN	Adapter current sense resistor, negative input. An optional 0.1-µF ceramic capacitor is placed from this pin to AGND for common-mode filtering. An optional 0.1-µF ceramic capacitor is placed from ACN to ACP to provide differential-mode filtering.
4	ACP	Adapter current sense resistor, positive input. Place this on the adapter side of the input current sense resistor. Recommend placing a 0.1-µF ceramic capacitor from ACP to AGND to provide common-mode filtering.
5	ACDET	AC adapter detected sense voltage input. Connect a voltage divider resistor from adapter input (before Bypass FET) to ACDET, and another resistor from ACDET to AGND, in order to program adapter detect threshold of 2.4 V. ACDET threshold should be greater than maximum battery regulation voltage, and lower than the minimum adapter voltage.
6	ACSET	AC adapter (input) current limit setting. Program input current limit by a resistor from ACSET to AGND. Input current is proportional to the current out of the ACSET pin.
7	AIRDET	Airline mode program pin. Program airline mode input voltage by a resistor divider between input voltage (before $\overline{\text{BYPASS}}$ FET) and AGND. VREF5 regulator and system power selector ($\overline{\text{BYPASS}}$ pin and $\overline{\text{ACDRV}}$ pin) are enabled 500 ms after AIRDET voltage rises above 1.2 V. Charge is disabled until 500 ms after AIRDET voltage rises above 1.2 V, and 8 ms after ACDET rises above 2.4 V.
8	$\overline{\text{BYPASS}}$	Gate drive for the adapter input BYPASS switch to prevent reverse discharge from the battery to the input. Connect this pin directly to the gate of the input bypass PMOS power FET. The drain of the FET is connected to the adapter input voltage node. The source of the FET is connected to the positive node of the input current-sense resistor. Recommend placing a 10-kΩ resistor from the gate to the source of the BYPASS FET to keep the FET off when there is no power to the IC. An optional capacitor can be placed from the gate to the source to slow-down the switching times. Adjusting the turn-on and turn-off times is typically not needed for this FET.
9	$\overline{\text{DPMDET}}$	Dynamic power management (DPM) input current loop active, open-drain output status. Logic low (LO) indicates input current is being limited by reducing the charge current. A 10-kΩ pull-up resistor to the host controller supply rail is needed.

DEVICE INFORMATION (continued)

TERMINAL FUNCTIONS (continued)

TERMINAL		DESCRIPTION
NO.	NAME	
10	LBSET	Low battery voltage threshold set. Program depleted battery pack threshold by a resistor from LBSET to AGND. The depleted voltage threshold is proportional to the voltage on the LBSET pin.
11	EAO	Error amplifier output for compensation. Connect the feedback compensation components from EAO to EAI. Typically, a capacitor in parallel with a series resistor and capacitor. See the compensation calculation procedures. This node is internally compared to the PWM saw-tooth oscillator.
12	EAI	Error amplifier negative input for compensation, also connect the feedback compensation components from EAI to EAO. Connect the input compensation components from FBO to EAI. See the compensation calculation procedures.
13	FBO	Feedback output for compensation. Connect the input compensation components from FBO to EAI. Typically, a resistor in parallel with a series resistor and capacitor. See the compensation calculation procedures.
14	AGND	Analog ground. Ground connection for low current sensitive analog and digital signals. Only connect to the PGND and GND nodes by connecting to the PowerPAD™ underneath the IC.
15	VREF5	5-V regulated voltage output, used for internal bias. Used to indicate adapter present status, since enabled by AC detected. Connect a 1-µF ceramic capacitor from VREF5 pin to AGND as close as possible to the IC .
16	VCC	IC analog positive supply. Connect to adapter input, or diode, or by putting a diode from adapter input and a diode from battery pack to VCC. Put a 1-µF ceramic capacitor from VCC to AGND, as close as possible to the IC.
17	$\overline{\text{IADSLP}}$	Adapter input current sense amplifier sleep mode enable logic input. Logic low (LO) input turns-off the input current sense amplifier (and enters sleep mode) when the input voltage falls below AIRDET threshold. Logic high (HI) input keeps-on the input current sense amplifier when the input voltage falls below AIRDET threshold and VCC is kept above 7 V. This allows measuring battery discharge current when the discharge path includes the voltage across ACP-ACN.
18	GND	Ground. Only connect to the AGND and PGND nodes by connecting to the PowerPAD™ underneath the IC.
19	ACGOOD	AC adapter voltage detected and above the AIRDET threshold, open-drain output. Logic high (HI) output indicates input voltage is above AIRDET threshold. A 10-kΩ pull-up resistor to the host controller supply rail is needed.
20	ISYNSET	Program current threshold for synchronous to nonsynchronous regulation transition. Place a resistor from ISYNSET to AGND to program the charge undercurrent threshold to force non-synchronous converter operation at low output current and prevent negative inductor current. Threshold should be set from inductor current ripple to the full value of inductor current ripple.
21	$\overline{\text{LOWBAT}}$	Low battery voltage, open-drain output. Logic low (LO) output on $\overline{\text{LOWBAT}}$ pin indicates the BAT voltage is below the LBSET depleted battery threshold. A 10-kΩ pull-up resistor to the host controller supply rail is needed.
22	IADAPT	Adapter current sense amplifier output. Current sense amplifier output voltage is 20x the current sense resistor differential voltage (ACP-ACN). Place a 0.1-µF capacitor from IADAPT to AGND for filtering the output ripple. Optionally, add an RC filter after the output capacitor for additional filtering.
23	IBAT	Battery charge current sense amplifier output. Current sense amplifier output voltage is 20x the current sense resistor differential voltage (SRP-SRN). Place a 0.1-µF capacitor from IBAPT to AGND for filtering the output ripple. Optionally, add an RC filter after the output capacitor for additional filtering.
24	SRSET	Battery charge current limit setting. Program battery charge current limit by a resistor from SRSET to AGND. Battery charge current is proportional to the current out of the SRSET pin.
25	BAT	Battery voltage remote sense. Directly connect a kelvin sense trace from the battery pack positive terminal to the BAT pin to accurately sense the battery pack voltage. Place a 0.1-µF capacitor from BAT to AGND close to the IC to filter high frequency noise.
26	SRN	Charge current sense resistor, negative input. Connect to the charge current sense resistor negative terminal. Optionally, add a 0.1-µF ceramic capacitor from SRN to AGND near the IC for common-mode filter.
27	SRP	Charge current sense resistor, positive input. Connect to the charge current sense resistor positive terminal. Placing a 0.1-µF ceramic capacitor from SRP to AGND near the IC for common-mode filter is recommend. Optionally, place a 0.1-µF ceramic capacitor from SRP to SRN near the IC for differential-mode filter.
28	SYNN	Charge overcurrent and charge undercurrent negative sense input. Connect to the charge current sense resistor negative terminal. If sensing the same sense resistor as SRN, the user can connect directly to the SRN pin and no further filter capacitors are needed. To sense a different sense resistor, add a 0.1-µF ceramic capacitor from SYNN to AGND near the IC for common-mode filter.
29	SYNP	Charge overcurrent and charge undercurrent negative sense input. Connect to the charge current sense resistor positive terminal. If sensing the same sense resistor as SRP, the user can connect directly to the SRP pin, and no further filter capacitors are needed. To sense a different sense resistor, add a 0.1-µF ceramic capacitor from SYNP to AGND near the IC for common-mode filter, and place a 0.1-µF ceramic capacitor from SYNP to SYNN near the IC for differential-mode filter.
30	SYS	System load, voltage sense. Connect directly to the system load node and the drain of the BAT PMOS power FET.

DEVICE INFORMATION (continued)

TERMINAL FUNCTIONS (continued)

TERMINAL		DESCRIPTION
NO.	NAME	
31	$\overline{\text{BATDRV}}$	Battery to system switch driver output. Gate drive for the battery to system load BAT PMOS power FET to isolate the system from the battery to prevent current flow from the system to the battery, while allowing a low impedance path from battery to system and while discharging the battery pack to the system load. Connect this pin directly to the gate of the input BAT PMOS power FET. Connect the source of the FET to the system load voltage node. Connect the drain of the FET to the battery pack positive node. Placing a 10-kΩ resistor from the gate to the source of the BAT FET to keep the FET off when there is no power to the IC is recommended. An optional capacitor is placed from the gate to the source to slow-down the switching times. The internal gate drive is asymmetrical allowing a quick turn-off and slower turn-off in addition to the internal break-before-make logic with respect to the $\overline{\text{ACDRV}}$.
32	CELLS	Battery pack cell select logic input. Logic low (LO) input programs 3-cell Li-Ion output voltage (12.6 V). Logic high (HI) input programs 4-cell Li-Ion output voltage (16.8 V)
33	STAT	Charger status, open-drain output. Logic low(LO) output indicates charger is on. Logic high (HI) output indicates controller is not charging. A 10-kΩ pull-up resistor to the host controller supply rail is needed.
34	PGND	Power ground. Ground connection for the high-current power converter nodes. Only connect to the AGND and GND nodes by connecting to the PowerPAD™ underneath the IC.
35	LODRV	PWM low side driver output. Connect directly to the gate of the low-side NMOS power FET with a short trace.
36	REGN	Low-side driver gate voltage regulator and source for high-side driver bootstrap voltage. Add a 1-µF ceramic capacitor from REGN pin to PGND pin, close to the IC. Place a small signal Schottky diode from REGN to BTST for bootstrap voltage.
37	PH	Synchronous buck phase node. Connect directly to the source of the high-side NMOS FET with a short trace. This node is the common connection between the high-side FET, low-side FET, and output inductor. Connect a 0.1-µF boot-strap ceramic capacitor from BTST to PH.
38	HIDRV	PWM high side driver output. Connect directly to the gate of the high-side NMOS power FET with a short trace.
39	BTST	High-side FET Boot-strap input pin. Connect to positive side of boot-strap capacitor. Connect a 0.1-µF bootstrap capacitor from the BTST pin to the PH node. Also, connect a bootstrap diode with the anode connected to the REGN pin and the cathode connected to the BTST pin. An optional 4.7-Ω - 15-Ω series resistor is placed between the BTST pin and the bootstrap-diode/capacitor junction to slow-down the turn-on time of the high-side FET for reducing ringing due to high dv/dt of the phase node.
40	PVCC	IC power positive supply. Connect directly to the drain of the high-side NMOS power FET. A 0.1-µF decoupling ceramic capacitor is recommended from PVCC to PGND.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)(1)(2)

	PIN	VALUE / UNIT
Supply voltage range	ACN, ACP, PVCC, $\overline{\text{ACDRV}}$, SYNN, SYNP, SRP, SRN , $\overline{\text{BATDRV}}$, BAT, $\overline{\text{BYPASS}}$, SYS, VCC	–0.3 V to 30 V
	PH	–1 V to 30 V
	LODRV, REGN, FBO, EAI, EAO, ACGOOD, ISYNSET, $\overline{\text{CHGEN}}$, VREF5, $\overline{\text{ACDET}}$, IBAT, $\overline{\text{STAT}}$, ACSET, AIRDET, $\overline{\text{DPMDET}}$, LBSET, $\overline{\text{IADSLP}}$, $\overline{\text{LOWBAT}}$, IADAPT, SRSET, CELLS	–0.3 V to 7 V
	BTST, HIDRV (with respect to AGND and PGND)	–1 V to 36 V
Maximum differential voltage	AGND-PGND, AGND-DGND	–0.3 V to 0.3 V
Maximum difference voltage	ACP–ACN , SRP–SRN, and SYNP–SYNN	0.6 V
Operating ambient temperature range (T_A)		–40°C to 85°C
Maximum junction temperature (T_J)		150°C
Storage temperature range (T_{stg})		–65°C to 150°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltages are with respect to AGND, unless otherwise noted. Currents are positive into, negative out of the specified terminal. Consult Packaging Section of the Data book for thermal limitations and considerations of packages.

RECOMMENDED OPERATING CONDITIONS

	PIN	MIN	NOM	MAX	UNIT
Supply voltage range	ACN, ACP, PVCC, $\overline{\text{ACDRV}}$, SRP, SRN, $\overline{\text{BATDRV}}$, BAT, $\overline{\text{BYPASS}}$, SYS, VCC, SYNN, SYNP	0		24	V
	PH	–0.5		24	V
	LODRV, REGN, VREF5	0		6.5	V
	FBO, EAI, EAO, ACGOOD, ISYNSET, $\overline{\text{CHGEN}}$, ACDET, STAT, ACSET, AIRDET, $\overline{\text{DPMDET}}$, LBSET, $\overline{\text{IADSLP}}$, $\overline{\text{LOWBAT}}$, SRSET, CELLS, IBAT, IADAPT, ACDET	0		5.5	V
	BTST, HIDRV	0		30	V
Maximum differential voltage	AGND-PGND, AGND-DGND			0	V
Maximum difference voltage	ACP–ACN, SYNN–SYNP, SRP–SRN			0.5	V
Junction temperature range (T_J)		-40		125	°C
Storage temperature range (T_{stg})		-55		150	°C

ELECTRICAL CHARACTERISTICS

8 Vdc ≤ $V_{(VCC)}$ ≤ 24 Vdc, 0°C ≤ T_J ≤ 125°C, all voltages with respect to AGND (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
BATTERY VOLTAGE REGULATION							
$V_{(BAT\_ICR)}$	VBAT Input voltage range	$V_{(BAT)}$		0		PVCC	V
	Battery regulation voltage Accuracy	12.6 V and 16.8 V	T_J = 0°C – 85°C	–0.4%		0.4%	
			T_J = 0°C – 125°C	–0.5%		0.5%	
$V_{(VBATREG)}$	BAT voltage regulation range	CELLS = 0			12.6		V
		CELLS = 1			16.8		
PWM AC ADAPTER INPUT CURRENT REGULATION, DPM (DYNAMIC POWER MANAGEMENT)							
$V_{(IREG\_DPM)}$	ACP-ACN differential voltage range for input current regulation	$V_{(IREG\_DPM)} = V_{(ACP)} - V_{(ACN)}$				200	mV
$V_{(ACSET)}$	Voltage on the ACSET pin				1		V
$G_{(ACSET)}$	ACSET gain				1000		V/A
	Current regulation accuracy	T_J = 0°C – 85°C, $V_{CC} \geq V_{CC}$ (min), $V_{CC} \geq V_{(BAT)} + V_{(DO-MAX)}$, (1) Over differential threshold range, $V_{(IREG)}$, Does not include error induced by the tolerance of the sense resistor, $R_{(SNS)}$	$V_{(ACP)} – V_{(ACN)}$ = 40 mV (4 A with 10 mΩ)	–3%		4%	
			$V_{(ACP)} – V_{(ACN)}$ = 20 mV (2 A with 10 mΩ)	–3%		7%	
			$V_{(ACP)} – V_{(ACN)}$ = 5 mV (0.5 A with 10 mΩ)	–25%		25%	
PWM BATTERY CHARGE CURRENT REGULATION							
$V_{(IREG\_CHG)}$	SRP-SRN differential voltage range for input current regulation	$V_{(IREG\_CHG)} = V_{(SRP)} - V_{(SRN)}$				200	mV
$V_{(SRSET)}$	Voltage on the SRSET pin				1		V
$G_{(SRSET)}$	SRSET gain				1000		V/A
	Current regulation accuracy	T_J = 0°C – 85°C, $V_{CC} \geq V_{CC}$ (min), $V_{CC} \geq V_{(BAT)} + V_{(DO-MAX)}$, (1) Over differential threshold range, $V_{(IREG)}$, Does not include error induced by the tolerance of the sense resistor, $R_{(SNS)}$	$V_{(SRP-SRN)}$ = 40 mV (4 A with 10 mΩ)	–3%		4%	
			$V_{(SRP-SRN)}$ = 20 mV (2 A with 10 mΩ)	–3%		7%	
			$V_{(SRP-SRN)}$ = 5 mV (0.5 A with 10 mΩ)	–25%		25%	
CHARGE CURRENT SENSE AMPLIFIER – IBAT AMPLIFIER							
$V_{(IBAT)}$	SRP, SRN common-mode input voltage range			2.5		20	V
	IBAT output voltage range	$V_{(IBAT)} = V_{(SRP,\ SRN)} \times G_{(IBAT)}$ $V_{(BAT)}$ > 2.5 V or $V_{(BAT)} > V_{(IBAT)} + V_{(DO-MAX)}$(1)		0		3.5	V
$G_{(IBAT)}$	Voltage gain	$G_{(IBAT)} = V_{(IBAT)} / V_{(SRP,\ SRN)}$			20		V/V
	Charge current sense amplifier output voltage accuracy	$V_{(BAT)}$ > 2.5 V or $V_{(BAT)} > V_{(IBAT)} + V_{(DO-MAX)}$(1)	$V_{(SRP-SRN)}$ = 40 mV (4 A with 10 mΩ)	–2%		2%	
			$V_{(SRP-SRN)}$ = 20 mV (2 A with 10 mΩ)	–3%		3%	
			$V_{(SRP-SRN)}$ = 5 mV (0.5 A with 10 mΩ)	–25%		25%	
$I_{(BAT\_LIM)}$	IBAT output current limit	IBAT shorted to AGND		4.5			mA

(1) $V_{(DO-max)}$ is defined as the maximum drop-out voltage. $V_{(DO-max)}$= 1 V unless other wise specified. In an actual application, $V_{(DO\ -\ MAX)} = (R_{(SNS)} \times I_O) + V_{(DSON\_HIGH\_SIDE\_FET)} + V_{(DSON\_BYPASS\_FET)}$.

ELECTRICAL CHARACTERISTICS (continued)

8 Vdc ≤ $V_{(VCC)}$ ≤ 24 Vdc, 0°C ≤ T_J ≤ 125°C, all voltages with respect to AGND (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
INPUT CURRENT SENSE AMPLIFIER - IADAPT AMPLIFIER							
$V_{(IADAPT)}$	ACP, ACN Common-mode input voltage range			0		24	V
	IADAPT output voltage range	$V_{(IADAPT)} = V_{(ACP, ACN)} \times G_{(IADAPT)}$ $V_{(SRP)}$ > 2.5 V or $V_{(SRP)} > V_{(IADAPT)}$ + 1 V		0		3.5	V
$G_{(IADAPT)}$	Voltage gain	$G_{(IADAPT)} = V_{(IADAPT)} / V_{(ACP, ACN)}$			20		V/V
	Adapter current sense amplifier output voltageaccuracy	$V_{(BAT)}$ > 2.5 V or $V_{(BAT)} > V_{(IADAPT)} + V_{(DO-MAX)}$ (1)	$V_{(ACP)} - V_{(ACN)}$ = 40 mV (4 A with 10 mΩ)	–2%		2%	
			$V_{(ACP)} - V_{(ACN)}$ = 20 mV (2 A with 10 mΩ)	–3%		3%	
			$V_{(ACP)} - V_{(ACN)}$ = 5 mV (0.5 A with 10 mΩ)	–25%		25%	
$I_{(ADAPT\_LIM)}$	IADAPT output current limit	IADAPT shorted to AGND		4.5			mA
OPERATING CONDITIONS							
	$V_{(VCC)}$, $V_{(PVCC)}$, input voltage operating range	Selector and charger operational.		8		24	V
QUIESCENT CURRENT – NO ADAPTER CONNECTED							
$I_{(VCC,PVCC)}$	VCC and PVCC quiescent current	$I_{(VCC,PVCC)} = (I_{(VCC)} + I_{(PVCC)})$ at $V_{(VCC)} = V_{(PVCC)}$ = 16.8 V				254	µA
$I_{(ACP,ACN)}$	ACP and ACN quiescent current	$I_{(ACP,ACN)} = (I_{(ACP)} + I_{(ACN)})$ at $V_{(ACP)} = V_{(ACN)} = V_{(VCC)} = V_{(PVCC)}$ = 16.8 V				1	µA
$I_{(BAT)}$	BAT quiescent current	$I_{(BAT)}$ at $V_{(BAT)} = V_{(VCC)} = V_{(PVCC)}$ = 16.8 V				17	µA
$I_{(SRP,SRN)}$	SRP and SRN quiescent current	$I_{(SRP,SRN)} = (I_{(SRP)} + I_{(SRN)})$ at $V_{(SRP)} = V_{(SRN)} = V_{(VCC)} = V_{(PVCC)}$ = 16.8 V				1	µA
$I_{(SYNN,SYNP)}$	SYNN and SYNP quiescent current	$I_{(SYNN,SYNP)} = (I_{(SYNN)} + I_{(SYNP)})$ at $V_{(SYNP)} = V_{(SYNN)} = V_{(VCC)} = V_{(PVCC)}$ = 16.8 V				1	µA
$I_{(SYS)}$	SYS quiescent current	$I_{(SYS)}$ at $V_{(SYS)} = V_{(VCC)} = V_{(PVCC)}$ = 16.8 V				25	µA
$I_{(PH)}$	PH quiescent current	$I_{(PH)}$ at $V_{(PH)} = V_{(VCC)} = V_{(PVCC)}$ = 16.8 V				1	µA
$I_{(BTST)}$	BTST quiescent current	$I_{(BTST)}$ at $V_{(BTST)} = V_{(VCC)} = V_{(PVCC)}$ = 16.8 V				1	µA
QUIESCENT CURRENT – ADAPTER CONNECTED AND READY TO CHARGE							
$I_{(VCC,PVCC)}$	VCC and PVCC quiescent current, while converter is not switching	$I_{(VCC,PVCC)} = (I_{(VCC)} + I_{(PVCC)})$ at $V_{(VCC)} = V_{(PVCC)}$ = 16.8 V, charger off ($\overline{CHGEN}$ = HI) = DISABLED				4.45	mA
$I_{(VCC\_SW)}$	VCC Current while converter is switching including gate drive current	$I_{(VCC\_SW)} = I_{(VCC)}$ FPWM = 300 kHz, charger on ($\overline{CHGEN}$ = LO) = ENABLED $Q_{(G)}$ at HIDRV = $Q_{(G)}$ at LODRV = 30 nC, [No Load on VREF5] Gate drive switching current = $Q_{(G)} \times$ FPWM = (30 nC + 30 nC) × 300kHz = 18 mA			25		mA
5-V REFERENCE LDO VOLTAGE AND AC DETECTION STATUS (VREF5, TURNS ON WHEN AIRDET DETECTED)							
V_{VREF5}	5V Regulator output voltage	Adapter detected ($V_{ACDET} > V_{(ACD)}$), V_{CC}> 7 V 0 → 10 mA, source current		4.75	5	5.25	V
V_{VREF5_SAT}	Saturation voltage when VREF5 is off	Adapter not detected, ($V_{ACDET} < V_{(ACD)}$) 0 →– 10 mA, ac adapter inserted, C_O = 1 µF, discharge load			0.15		V
I_{VREF5_LIM}	Short-circuit current	$V_{(VREF5)}$ = AGND			20		mA
UNDERVOLTAGE LOCKOUT CIRCUIT							
UVLO	Undervoltage lockout threshold	VREF5 rising, POR mode set at VREF5 < $V_{(UVLO)}$			3.7		V
	$V_{(UVLO)}$ hysteresis	VREF5 falling			100		mV
CONTROL LOGIC INPUTS ($\overline{CHGEN}$, CELLS, IADSPL)							
V_{IL}	Input low threshold level	2.7 V < $V_{(pull-up)}$ < 5.5 V				0.8	V
V_{IH}	Input high threshold level	2.7 V < $V_{(pull-up)}$ < 5.5 V		2.1			V
I_{lkg}	Leakage current	Pin V = 5.5 V				1	µA
OPEN DRAIN OUTPUT (ACGOOD, STAT, LOWBAT, $\overline{DPMDET}$)							
$V_{(OL\_sat)}$	Output saturation voltage	I = 5 mA				0.5	V
I_{lkg}	Leakage current	$V_{(PULL-UP)}$ = 5 V				1	µA
CHARGE OVERCURRENT COMPARATOR							
$V_{(OLP)}$	Overcurrent protection threshold	$V_{(SRP-SRN)}$ rising			190		$\%I_{(REG\_CHG)}$
$V_{(OLPH)}$	Hysteresis	$V_{(SRP-SRN)}$ falling			20		$\%I_{(REG\_CHG)}$
CHARGE UNDERCURRENT THRESHOLD (SYNCHRONOUS to NONSYNCHRONOUS CURRENT)							
$V_{(ISYNSET)}$	ISYNSET voltage				1		V
$G_{(ISYNSET)}$	ISYNSET gain				500		V/A
THERMAL SHUTDOWN							
$T_{(SHUT)}$	Thermal shutdown threshold	T_J rising, Charge disabled at T_J > $T_{(SHUT)}$			145		°C
$T_{(SHUTH)}$	Hysteresis	T_J falling, Charge enabled at T_J < $T_{(SHUT)} - T_{(SHUTH)}$			15		°C
	Deglitch time, thermal shutdown	T_J rising/falling			8		ms

ELECTRICAL CHARACTERISTICS (continued)

8 Vdc ≤ $V_{(VCC)}$ ≤ 24 Vdc, 0°C ≤ T_J ≤ 125°C, all voltages with respect to AGND (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ACDET and AIRDET STATUS COMPARATOR INPUT CURRENT SPECIFICATION						
$I_{(bias)}$	Input bias currents at pin ACDET , AIRDET	$V_{(ACDET)}$ = 2.4V, $V_{(AIRDET)}$ = 1.2V		0.1		µA
AC ADAPTER DETECT COMPARATOR (ACDET)						
$V_{(ACD)}$	AC adapter detect threshold	$V_{(ACDET)}$ rising, When adapter detected, VREF5 is enabled, and REGN regulates to 6 V	2.371	2.4	2.429	V
$V_{(ACDH)}$	AC adapter detect hysteresis	$V_{(ACDET)}$ falling		15		mV
	AC adapter detected deglitch time	$V_{(ACDET)}$ rising		8		ms
	AC adapter not detected deglitch time	$V_{(ACDET)}$ falling		8		ms
AIRLINE ADAPTER DETECT COMPARATOR (AIRDET)						
$V_{(AIRD)}$	AIRLINE adapter detect threshold	$V_{(AIRDET)}$ rising, When adapter detected, VREF5 is enabled, and REGN regulates to 6 V	1.176	1.2	1.224	V
$V_{(AIRDH)}$	AIRLINE adapter detect hysteresis	$V_{(AIRDET)}$ falling		15		mV
	AIRLINE adapter detect deglitch time	$V_{(AIRDET)}$ rising		8		ms
	AIRLINE adapter detect not deglitch time	$V_{(AIRDET)}$ falling		1		µs
SYSTEM (SYS) - BATTERY (BAT) COMPARATOR						
$V_{(SYS-BAT)}$	System voltage above pack voltage at $V_{(VS,BAT)}$ > $V_{(SYS)}$	$V_{(SYS)}$ falling with respect to $V_{(BAT)}$		250	300	mV
$V_{(SYS-BAT)}$	Hysteresis	$V_{(SYS-BAT)}$ rising with respect to $V_{(BAT)}$		50		mV
	$V_{(SYS-BAT)}$ falling below threshold deglitch time	$V_{(SYS)}$ falling with respect to $V_{(BAT)}$		1		µs
	$V_{(SYS-BAT)}$ rising above threshold deglitch time	$V_{(SYS-BAT)}$ rising with respect to $V_{(BAT)}$		8		ms
LOW BATTERY DETECT COMPARATOR ($V_{(LOWBAT)} = K_{(LBSET)} \times I_{(LBSET)} \times R_{(LBSET)}$)						
$I_{(LBSET)}$	LBSET current	$V_{(ACDET)}$ > 2.4 V	4.8	5	5.15	µA
$K_{(LBSET)}$	LBSET scale factor	$V_{(ACDET)}$ > 2.4 V, CELLS = 0 (#CELLS = 3), CELLS = 1 (#CELLS = 4)		2		V/V
	LOWBAT deglitch time	Rising and falling		1		s
BYPASS P-Channel MOSFET DRIVER ($\overline{BYPASS}$)						
$R_{(DS\_BYP)\ Hi}$	$\overline{BYPASS}$ off-state resistance	Driver output = HI, $\overline{BYPASS}$ = $V_{(PVCC)}$, $V_{(PVCC)}$ = 18 V		1	2	kΩ
$R_{(DS\_BYP)\ Lo}$	$\overline{BYPASS}$ on-state resistance	Driver output = LO, $\overline{BYPASS}$ = $V_{(PVCC)}$ - $V_{(REGBYPASS)}$, $V_{(PVCC)}$ = 18 V		1	2	kΩ
$V_{(REGBYPASS)}$	Drive regulator turn-on voltage for $\overline{BYPASS}$ with respect to $V_{(PVCC)}$	$V_{(VCC,\ \overline{BYPASS})}$, $V_{(VCC)}$ > 13 V, $I_{(\overline{BYPASS})}$ = 5 mA	-5	-6	-7.5	V
AC ADAPTER P-Channel MOSFET DRIVER ($\overline{ACDRV}$)						
$R_{(DS\_AC)\ Hi}$	$\overline{ACDRV}$ off-state resistance	Driver output = HI, $\overline{ACDRV}$ = PVCC, $V_{(PVCC)}$ = 18 V		100	150	Ω
$R_{(DS\_AC)\ Lo}$	$\overline{ACDRV}$ on-state resistance	Driver output = LO, $\overline{ACDRV}$ =$V_{(PVCC)}$-$V_{(REGAC)}$, $V_{(PVCC)}$ = 18 V		10	20	kΩ
$V_{(REGAC)}$	Drive regulator turn-on voltage for $\overline{ACDRV}$ with respect to $V_{(PVCC)}$	$V_{(VCC,\ \overline{ACDRV})}$, $V_{(VCC)}$ > 13 V, $I_{(\overline{ACDRV})}$ = 5 mA	-5	-6.5	-7.5	V
BATTERY P-Channel MOSFET DRIVER ($\overline{BATDRV}$)						
$R_{(DS\_BAT)\ Hi}$	$\overline{BATDRV}$ off-state resistance	Driver output = HI, $V_{(PVCC)}$ = 18 V		100	150	Ω
$R_{(DS\_BAT)\ Lo}$	$\overline{BATDRV}$ on-state resistance	Driver output = LO, $\overline{BATDRV}$=$V_{(PVCC)}$-$V_{(REGBAT)}$, $V_{(PVCC)}$ = 18 V		10	20	kΩ
$V_{(REGBAT)}$	Drive regulator negative turn-on voltage for $\overline{BATDRV}$ with respect to $V_{(SYS)}$	$V_{(VCC,\ \overline{BATDRV})}$, $V_{(VCC)}$ > 13 V, $I_{(\overline{BATDRV})}$ = 5 mA	-5	-6.5	-7.5	V
SYSTEM POWER SELECTOR TIMING						
	Dead time when switching between ACDRV and BATDRV	No load at ACDRV and BATDRV		1		µs
BYPASS SWITCH TIMING						
	Delay to turn-off BYPASS			1		µs
PWM HIGH-SIDE N-Channel MOSFET DRIVER (HIDRV)						
$R_{(DS\_HIDRV)\ Hi}$	High-side on-state resistance	HSD switch on, HIDRV = HI, $V_{(BOOST,PH)}$ = 5.5 V		5.6	7.6	Ω
$R_{(DS\_HIDRV)\ Lo}$	High-side off-state resistance	HSD switch off, HIDRV = LO, $V_{(BOOST,PH)}$ = 5.5 V		1.5	2.5	Ω
PWM LOW-SIDE N-Channel MOSFET DRIVER (LODRV)						
$R_{(DS\_LODRV)\ Hi}$	Low-side on-state resistance	LSD switch on, LODRV = HI, $V_{(PVCC)}$ = 7 V		5.6	7.6	Ω
$R_{(DS\_LODRV)\ Lo}$	Low-side off-state resistance	LSD switch off, LODRV = LO, $V_{(PVCC)}$ = 7 V		1.5	2.5	Ω

ELECTRICAL CHARACTERISTICS (continued)

8 Vdc ≤ $V_{(VCC)}$ ≤ 24 Vdc, 0°C ≤ T_J ≤ 125°C, all voltages with respect to AGND (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
PWM LOW-SIDE DRIVER REGULATOR (REGN)						
$V_{O(HREGN)}$	REGN output voltage	$V_{(REGN)}$ at $I_{(REGN)}$ = 10 mA, sourcing, Adapter detected ($V_{(ACDET)}$ > $V_{(ACD)}$), $V_{(PVCC)}$ > 7 V	5.5	6	6.5	V
		$V_{(REGN)}$ at $I_{(REGN)}$ = 10 mA, sourcing, Adapter not detected, (V_{ACDET} < $V_{(ACD)}$), $V_{(PVCC)}$ > 7 V		4.2		V
$I_{O(REGN\_SW)}$	REGN output current while charger switching	2 times 25 nC load, fs = 300 kHz		15		mA
$I_{(REGN\_LIM)}$	REGN Current limit Adapter detected	$V_{(REGN)}$ = 5 V ($V_{(ACDET)}$ > $V_{(ACD)}$), $V_{(PVCC)}$> 7 V		100		mA
		$V_{(REGN)}$ = 0 V, shorted ($V_{(ACDET)}$ > $V_{(ACD)}$), $V_{(PVCC)}$> 7 V	13.3			mA
	REGN Current limit Adapter not detected	$V_{(REGN)}$ = 4.2 V ($V_{(ACDET)}$ < $V_{(ACD)}$), $V_{(PVCC)}$> 7 V		15		mA
PWM DRIVERS TIMING						
	Dead time when switching between LSD and HSD, no load at LSD and HSD			30		ns
PWM OSCILLATOR						
$V_{(RAMPLO)}$	PWM oscillator ramp voltage , low value	0% duty cycle occurs below this threshold		0.35		V
$V_{(RAMPHI)}$	PWM oscillator ramp voltage , high value	Near 100% duty cycle occurs above this threshold			3	V
$V_{PP(RAMP)}$	PWM ramp peak-to-peak amplitude			0.1×VCC		V
$V_{(RAMPCL)}$	PWM oscillator ramp clamp voltage			3.5		V
f_S	PWM oscillator frequency (300 kHz)		265	300	345	kHz
INTERNAL SOFT START (8 steps to Ireg)						
	SRSET pin voltage number of steps during soft start.	Eight steps of charge current regulation to get to programmed value SRSET = 1 V.		8		step
	Step Duration.	Eight steps of charge current regulation to get to programmed value SRSET = 1 V.	0.8	1	1.2	ms/step
CHARGER SECTION POWER-UP SEQUENCING						
	Time delay between power up of charger block references (first) and start charge (second)			1		ms
	Time delay from adapter detected until ACDRV enable and charger block enable			500		ms

TYPICAL CHARACTERISTICS

(Default Operating Conditions: V_I = 20 V, $V_{(BAT)}$ = 12.6 V, $I_{(charge)}$ = 3 A, unless otherwise specified)

VREF5 LOAD REGULATION vs LOAD CURRENT

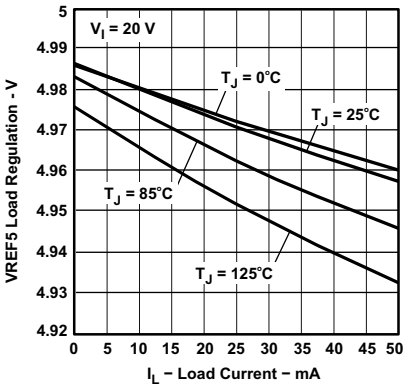


Figure 1.

REGN LOAD REGULATION vs LOAD CURRENT

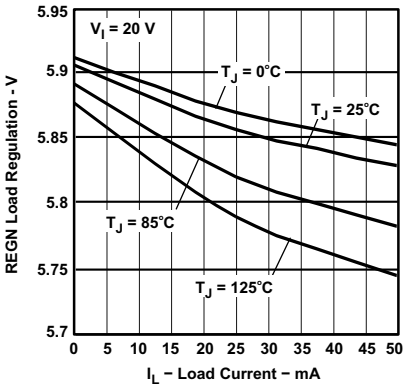


Figure 2.

REGN CURRENT LIMIT vs FORCED REGN VOLTAGE

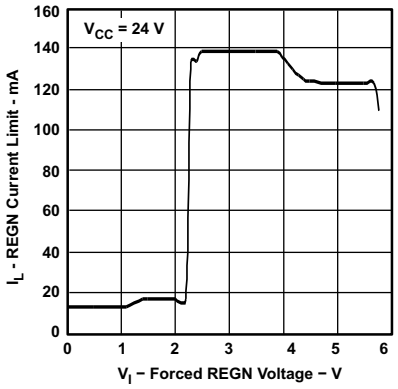


Figure 3.

CHARGE CURRENT REGULATION ACCURACY vs SRP-SRN VOLTAGE

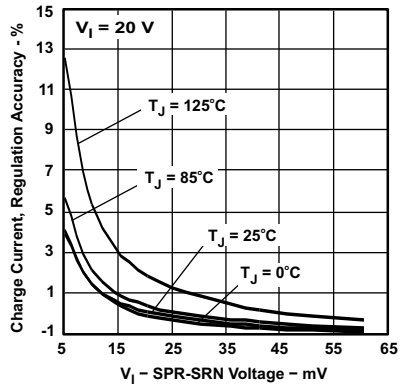


Figure 4.

INPUT CURRENT REGULATION (DPM) ACCURACY vs ACP-ACN VOLTAGE

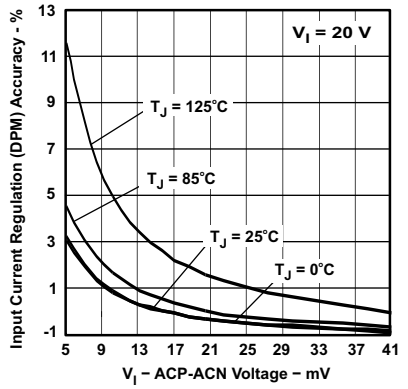


Figure 5.

$V_{(IADAPT)}$ = DPM CURRENT SENSE AMPLIFIER ACCURACY vs ACP-ACN VOLTAGE

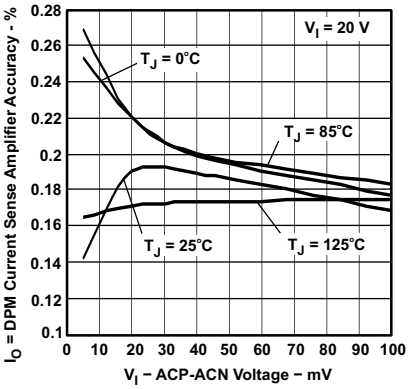


Figure 6.

TYPICAL CHARACTERISTICS (continued)

$V_{(IBAT)}$ = CHARGE SENSE AMPLIFIER ACCURACY vs SRP-SRN VOLTAGE

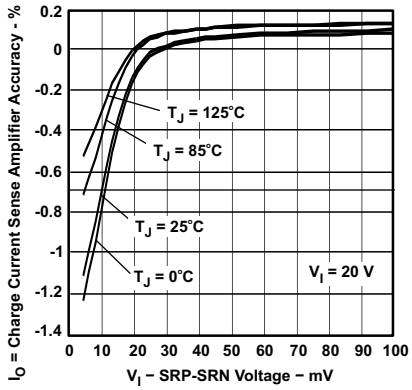


Figure 7.

300-kHz SWITCHING FREQUENCY vs INPUT VOLTAGE

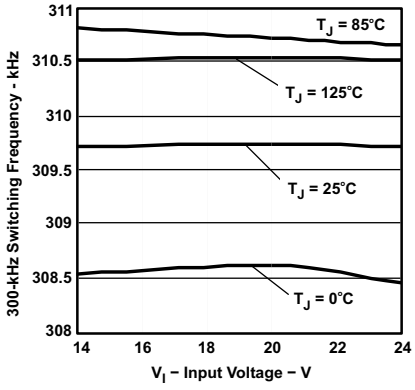


Figure 8.

EFFICIENCY vs BATTERY CHARGE CURRENT

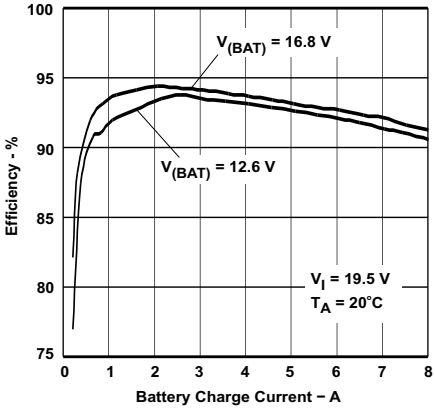


Figure 9.

BATTERY REMOVAL (CONSTANT CURRENT MODE)

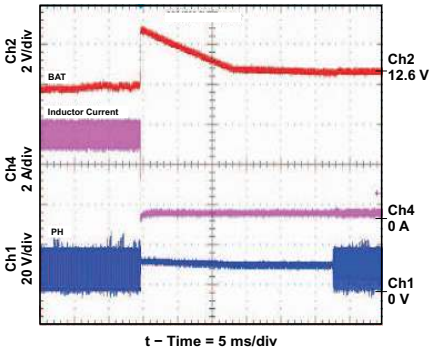


Figure 10.

REGULATION CURRENT vs SYSTEM CURRENT

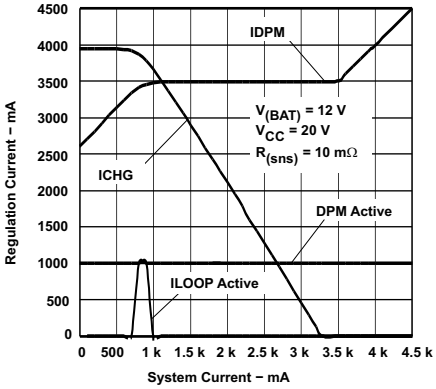


Figure 11.

TRANSIENT SYSTEM LOAD

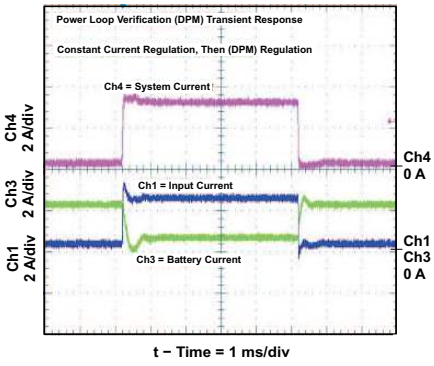


Figure 12.

SYSTEM SELECTOR GATE DRIVES AFTER ACDET

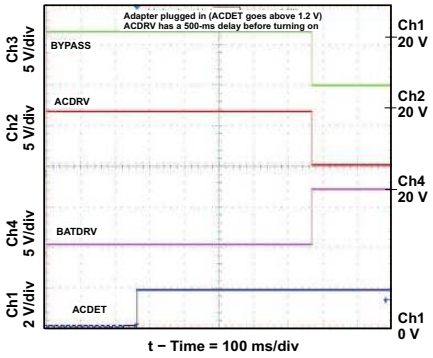


Figure 13.

SYSTEM SELECTOR ADAPTER INSERTION

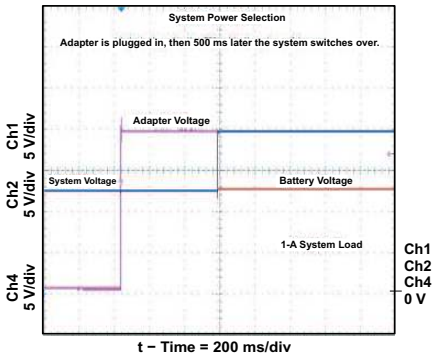


Figure 14.

SYSTEM SELECTOR ADAPTER REMOVAL

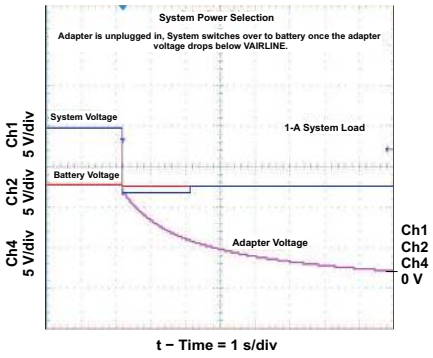


Figure 15.

TYPICAL CHARACTERISTICS (continued)

REGN VREF5 POWER UP

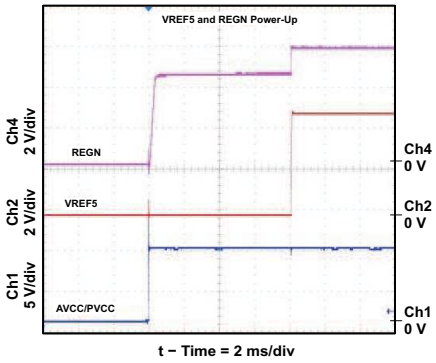


Figure 16.

SOFTSTART CHARGE CURRENT

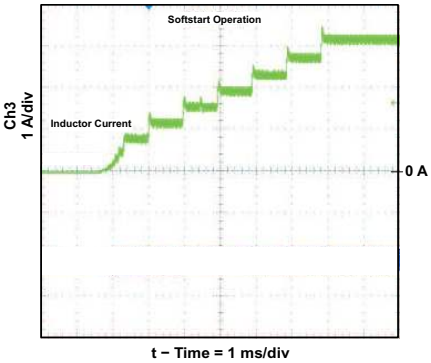


Figure 17.

NON-SYNCHRONOUS TO SYNCHRONOUS TRANSITION

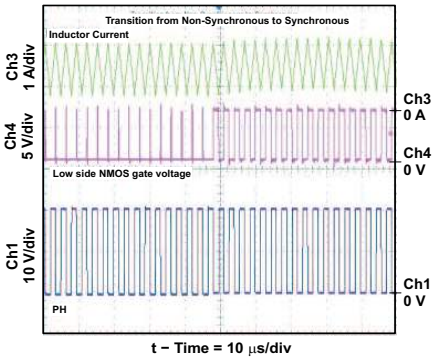


Figure 18.

SYNCHRONOUS TO NON-SYNCHRONOUS TRANSITION

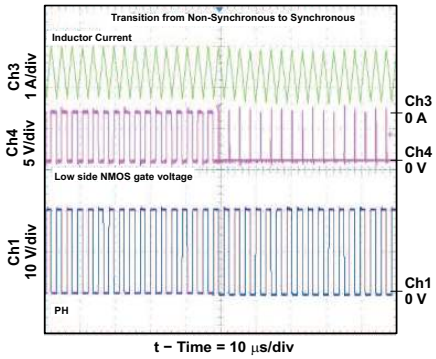


Figure 19.

NEAR 100% DUTY CYCLE BTST RECHARGE PULSE

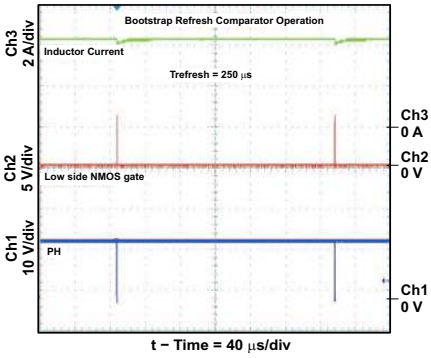


Figure 20.

BATTERY SHORT RESPONSE

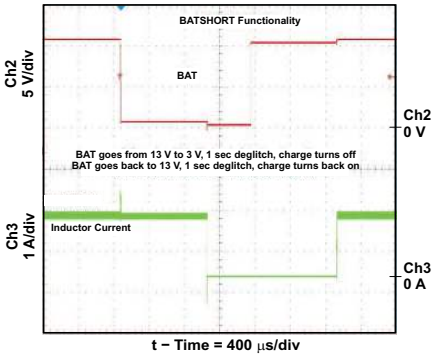


Figure 21.

CHARGE OVERCURRENT

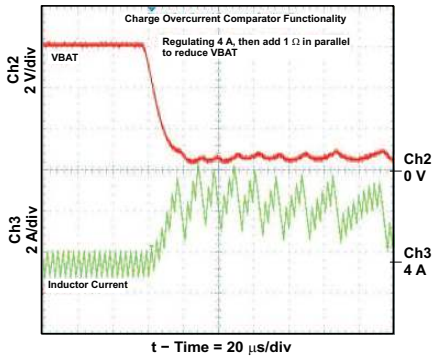


Figure 22.

SWITCHING CONTINUOUS CURRENT MODE (CCM)

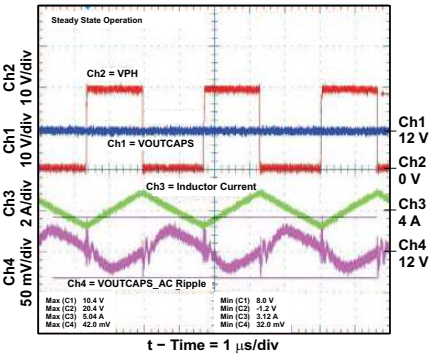


Figure 23.

SWITCHING DISCONTINUOUS CURRENT MODE VS (DCM)

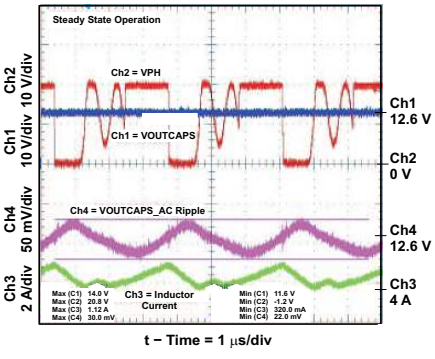


Figure 24.

SIMPLIFIED BLOCK DIAGRAM

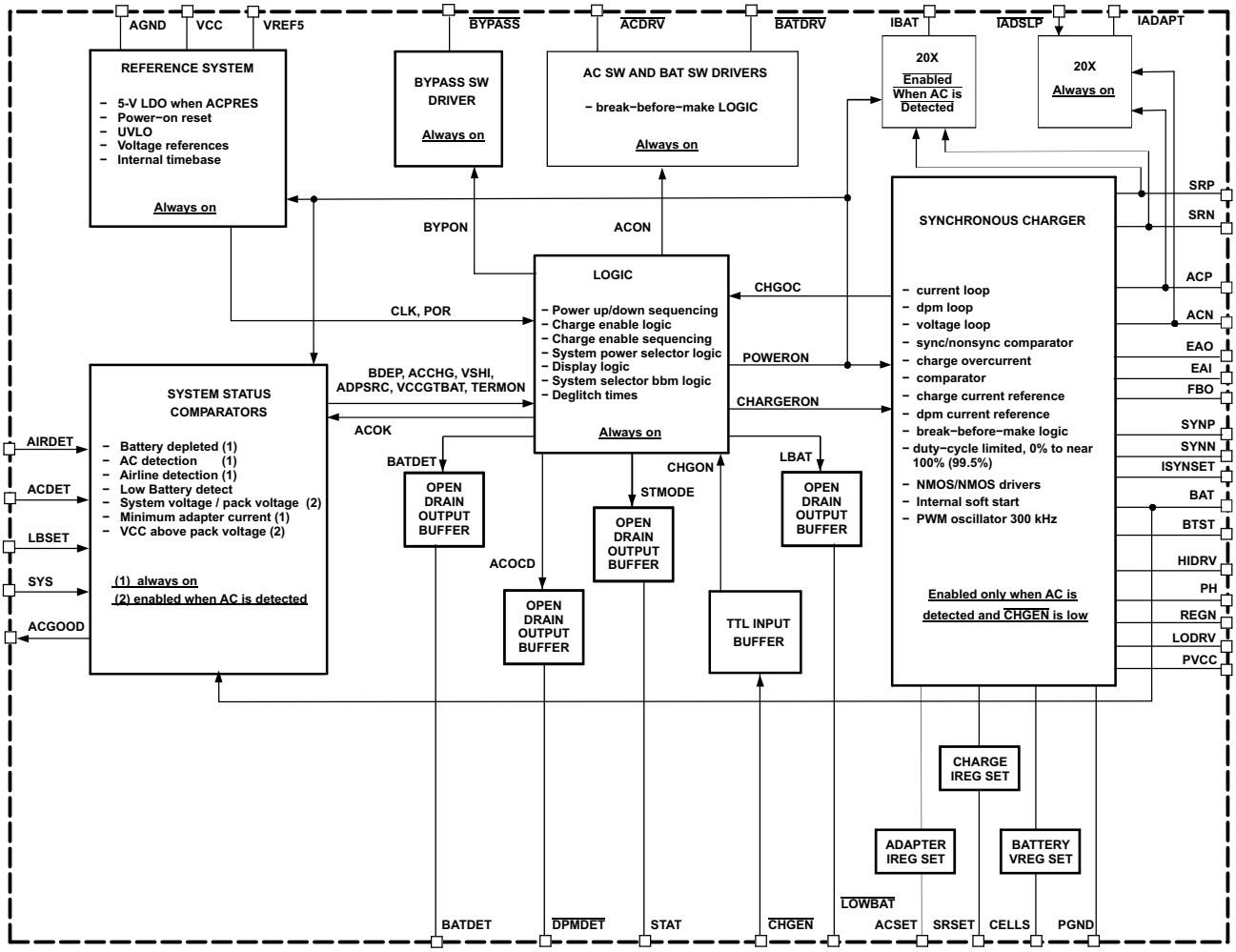


Figure 25. bq24730 Simplified Block Diagram

TYPICAL APPLICATION bq24730 [V_I = 20 V, $I_{I(lim)}$ = 4.76 A, $I_{(charge)}$ = 3 A, $V_{(BAT)}$ = 16.8 V 4-cells]

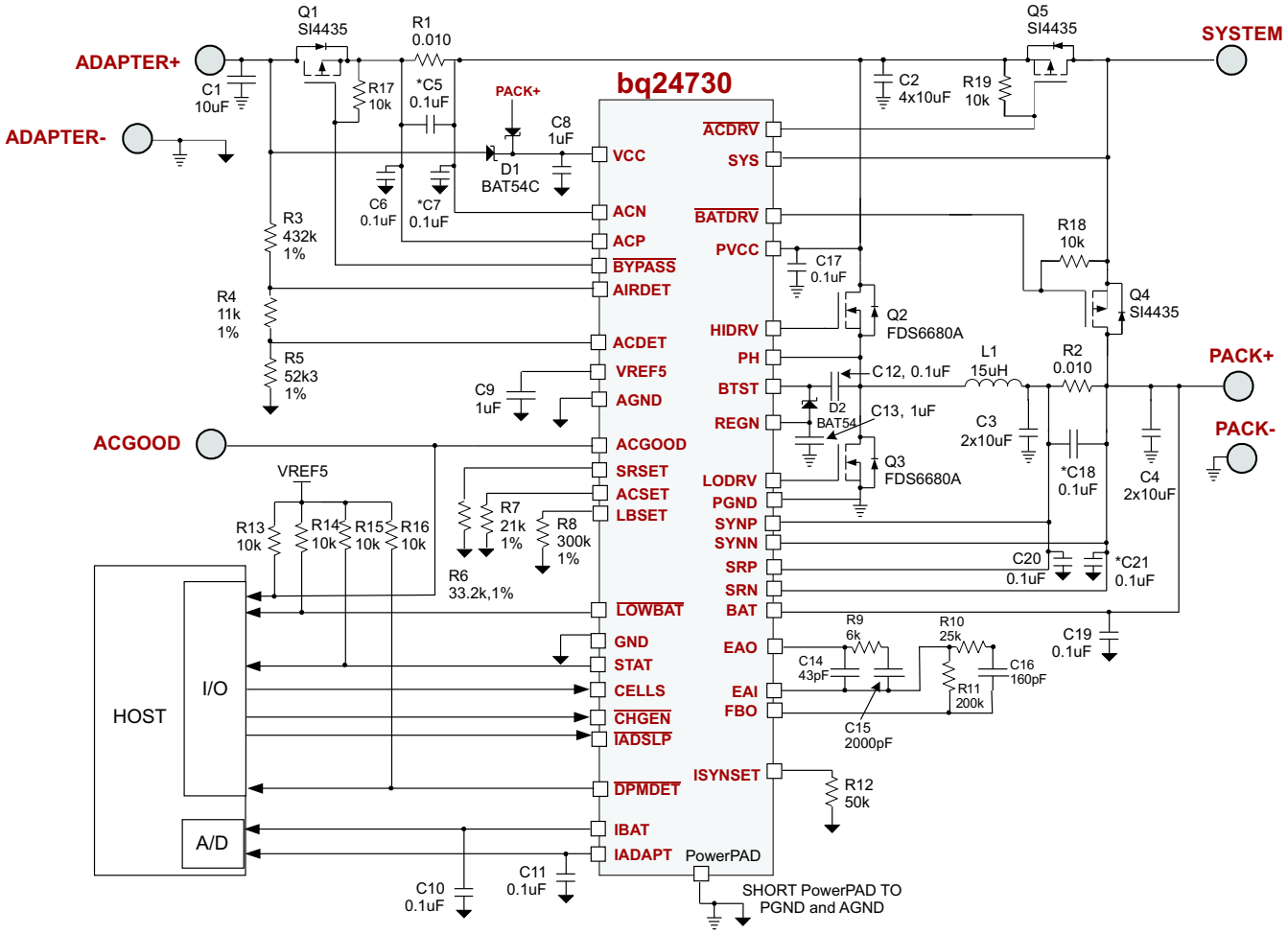


Figure 26. bq24730 Host Control With System Power Selector

BOM Key Components (For Figure 26, bq24730 Typical Application Circuit)

Reference Designator	Qty	Description(1)
Q2, Q3	2	N-channel MOSFET, 30V, 12.5A, SO-8, FDS6680A
Q1, Q4, Q5	3	P-channel MOSFET, -30V,-6A, SO-8, Vishay-Siliconix, Si4435
D1	1	Diode, Dual Schottky, 30V, 200mA, SOT23, Fairchild, BAT54C
D2	1	Diode, Single Schottky, 30V, 200mA, SOT23, Fairchild, BAT54
L1	1	Inductor, 15µH, 5A, 25mΩ, Coiltronics, DR127-150
R1, R2	2	Sense Resistor, 10 mΩ, 1%, 0.5W, 2010, Vishay-Dale, WSL2010R0100F
C1, C2, C3, C4	4	Capacitor, Ceramic, 10µF, 35V, 20%, X5R, 1206, Panasonic, ECJ-3YB1E106M
C8, C9	2	Capacitor, Ceramic, 1µF, 25V, 10%, X7R, 2012, TDK, C2012X7R1E105K
C6, C10, C11, C12, C13, C17, C19, C20, (C5, C7, C18 and C21 optional)	12	Capacitor, Ceramic, 0.1µF, 50V, 10%, X7R, 0805, Kemet, C0805C104K5RACTU
C14	1	Capacitor, Ceramic, 43pF, 50V, 5%, NPO, 0603
C15	1	Capacitor, Ceramic, 2000pF, 50V, 5%, X7R, 0805
C16	1	Capacitor, Ceramic, 160pF, 50V, 5%, NPO, 0603

(1) The manufacturer's part number are used for test purposes only.

BOM Key Components (For Figure 26, bq24730 Typical Application Circuit) (continued)

Reference Designator	Qty	Description(1)
R3	1	Resistor, Chip, 432kΩ, 1/16W, 1%, 0402
R4	1	Resistor, Chip, 11kΩ, 1/16W, 1%, 0402
R5	1	Resistor, Chip, 52.3kΩ, 1/16W, 1%, 0402
R6	1	Resistor, Chip, 33.2kΩ, 1/16W, 1%, 0402
R7	1	Resistor, Chip, 21kΩ, 1/16W, 1%, 0402
R8	1	Resistor, Chip, 300kΩ, 1/16W, 1%, 0402
R9	1	Resistor, Chip, 6kΩ, 1/16W, 1%, 0402
R10	1	Resistor, Chip, 25kΩ, 1/16W, 1%, 0402
R11	1	Resistor, Chip, 200kΩ, 1/16W, 1%, 0402
R12	1	Resistor, Chip, 50kΩ, 1/16W, 1%, 0402
R13, R14, R15, R16, R17, R18, R19	7	Resistor, Chip, 10kΩ, 1/16W, 5%, 0402

Typical bq24730 With Battery Discharge Current Sensing [V_I = 20 V, $I_{I(lim)}$ = 4.76 A, $I_{(charge)}$ = 3 A, $V_{(BAT)}$ = 16.8 V 4-cells]

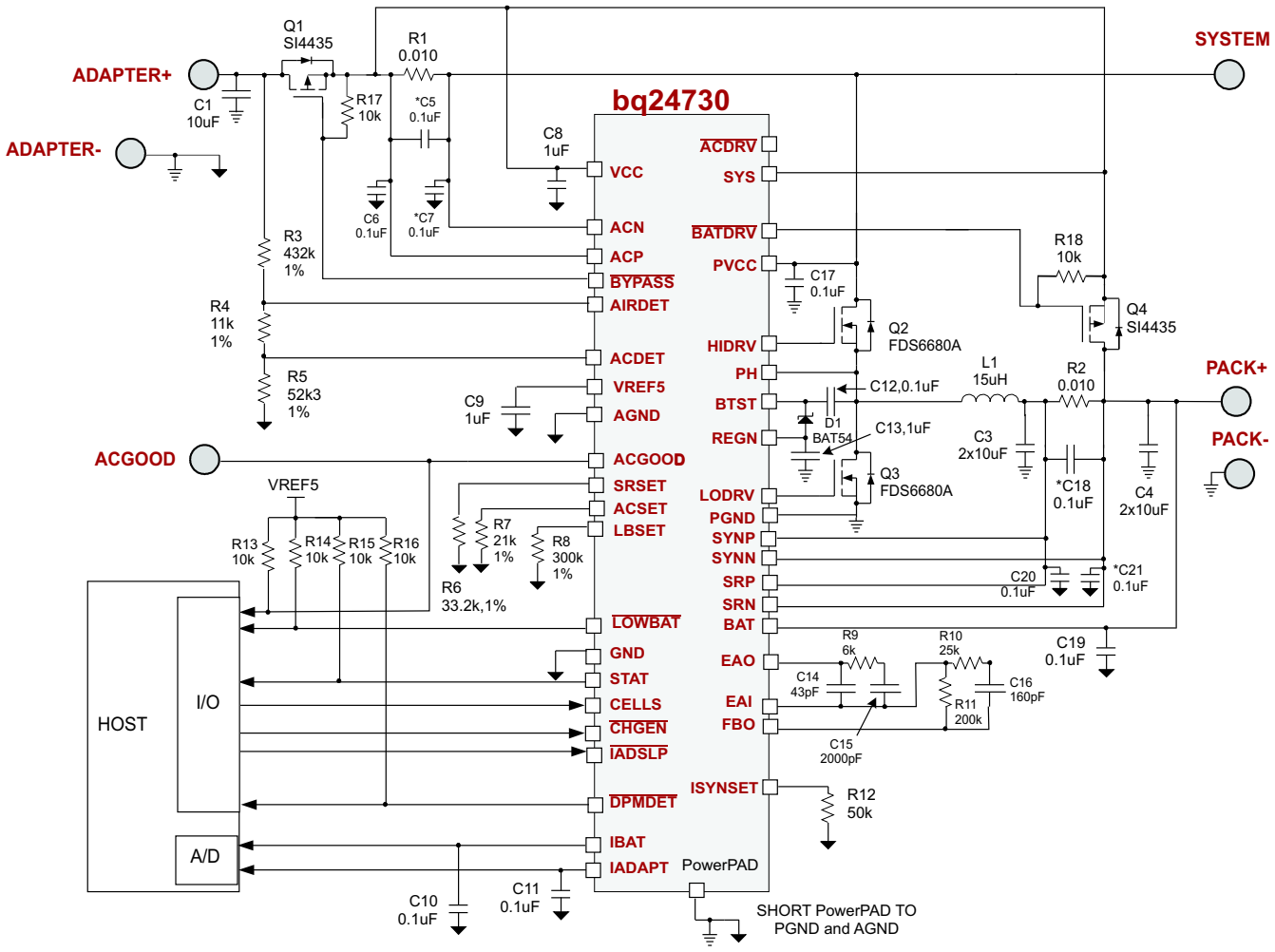


Figure 27. Typical Application Circuit bq24730 With Battery Discharge Current Sensing When Adapter Removed.

ACP and ACN are used to sense and regulate input current when the adapter is present. ACP and ACN are used to sense battery discharge current when the adapter removed

Typical bq24730 Narrow VDC (NVDC) Application (2 sense resistors), [V_I = 20 V, $I_{I(lim)}$ = 4.76 A, $I_{(charge)}$ = 3 A, $V_{(BAT)}$ = 16.8 V 4-cells]

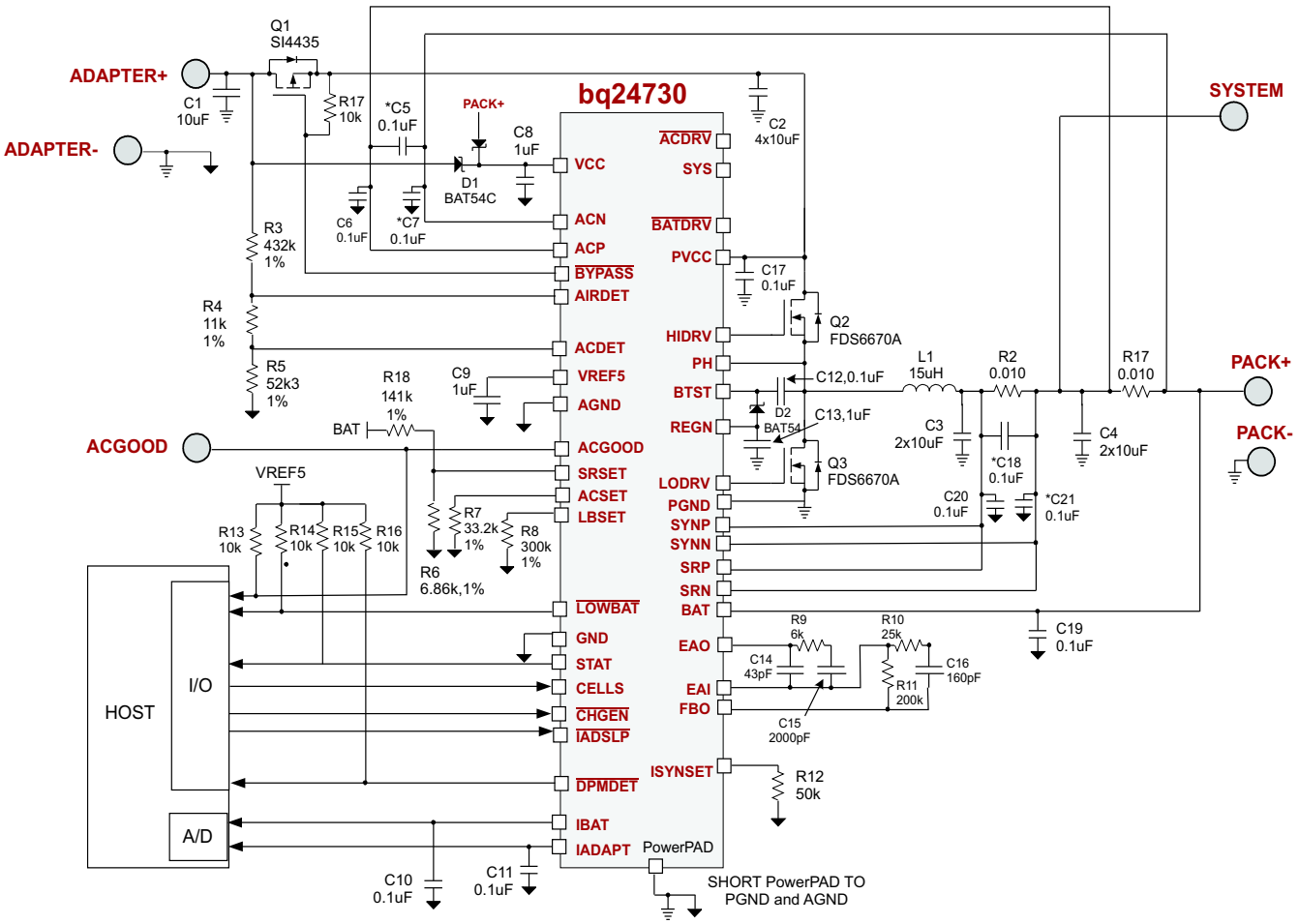


Figure 28. bq24730 Host Control, NVDC (no system power selector) Using 2 Sense Resistors. ACP and ACN Directly Regulating Converter Current while Indirectly Limiting Input Current

Typical bq24730 Narrow VDC (NVDC) Application (3 sense resistors), [V_I = 20 V, $I_{I(lim)}$ = 4.76 A, $I_{(charge)}$ = 3 A, $V_{(BAT)}$ = 16.8 V 4-cells]

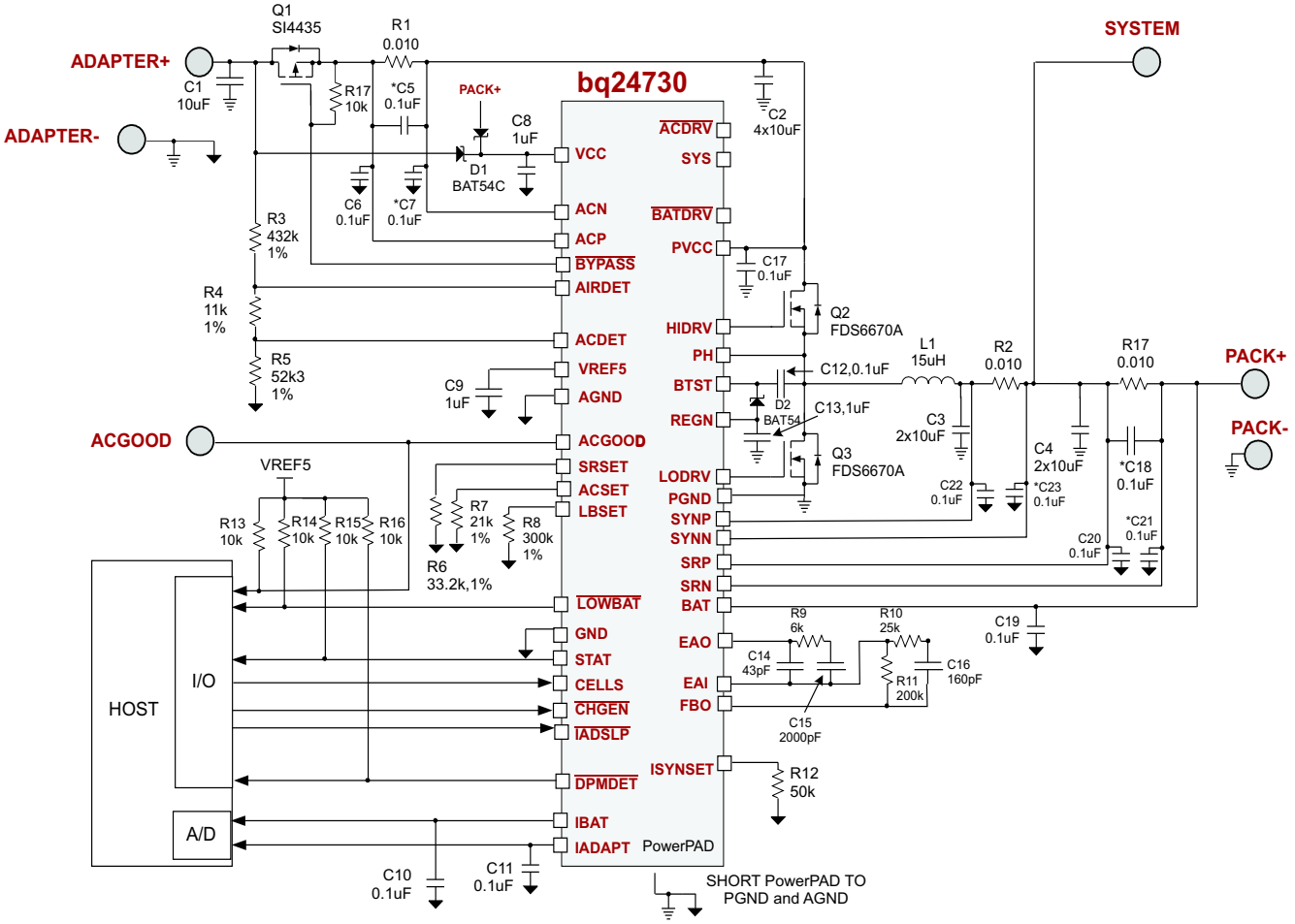


Figure 29. bq24730 Host Control, NVDC (no system power selector) Using 3 Sense Resistors. Input Current is Directly Limited for Highest Accuracy.

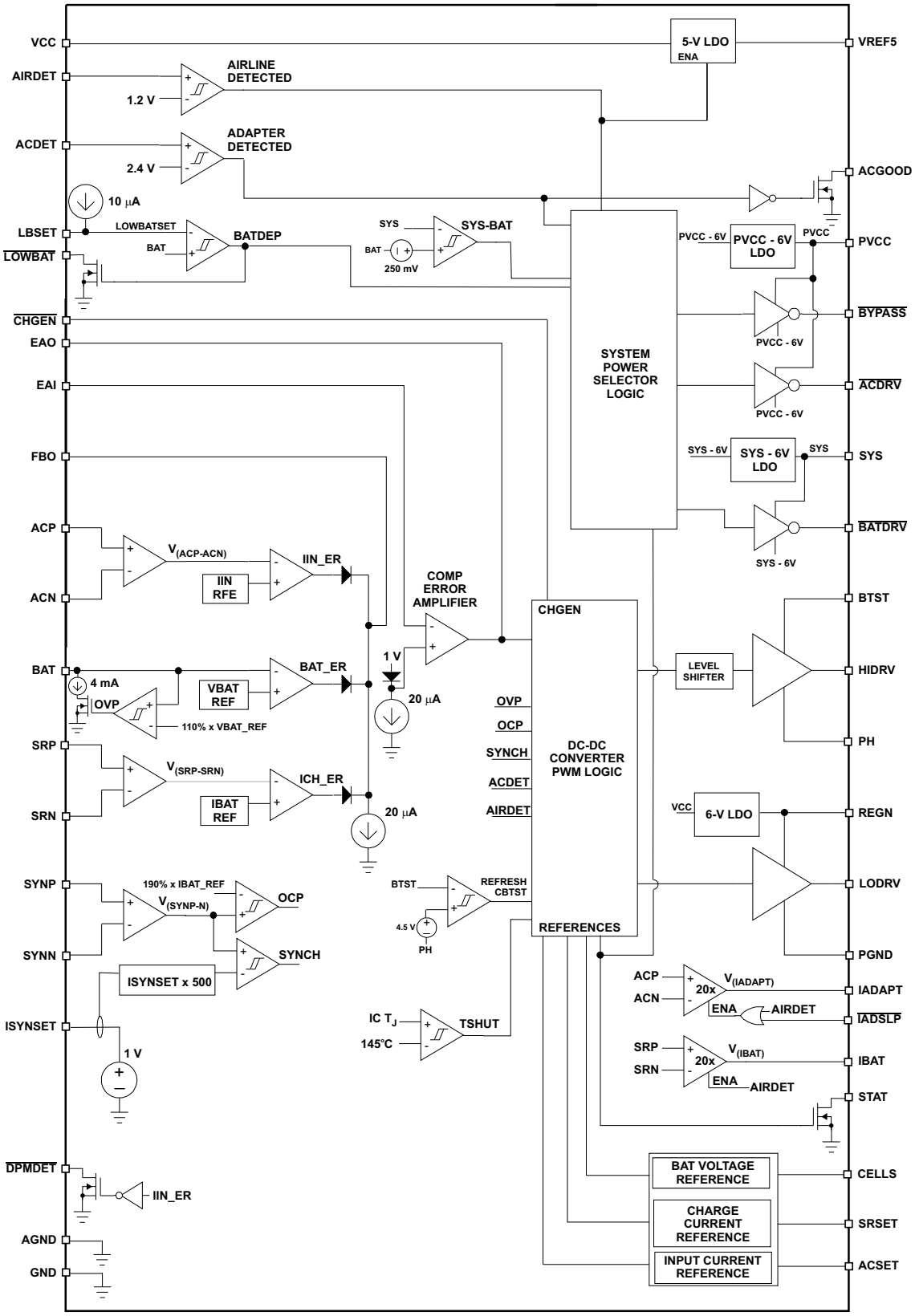


Figure 30. bq24730 Functional Block Diagram

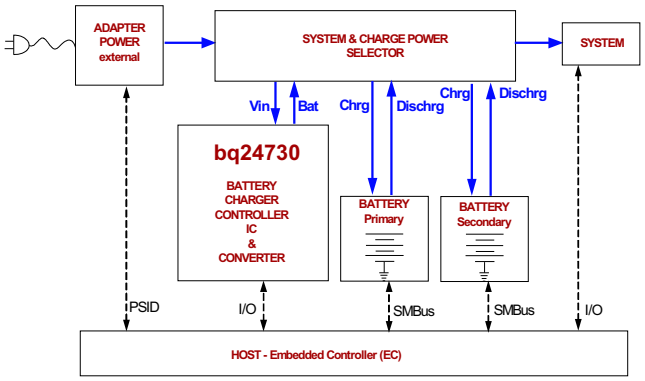


Figure 31. Host Controller

BLOCK DESCRIPTION

Detail Block Diagram

The bq24730 charge controller can be used to charge Li-ion, NiMH, or NiCd batteries. The high efficiency synchronous buck controller uses n-channel power MOSFETs for both the high-side control device and the low-side synchronous device. The controller offers high regulation accuracy of the charge current, battery voltage, and input current limits. The low offset of the current loops allow using sense resistors with low-value, such as 10 mΩ.

An embedded controller host programs the battery voltage, charge current, and input current regulation limit thresholds through a hardware control interface or a fixed on the system, using resistors. The embedded host can control the operation of the charger, and monitor the status of the charger through logic I/O.

The voltage loop regulates the battery voltage to the programmed value to either 12.6V or 16.8V, and prevents the voltage from exceeding that value when the battery is connected. The charge current loop regulates the battery charge current to the programmed value, and prevents the charge current from exceeding that value. Through the use of dynamic power management (DPM), the input current loop regulates the battery charge current to the programmed value, and prevents the input current from exceeding that value. The three regulation loops operate independently, yet only require a single loop compensation network.

The system power selector function selects the appropriate power source for the system load. If the adapter is detected, then the adapter is connected to the system load. When the adapter is removed, the battery is selected to power the system load.

Power Up

When the adapter is not detected, the REGN output voltage is 4.6 V and the VREF5 LDO regulator is off, to lower the power consumption from the battery. The VREF5 LDO is pulled-down to AGND when the adapter is not detected. The REGN LDO regulator begins to regulate at 4.6 V when the input VCC voltage is greater than 6 V. The REGN output voltage is then 6 V when the adapter is detected, and the VCC is greater than 7 V. If adapter is detected, but VCC is less than 7 V, then the REGN is in dropout, and REGN output voltage depends on the VCC voltage and REGN load current. The VREF5 LDO is allowed to turn-on and regulate to 5 V, 5 ms after REGN is 6 V and the adapter is detected. There is a 500-ms delay from the time the adapter is detected, until the ACFET from the system power selector is allowed to turn-on, and until the charger is allowed to turn-on. The battery continues to be connected to the system during this 500-ms delay.

BLOCK DESCRIPTION (continued)

Air Detect, AIRDET

Airline mode allows the bq24730 to power-up, and it commands the system power selector to disconnect the battery from the system load (diode OR), and then connect the input voltage to the system. Charging the battery pack is not allowed until the ACDET is exceeded, as most airlines do not allow charging the battery during a flight. The AIRDET (airline detect) threshold is programmed by an external resistor voltage divider between the adapter and AGND. The internal AIRDET comparator has a 1.2-V rising-edge threshold and a 15-mV falling-edge hysteresis. The airline detect value should typically be programmed to a value greater than the maximum battery voltage, and lower than the minimum allowed airline voltage. The adapter sense connection of the resistor divider should be placed before the BYPASS FET in order to sense the true adapter input voltage whether the BYPASS is on or off.

When the sensed adapter voltage rises above the AIRDET threshold, VREF5 5 volt regulator is enabled. 500 ms after the threshold is detected, the ACGOOD open-drain logic output comes up (HI), the BATDRV is turned off, then the ACDRV is turned on. The VREF5 LDO output can also be used to indicate when the adapter is detected.

Adapter Detect, ACDET

ACDET is used to detect the proper external adapter is connected (instead of power from an airplane) and allow charging. Charging is not allowed when the sensed adapter input voltage is below the ACDET threshold. The AC detect threshold is typically programmed above the air detect threshold. The ACDET (adapter detect) threshold is programmed by an external resistor voltage divider between the adapter and AGND. The internal ACDET comparator has a 2.4-V rising-edge threshold and a 15-mV falling-edge hysteresis. The adapter detect value should typically be programmed to a value greater than the maximum battery voltage, higher than the AIRDET threshold, and lower than the minimum allowed adapter voltage. Setting the ACDET threshold to the same threshold as the AIRDET is possible. The adapter sense connection of the resistor divider should be placed before the BYPASS FET in order to sense the true adapter input voltage whether the BYPASS is on or off.

System Power Selector

The bq24730 can automatically switch between adapter power or battery power to the system load. The battery is connected to the system when there is no adapter detected. The adapter is connected to the system when the adapter is detected. An automatic break-before-make logic prevents shoot-through currents when the selector switches.

When no airline is detected the ACDRV pin is pulled to the PVCC pin to keep the external ACFET p-channel power MOSFET off, disconnecting the adapter from system. The break-before-make logic waits until the ACFET is off and the System to battery voltage comparator indicates the system voltage is within 250 mV of the battery (SYS voltage falling-edge, with a 50-mV hysteresis SYS voltage rising-edge). This prevents shoot-through currents or large discharge currents from going into the battery. The BATDRV pin is then set to the SYS pin voltage minus 6 V by an internal regulator in order to turn on the external BATFET p-channel power MOSFET, connecting the battery pack to the system.

When airline is detected there is a 500-ms delay; then, the BATDRV is set to the SYS pin voltage to turn off the external BATFET p-channel power MOSFET, in order to disconnect the battery. The break-before-make logic waits until the BATFET is off to prevent shoot-through currents. The ACDRV pin is then set to the PVCC pin voltage minus 6 V by an internal regulator in order to turn on the external ACFET p-channel power MOSFET, connecting the adapter to the system.

Asymmetrical gate drives (100 Ω turn-off; 10 kΩ turn-on) for the ACDRV and BATDRV drivers provide fast turn-off and slow turn-on of the ACFET and BATFET to help the break-before-make logic and to allow a soft-start at turn-on of either FET. The soft-start time can be further increased by putting a capacitor from gate to source of the p-channel power MOSFETs.

BLOCK DESCRIPTION (continued)

Low Battery Comparator, LBSET and $\overline{\text{LOWBAT}}$

Whenever the battery is connected to the system (with adapter present, or no adapter present), there is a Low Battery comparator that monitors the battery voltage, and alerts the host and charge controller that the battery has been depleted. The low battery (battery depleted) threshold is programmed by a resistor from the LBSET pin to AGND. A 5 μA current source out of the LBSET pin is multiplied by the resistor from LBSET to AGND, then gained by 2, to set the low battery threshold voltage. The programmed Low Battery voltage is programmed on a *per cell* basis, so that the threshold value changes automatically with the CELLS pin between 3 cells or 4 cells. The programming resistor is calculated by R(LBSET) = (VBATDEP / (2 x 5 μA)), where VBATDEP is the low battery threshold voltage *per cell*. The number of cells is determined by the CELLS pin, logic low (LO) input programs 3-cell, logic high (HI) input programs 4-cell. If the battery voltage falls below the low battery (battery depleted) threshold, then the $\overline{\text{LOWBAT}}$ open drain output pin is pulled low (LO), battery is disconnected from the system (BATDRV off), and the adapter is connected to the system (ACDRV on). There is a 1 second deglitch time to prevent false triggering on both rising and falling edges. A pull-up resistor from $\overline{\text{LOWBAT}}$ to the host controller supply rail is needed to achieve the logic voltage level for the host controller.

Bypass FET

The BYPASS pin is used to control an input FET that is off to prevent reverse discharge from the battery to the adapter, and is on during input current draw to the system or battery, to minimize the power dissipation, as compared to using a Schottky diode. If no adapter is detected, the BYPASS FET is off, by setting the BYPASS pin to the PVCC pin. When the adapter is detected there is a 500-ms delay, then an ACP-to-BAT voltage comparator is used to control the BYPASS pin. The BYPASS driver is set to the PVCC pin voltage when the adapter voltage (ACP pin) is not more than 250 mV (ACP voltage falling-edge) above the battery voltage (BAT pin), in order to turn off the external BYPASS p-channel power MOSFET. There is a 50 mV (ACP voltage rising-edge) hysteresis, to protect from noise and prevent chatter. When adapter is detected and the ACP pin voltage is greater than 300 mV above the BAT pin voltage, the BYPASS pin voltage is set to PVCC pin voltage minus 6 V, in order to turn on the external BYPASS p-channel power MOSFET.

The ACP-to-BAT comparator also prevents the battery voltage from holding-up the ACDET sensed value and falsely detecting ACDET when the adapter is removed, this prevents the system power selector from *getting stuck* in an *adapter always detected* state. When ACP gets near to BAT, the external BYPASS p-channel power MOSFET is turned off. This isolates the ACDET network from the battery, and allows the adapter input node to discharge to PGND.

The BYPASS driver has a symmetrical gate drive of 1 kΩ turn-on and turn-off and does not need to be slowed down.

Enabling Charge

The power-on-reset default is charge disabled. Charge can only be enabled 500 ms after adapter is detected (after ACDET pin voltage rising above 2.4 V), to allow the adapter input voltage to settle. Pull the $\overline{\text{CHGEN}}$ pin low to initiate charge.

The conditions that makes the charger not ready to charge are: ACDET pin voltage not above 2.4 V, 500-ms delay after adapter detected not over, REGN voltage not up, or VREF5 voltage not up. While charging an overcurrent condition, overvoltage condition on BAT, or an overtemperature of the component, causes the charger to be disabled. The STAT pin is logic low (open-drain pulled low) when the charger is on; and STAT pin is logic high (open-drain off) when the charger is disabled by any of the above conditions.

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BLOCK DESCRIPTION (continued)

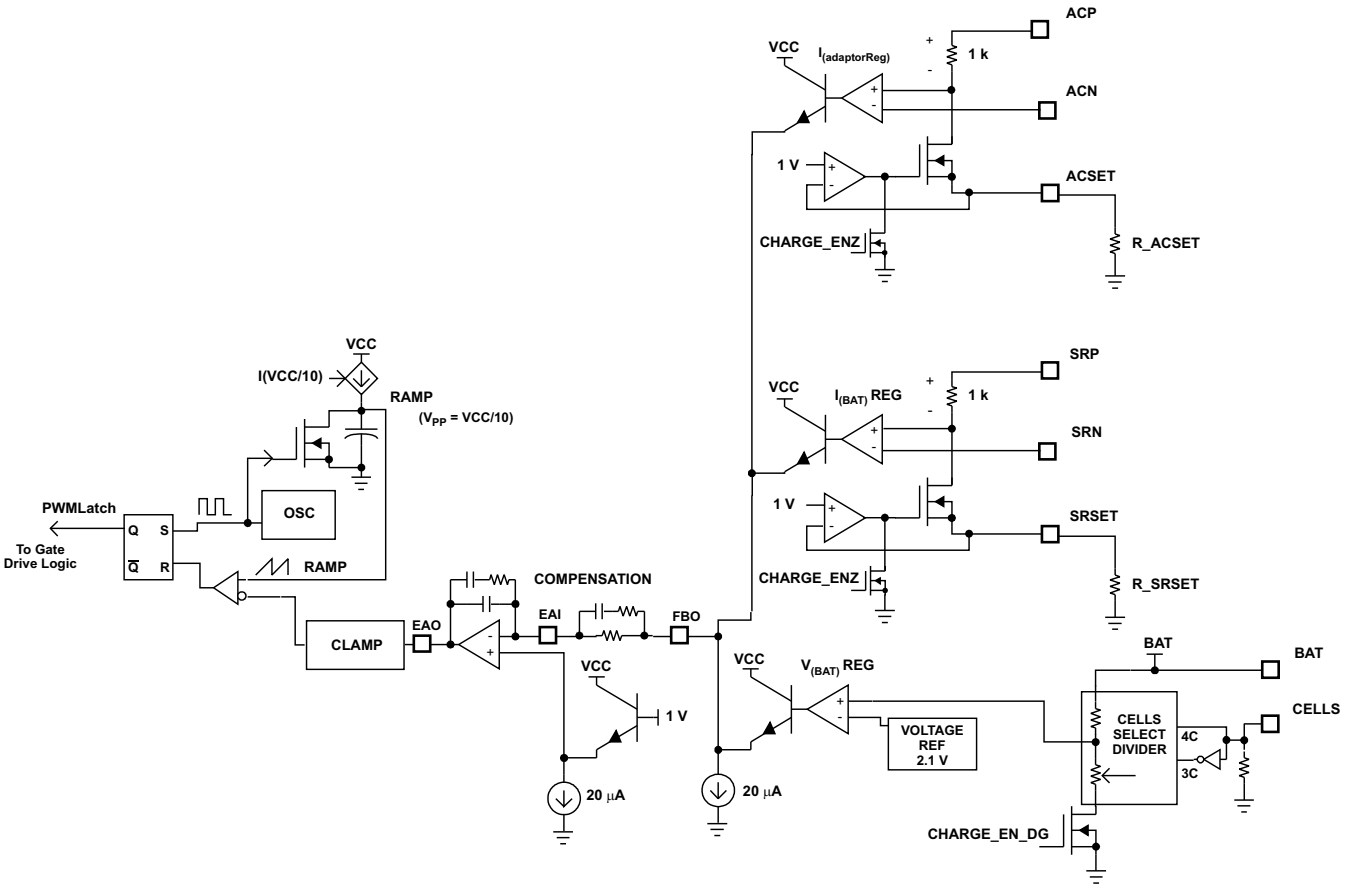


Figure 32. PWM Control Logic

Converter Operation

The synchronous buck PWM converter uses a fixed frequency voltage mode with feed-forward control scheme. A type III compensation network allows using ceramic output capacitors. The compensation input stage is connected between the feedback output (FBO) pin and the error amplifier input (EAI) pin. The feedback compensation stage is connected between the error amplifier input (EAI) pin and error amplifier output (EAO) pin. The compensation components connected to EAI, EAO, and FBO can be calculated using the bq24730 Compensation Calculation application note.

An internal saw-tooth ramp is compared to the EAO pin error control signal to vary the duty-cycle of the converter. The ramp height is one-tenth of the input adapter voltage making it always directly proportional to the input adapter voltage. This cancels out any loop gain variation due to a change in input voltage, and simplifies the loop compensation. The ramp is offset by 300 mV in order to allow zero percent duty-cycle, when the EAO signal is below the ramp. The EAO signal is also allowed to exceed the saw-tooth ramp signal in order to get a 100% duty-cycle PWM request. Internal gate drive logic allows achieving 99.98% duty-cycle while ensuring the N-channel upper device always has enough voltage to stay fully on. If the BTST pin to PH pin voltage falls below 4.5 V for more than 3 cycles, then the high-set n-channel power MOSFET is turned off and the low-side n-channel power MOSFET is turned on to pull the PH node down and recharge the BTST capacitor. Then the high-side driver returns to 100% duty-cycle operation until the voltage is detected to fall low again due to leakage current discharging the BTST capacitor below the 4.5 V, and the reset pulse is reissued.

The fixed frequency oscillator keeps tight control of the switching frequency under all conditions of input voltage, battery voltage, charge current, and temperature, simplifying output filter design and keeping it out of the audible noise region. The switching frequency is fixed at 300 kHz.

BLOCK DESCRIPTION (continued)

The charge current sense resistor should be placed with at least half or more of the total output capacitance placed before the sense resistor contacting both sense resistor and the output inductor; and the other half or remaining capacitance placed after the sense resistor. The output capacitance should be divided and placed onto both sides of the charge current sense resistor. A ratio of 50:50 percent gives the best performance; but the node in which the output inductor and sense resistor connect should have a minimum of 50% of the total capacitance. This capacitance provides sufficient filtering to remove the switching noise and give better sense accuracy. The type III compensation is already providing phase boost near the cross-over frequency, giving sufficient phase margin.

Synchronous versus Nonsynchronous Operation

The charger operates in non-synchronous mode when the sensed charge current is below the ISYNSET programmed value. When above the ISYNSET programmed value, the charger operates in synchronous mode.

During synchronous mode, the low-side n-channel power MOSFET is on, when the high-side n-channel power MOSFET is off. The internal gate drive logic ensures there is break-before-make switching to prevent shoot-through currents. During the dead-time where both FETs are off, the back-diode of the low-side power MOSFET conducts the inductor current. Having the low-side FET turn-on keeps the power dissipation low, and allows safely charging at high currents. During Synchronous mode the inductor current is always flowing and operates in Continuous Conduction Mode (CCM) creating a fixed two-pole system. During non-synchronous operation: after the high-side n-channel power MOSFET turns off, and after the break-before-make dead-time, the low-side n-channel power MOSFET turns on for around 80 ns, then the low-side power MOSFET turns off and stays off until the beginning of the next cycle, where the high-side power MOSFET is turned on again. The 80 ns low-side MOSFET on-time is done to ensure the bootstrap capacitor is always recharged and able to keep the high-side power MOSFET on during the next cycle. This is important for battery chargers, where unlike regular dc-dc converters, there is a battery load that maintains a voltage and can both source and sink current. The 80 ns low-side pulse pulls the PH node (connection between high and low-side MOSFET) down, allowing the bootstrap capacitor to recharge up to the REGN LDO value. After the 80 ns, the low-side MOSFET is kept off to prevent negative inductor current from occurring. The inductor current is blocked by the off low-side MOSFET, and the inductor current becomes discontinuous. This mode is called Discontinuous Conduction Mode (DCM).

During the DCM mode the loop response automatically changes and has a single pole system at which the pole is proportional to the load current, because the converter does not sink current, and only the load provides a current sink. This means at very low currents the loop response is slower, as there is less sinking current available to discharge the output voltage.

At very low currents during non-synchronous operation, there may be a small amount of negative inductor current during the 80 ns *recharge pulse*. The charge should be low enough to be absorbed by the input capacitance.

Whenever the converter goes into zero percent duty-cycle, the high-side MOSFET does not turn-on, and the low-side MOSFET does not turn-on (no 80 ns recharge pulse), so there is no discharge from the battery.

ISYNSET

The ISYNSET pin is used to program the charge current threshold at which the charger changes from non-synchronous operation into synchronous operation. This is important to prevent negative inductor current. Negative inductor current may cause a *boost* effect in which the input voltage increases as power is transferred from the battery to the input capacitors—this can lead to an overvoltage on the PVCC node and potentially cause some damage to the system.

This programmable value allows setting the current threshold for any inductor current ripple, and avoiding negative inductor current. The SYNP and SYNN pins are used to sense across the charge current sense resistor.

To program the threshold, a resistor is connected from the ISYNSET pin to AGND. The minimum synchronous threshold should be set from the inductor current ripple to the full ripple current, where the inductor current ripple is given by.

BLOCK DESCRIPTION (continued)

$$\Delta I_L = \frac{\left(V_I max + V_{(BAT)} min\right)}{L_{OUT}} \times \frac{V_{(BAT)} min}{V_I max} \times \frac{1}{f_{SW}} \quad (1)$$

where:

$$R_{SYNSET} = \frac{(1\ V) \times (500\ \Omega)}{\Delta I_L \times R_{SNS}} \quad (2)$$

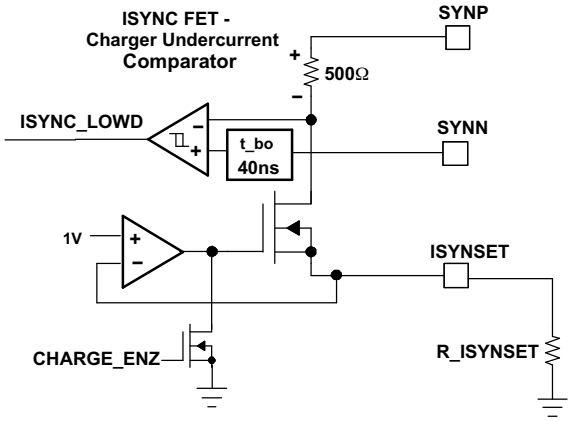
$V_I$max is the maximum adapter voltage, $V_{(BAT)}$min is the minimum battery voltage, f_S is the switching frequency, and L_{OUT} is the minimum output inductor value.

The ISYNSET pin is internally regulated to 1 V. When the $R_{(SYNSET)}$ resistor is connected to AGND, it sets an ISYNSET current equal to 1 V/$R_{(SYNSET)}$. The ISYNSET current internally flows through a 500 Ω creating a voltage at which the voltage across $R_{(SENSE)}$ is compared. The ISYN charge current threshold is the voltage divided by the $R_{(SENSE)}$ sense resistor value. The $R_{(SYNSET)}$ resistor value is calculated by:

$$V_{O(RIPPLE)} = \left(I_{(RIPPLE)}\right) \times \frac{\left(\frac{V_{(BAT)}\,min}{V_I\,max}\right) \times \left(\frac{1}{F_{SW}}\right)}{C_O} + \left(\frac{ESR}{2} \times \frac{I_{(RIPPLE)}}{2} + \right)\frac{ESR}{2} + r_{(SENSE)}\left(\times \frac{I_{(RIPPLE)}}{2}\right)$$

$$+ ESL \times \frac{I_{RIPPLE}}{\left(\frac{V_{(BAT)}\,min}{V_I\,max}\right) \times \left(\frac{1}{F_{SW}}\right)} \quad (3)$$

where ISYN is the charge current threshold at which the converter changes to synchronous operation.



NOTE: Patent Pending

Figure 33. Synchronous to Non-Synchronous threshold, ISYNSET, Block – Charger Under Current (prevents negative inductor current)

Battery Voltage Regulation Loop

The BAT pin is used to sense the battery voltage and should be connected as close to the battery as possible, or directly to the output capacitor. A 0.1-µF ceramic capacitor from BAT to AGND is recommended - added as close to the BAT pin as possible to decouple high frequency noise.

The voltage regulation feedback is through the BAT pin. This input is tied directly to the positive side of the battery pack. The bq24730 monitors the battery-pack voltage between the BAT and AGND pins. The regulation voltage is programmed through the CELLS pin. Logic low (LO) input on CELLS pin programs 12.4 V regulation voltage (3-cells). Logic high (HI) input on CELLS pin programs 16.8V regulation voltage (4-cells).

BLOCK DESCRIPTION (continued)

Setting Charge Voltage (CELLS pin) for 3-cell or 4-cell Li-Ion Battery Packs

The charge voltage can be programmed for either a 3-cell or 4-cell Li-Ion battery through the CELLS pin. The 3-cells Li+ battery pack regulation voltage is 12.6 V; and the 4-cells Li+ battery pack regulation voltage is 16.8 V. A low (LO) logic input on the CELLS pin programs the charger to 12.6 V. A high (HI) logic input on the CELLS pin programs the charger to 16.8 V. The default power-up-reset voltage value is 0 V, charger disabled.

Setting Charge Voltage (CELLS pin) for up to 12-cell NiMH Battery Packs

NiMH batteries typically do not use a voltage regulation mode during charging, and only use a constant charge current mode. In this case, the voltage regulation is not used for charging, but instead is used to limit the output voltage for a case where the pattery pack is disconnected and the system can not withstand the input voltage. The regulation voltage should be set at a voltage higher than the maximum battery pack voltage. NiMH cells typically have 1.35 V maximum. The CELLS Low (LO) setting limits voltage to 12.6 V, so this allows up to 9 NiMH cells to be charged. The CELLS High(HI) setting limits voltage to 16.8 V, so this allows up to 12 NiMH cells to be charged. The default power-up-reset voltage value is 0 V, charger disabled.

Battery Charge Current Regulation Loop

The battery charge current loop can use a 10-mΩ sense resistor; however, resistors of other values can also be used. The larger the sense resistance, the larger the sensed voltage, and the higher the regulation accuracy, but at the expense of higher conduction losses. The SRP and SRN pins are used to sense across the sense resistor.

The battery charge current, $I_{O(CHARGE)}$, is established by setting the external sense resistor, $R_{(SNS\_CHG)}$, and the SRSET programming resistor, $R_{(SRSET)}$. $R_{(SRSET)}$ programs $V_{(IREG\_CHG)}$, the differential voltage that is regulated across SRP-SRN to any value up to 200 mV. $R_{(SNS\_CHG)}$ should be chosen based on the regulation threshold $V_{(IREG\_CHG)}$, across this resistor.

$$R_{(SNS\_CHG)} = V_{(IREG\_CHG)} / I_{O(CHARGE)}$$

Setting Charge Current (SRSET pin)

The charge current can be programmed through a resistor from the SRSET pin to AGND. The charge current can be programmed to any value up to a maximum possible current of 20 A using a 10-mΩ sense resistor. The SRSET is internally kept at 1 V. The resistor from SRSET to AGND sets a current out of the SRSET pin. This current is gained up by an internal 1000-Ω resistor, to set the voltage across the SRP-SRN pins. The SRP and SRN pins are connected across the charge current sense resistor. The charge current is the programmed voltage across the (SRP-SRN) sense resistor, divided by the sense resistor value. The default power-up-reset current value is 0 A, charger disabled. Any sense resistor value could be used to set the charge current. The controller can use a 10 mΩ sense resistor. The accuracy increases as the programmed (SRP-SRN) differential voltage increases, so increasing the sense resistor value will help increase accuracy. The SRSET programming resistor can be calculated by the following equation.

$$R_{SRSET} = \frac{(1\ V)\ x\ (1\ k\Omega)}{I_{CH}\ x\ R_{SENSE}} \quad (4)$$

Input Current Regulation Loop (DPM)

The ACP and ACN pins are used to sense across the sense resistor. The input current loop can use a 10-mΩ sense resistor; however, resistors of other values can also be used. The larger the sense resistance, the larger the sensed voltage, and the higher the regulation accuracy, but at the expense of higher conduction losses.

The input current, $I_{I(DPM)}$, is established by setting the external sense resistor, $R_{(SNS\_DPM)}$, and the ACSET programming resistor, $R_{(ACSET)}$. $R_{(ACSET)}$ programs $V_{(IREG\_DPM)}$, the differential voltage that is regulated across ACP-ACN to any value up to 200 mV. $R_{(SNS\_DPMG)}$ should be chosen based on the regulation threshold $V_{(IREG\_DPM)}$, across this resistor.

$$R_{(SNS\_DPM)} = V_{(IREG\_DPM)} / I_{O(CHARGE)}$$

BLOCK DESCRIPTION (continued)

Setting Input (DPM) Current (ACSET pin)

The input (DPM) current can be programmed through a resistor from the ACSET pin to AGND. The input current can be programmed to any value up to a maximum possible current of 20 A using a 10-mΩ sense resistor. The ACSET is internally kept at 1 V. The resistor from ACSET to AGND sets a current out of the ACSET pin. This current is gained up by an internal 1000-Ω resistor, to set the voltage across the ACP-ACN pins. The ACP and ACN pins are connected across the input current sense resistor. The input current is the programmed voltage across the (ACP-ACN) sense resistor, divided by the sense resistor value. The default power-up-reset current value is 0 A, charger disabled. Any sense resistor value could be used to set the input current. The controller can use a 10 mΩ sense resistor. The accuracy increases as the programmed (ACP-ACN) differential voltage increases, so increasing the sense resistor value will help increase accuracy. The ACSET programming resistor can be calculated by the following equation.

$$R_{ACSET} = \frac{(1\ V)\ x\ (1\ k\Omega)}{I_{DPM}\ x\ R_{SENSE}} \quad (5)$$

Dynamic Power Management Input Current Limit Detected, $\overline{\text{DPMDET}}$

The $\overline{\text{DPMDET}}$ open drain output pin indicates that the dynamic power management (DPM) input current loop is active. Logic low (LO) output indicates input current is being limited by reducing the charge current. A pull-up resistor from the $\overline{\text{DPMDET}}$ pin to the host controller supply rail is needed. The host controller can use the $\overline{\text{DPMDET}}$ signal to throttle back on the system power load, or to adjust the charge safety timer from the host since charge current would be lowered.

High Accuracy Current Sense Amplifiers (CSA), IADAPT for Input Current, and IBAT for Charge Current, $\overline{\text{IADSLP}}$

Industry standard, high accuracy current sense amplifiers (CSA) are used to monitor the input current and the charge current through the analog voltage output of the IADAPT pin and IBAT pin, respectively. The current sense amplifier from the input current (voltage across ACP-ACN pins) and the current sense amplifier of the charge current (voltage across SRP-SRN pins), amplify the input sensed voltage by 20x, through the IADAPT and IBAT pins.

The IBAT current sense amplifier is always disabled when adapter voltage is below the AIRDET threshold; and the IBAT current sense amplifier is always enabled when adapter voltage is above the AIRDET threshold.

When $\overline{\text{IADSLP}}$ input pin is low (LO): the IADAPT current sense amplifier is disabled when adapter voltage is below the AIRDET threshold; and the IADAPT current sense amplifier is enabled when adapter voltage is above the AIRDET threshold. However, when $\overline{\text{IADSLP}}$ input pin is high (HI): the IADAPT current sense amplifier is enabled both when adapter voltage is below an when above the AIRDET threshold (as long as VCC is above 7 V, such as is the case when a battery is connected and supplying power to VCC). This ability of keeping the IADAPT active when no adapter is available, allows sensing the battery discharge current when the ACP-ACN pins are in the discharge path from the battery to the system load. (See Figure 33, battery discharge sensing typical application circuit).

The IADAPT and IBAT outputs are voltage sources 20 times their input differential voltage. If the user wants to lower the voltage, use a sense resistor from IADAPT to AGND, or from IBAT to AGND, and still achieve high accuracy overtemperature as the external resistors' thermal coefficients can be matched reasonably well.

A 0.1-µF capacitor connected on the output is recommended for decoupling high-frequency noise. An additional RC filter, after the 0.1-µF capacitor, is optional if additional filtering is desired. Note that adding filtering also adds additional response delay.

Automatic Internal Soft-Start Charger Current

The charger automatically soft-starts the charger regulation current every time the charger is enabled, in order to ensure there is no overshoot or stress on the output capacitors or the power converter. The soft-start consists of stepping-up the charge regulation current into eight evenly divided steps up to the programmed charge current. Duration of each step is around 1 ms, for a typical rise time of 8 ms. No external components are needed for this function.

BLOCK DESCRIPTION (continued)

The bq24730 current regulation loop reference steps-up whenever charge is enabled, and when returning from fault/suspend mode into charge where the current regulator is turned on. The loop should take control within a few hundred micro-seconds with very little overshoot due to the LC output filter and the high compensation loop bandwidth with 300 kHz operating frequency; therefore, the reference could ramp up from precharge to fast-charge within 50 µs to 500 ms. Going into fault/suspend mode, short circuit ($V_{(BAT)} < V_{(UVT)}$), Sleepmode ($V_{(ACP)} < V_{(BAT)}$), or UVLO (VCC < 3.7 V) initiates an immediate shut-off of the high-side PWM FET by setting its gate to $V_{(PH)}$. The output inductor and battery load determines the ramp-down rate as it *freewheels* through the Schottky diode.

Charger Overcurrent Protection

The charger has a secondary overcurrent protection function that monitors the charge current, and prevents it from exceeding 190% of the programmed charge current. The high-side gate drive turns off and automatically resume when the current falls below the overcurrent threshold

Current Regulation Down to Zero Battery Voltage

The bq24730 charger regulates charge current down to zero volts on the battery BAT voltage. When battery BAT voltage initially falls below a 2 V threshold, the converter immediately turns off both high-side and low-side FETs and reduces the PWM duty-cycle to zero in order to stop current flow due to a possible short, then it resumes increasing the duty-cycle and regulating the current. This fast response mechanism ensures there is no overcurrent surge due to an external short circuit that could cause damage to the battery, charger, or system.

The embedded controller host should reduce the charge current regulation threshold for pre-charging a deeply discharged battery. This can be done by switching in parallel resistors in and out from the SRSET pin to ground. A deeply discharged battery can be detected by using the programmable LBSET (LOWBAT) comparator of the IC.

Battery Overvoltage Protection

As an extra level of protection, the bq24730 has an overvoltage protection function, in which the converter is turned off when the BAT voltage is detected to be above 110% of the programmed battery regulation threshold. During this overvoltage condition, a 4-mA current sink from the BAT pin to AGND pin turns on to reduce the response time to bring down the battery voltage during otherwise no-load conditions such as battery removal or battery disconnect for pulse-charge schemes. This reduces the battery node voltage overshoot and reduce the battery voltage regulation response time, with low or no load conditions.

The converter stays off and the 4-mA current sink remains on until the battery voltage falls below 102% of the programmed battery regulation threshold. Afterward, the converter reenables and continues regulating the BAT voltage as normal.

Thermal Shutdown Protection

The QFN package has low thermal impedance which provides good thermal conduction from the silicon to the ambient, to keep junctions temperatures low. As added level of protection, the charger converter turns off and self-protects whenever the junction temperature exceeds the TSHUT threshold of 145°C. The charger stays off until the junction temperature falls below 130°C.

Charge Termination for Li-Ion or Li-Polymer

The primary termination method for Li-Ion and Li-Polymer is minimum current. Secondary temperature termination methods is also provided for additional safety. The host controls the charge initiation and the termination. A battery pack gas gauge assists the hosts on setting the voltages and determining when to terminate based on the battery pack state of charge.

DESIGN CONSIDERATION EXAMPLE AND APPLICATION INFORMATION

System Requirements (See Figure 26)

For a system using a 20 V, ±5%, 95-W adapter, use a 12.6-V (3-cell) or 16.8-V (4-cell) battery, with a charge current regulation threshold of 3 A. The battery pack voltage varies from a deeply discharged voltage of 3-V per cell, and up to a regulation voltage of 4.2-V per cell— giving ranges of 9-V to 12.6-V for 3-cell batteries, and 12-V to 16.8-V for 4-cell batteries.

Select the Sense Resistors

For this design example, a 10-mΩ sense resistor is selected for both the input current and output charge current sense resistors.

The charger operates with low resistance. If the thermal dissipation is tolerable, a larger sense resistor (such as 20 mΩ) is used to provide greater accuracy in the regulation and current sense amplifier.

The power dissipation for each sense resistor is:

$$P_{(RSENSE\_INPUT)} = R_{(SENSE\_DPM)} \times I_{(INPUT\_REG)}{}^{2} = 10\ m\Omega \times \left(\frac{95\ W}{19\ V}\right)^{2} = 250\ mW \quad (6)$$

where the maximum input current is the input power limit divided by the input voltage.

$$P_{(RSENSE\_CHRG)} = R_{(SENSE\_CHRG)} \times I_{(INPUT\_REG)}{}^{2} = 10\ m\Omega \times (3A)^{2} = 90\ mW \quad (7)$$

A 0.5 W, 2010 rating provides sufficient margin.

Select Switching Frequency:

Switching frequency = 300 kHz, fixed.

Selecting the Output Inductor

Inductor is designed for current ripple 40% of the 3-A regulation threshold ($I_{(RIPPLE)}$ = 1.2 A).

$$L_{out} = \frac{\left(V_I\,max - V_{(BAT)}\,min\right) \times \left(\frac{V_{(BAT)}{}^{min}}{V_{I}{}^{max}}\right) \times \left(\frac{1}{f_{SW}}\right)}{40\% \times I_{(CHRG\_REG)}} \quad (8)$$

Where the $V_I$max is the maximum input voltage, $V_{(BAT)}$min is the minimum battery voltage, and f_{SW} is the switching frequency.

$$L_{out} = \frac{(21\ V - 9\ V) \times \left(\frac{9\ V}{21\ V}\right) \times \left(\frac{1}{300\ kHz}\right)}{40\% \times 3A} \quad (9)$$

L_{OUT} = 14.3 µH ≈ 15 µH, a standard 15-µH part is selected.

Selecting the Output Capacitor

The rule for selecting ceramic capacitors as the bulk output capacitor is to select 10 µF per 1 A of charge current. In this case, a 3-A charge regulation current requires 30-µF minimum output capacitance. In this example, 40-µF is used. Four 10-µF, X5R 25-V ceramic capacitors are recommended instead of 22 µF, because of a better trade-off with the voltage rating, size, capacitance variation, and cost.

The output capacitors is divided evenly. Place the charge current sense resistor between the capacitors. This provides filtering and a higher phase margin for accurate current sensing and regulation.

With this output capacitance, the steady state output ripple voltage is:

DESIGN CONSIDERATION EXAMPLE AND APPLICATION INFORMATION (continued)

$$V_{O(RIPPLE)} = \left(I_{(RIPPLE)}\right) \times \frac{\left(\frac{V_{(BAT)}{}^{min}}{V_I{}^{max}}\right) \times \left(\frac{1}{F_{SW}}\right)}{C_O} + \left(\frac{ESR}{2} \times \frac{I_{(RIPPLE)}}{2} + \right)\frac{ESR}{2} + r_{(SENSE)}\left(\times \frac{I_{(RIPPLE)}}{2}\right)$$

$$+ ESL \times \frac{I_{RIPPLE}}{\left(\frac{V_{(BAT)}{}^{min}}{V_I{}^{max}}\right) \times \left(\frac{1}{F_{SW}}\right)} \quad (10)$$

where ESR is the equivalent series resistance of the capacitors (10 mΩ each giving 5 mΩ for two capacitors before the sense resistor and 5 mΩ for two capacitors after the sense resistor), and ESL is the equivalent series inductance of the capacitors (0.5 nH).

$$V_{O(RIPPLE)} = \frac{1.2\ A \times \left(\frac{9V}{21\ V}\right) \times \left(\frac{1}{300\ kHz}\right)}{40\ \mu F} + (5\ m\Omega \times 0.6\ A + 15\ m\Omega \times 0.6\ A) + \left[0.5\ nH \times \frac{1.2\ A}{\left(\frac{9\ V}{21\ V}\right) \times \left(\frac{1}{300\ kHz}\right)}\right] \quad (11)$$

$V_{(OUT\_RIPPLE)}$ = 57 mV + 14 mV + 0.56 mV = 72 mV ripple voltage (which equals 0.6% of 12.6 V) worst case peak-to-peak steady state ripple when the battery is removed and the charger is on.

Selecting the Input Capacitor

The input capacitance is at a minimum the same as the output capacitance. Lower capacitance is used directly at the converter input when the input is tied directly to the system load while charging. The capacitors are placed as close as possible to the high-side FET drain (PVCC) and low-side FET source (PGND). A rule for selecting ceramic capacitors as the bulk output capacitor is to select 10 µF per 1 A of charge current. In this case, a 3-A charge regulation current requires 30-µF minimum output capacitance. In this example, 40-µF is used. Four 10-µF, X5R 25-V ceramic capacitors are recommended instead of 22 µF, because of a better trade-off with the voltage rating, size, capacitance variation, and cost. The input ripple voltage is usually larger because the input current ripple through the capacitor is the full charge current.

$$V_{I(RIPPLE)} = \frac{I_{(CHRG)} \times \left(\frac{V_{(BAT)}{}^{min}}{V_I{}^{max}}\right) \times \left(\frac{1}{f_{SW}}\right)}{C_I} + \left(\frac{ESR}{4} \times I_{(CHRG)}\right) + ESL \times \frac{I_{(CHRG)}}{\left(\frac{V_{(BAT)}{}^{min}}{V_I{}^{max}}\right) \times \left(\frac{1}{f_{SW}}\right)} \quad (12)$$

where $I_{(CHRG)}$ is the charge regulation current.

$$V_{I(RIPPLE)} = \frac{3\ A \times \left(\frac{9\ V}{21\ V}\right) \times \left(\frac{1}{300\ kHz}\right)}{40\ \mu F} + \left(\frac{10\ m\Omega}{4} \times 3\ A\right) + 0.5\ nH \times \frac{3\ A}{\left(\frac{9\ V}{21\ V}\right) \times \left(\frac{1}{300\ kHz}\right)} \quad (13)$$

$V_{I(RIPPLE)}$ = 143 mV + 10 mV + 1.4 mV = 154 mV which is 0.77% of the nominal 20-V input voltage.

Note that a single 10-µF capacitor is used from PVCC (close to the drain of the high-side FET) to PGND, when the system load is connected to PVCC, because the capacitors on the system rail provide the hold-up capacitance needed.

DESIGN CONSIDERATION EXAMPLE AND APPLICATION INFORMATION (continued)

Selecting the High-Side Power MOSFET, Q2

The high-side power MOSFET should be an NMOS power MOSFET with a standard voltage rating of 30 V to support the 20-V input voltage. The current carrying capability should be at least 2x the maximum charge current. Both the $r_{DS(on)}$ and the gate charge contribute to the power dissipation, while the worst case condition occurs at max duty cycle (minimum input voltage and maximum battery voltage). The gate drive losses are the only component that directly dissipate heat in the charger IC.

The FDS6680A was selected. The FDS6680A is a NMOS, 30-V, 12-mΩ device in an SO-8 package.

The conduction losses equal:

$$P_{(CON)} = I_{(CHRG)}{}^{2} \times \left[\sqrt{\frac{V_{(BAT)}\,max}{V_I\,min}}\right] \times \left(r_{DS(on)}\right) \tag{14}$$

where the charger's 6-V gate drive voltage helps reduce the $r_{DS(on)}$ for lower conduction losses.

The first order approximation switching losses equal:

$$P_{(SW)} = I_{(CHRG)} \times V_I\,min \times \left[\frac{\left(Q_{(GS)} + Q_{(GD)}\right)}{i_{(G)}}\right] \times f_{SW} \tag{15}$$

and the gate drive losses are:

$P_{(GD)} = Q_{(GTOT)} \times V_I mim \times f_{SW}$.

Where $G_{(GS)}$ is the gate charge from threshold current conducts until full charge current conducts; $Q_{(GD)}$ is the miller charge where the drain voltage drops, and the $Q_{(GTOT)}$ is the total gate charge form off to fully-enhanced on. The full input voltage is used for gate drive calculation because the internal gate drive regulator dissipates the drop from input voltage to the 6-V output voltage which must be added to charging the gates to 6-V every cycle.

$$P_{(CON)} = (3A)^2 \times \left(\sqrt{\frac{16.8\ V}{19\ V}}\right) \times (12\ m\Omega) = 102\ mW$$

$$P_{(SW)} = 3\ A \times 19\ V \times \left(\frac{(5\ nC + 7\ nC)}{1\ A}\right) \times 300\ kHz = 206\ mW$$

$$P_{(GD)} = 18\ nC \times 19\ V \times 300\ kHz = 103\ mW \tag{16}$$

Selecting the Low-Side Power MOSFET, Q3

The low-side power MOSFET should be an NMOS power MOSFET with a standard voltage rating of 30 V to support the 20-V input voltage. The current carrying capability should be at least 2x the maximum charge current. By nature of the synchronous rectifier operation, the drain-to-source voltage is always low at full charge current when the low-side FET turns on—this makes switching losses insignificant, except for the reverse recovery and dead-time contributors that arise from letting the body-diode conduct. The conduction losses and gate drive losses are the dominant power dissipation; while, the worst case condition occurs at minimum duty cycle (maximum input voltage and minimum battery voltage). The gate drive losses are the only component that directly dissipate heat in the charger IC. Note that the reverse recovery losses are included in this calculation, but the dissipation occurs in the high-side power MOSFET.

The FDS6680A was selected. The FDS6680A is an NMOS, 30-V, 12-mΩ device in an SO-8 package.

The conduction losses equal:

DESIGN CONSIDERATION EXAMPLE AND APPLICATION INFORMATION (continued)

$$P_{(CON)} = I_{(CHRG)}{}^2 \times \left(\sqrt{\frac{V_{(BAT)}\,max}{V_I\,min}} \right) \times \left(r_{DS(on)} \right) \quad (17)$$

where the charger's 6-V gate drive voltage helps reduce the $r_{DS(on)}$ for lower conduction losses.

The first order approximation switching losses are dominated by reverse recovery losses and dead-time losses given by:

$$P_{(SW)} = V_I max \times Q_{(RR)} \times f_{SW} + I_{(CGRG)} \times V_{(F)} \times 2 \times t_{(dead\text{-}time)} \times f_{SW}$$

and the gate drive losses are :

$$P_{(GD)} = Q_{(GTOT)} \times V_I mim \times f_{SW}.$$

Where $t_{(dead\text{-}time)}$ is the dead-time where both FETs are off on either edge, $Q_{(RR)}$ is the reverse recovery charge, $Q_{(GTOT)}$ is the total gate charge form off to fully-enhanced on. The full input voltage is used for gate drive calculation because the internal gate drive regulator dissipates the drop from input voltage to the 6-V output voltage which must be added to charging the gates to 6 V every cycle.

$$P_{(CON)} = (3A)^2 \times \left(\sqrt{1 - \frac{9\ V}{21\ V}} \right) \times (12\ m\Omega) = 81\ mW$$

$$P_{(SW)} = 21\ V \times 21\ nC \times 300\ kHz + 3\ A \times 0.8\ V \times 2 \times 30\ ns \times 300\ kHz = 132\ mW + 43.2\ mW = 175\ mW$$

$$P_{(GD)} = 18\ nC \times 21\ V \times 300\ kHz = 113\ mW \quad (18)$$

Power MOSFET Thermal Limit Verification

The thermal limit verification should allow for a 40°C temperature rise from 85°C ambient to 124°C silicon junction temperatures. For SO-8, the $R\theta_{JA}$ is 50°C/W.

The low-side power FET expected temperature rise is:

$$\Delta T_{(LOW\_SIDE)} = R\theta_{JA} \times P_{(LOSS\_LOW\text{-}SIDE)} = \frac{50^\circ C}{W} \times (81\ mW + 43.2\ mW) = 6.2\ ^\circ C \quad (19)$$

The high-side power FET expected temperature rise is:

$$\Delta T_{(HIGH-SIDE)} = R_\theta JA \times P_{(LOSS\_HIGH\_SIDE)} = \frac{50^o C}{W} \times (102\ mW + 206\ mW + 132\ mW) = 22^o C \quad (20)$$

Optional Schottky Diode across Low-Side FET

An optional Schottky diode can be used across the low-side power MOSFET (with cathode to drain and anode to source) to help reduce both the $V_{(F)}$ losses and reverse recovery losses. The Schottky diode is selected on the basis of the $V_{(F)}$ at $I_{(CHRG)}$, but a power rating for the full current is not required since the Schottky primarily conducts during the dead-times, which is a fraction of the total switching period.

Power loss for the Schottky are:

$$P_{(SW)} = I_{(CHRG)} \times V_F \times 2 \times t_{(dead\text{-}time)} \times f_{SW} = 3\ A \times 0.5\ V \times 2 \times 30\ ns \times 300\ kHz = 27\ mW$$

Selecting the System Power Selector Power MOSFETs, Q1, Q4, Q5

The system power selector power MOSFETs (Q1, Q4, Q5) should be PMOS power MOSFETs with a standard voltage rating of 30 V to support the 20-V input voltage, and must have a low $r_{DS(on)}$ to minimize conduction losses. The continuous current carrying capability should be at least 2x the maximum charge current. Both the $r_{DS(on)}$ and the gate charge contribute to the power dissipation, while the worst case condition occurs at max duty cycle (minimum input voltage and maximum battery voltage). The gate drive losses are the only component that directly dissipate heat in the charger IC.

The SI4435 was selected for Q1, Q4, and Q5. The SI4435 is a PMOS, 30-V, 35-mΩ device in an SO-8 package.

DESIGN CONSIDERATION EXAMPLE AND APPLICATION INFORMATION (continued)

The conduction losses equal:

$P_{(CON)} = I_{(RMS)}^2 \times r_{DS(on)}$,

$I_{(RMS\_Q1)} = I_{(RMS\_Q2)} = I_{(RMS\_Q5)} = I_{(SYS)}max$

where $I_{(RMS)}$ is the RMS current expected for each MOSFET, and $I_{(SYS)}max$ is the maximum continuous system current.

Note that for Q1, the charge current is not used because the charge current drops to zero as the system current ($I_{(SYS)}max$) equals or exceeds the programmed input current DAC threshold (IDPM). This is assuming the typical case where $I_{(SYS)}max > I_{(DPM)}$.

The system power selector's -6-V gate drive voltage helps reduce the $r_{DS(on)}$ for lower conduction losses.

Calculate the Bootstrap Capacitor

The minimum bootstrap capacitor is calculated by the high-side turn-on charge requirements per cycle and the gate drive voltage required. The total gate charge for the FDS6680A high-side power FET is $Q_{(GTOT)}$ = 18 nC, and the maximum gate drive voltage drop allowed is $V_{(DROP)}$ = 0.5 V. The switching frequency of 300 kHz gives a cycle period of 3.33 μs.

$$C_{(BTST)}min = \frac{Q_{(GTOT)}}{V_{(DROP)}max} = \frac{18\ nC}{0.5\ V} = 36\ nF \quad (21)$$

Select $C_{(BTST)}$ = C12 = 100 nF = 0.1 μF. Connect C12 between the PH and the BTST pins. Also connect a bootstrap Schottky diode, D2 , from the REGN pin to the BTST pin. The current rating for the bootstrap diode, D2, is determined by:

$$I_{(DBTST\_RATING)}min = \frac{Q_{(GTOT)}}{T_S} = \frac{18\ nC}{3.33\ \mu s} = 5.4\ mA \quad (22)$$

Use a 100-mA rated Schottky diode.

An optional 4.7-Ω bootstrap resistor is placed between the BTST pin and the node where C12 and D2 are connected, in order to minimize ringing by lowering slew rate on the PH node voltage. For lower gate charge FETs, a larger resistor value can be used up to 10 Ω or 15 Ω. Using larger resistor values increase the switching losses, and lower the efficiency.

Calculate the ACDET and AIRDET Programming Resistors

When airline is detected (AIRDET), the input source is connected to the system load but, the charge is disabled until the adapter is detected (ACDET). For a 12-V airline power source, the AIRDET is set to detect airline mode at 11.5 V. The adapter voltage detect threshold is set to a value less than the minimum adapter voltage, and higher than the maximum battery pack voltage.

NOTE: do not set the ACDET value less than the maximum battery pack voltage, otherwise the adapter removal will never be detected when the battery is connected. The battery pack can potentially be drained when no adapter is present. For this design example, $V_I$min = 19.5 V, $V_{(BAT)}$max = 16.8 V; therefore, select an adapter detect (ACDET) voltage of $V_{(ADAPT\_DET)}$ = 19 V.

The ACDET pin threshold voltage is 2.4 V, and the AIRDET pin threshold voltage is 1.2 V. The total resistance of the resistor divider chain is set to 500 kΩ to minimize leakage current. The resistor chain resistors, R3, R4, R5 are calculated by the following equations, and selecting $R_{(TOTAL)}$ = (R3 + R4 + R5) ≈ 500 kΩ.

DESIGN CONSIDERATION EXAMPLE AND APPLICATION INFORMATION (continued)

$$(R4 + R5) = \frac{2.4\ V \times R_{(TOTAL)}}{V_{(ADAPT\_DET)}} = \frac{2.4\ V \times 500\ k\Omega}{19\ V} = 63.2\ k\Omega \quad (23)$$

$$R5 = \frac{1.2\ V \times R_{(TOTAL)}}{V_{(AIRLINE\_DET)}} = \frac{1.2\ V \times 500\ k\Omega}{11.5\ V} = 52.2\ k\Omega \quad (24)$$

$$R4 = (R4 + R5) - R5 = 63.2\ k\Omega - 52.2\ k\Omega = 11\ k\Omega \quad (25)$$

$$R3 = (R3 + R4 + R5) - (R4 + R5) = 500\ k\Omega - 63.2\ k\Omega = 436.8\ k\Omega \quad (26)$$

Select the standard 1% resistor values of R3 = 432 kΩ, R4 = 11 kΩ, and R5 = 52.3 kΩ.

If airline mode is not needed, then set the AIRDET voltage threshold to be the same as the ACDET voltage threshold. Thus, both are set at 19 V by selecting standard 1% resistor values of R3 = 432 kΩ , R4 = 31.6 kΩ, and R5 = 31.6 kΩ.

Calculate the SRSET Programming Resistor

The charge current is defined as 3 A.

The $R_{(SRSET)}$ is calculated by the following equation:

$$R6 = R_{(SRSET)} = \frac{1\ V \times 1000\ \Omega}{I_{(CHARGE)} \times R_{(SENSE)}} = \frac{1\ V \times 1000\ \Omega}{3\ A \times 10\ m\Omega} = 33.3\ k\Omega$$

A standard 1%, 33.2 kΩ resistor is used.

Calculate the ACSET Programming Resistor

The input current limit is determined from the adapter power rating of 95 W and the adapter voltage of 20 V.

$$I_I = \frac{95\ W}{20\ V} = 4.75\ A \quad (27)$$

The $R_{(ACSET)}$ is calculated by the following equation:

$$R7 = R_{(ACSET)} = \frac{1\ V \times 1000\ \Omega}{I_{(IN)} \times R_{(SENSE)}} = \frac{1\ V \times 1000\ \Omega}{4.75\ A \times 10\ m\Omega} = 21\ k\Omega$$

A standard 1%, 21 kΩ resister is used.

DESIGN CONSIDERATION EXAMPLE AND APPLICATION INFORMATION (continued)

Calculate the ISYNSET Programming Resistor

The inductor current ripple is defined by:

$$\Delta I_L = \frac{\left(V_I max - V_{(BAT)} min\right) \times \left(\frac{V_{(BAT)}{}^{min}}{V_I{}^{max}}\right) \times \left(\frac{1}{f_{SW}}\right)}{L_{out}} \quad (28)$$

where the $V_I$max is the maximum input voltage, $V_{(BAT)}$min is the minimum battery voltage, and f_{SW} is the switching frequency.

$$\Delta I_L = \frac{(21\ V - 9\ V) \times \left(\frac{9\ V}{21\ V}\right) \times \left(\frac{1}{300\ kHz}\right)}{15\ \mu H} \quad (29)$$

The worst case inductor current ripple is ΔI_L = 1.14 A. To set the $I_{(SYNSET)}$ threshold to a value between $\frac{\Delta I_L}{2}$: and ΔI_L . Set $I_{(SYNSET)}$ = 1 A. $R_{(SYNSET)}$ is calculated by the following equation:

$$R12 = R_{(SYNSET)} = \frac{1\ V \times 500\ \Omega}{I_{(SYNSET)} \times R_{(SENSE)}} = \frac{1\ V \times 500\ \Omega}{1\ A \times 10\ m\Omega} = 50\ k\Omega. \quad (30)$$

Calculate the LOW BAT Programming Resistor

The battery depleted threshold to be programmed is a 3-V cell.

The LBSET programming resistor is calculated as:

$$R8 = R_{(LBSET)} = \frac{3\ V}{2\ x\ 5\ \mu A} = 300\ k\Omega \quad (31)$$

NARROW VOLTAGE DC (NVDC) EXAMPLE & APPLICATION INFORMATION

System Requirements (See Figure 26)

The bq24730 allows implementation of an NVDC charger. NVDC is an initiative by INTEL intended to increase notebook system efficiency by lowering the voltgage range of the system load in notebooks, which allows the optimization of devices to minimize power loss. In NVDC, the adapter is not allowed to connect to the system load. Instead, the system load is only connected to the output of the battery charger. This ensures the system load only detects the minimum to maximum voltage of the battery pack. Although this method of connecting the load directly to the battery pack has already been used for various other applications, the system approach to optimize efficiency motivation is making it more popular. In NVDC, the charger is required to process both charge current and system load at the same time; therefore, the power stage (Q2, Q3, L1, R2) needs to be designed accordingly for the increase in total current. The selector FETs Q4 and Q5 are not needed. The converter current is different from the battery sense current, so two output sense resistors are needed.

The SYNN and SYNP current sense pins allow sensing the converter current (for protection) independantly of the battery charge current. Figure 28 shows a method to implement an NVDC charger using only the two output sense resistors. The input current is limited, but is not directly sensed. Input current is indirectly regulated by connecting ACP/ACN and SYNN/SYNP pins across the converter protection resistor, and adding a resistor from the SRSET pin to the battery positive node in addition to the programming resistor from ACSET to GND.

If input current sense/limit accuracy and is absolutely necesary, then three sense resistors can be used, as shown in Figure 29.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
BQ24730RGFR	NRND	QFN	RGF	40	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
BQ24730RGFRG4	NRND	QFN	RGF	40	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
BQ24730RGFT	NRND	QFN	RGF	40	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
BQ24730RGFTG4	NRND	QFN	RGF	40	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR

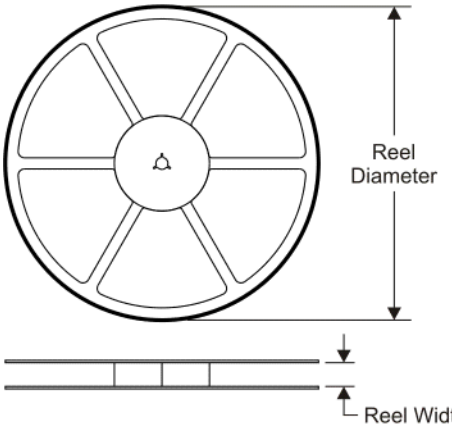
(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

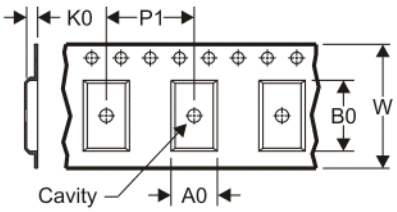
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

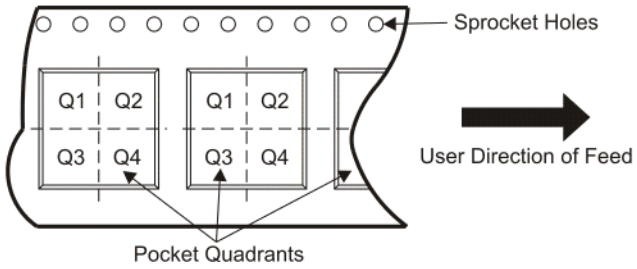


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

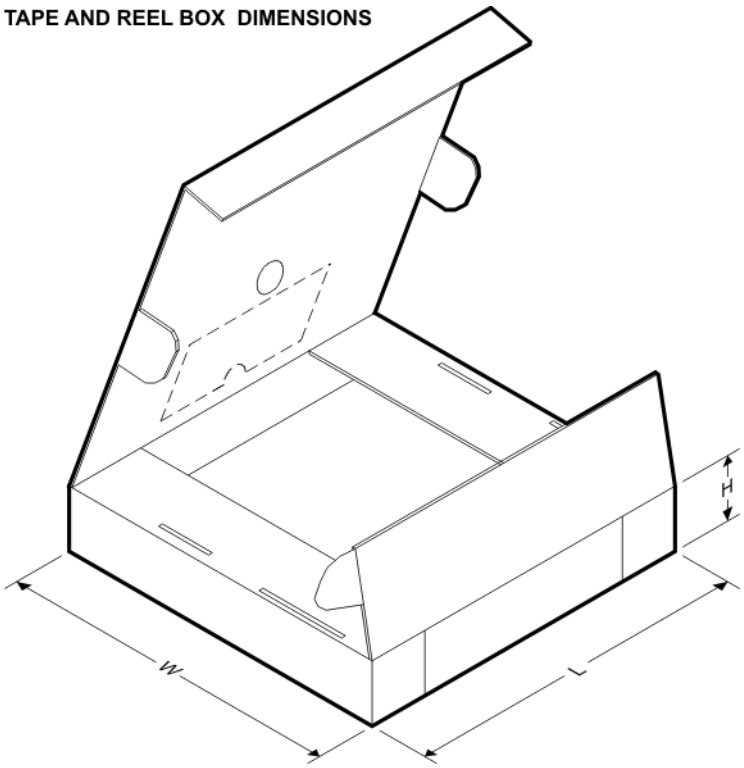
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
BQ24730RGFR	QFN	RGF	40	3000	330.0	16.4	5.25	7.25	1.45	8.0	16.0	Q1
BQ24730RGFT	QFN	RGF	40	250	180.0	16.4	5.25	7.25	1.45	8.0	16.0	Q1

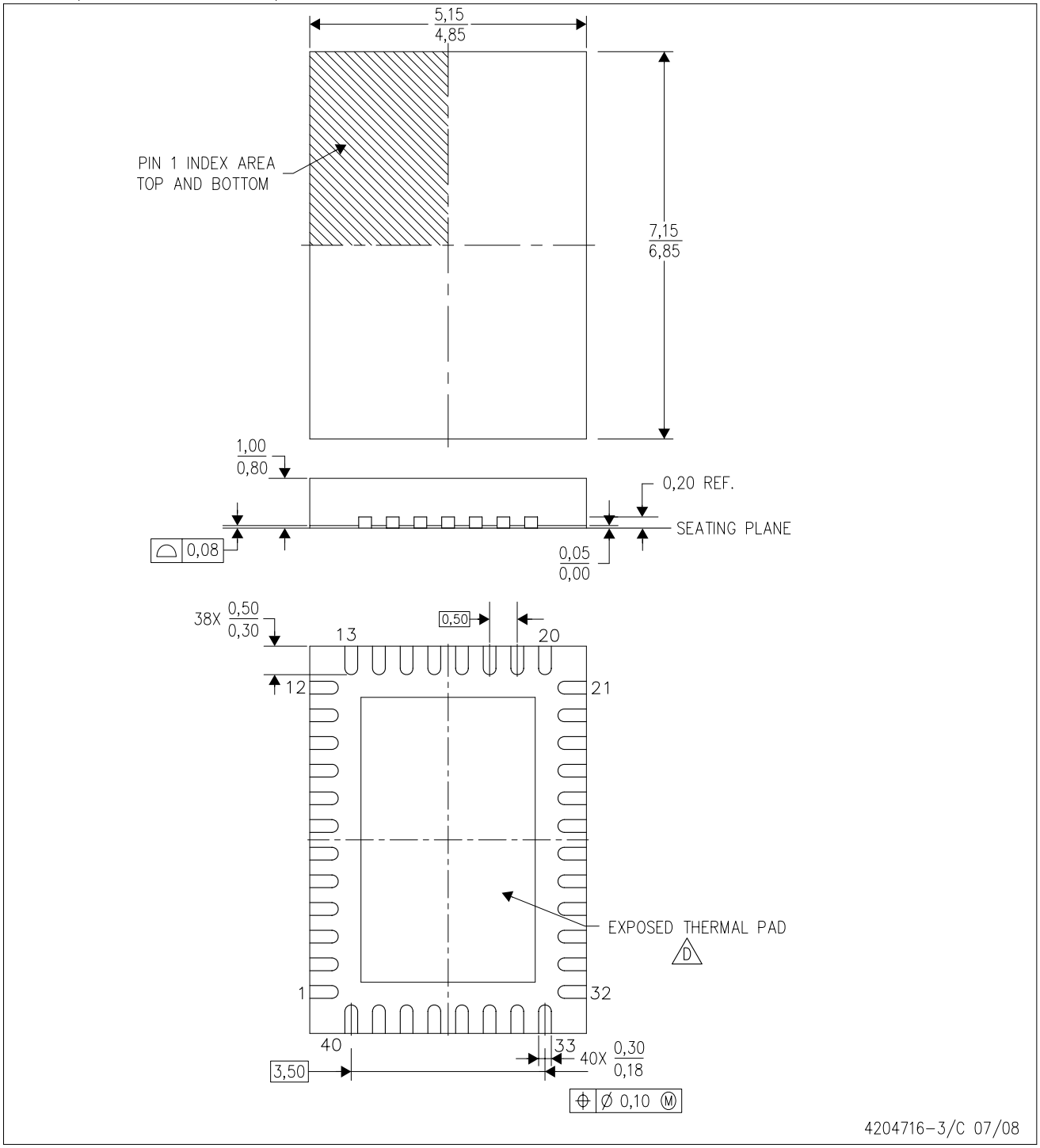
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
BQ24730RGFR	QFN	RGF	40	3000	346.0	346.0	33.0
BQ24730RGFT	QFN	RGF	40	250	190.5	212.7	31.8

RGF (R–VQFN–N40) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
E. Falls within JEDEC MO–220.

THERMAL PAD MECHANICAL DATA

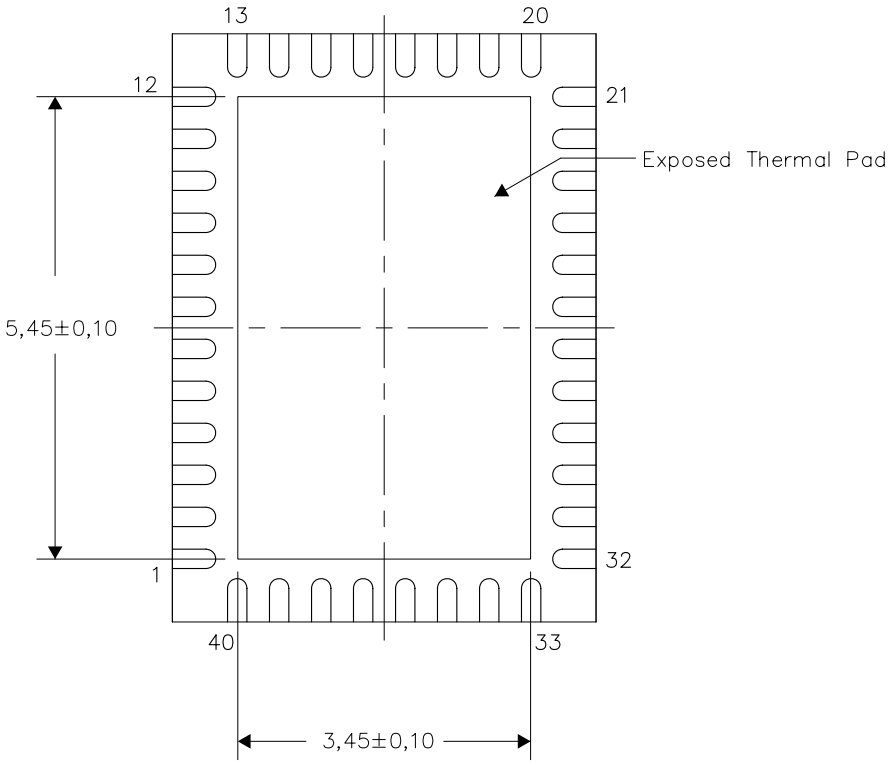
RGF (R–PVQFN–N40)

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

NOTE: All linear dimensions are in millimeters

Exposed Thermal Pad Dimensions

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