HARRIS SEMICONDUCTOR

HI2301

NOT RECOMMENDED FOR NEW DESIGNS
See HI2302

January 1998

8-Bit, 30 MSPS, Video A/D Converter with Amplifier/Clamp

Features

- Resolution . . . . . 8-Bit ±0.5 LSB (DNL)
- Maximum Sampling Frequency . . . . . 30 MSPS
- Low Power Consumption, 120mW (Including Reference Current)
- Standby Function
- Amplifier Functions
  - Built-In 3x Amplifier (15MHz Band)
  - 2-Input Selector Function Provided
- Built-In Input Clamp Function (DC Restore)
- Clamp ON/OFF Function
- Internal Voltage Reference
- Three-State TTL Compatible Output
- Power Supply . . . . . +5V Single or +4.75/3.3V Dual
- Direct Replacement for Sony CXD2301

Applications

- Desktop Video
- Multimedia
- Video Digitizing
- Image Scanners

Description

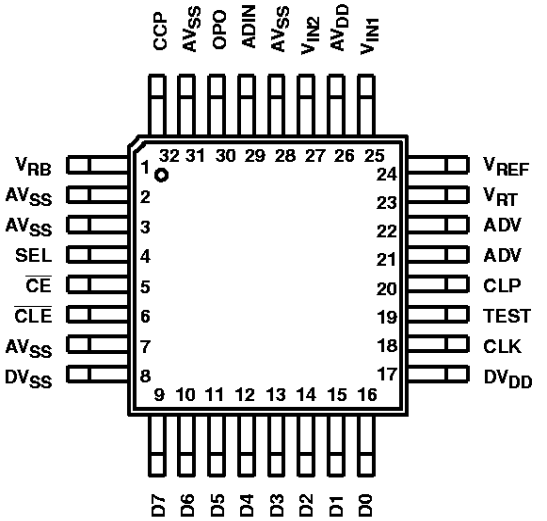
The HI2301 is an 8-bit CMOS analog-to-digital converter for video use that features a sync clamp function and on-chip amplifier. The adoption of a 2-step parallel method realizes low power consumption and a maximum conversion speed of 30 MSPS.

Ordering Information

PART NUMBER	TEMP. RANGE (^{o}C)	PACKAGE	PKG. NO.
HI2301JCQ	-20 to 75	32 Ld MQFP	Q32.7x7-S

Pinout

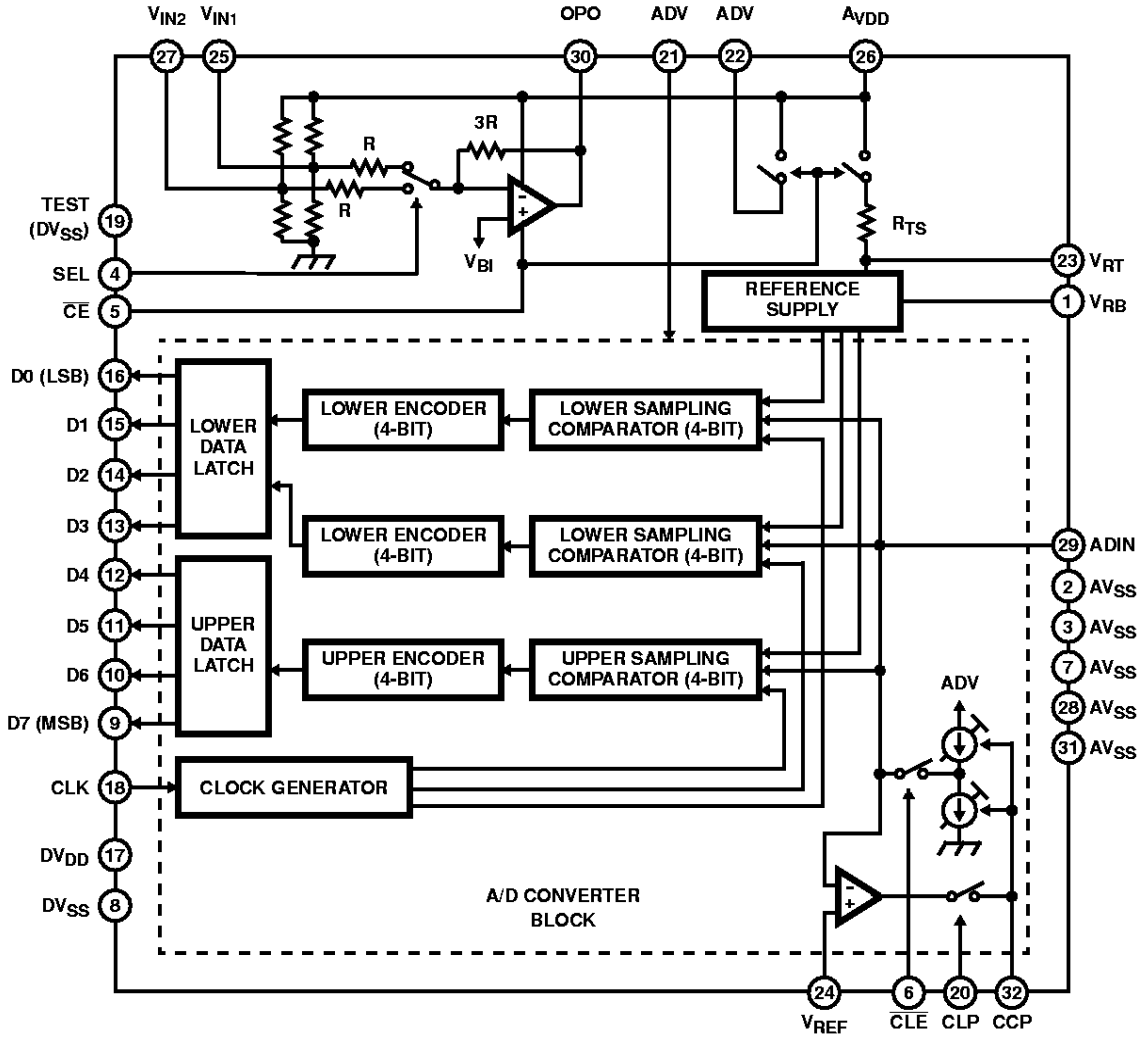
HI2301
(MQFP)
TOP VIEW



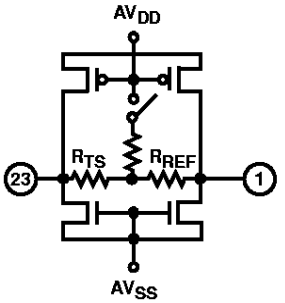
CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

File Number **4104.2**

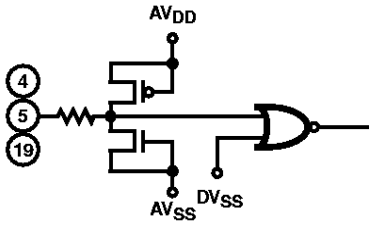
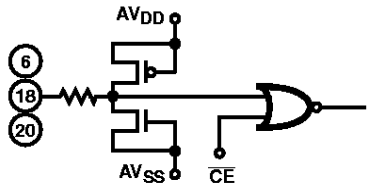
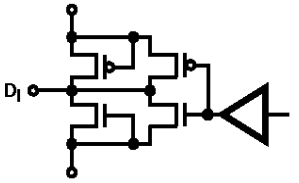
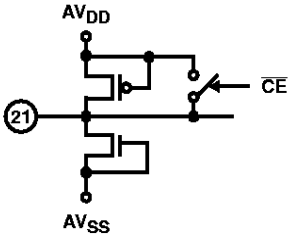
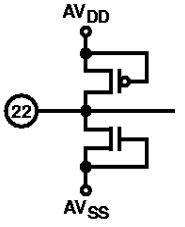
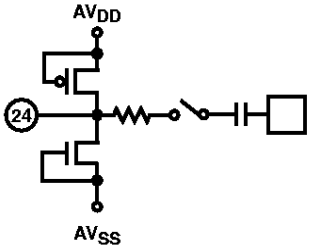
Functional Block Diagram



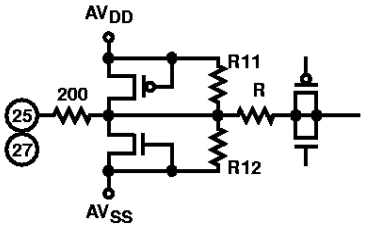
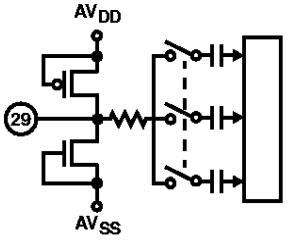
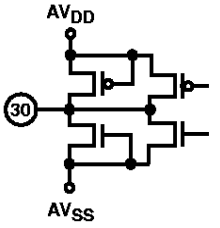
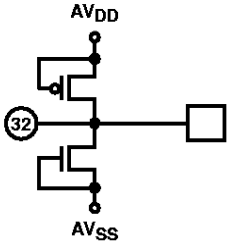
Pin Descriptions

PIN NO.	SYMBOL	EQUIVALENT CIRCUIT	DESCRIPTION
1	V_{RB}		Reference voltage (bottom) connect to AV_{SS} for normal use. When another external voltage is input, connect an external 0.1µF capacitor and retain a 1.5V differential compared to the top reference voltage.
23	V_{RT}		Reference voltage (top) by setting V_{RB} to AV_{SS}, outputs approximately 1.5V. Connect only a 0.1µF external by-pass capacitor for normal use. When another external voltage is input, it must be 2.2V or lower.
2, 3, 7, 28, 31	AV_{SS}		Analog GND.

Pin Descriptions (Continued)

PIN NO.	SYMBOL	EQUIVALENT CIRCUIT	DESCRIPTION
4	SEL		Switches the input of the 3x amplifier. When SEL is at Low level, V_{IN1} is selected. When SEL is at High level, V_{IN2} is selected.
5	$\overline{CE}$		Standby function ON/OFF selector. In standby state when High.
19	TEST		Fix to V_{SS} for normal use.
6	$\overline{CLE}$		When $\overline{CLE}$ = Low: Clamp function is enabled. When $\overline{CLE}$ = High: Clamp function is disabled, and only the normal A/D converter function is enabled.
18	CLK		Clock Input.
20	CLP		Inputs the clamp pulse to Pin 20 (CLP). Clamps the High interval signal voltage.
8	DV_{SS}		Digital GND.
9 to 16	D_7 to D_0		D_7 (MSB) to D_0 (LSB) output. Outputs Low level in standby. In operation, the phase of D_7 to D_0 output is inverted against the phase of ADIN.
17	D_{VDD}		5V or 3.3V
21	ADV		Short Pins 21 and 22, and connect 0.1µF external capacitor.
22	ADV		
24	V_{REF}		Clamp reference voltage input. Clamps so that the reference voltage and the clamp interval ADIN input signal are equal. The reference voltage is more than 0.5V.

Pin Descriptions (Continued)

PIN NO.	SYMBOL	EQUIVALENT CIRCUIT	DESCRIPTION
25	V_{IN1}		Amplifier input pin. Biased internal at 1.9V (when AV_{DD} = 5V) or at 1.8V (when AV_{DD} = 4.75V). When standby as well. When SEL is at Low level, V_{IN1} is selected for input; when SEL is at High level, V_{IN2} is selected for input.
27	V_{IN2}		
26	AV_{DD}		5V or 4.75V
29	ADIN		A/D converter block analog input.
30	OPO		Amplifier Output. The phase of this output is inverted against the phase of $V_{IN1, 2}$. In standby mode, it becomes high-impedance output condition.
32	CCP		Integrates the clamp control voltage. The relationship between the CCP voltage variation and the ADIN voltage is positive phase.

The following table shows the status of the digital output pins when the TEST pin is used with the $\overline{CE}$ and SEL pins.

TEST	CE	SEL	D1	D2	D3	D4	D5	D6	D7	D8
L	L	X	D1	D2	D3	D4	D5	D6	D7	D8
L	H	X	L	L	L	L	L	L	L	L
H	L	X	TEST MODE							
H	H	L	H	L	H	L	H	L	H	L
H	H	H	L	H	L	H	L	H	L	H

Digital Output

The following table shows the correlation between the ADIN input voltage and the digital output code. Take notice that the phase of ADIN input signal voltage is inverted against the phase of the digital output.

ADIN INPUT SIGNAL VOLTAGE	STEP	DIGITAL OUTPUT CODE MSB							LSB
V_{RT}	0	0	0	0	0	0	0	0	0
•	•				•				
•	•				•				
•	•				•				
•	127	0	1	1	1	1	1	1	1
•	128	1	0	0	0	0	0	0	0
•	•				•				
•	•				•				
•	•				•				
V_{RB}	255	1	1	1	1	1	1	1	1

Absolute Maximum Ratings $T_A = 25^oC$

Supply Voltage (V_{DD}) 7V
Reference Voltage (V_{RT}, V_{RB}) . . . . . V_{DD} 0.5 to V_{SS} -0.5V
Input Voltage, Analog (V_{IN}) . . . . . V_{DD} 0.5 to V_{SS} -0.5V
Input Voltage, Digital (V_{IH}, V_{IL}) . . . . . V_{DD} 0.5 to V_{SS} -0.5V
Output Voltage, Digital (V_{OH}, V_{OL}) . . . . . V_{DD} 0.5 to V_{SS} -0.5V

Operating Conditions

Supply Voltage (IDV_{SS} - $AV_{SS}I$) . . . . . 0 to 100mV
Single Power Supply (AV_{DD}, DV_{DD}) . . . . . 5.0 ±0.25V
Dual Power Supply (AV_{DD}) . . . . . 4.75 ±0.25V
(DV_{DD}) . . . . . 3.3 ±0.3V
Reference Input Voltage (V_{RB}) . . . . . 0V to 2.2V
(V_{RT}) . . . . . 0V to 2.2V
Analog Input (ADIN) . . . . . More than $1.2V_{P-P}$
Clock Pulse width, t_{PW1} . . . . . 16ns (Min)
t_{PW0} . . . . . 16ns (Min)
Temperature Range (T_{OPR}) . . . . . -20 to 75°C

Thermal Information

Thermal Resistance (Typical, Note 1) θ_{JA} (°C/W)
MQFP Package 122
Maximum Junction Temperature (Plastic Package) . . . . . 150°C
Maximum Storage Temperature Range . . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . . 300°C
(Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

Electrical Specifications; When using a single power supply (f_C = 30 MSPS, AV_{DD} = DV_{DD} = +5V, V_{RB} = 0V, V_{RT} = 1.5V, T_A = 25°C

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNITS
Supply Current	$I_{AD} + I_{DD}$	f_C = 35 MSPS, NTSC Ramp Wave Input		-	27	35	mA
Standby Supply Current	I_{STB}	$\overline{CE}$ = DV_{DD}		-	130	200	µA
Max Conversion Rate	f_C Max	V_{IN} = 0V to 1.5V, f_{IN} = 1kHz Ramp		30	-	-	MSPS
Min Conversion Rate	f_C Min			-	-	0.5	MSPS
ADIN Input Band (At -1dB)	BW			-	20	-	MHz
ADIN Input Capacitance	C_{ADIN}	V_{IN} = 0.75V + $0.07V_{RMS}$		-	8	-	pF
Reference Resistance (V_{RT} to V_{RB})	R_{REF}			230	330	440	Ω
Self Bias	V_{RT}	V_{RB} = AV_{SS}		1.38	1.52	1.66	V
Offset Voltage	EOT			-40	-20	0	mV
	EOB			+25	+45	+65	mV
Digital Input Voltage	V_{IH}			3.5	-	-	V
	V_{IL}			-	-	0.5	V
Digital Input Current	I_{IH}	DV_{DD} = Max	V_{IH} = V_{DD}	-	-	5	µA
	I_{IL}		V_{IL} = 0V	-	-	5	µA
Digital Output Current	I_{OH}	DV_{DD} = Min	V_{OH} = V_{DD} - 0.5V	-1.1	-2.5	-	mA
	I_{OL}		V_{OL} = 0.4V	3.7	6.5	-	mA
Output Data Delay	t_{DL}	With TTL 1 Gate and 10pF Load		7	13	25	ns
Integral Nonlinearity Error	E_L	f_C = 30 MSPS, V_{IN} = 0V To 1.5V		-	+0.5	+1.3	LSB
Differential Gain Error	DG	NTSC 40 IRE Mod Ramp, f_C = 14.3 MSPS		-	1	-	%
Differential Phase Error	DP			-	0.5	-	Degrees
Aperture Jitter	t_{AJ}			-	30	-	ps
Sampling Delay	t_{SD}			-	2	-	ns
Clamp Offset Voltage	E_{OC}	V_{ADIN} = DC PWS = 3µ	V_{REF} = 0.5V	0	+20	+40	mV
			V_{REF} = 1.5V	-40	-20	0	mV

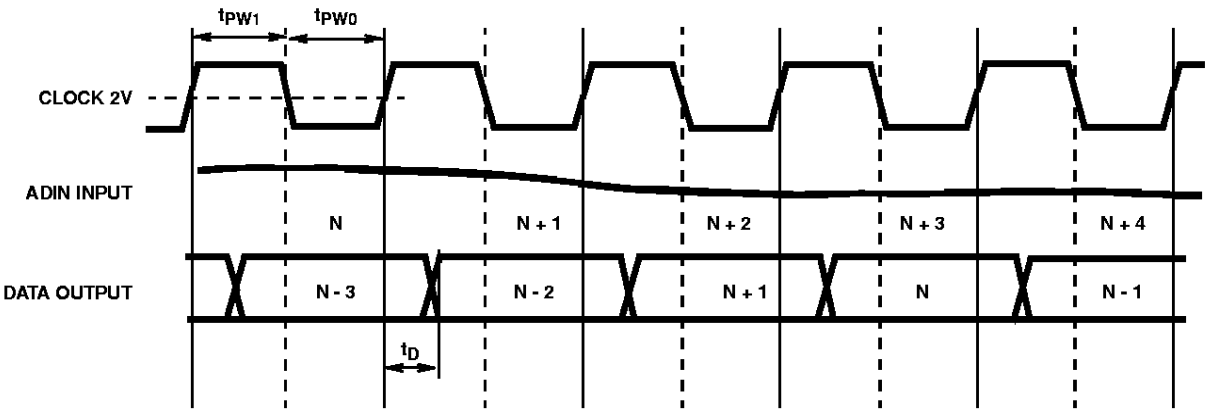
Electrical Specifications Electrical Specifications; When using a single power supply (f_C = 30 MSPS, AV_{DD} = DV_{DD} = +5V, V_{RB} = 0V, V_{RT} = 1.5V, T_A = 25°C **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Clamp Pulse Delay	t_{CPD}		-	25	-	ns
Amplifier Gain		DC To 15MHz	8.5	9.5	10.5	dB
V_{IN1} and V_{IN2} Bias Voltage	$V_{BI1,2}$	When Open	-	1.9	-	V
V_{IN1} and V_{IN2} Input Resistance	$R_{I1,2}$		19	27	35	kW
V_{IN1} and V_{IN2} Input Capacitance	$C_{I1,2}$		-	15	-	pF

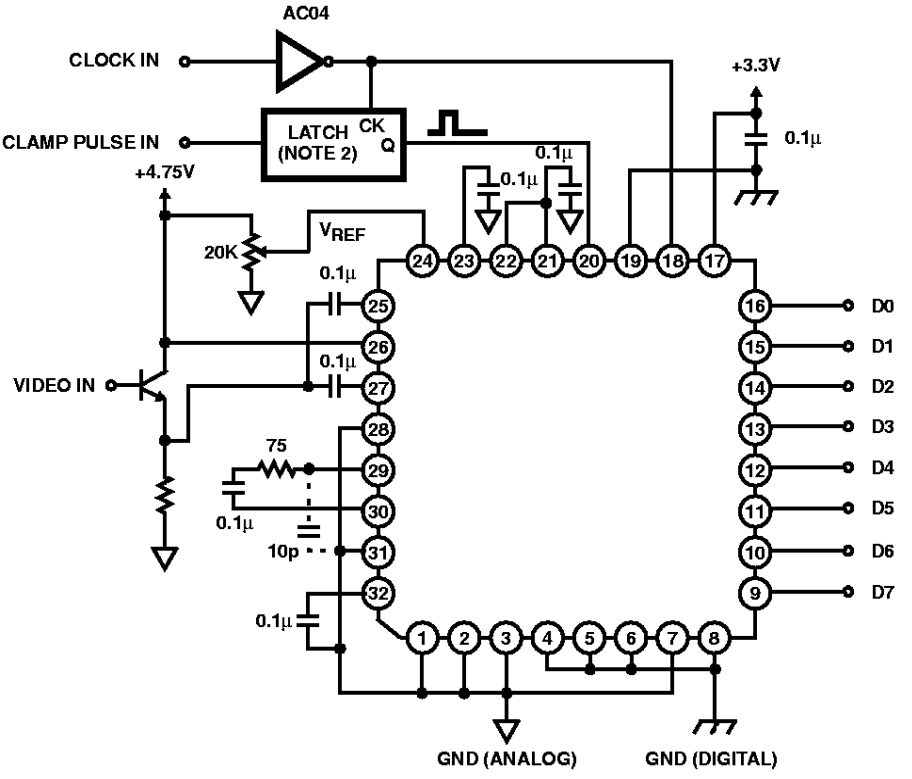
Electrical Specifications When Using a Dual Power Supply (f_C = 30 MSPS, AV_{DD} = DV_{DD} = +5V, V_{RT} = 1.5V, V_{RT} = 1.5V, T_A = 25°C

(2) When Using A Dual Power Supply	f_C = 30 MSPS, AV_{DD} = 4.75V, DV_{DD} = 0V, V_{RT} = 1.5V, T_A = 25°C					
Analog Supply Current	I_{AD}	f_C = 30 MSPS, NTSC Ramp Wave Input	-	24	32	mA
Digital Supply Current	I_{DD}	f_C = 30 MSPS, NTSC Ramp Wave Input	-	1	2	mA
Standby Supply Current	I_{STB}	$\overline{CE}$ = DV_{DD}	-	130	200	µA
Maximum Conversion Rate	f_C Max	V_{IN} = 0 to 1.5V, f_{IN} = 1kHz Ramp	30	-	-	MSPS
Minimum Conversion Rate	f_C Min		-	-	0.5	MSPS
ADIN Input Band (at -1dB)	BW		-	20	-	MHz
ADIN Input Capacitance	C_{ADIN}	V_{IN} = 0.75V + 0.07V_{RMS}	-	8	-	pF
Referenced Resistance (V_{RT} to V_{RB})	R_{REF}		230	330	440	Ω
Self Bias	V_{RT}	V_{RB} = AV_{SS}	1.44	1.52	1.6	V
Offset Voltage	E_{OT}		-40	-20	0	mV
	E_{OB}		+25	+45	+65	mV
Digital Input Voltage	V_{IH}		2.5	-	-	V
	V_{IL}		-	-	0.5	V
Digital Input Current	I_{IH}	DV_{DD} = Max, V_{IH} = DV_{DD}	-	-	5	µA
	I_{IL}	V_{IL} = 0V	-	-	5	µA
Digital Output Current	I_{OH}	DV_{DD} = Min, V_{OH} = V_{DD} -0.5V	-1.1	-2.5	-	mA
	I_{OL}	V_{OL} = 0.4V	3.7	6.5	-	mA
Output Data Delay	t_{DL}	With TTL 1 Gate and 10pF Load	7	13	25	ns
Integral Nonlinearity Error	E_L	f_C = 30 MSPS, V_{IN} = 0 to 1.5V	-	+0.5	+1.3	LSB
Differential Nonlinearity Error	E_D	f_C = 30 MSPS, V_{IN} = 0 to 1.5V	-	0.3	0.5	LSB
Differential Gain Error	DG	NTSC 40 IRE Mod Ramp, f_C = 14.3 MSPS	-	1	-	%
Differential Phase Error	DP		-	0.5	-	deg
Aperture Jitter	t_{AJ}		-	30	-	ps
Sampling delay	t_{SD}		-	2	-	ns
Clamp Offset Voltage	E_{OC}	V_{IN} = DC, PWS = 3µs, V_{REF} = 0.5V	0	+20	+40	mV
		V_{REF} = 1.5V	-40	-20	0	mV
Clamp Pulse Delay	t_{CPD}		-	25	-	ns
3x Amplifier Gain		DC to 15MHz	8.5	9.5	10.5	dB
V_{IN1} and V_{IN2} Bias Voltage	$V_{BI1,2}$	When Open	-	1.8	-	V
V_{IN1} and V_{IN2} Input Resistance	$R_{I1,2}$		19	27	35	kΩ
V_{IN1} and V_{IN2} Input Capacitance	$C_{I1,2}$		-	15	-	pF

Timing Chart



Application Circuits

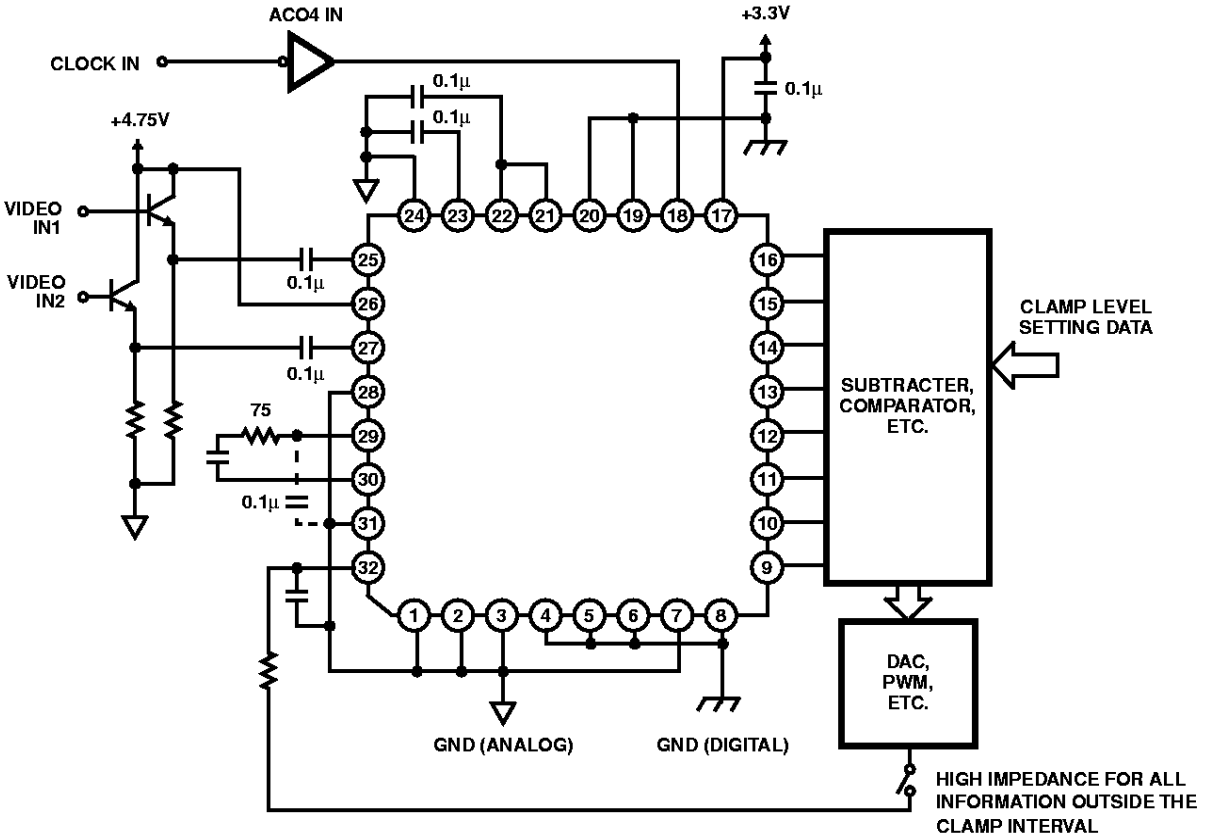


NOTE:

2. Although the ADC sampling clock latches the clamp pule, it is not needed for basic clamp operation. However, depending on the relationship between the sampling frequency and the clamp pulse frequency, a small beat might be generated as V_{SAG}. The latch circuit is valid at this time.

FIGURE 1. CLAMP USAGE EXAMPLE (USING SELF BIAS, CIRCUIT WHEN USING THE INTERNAL AMPLIFIER)

Application Circuits (Continued)



NOTES:

3. The relationship between the CCP voltage (Pin 32) variation and the ADIN voltage variation is position phase.
4. $\Delta ADIN/\Delta V_{CCP} = 3.0$ ($f_S = 30$ MSPS).

FIGURE 2. DIGITAL CLAMP USAGE EXAMPLE (USING SELF BIAS), CIRCUIT WHEN USING THE INTERNAL AMPLIFIER

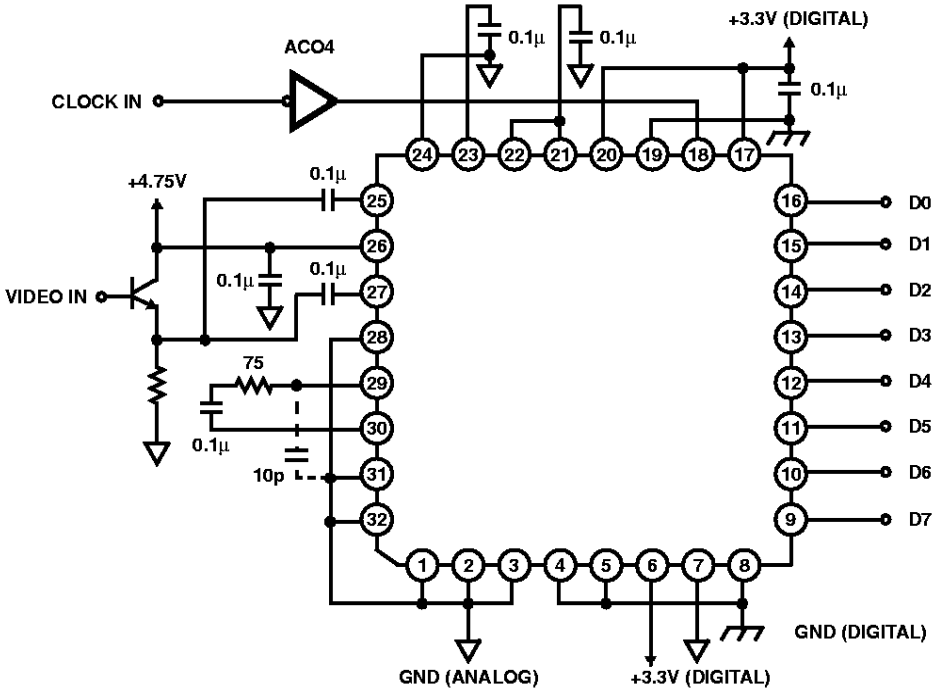
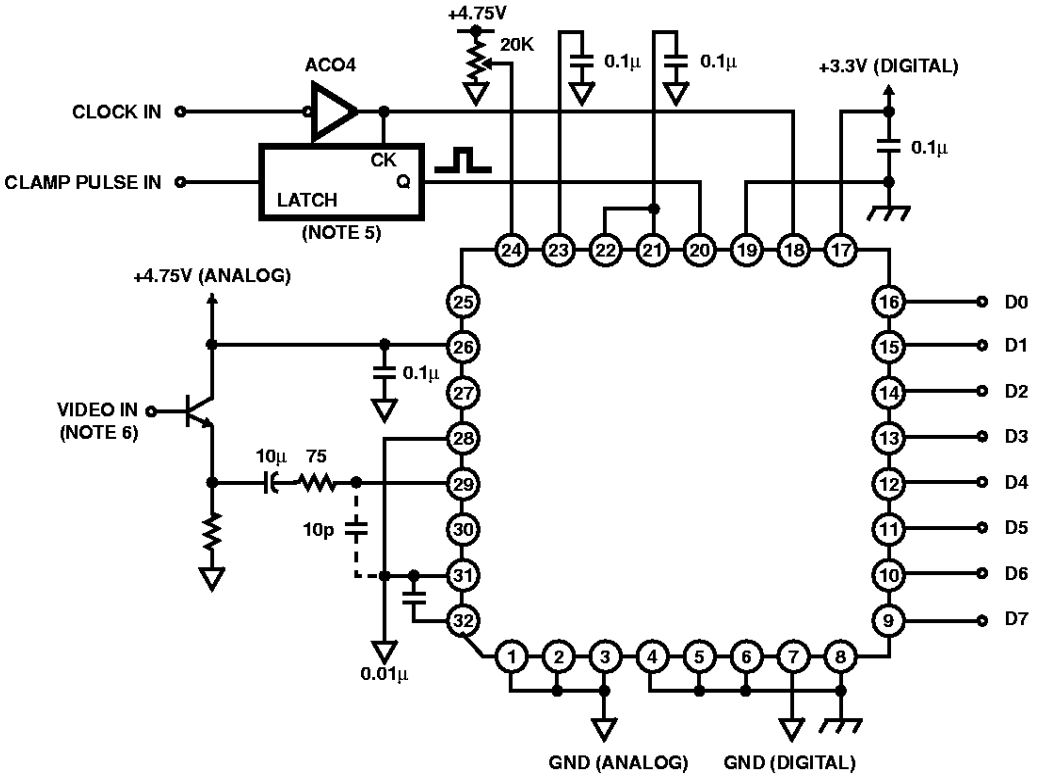


FIGURE 3. WHEN NOT USING THE CLAMP, CIRCUIT WHEN USING THE INTERNAL AMPLIFIER

Application Circuits (Continued)

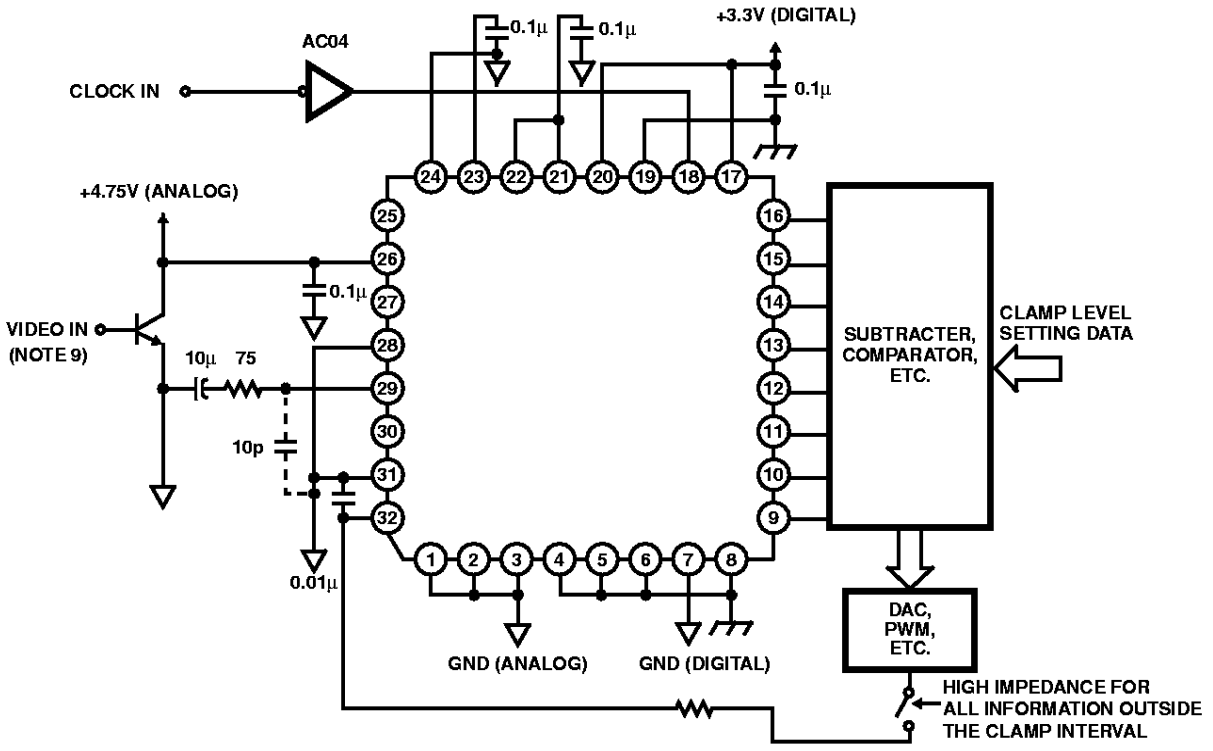


NOTES:

5. Although the ADC sampling clock latches the clamp pulse, it is not needed for basic clamp operation. However, depending on the relationship between the sampling frequency and the clamp pulse frequency, a small abeat might be generated as V_{SAG}. The latch circuit is valid at this time.
6. Take care that the phase of ADIN input is inverted against the phase of the digital output, because the use of the built-in inverting amplifier is standard. (Refer to “Digital Output”.)

FIGURE 4. CLAMP USAGE EXAMPLE WHEN NOT USING THE INTERNAL AMPLIFIER

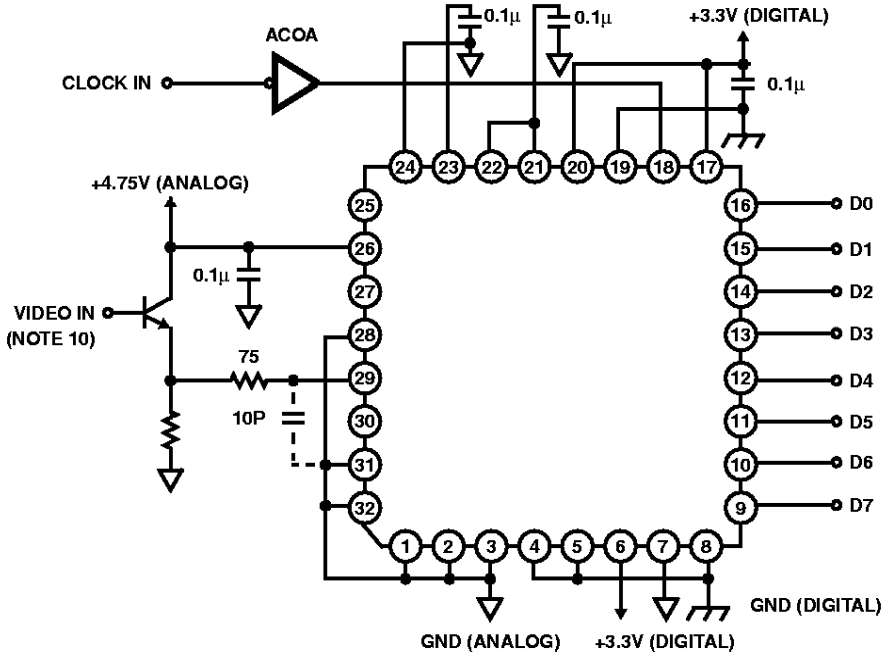
Application Circuits (Continued)



NOTES:

7. The relationship between the CCP voltage (Pin 32) variation and the ADIN voltage variation is positive phase.
8. $\Delta V_{ADIN}/\Delta V_{CCP}$ = 3.0 (f_S = 20 MSPS).
9. Take care that the phase of ADIN input is inverted against the phase of the digital output, because the use of the built-in inverting amplifier is standard. (Refer to "Digital Output.")

FIGURE 5. DIGITAL CLAMP USAGE EXAMPLE



NOTE:

10. Take care that the phase of ADIN input is inverted against the phase of the digital output, because the use of the built-in inverting amplifier is standard. (Refer to "Digital Output".)

FIGURE 6. WHEN NOT USING THE CLAMP

Typical Performance Curves

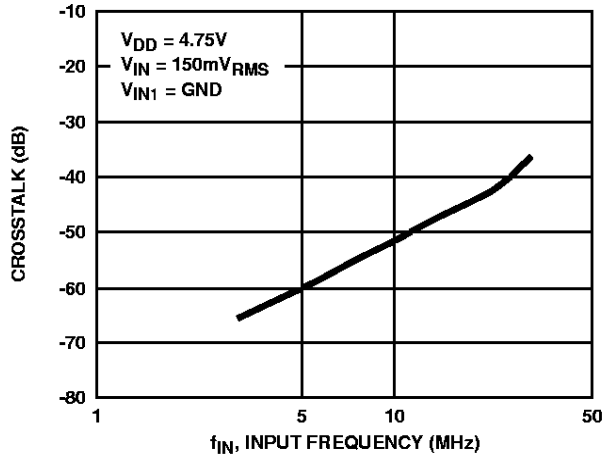


FIGURE 7. INPUT FREQUENCY OF V_{IN2} vs CROSSTALK $V_{IN2} \rightarrow V_{IN1}$

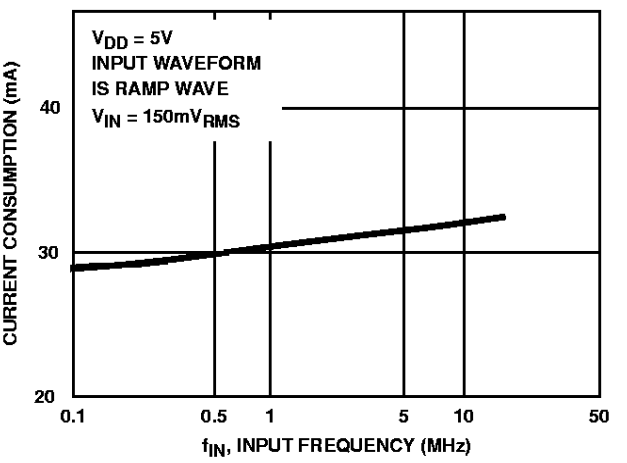


FIGURE 8. INPUT FREQUENCY vs CURRENT CONSUMPTION

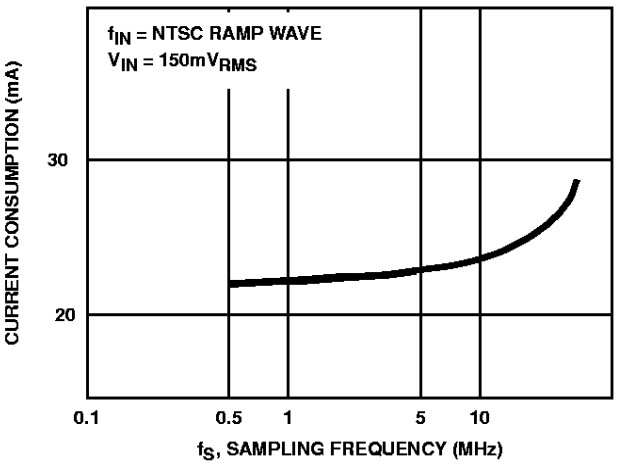


FIGURE 9. SAMPLING FREQUENCY vs CURRENT CONSUMPTION

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