# KS22/KS20 Microcontroller

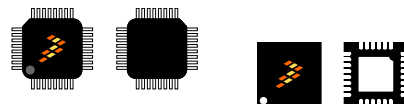**120 MHz ARM® Cortex®-M4, with up to 256 KB Flash**

The KS2x product family is built on the ARM® Cortex®-M4 processor with lower power and higher memory densities in multiple packages. This device offers 120 MHz performance with an integrated single-precision floating point unit (FPU). Embedded flash memory sizes range from 128 KB to 256KB. This device also includes:

- USB FS OTG 2.0 with crystal-less functionality
- FlexCAN, supporting CAN protocol according to the ISO 11898-1 standard and CAN 2.0 B protocol specifications
- FlexIO, a highly configurable module providing a wide range of protocols including, but not limited to UART, LPI2C, SPI, I2S, and PWM/Waveform generation.

| MKS22FN256Vxx12 |
| MKS22FN128Vxx12 |
| MKS20FN256Vxx12 |
| MKS20FN128Vxx12 |

100 & 64 LQFP (LL & LH)
14×14×1.7 mm Pitch 0.5 mm; 10×10×1.6 mm Pitch 0.5 mm

48 QFN (FT)
7×7×0.65 mm Pitch 0.5 mm

## Performance
- 120 MHz ARM Cortex-M4 core with DSP instructions delivering 1.25 Dhrystone MIPS per MHz

## Memories and memory interfaces
- Up to 256 KB of embedded flash and 64 KB of SRAM
- Preprogrammed Kinetis Flashloader for one-time, in-system factory programming

## System peripherals
- Flexible low-power modes, multiple wake up sources
- 16-channel asynchronous DMA controller
- Independent external and software watchdog monitor

## Clocks
- Two crystal oscillators: 32 kHz (RTC), and 32-40 kHz or 3-32 MHz
- Three internal oscillators: 32 kHz, 4 MHz, and 48 MHz
- Multi-purpose clock generator (MCG) with PLL and FLL

## Security and integrity modules
- Hardware CRC module
- 128-bit unique identification (UID) number per chip
- Hardware random-number generator
- Flash access control (FAC) to protect proprietary software

## Human-machine interfaces
- Up to 66 general-purpose input/output pins (GPIO)

## Analog modules
- One 16-bit ADC module with up to 17 single-end channels and 4 differential channels, and up to 1.2 Msps at ≤ 13-bit mode
- One 12-bit DAC module
- One analog comparator (CMP) module

## Communication interfaces
- USB full-speed 2.0 device controller
- One FlexIO module
- Three UART modules (one supporting ISO7816, and the other two operating up to 1.5 Mbit/s)
- One LPUART module supporting asynchronous operation in low-power modes
- Two LPI2C modules supporting up to 5 Mbit/s, asynchronous operation in low-power modes supported
- Two 16-bit SPI modules supporting up to 30 Mbit/s
- Two FlexCAN modules for KS22, One FlexCAN for KS20
- Two I2S modules

## Timers
- Three 16-bit low-power timer PWM modules (TPM)
- One low-power timer (LPTMR)
- Periodic interrupt timer (PIT)
- Real time clock (RTC), with independent power domain
- Programmable delay block (PDB)

**Operating characteristics**
- Voltage range (including flash writes): 1.71 to 3.6 V
- Temperature range (ambient): –40 to 105 °C

## Related Resources

| Type | Description | Resource |
|---|---|---|
| Selector Guide | The Freescale Solution Advisor is a web-based tool that features interactive application wizards and a dynamic product selector. | Solution Advisor |
| Product Brief | The Product Brief contains concise overview/summary information to enable quick evaluation of a device for design suitability. | KS22PB [1] |
| Reference Manual | The Reference Manual contains a comprehensive description of the structure and function (operation) of a device. | KS22P100M120SF0RM[1] |
| Data Sheet | The Data Sheet includes electrical characteristics and signal connections. | This document: KS22P100M120SF0[1] |
| Chip Errata | The chip mask set Errata provides additional or corrective information for a particular device mask set. | KINETIS_K_0N87R [1] |
| Package drawing | Package dimensions are provided in package drawings. | LQFP 100-pin: 98ASS23308W  LQFP 64-pin: 98ASS23234W  QFN 48-pin: 98ASA00616D |

1. To find the associated resource, go to http://www.freescale.com and perform a search using this term.
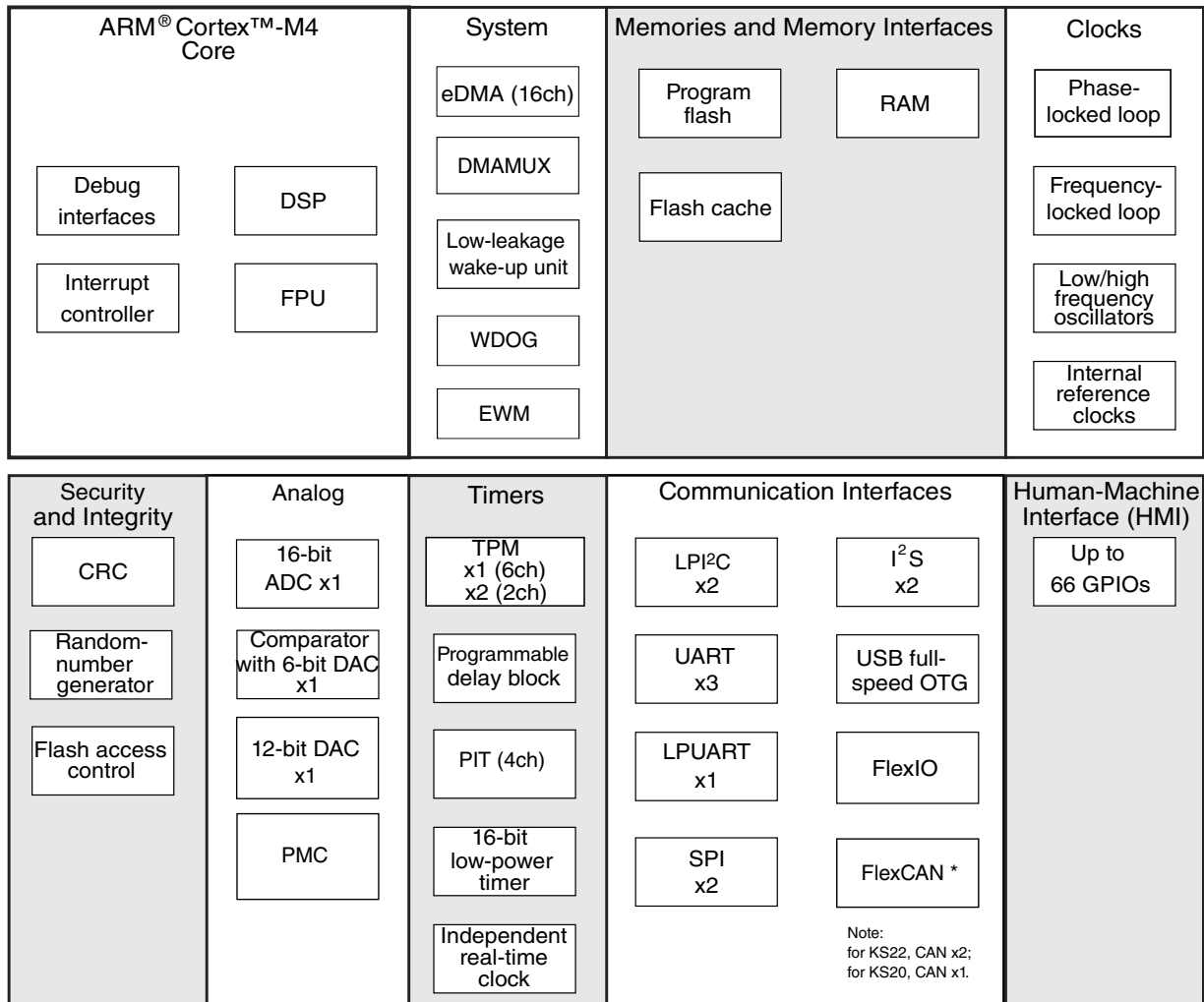
**Figure 1. Functional block diagram**

**NOTE**

DAC0 and $I^2$S1 are NOT supported in the 48-QFN package. For more details, see the "Signal Multiplexing and Pin Assignments" section.

# Table of Contents

# 1 Ordering information

The following chips are available for ordering.

**Table 1. Ordering information**

| Product | | Memory | | Package | | IO and ADC channel | | | Communication |
|---|---|---|---|---|---|---|---|---|---|
| Part number | Marking (Line1/Line2) | Flash (KB) | SRAM (KB) | Pin count | Package | GPIOs | GPIOs (INT/HD) [1] | ADC channels (SE/DP) [2] | FlexCAN |
| MKS22FN256VLL12 | MKS22FN256 / VLL12 | 256 | 64 | 100 | LQFP | 66 | 66/8 | 17/4 | 2 |
| MKS22FN256VLH12 | MKS22FN256 / VLH12 | 256 | 64 | 64 | LQFP | 40 | 40/8 | 14/2 [3] | 2 |
| MKS22FN256VFT12 | MKS22FN256 / VFT12 | 256 | 64 | 48 | QFN | 35 | 35/8 | 13/— | 2 |
| MKS22FN128VLL12 | MKS22FN128 / VLL12 | 128 | 64 | 100 | LQFP | 66 | 66/8 | 17/4 | 2 |
| MKS22FN128VLH12 | MKS22FN128 / VLH12 | 128 | 64 | 64 | LQFP | 40 | 40/8 | 14/2 [3] | 2 |
| MKS22FN128VFT12 | MKS22FN128 / VFT12 | 128 | 64 | 48 | QFN | 35 | 35/8 | 13/— | 2 |
| MKS20FN256VLL12 | MKS20FN256 / VLL12 | 256 | 64 | 100 | LQFP | 66 | 66/8 | 17/4 | 1 |
| MKS20FN256VLH12 | MKS20FN256 / VLH12 | 256 | 64 | 64 | LQFP | 40 | 40/8 | 14/2 [3] | 1 |
| MKS20FN256VFT12 | MKS20FN256 / VFT12 | 256 | 64 | 48 | QFN | 35 | 35/8 | 13/— | 1 |
| MKS20FN128VLL12 | MKS20FN128 / VLL12 | 128 | 64 | 100 | LQFP | 66 | 66/8 | 17/4 | 1 |
| MKS20FN128VLH12 | MKS20FN128 / VLH12 | 128 | 64 | 64 | LQFP | 40 | 40/8 | 14/2 [3] | 1 |
| MKS20FN128VFT12 | MKS20FN128 / VFT12 | 128 | 64 | 48 | QFN | 35 | 35/8 | 13/— | 1 |

1. INT: interrupt pin numbers; HD: high drive pin numbers
2. SE: single-ended; DP: differential pair
3. ADC0_DP1 is for single-ended (SE) mode only in 64-LQFP.

# 2 Overview

The following figure shows the system diagram of this device.
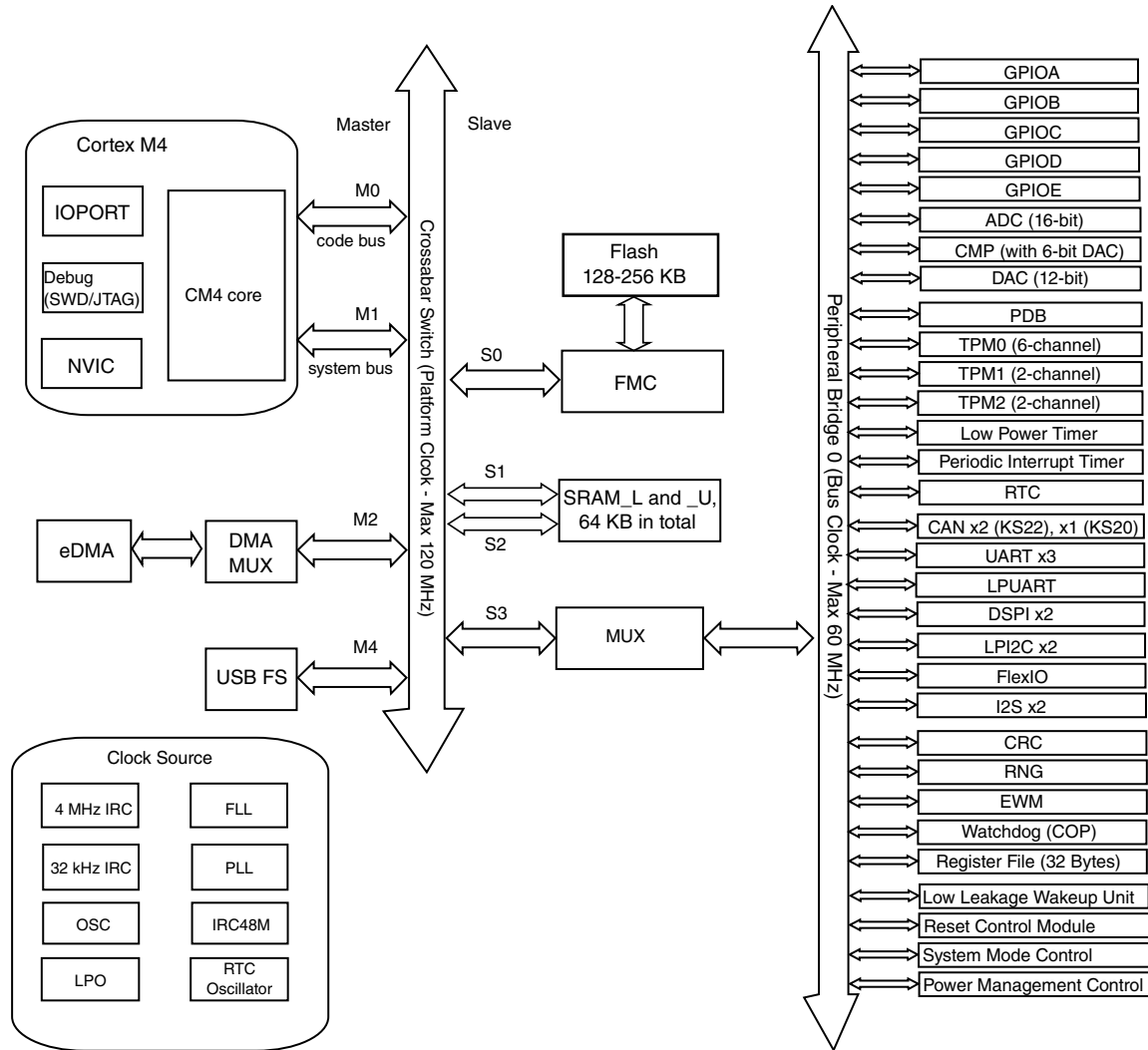


**Figure 2. System diagram**

The crossbar switch connects bus masters and slaves using a crossbar switch structure. This structure allows up to four bus masters to access different bus slaves simultaneously, while providing arbitration among the bus masters when they access the same slave.

## 2.1  System features

The following sections describe the high-level system features.

### 2.1.1  ARM Cortex-M4 core

The ARM Cortex-M4 is the member of the Cortex M Series of processors targeting microcontroller cores focused on very cost sensitive, deterministic, interrupt driven environments. The Cortex M4 processor is based on the ARMv7 Architecture and Thumb®-2 ISA and is upward compatible with the Cortex M3, Cortex M1, and Cortex M0 architectures. Cortex M4 improvements include an ARMv7 Thumb-2 DSP (ported from the ARMv7-A/R profile architectures) providing 32-bit instructions with SIMD (single instruction multiple data) DSP style multiply-accumulates and saturating arithmetic.

### 2.1.2  NVIC

The Nested Vectored Interrupt Controller supports nested interrupts and 16 priority levels for interrupts. In the NVIC, each source in the IPR registers contains 4 bits. It also differs in number of interrupt sources and supports 240 interrupt vectors.

The Cortex-M family uses a number of methods to improve interrupt latency . It also can be used to wake the MCU core from Wait and VLPW modes.

### 2.1.3  AWIC

The asynchronous wake-up interrupt controller (AWIC) is used to detect asynchronous wake-up events in Stop mode and signal to clock control logic to resume system clocking. After clock restarts, the NVIC observes the pending interrupt and performs the normal interrupt or event processing. The AWIC can be used to wake MCU core from Partial Stop, Stop and VLPS modes.

Wake-up sources for this SoC are listed as below:

**Table 2.  AWIC Partial Stop, Stop and VLPS Wake-up Sources**

| Wake-up source | Description |
|---|---|
| Available system resets | $\overline{\text{RESET}}$ pin and WDOG when LPO is its clock source, and JTAG |
| Low voltage detect | Power Mode Controller |
| Low voltage warning | Power Mode Controller |
| High voltage detect | Power Mode Controller |
| Pin interrupts | Port Control Module - Any enabled pin interrupt is capable of waking the system |
| ADC | The ADC is functional when using internal clock source |
| CMP | Since no system clocks are available, functionality is limited, trigger mode provides wakeup functionality with periodic sampling |
| LPI$^2$C | Functional when using clock source which is active in Stop and VLPS modes |
| FlexIO | Functional when using clock source which is active in Stop and VLPS modes |
| TPM | Functional when using clock source which is active in Stop and VLPS modes |
| UART | Active edge on RXD |
| LPUART | Functional when using clock source which is active in Stop and VLPS modes |
| USB FS/LS Controller | Wakeup |
| LPTMR | Functional when using clock source which is active in Stop and VLPS modes |
| RTC | Functional in Stop/VLPS modes |
| I2S (SAI) | Functional when using an external bit clock or external master clock |
| TPM | Functional when using clock source which is active in Stop and VLPS modes |
| CAN | Wakeup on edge (CANx_RX) |
| NMI | Non-maskable interrupt |

## 2.1.4  Memory

This device has the following features:
- 64 KB of embedded RAM accessible (read/write) at CPU clock speed with 0 wait states.
- The non-volatile memory is divided into
    - 128/256 KB of embedded program memory

The program flash memory contains a 16-byte flash configuration field that stores default protection settings and security information. The page size of program flash is 2 KB.

The protection setting can protect 32 regions of the program flash memory from unintended erase or program operations.

The security circuitry prevents unauthorized access to RAM or flash contents from debug port.

- System register file

This device contains a 32-byte register file that is powered in all power modes.

Also, it retains contents during low power modes and is reset only during a power-on reset.

## 2.1.5 Reset and boot

The following table lists all the reset sources supported by this device.

**NOTE**

In the following table, Y means the specific module, except for the registers, bits or conditions mentioned in the footnote, is reset by the corresponding Reset source. N means the specific module is not reset by the corresponding Reset source.

**Table 3. Reset source**

| Reset sources | Descriptions | Modules | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | PMC | SIM | SMC | RCM | LLWU | Reset pin is negated | RTC | LPTMR | Others |
| POR reset | Power-on reset (POR) | Y | Y | Y | Y | Y | Y | Y | Y | Y |
| System resets | Low-voltage detect (LVD) | Y[1] | Y | Y | Y | Y | Y | N | Y | Y |
| | Low leakage wakeup (LLWU) reset | N | Y[2] | N | Y | N | Y[3] | N | N | Y |
| | External pin reset (RESET) | Y[1] | Y[2] | Y[4] | Y | Y | Y | N | N | Y |
| | Watchdog (WDOG) reset | Y[1] | Y[2] | Y[4] | Y[5] | Y | Y | N | N | Y |
| | Multipurpose clock generator loss of clock (LOC) reset | Y[1] | Y[2] | Y[4] | Y[5] | Y | Y | N | N | Y |
| | Multipurpose clock generator loss of lock (LOL) reset | Y[1] | Y[2] | Y[4] | Y[5] | Y | Y | N | N | Y |
| | Stop mode acknowledge error (SACKERR) | Y[1] | Y[2] | Y[4] | Y[5] | Y | Y | N | N | Y |
| | Software reset (SW) | Y[1] | Y[2] | Y[4] | Y[5] | Y | Y | N | N | Y |
| | Lockup reset (LOCKUP) | Y[1] | Y[2] | Y[4] | Y[5] | Y | Y | N | N | Y |

*Table continues on the next page...*

**Table 3. Reset source (continued)**

| Reset sources | Descriptions | Modules | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | PMC | SIM | SMC | RCM | LLWU | Reset pin is negated | RTC | LPTMR | Others |
| | MDM DAP system reset | Y[1] | Y[2] | Y[4] | Y[5] | Y | Y | N | N | Y |
| Debug reset | Debug reset | Y[1] | Y[2] | Y[4] | Y[5] | Y | Y | N | N | Y |

1. Except PMC_LVDSC1[LVDV] and PMC_LVDSC2[LVWV]
2. Except SIM_SOPT1
3. Only if $\overline{RESET}$ is used to wake from VLLS mode.
4. Except SMC_PMCTRL, SMC_STOPCTRL, SMC_PMSTAT
5. Except RCM_RPFC, RCM_RPFW, RCM_FM

This device supports booting from:
- internal flash

## 2.1.6 Clock options

The MCG module controls which clock source is used to derive the system clocks. The clock generation logic divides the selected clock source into a variety of clock domains, including the clocks for the system bus masters, system bus slaves, and flash memory . The clock generation logic also implements module-specific clock gating to allow granular shutoff of modules.

The primary clocks for the system are generated from the MCGOUTCLK clock. The clock generation circuitry provides several clock dividers that allow different portions of the device to be clocked at different frequencies. This allows for trade-offs between performance and power dissipation.

Various modules, such as the USB OTG Controller, have module-specific clocks that can be generated from the IRC48MCLK or MCGPLLCLK or MCGFLLCLK clock. In addition, there are various other module-specific clocks that have other alternate sources. Clock selection for most modules is controlled by the SOPT registers in the SIM module.

For more details on the clock operations and configurations, see the Clock Distribution chapter in the Reference Manual.

The following figure is a high level block diagram of the clock generation.

CG — Clock gate
**Note:** See subsequent sections for details on where these clocks are used.
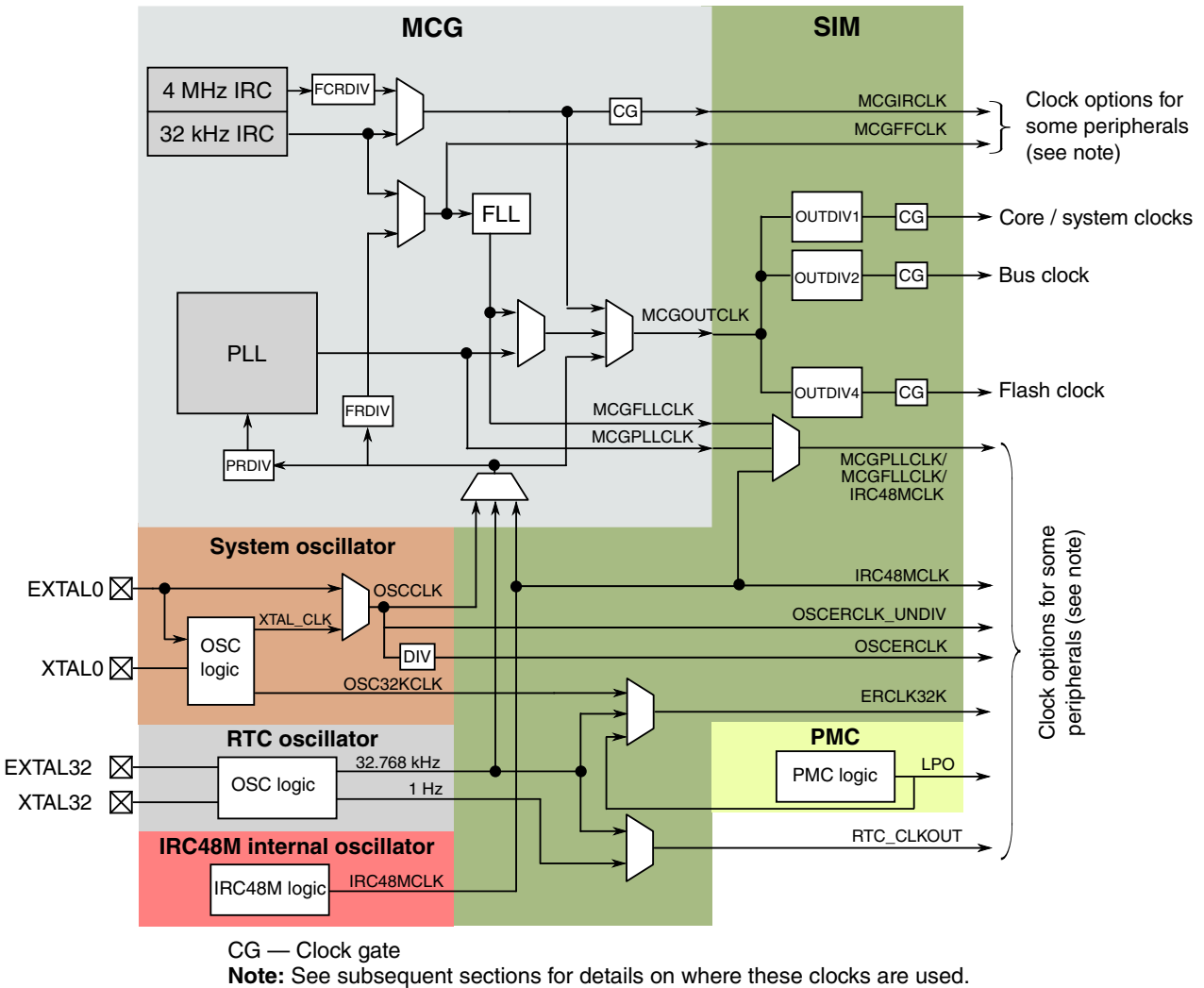
**Figure 3. Clock block diagram**

In order to provide flexibility, many peripherals can select the clock source to use for operation. This enables the peripheral to select a clock that will always be available during operation in various operational modes.

The following table summarizes the clocks associated with each module.

**Table 4.   Module clocks**

| Module | Bus interface clock | Internal clocks | I/O interface clocks |
|---|---|---|---|
| **Core modules** | | | |
| ARM Cortex-M4 core | System clock | Core clock | — |
| NVIC | System clock | — | — |
| DAP | System clock | — | — |

*Table continues on the next page...*

## Table 4. Module clocks (continued)

| Module | Bus interface clock | Internal clocks | I/O interface clocks |
|---|---|---|---|
| ITM | System clock | — | — |
| cJTAG, JTAGC | — | — | JTAG_CLK |
| **System modules** | | | |
| DMA | System clock | — | — |
| DMA Mux | Bus clock | — | — |
| Port control | Bus clock | LPO | — |
| Crossbar Switch | System clock | — | — |
| Peripheral bridges | System clock | Bus clock, Flash clock | — |
| LLWU, PMC, SIM, RCM | Flash clock | LPO | — |
| Mode controller | Flash clock | — | — |
| MCM | System clock | — | — |
| EWM | Bus clock | LPO | — |
| Watchdog timer | Bus clock | LPO | — |
| **Clocks** | | | |
| MCG | Flash clock | MCGOUTCLK, MCGPLLCLK, MCGFLLCLK, MCGIRCLK, OSCCLK, RTC OSC, IRC48MCLK | — |
| OSC | Bus clock | OSCERCLK, OSCCLK, OSCERCLK_UNDIV, OSC32KCLK | — |
| IRC48M | — | IRC48MCLK | — |
| **Memory and memory interfaces** | | | |
| Flash Controller | System clock | Flash clock | — |
| Flash memory | Flash clock | — | — |
| **Security** | | | |
| CRC | Bus clock | — | — |
| RNGA | Bus clock | — | — |
| **Analog** | | | |
| ADC | Bus clock | OSCERCLK , IRC48MCLK | — |
| CMP | Bus clock | — | — |
| DAC | Bus clock | — | — |
| **Timers** | | | |
| TPM | Bus clock | TPM clock | TPM_CLKIN0, TPM_CLKIN1 |
| PDB | Bus clock | — | — |
| PIT | Bus clock | — | — |
| LPTMR | Flash clock | LPO, OSCERCLK, MCGIRCLK, ERCLK32K | — |
| RTC | Flash clock | EXTAL32 | — |
| **Communication interfaces** | | | |

*Table continues on the next page...*

**Table 4. Module clocks (continued)**

| Module | Bus interface clock | Internal clocks | I/O interface clocks |
|---|---|---|---|
| USB FS OTG | System clock | USB FS clock | — |
| DSPI | Bus clock | — | DSPI_SCK |
| LPI$^2$C | Bus clock | LPI2C clock | I2C_SCL |
| UART0, UART1 | System clock | — | — |
| UART2 | Bus clock | — | — |
| LPUART0 | Bus clock | LPUART0 clock | — |
| I$^2$S | Bus clock | I$^2$S master clock | I2S_TX_BCLK, I2S_RX_BCLK |
| FlexCAN | Bus clock | FlexCAN clock | — |
| FlexIO | Bus clock | FlexIO clock | — |
| **Human-machine interfaces** | | | |
| GPIO | Platform clock | — | — |

## 2.1.7  Security

Security state can be enabled via programming flash configure field (0x40e). After enabling device security, the SWD/JTAG port cannot access the memory resources of the MCU.

| External interface | Security | Unsecure |
|---|---|---|
| SWD/JTAG port | Can't access memory source by SWD/JTAG interface | the debugger can write to the Flash Mass Erase in Progress field of the MDM-AP Control register to trigger a mass erase (Erase All Blocks) command |

## 2.1.7.1  Flash Access Control (FAC)

The FAC is a native or third-party configurable memory protection scheme optimized to allow end users to utilize software libraries while offering programmable restrictions to these libraries. The flash memory is divided into equal size segments that provide protection to proprietary software libraries. The protection of these segments is controlled as the FAC provides a cycle-by-cycle evaluation of the access rights for each transaction routed to the on-chip flash memory. Configurability allows an increasing number of protected segments while supporting two levels of vendors adding their proprietary software to a device.

## 2.1.8  Power management

The Power Management Controller (PMC) expands upon ARM's operational modes of Run, Sleep, and Deep Sleep, to provide multiple configurable modes. These modes can be used to optimize current consumption for a wide range of applications. The WFI or WFE instruction invokes a Wait or a Stop mode, depending on the current configuration. For more information on ARM's operational modes, See the ARM® Cortex® User Guide.

The PMC provides High Speed Run (HSRUN), Normal Run (RUN), and Very Low Power Run (VLPR) configurations in ARM's Run operation mode. In these modes, the MCU core is active and can access all peripherals. The difference between the modes is the maximum clock frequency of the system and therefore the power consumption. The configuration that matches the power versus performance requirements of the application can be selected.

The PMC provides Wait (Wait) and Very Low Power Wait (VLPW) configurations in ARM's Sleep operation mode. In these modes, even though the MCU core is inactive, all of the peripherals can be enabled and operate as programmed. The difference between the modes is the maximum clock frequency of the system and therefore the power consumption.

The PMC provides Stop (Stop), Very Low Power Stop (VLPS), Low Leakage Stop (LLS), and Very Low Leakage Stop (VLLS) configurations in ARM's Deep Sleep operational mode. In these modes, the MCU core and most of the peripherals are disabled. Depending on the requirements of the application, different portions of the analog, logic, and memory can be retained or disabled to conserve power.

The Battery Backup mode allows the VBAT voltage domain to operate while the rest of the device is disabled to conserve power. All modules in the VBAT domain are functional in this mode of operation.

The Nested Vectored Interrupt Controller (NVIC), the Asynchronous Wake-up Interrupt Controller (AWIC), and the Low Leakage Wake-Up Controller (LLWU) are used to wake up the MCU from low power states. The NVIC is used to wake up the MCU core from WAIT and VLPW modes. The AWIC is used to wake up the MCU core from STOP and VLPS modes. The LLWU is used to wake up the MCU core from LLS and VLLSx modes.

For additional information regarding operational modes, power management, the NVIC, AWIC, or the LLWU, please refer to the Reference Manual.

The following table provides information about the state of the peripherals in the various operational modes and the modules that can wake MCU from low power modes.

**Table 6.   Peripherals states in different operational modes**

| Core mode | Device mode | Descriptions |
|---|---|---|
| Run mode | High Speed Run | In HSRun mode, MCU is able to operate at a faster frequency, and all device modules are operational. |
| | Run | In Run mode, all device modules are operational. |
| | Very Low Power Run | In VLPR mode, all device modules are operational at a reduced frequency except the Low Voltage Detect (LVD) monitor, which is disabled. |
| Sleep mode | Wait | In Wait mode, all peripheral modules are operational. The MCU core is placed into Sleep mode. |
| | Very Low Power Wait | In VLPW mode, all peripheral modules are operational at a reduced frequency except the Low Voltage Detect (LVD) monitor, which is disabled. The MCU core is placed into Sleep mode. |
| Deep sleep | Stop | In Stop mode, most peripheral clocks are disabled and placed in a static state. Stop mode retains all registers and SRAMs while maintaining Low Voltage Detection protection. In Stop mode, the ADC, DAC, CMP, LPTMR, RTC, and pin interrupts are operational. The NVIC is disabled, but the AWIC can be used to wake up from an interrupt. |
| | Very Low Power Stop | In VLPS mode, the contents of the SRAM are retained. The CMP (low speed), ADC, OSC, RTC, LPTMR, TPM, FlexIO, LPUART, LPI2C,USB, and DMA are operational, LVD and NVIC are disabled, AWIC is used to wake up from interrupt. |
| | Low Leakage Stop (LLS3/LLS2) | State retention power mode. Most peripherals are in state retention mode (with clocks stopped), but LLWU, LPTimer, RTC, CMP, DAC can be used. NVIC is disabled; LLWU is used to wake up. <br><br>**NOTE:**  The LLWU interrupt must not be masked by the interrupt controller to avoid a scenario where the system does not fully exit stop mode on an LLS recovery. <br><br>In LLS3 mode, all SRAM is operating (content retained and I/O states held). In LLS2 mode, a portion of SRAM_U remains powered on (content retained and I/O states held). |
| | Very Low Leakage Stop (VLLSx) | Most peripherals are disabled (with clocks stopped), but LLWU, LPTimer, RTC, CMP, DAC can be used. NVIC is disabled; LLWU is used to wake up. <br><br>In VLLS3, SRAM_U and SRAM_L remain powered on (content retained and I/O states held). <br><br>In VLLS2, SRAM_L is powered off. A portion of SRAM_U remains powered on (content retained and I/O states held). <br><br>In VLLS1 and VLLS0, all of SRAM_U and SRAM_L are powered off. The 32-byte system register file and 32-byte VBAT register file remain powered for customer-critical data. <br><br>In VLLS0, The POR detect circuit can be optionally powered off. |
| Powered Off | Battery Backup | The RTC and 32-byte VBAT register file are powered from the VBAT domain and is fully functional. The rest of the device is powered down. |

## 2.1.9   LLWU

The LLWU module is used to wake MCU from low leakage power mode (LLS and VLLSx) and functional only on entry into a low-leakage power mode. After recovery from LLS, the LLWU is immediately disabled. After recovery from VLLSx, the LLWU continues to detect wake-up events until the user has acknowledged the wake-up event.

The following is internal peripheral and external pin inputs as wakeup sources to the LLWU module.

**Table 7.   Wakeup sources for LLWU inputs**

| Input | Wakeup source |
|---|---|
| LLWU_P0 | PTE1/LLWU_P0 pin |
| LLWU_P1 | PTE2/LLWU_P1 pin |
| LLWU_P2 | PTE4/LLWU_P2 pin |
| LLWU_P3 | PTA4/LLWU_P3 pin[1] |
| LLWU_P4 | PTA13/LLWU_P4 pin |
| LLWU_P5 | PTB0/LLWU_P5 pin |
| LLWU_P6 | PTC1/LLWU_P6 pin |
| LLWU_P7 | PTC3/LLWU_P7 pin |
| LLWU_P8 | PTC4/LLWU_P8 pin |
| LLWU_P9 | PTC5/LLWU_P9 pin |
| LLWU_P10 | PTC6/LLWU_P10 pin |
| LLWU_P11 | PTC11/LLWU_P11 pin |
| LLWU_P12 | PTD0/LLWU_P12 pin |
| LLWU_P13 | PTD2/LLWU_P13 pin |
| LLWU_P14 | PTD4/LLWU_P14 pin |
| LLWU_P15 | PTD6/LLWU_P15 pin |
| LLWU_P16 | Reserved |
| LLWU_P17 | Reserved |
| LLWU_P18 | Reserved |
| LLWU_P19 | Reserved |
| LLWU_P20 | Reserved |
| LLWU_P21 | Reserved |
| LLWU_P22 | Reserved |
| LLWU_P23 | Reserved |
| LLWU_P24 | Reserved |
| LLWU_P25 | Reserved |
| LLWU_P26 | USBVDD |

*Table continues on the next page...*

**Table 7.   Wakeup sources for LLWU inputs (continued)**

| Input | Wakeup source |
|---|---|
| LLWU_P27 | USB0_DP |
| LLWU_P28 | USB0_DM[2] |
| LLWU_P29 | Reserved |
| LLWU_P30 | Reserved |
| LLWU_P31 | Reserved |
| LLWU_M0IF | LPTMR[3] |
| LLWU_M1IF | CMP0 |
| LLWU_M2IF | Reserved |
| LLWU_M3IF | Reserved |
| LLWU_M4IF | Reserved |
| LLWU_M5IF | RTC Alarm[3] |
| LLWU_M6IF | Reserved |
| LLWU_M7IF | RTC Seconds[3] |

1. If NMI was enabled on entry to LLS/VLLS, asserting the NMI pin generates an NMI interrupt on exit from the low power mode. NMI can also be disabled via the FOPT[NMI_DIS] bit.
2. As a wakeup source of LLWU, USB0_DP and USB0_DM are only available when the chip is in USB host mode.
3. It requires the peripheral and the peripheral interrupt to be enabled. The LLWU's WUME bit enables the internal module flag as a wakeup input. After wakeup, the flags are cleared based on the peripheral clearing mechanism.

## 2.1.10   Debug controller

This device has extensive debug capabilities including run control and tracing capabilities. The standard ARM debug port supports SWD/JTAG interface. Also the cJTAG interface is supported on this device.

## 2.1.11   Computer operating properly (COP) watchdog timer

The computer operating properly (COP) watchdog timer (WDOG) monitors the operation of the system by expecting periodic communication from the software. This communication is generally known as servicing (or refreshing) the COP watchdog. If this periodic refreshing does not occur, the watchdog issues a system reset.

## 2.2   Peripheral features

The following sections describe the features of each peripherals of the chip.

## 2.2.1   eDMA and DMAMUX

The eDMA is a highly programmable data-transfer engine optimized to minimize any required intervention from the host processor. It is intended for use in applications where the data size to be transferred is statically known and not defined within the transferred data itself. The DMA controller in this device implements 16 channels which can be routed from up to 63 DMA request sources through DMA MUX module.

Main features of eDMA are listed below:
- All data movement via dual-address transfers: read from source, write to destination
- 16-channel implementation that performs complex data transfers with minimal intervention from a host processor
- Transfer control descriptor (TCD) organized to support two-deep, nested transfer operations
- Channel activation via one of three methods
- Fixed-priority and round-robin channel arbitration
- Channel completion reported via programmable interrupt requests
- Programmable support for scatter/gather DMA processing
- Support for complex data structures

## 2.2.2   TPM

This device contains three low power Timer/PWM Modules (TPM), one with 6 channels and the other two with 2 channels. All TPM modules are functional in Stop/VLPS mode if the clock source is enabled.

The TPM features are as follows:
- TPM clock mode is selectable (can increment on every edge of the asynchronous counter clock, or only on on rising edge of an external clock input synchronized to the asynchronous counter clock)
- Prescaler divide-by 1, 2, 4, 8, 16, 32, 64, or 128
- Include a 16-bit counter
- Include 6 or 2 channels (1×6ch, 2×2ch) that can be configured for input capture, output compare, edge-aligned PWM mode, or center-aligned PWM mode
- Support the generation of an interrupt and/or DMA request per channel or counter overflow

- Support selectable trigger input to optionally reset or cause the counter to start or stop incrementing
- Support the generation of hardware triggers when the counter overflows and per channel

## 2.2.3  ADC

This device contains one ADC module. This ADC module supports hardware triggers from TPM, LPTMR, PIT, RTC, external trigger pin and CMP output. It supports wakeup of MCU in low power mode when using internal clock source or external crystal clock.

ADC module has the following features:
- Linear successive approximation algorithm with up to 16-bit resolution
- Up to four pairs of differential and 17 single-ended external analog inputs
- Support selectable 16-bit, 13-bit, 11-bit, and 9-bit differential output mode, or 16-bit, 12-bit, 10-bit, and 8-bit single-ended output modes
- Single or continuous conversion
- Configurable sample time and conversion speed/power
- Selectable clock source up to three
- Operation in low-power modes for lower noise
- Asynchronous clock source for lower noise operation with option to output the clock
- Selectable hardware conversion trigger
- Automatic compare with interrupt for less-than, greater-than or equal-to, within range, or out-of-range, programmable value
- Temperature sensor
- Hardware average function up to 32×
- Voltage reference: from external
- Self-calibration mode

### 2.2.3.1  Temperature sensor

This device contains one temperature sensor internally connected to the input channel of AD26, see Table 66 for details of the linearity factor.

The sensor must be calibrated to gain good accuracy, so as to provide good linearity, see also AN3031.

## 2.2.4 DAC

The 12-bit digital-to-analog converter (DAC) is a low-power, general-purpose DAC. The output of the DAC can be placed on an external pin or set as one of the inputs to the analog comparator, or ADC.

DAC module has the following features:
- On-chip programmable reference generator output. The voltage output range is from $1/4096 \, V_{in}$ to $V_{in}$, and the step is $1/4096 \, V_{in}$, where $V_{in}$ is the input voltage.
- $V_{in}$ can be selected from the reference source $V_{DDA}$
- Static operation in Normal Stop mode
- 16-word data buffer supported with multiple operation modes
- DMA support

## 2.2.5 CMP

The device contains one high-speed comparator and two 8-input multiplexers for both the inverting and non-inverting inputs of the comparator. Each CMP input channel connects to both muxes.

The CMP includes one 6-bit DAC, which provides a selectable voltage reference for various user application cases. Besides, the CMP also has several module-to-module interconnects in order to facilitate ADC triggering, TPM triggering, and interfaces.

The CMP has the following features:
- Inputs may range from rail to rail
- Programmable hysteresis control
- Selectable interrupt on rising-edge, falling-edge, or both rising or falling edges of the comparator output
- Selectable inversion on comparator output
- Capability to produce a wide range of outputs such as sampled, digitally filtered
- External hysteresis can be used at the same time that the output filter is used for internal functions
- Two software selectable performance levels: shorter propagation delay at the expense of higher power and Low power with longer propagation delay
- DMA transfer support
- Functional in all modes of operation except in VLLS0 mode
- The filter functions are not available in Stop, VLPS, LLS, or VLLSx modes
- Integrated 6-bit DAC with selectable supply reference source and can be power down to conserve power
- Two 8-to-1 channel mux

## 2.2.6  RTC

The RTC is an always powered-on block that remains active in all low power modes. The time counter within the RTC is clocked by a 32.768 kHz clock sourced from an external crystal using the RTC oscillator.

RTC is reset on power-on reset, and a software reset bit in RTC can also initialize all RTC registers.

The RTC module has the following features
  • 32-bit seconds counter with roll-over protection and 32-bit alarm
  • 16-bit prescaler with compensation that can correct errors between 0.12 ppm and 3906 ppm
  • Register write protection with register lock mechanism
  • 1 Hz square wave or second pulse output with optional interrupt

## 2.2.7  PIT

The Periodic Interrupt Timer (PIT) is used to generate periodic interrupt to the CPU. It has four independent channels and each channel has a 32-bit counter. Both channels can be chained together to form a 64-bit counter.

Channel 0 can be used to periodically trigger DMA channel 0, and channel 1 can be used to periodically trigger DMA channel 1. Either channel can be programmed as an ADC trigger source, or TPM trigger source. Channel 0 can be programmed to trigger DAC.

The PIT module has the following features:
  • Each 32-bit timers is able to generate DMA trigger
  • Each 32-bit timers is able to generate timeout interrupts
  • Two timers can be cascaded to form a 64-bit timer
  • Each timer can be programmed as ADC/TPM trigger source

## 2.2.8  PDB

The Programmable Delay Block (PDB) provides controllable delays from either an internal or an external trigger, or a programmable interval tick, to the hardware trigger inputs of ADCs and/or generates the interval triggers to DACs, so that the precise

timing between ADC conversions and/or DAC updates can be achieved. The PDB can optionally provide pulse outputs (Pulse-Out's) that are used as the sample window in the CMP block.

The PIT module has the following features:
- Up to 15 trigger input sources and one software trigger source
- Up to 8 configurable PDB channels for ADC hardware trigger
- Up to 8 pulse outputs (pulse-out's)

## 2.2.9  LPTMR

The low-power timer (LPTMR) can be configured to operate as a time counter with optional prescaler, or as a pulse counter with optional glitch filter, across all power modes, including the low-leakage modes. It can also continue operating through most system reset events, allowing it to be used as a time of day counter.

The LPTMR module has the following features:
- 16-bit time counter or pulse counter with compare
    - Optional interrupt can generate asynchronous wakeup from any low-power mode
    - Hardware trigger output
    - Counter supports free-running mode or reset on compare
- Configurable clock source for prescaler/glitch filter
- Configurable input source for pulse counter

## 2.2.10  CRC

This device contains one cyclic redundancy check (CRC) module which can generate 16/32-bit CRC code for error detection.

The CRC module provides a programmable polynomial, WAS, and other parameters required to implement a 16-bit or 32-bit CRC standard.

The CRC module has the following features:
- Hardware CRC generator circuit using a 16-bit or 32-bit programmable shift register
- Programmable initial seed value and polynomial
- Option to transpose input data or output data (the CRC result) bitwise or bytewise.
- Option for inversion of final CRC result
- 32-bit CPU register programming interface

## 2.2.11  UART

This device contains 3 basic universal asynchronous receiver/transmitter (UART) modules with DMA function supported. Generally, this module is used in RS-232, RS-485, and other communications. It also supports LIN slave operation and ISO7816.

The UART module has the following features:
- Full-duplex operation
- 13-bit baud rate selection with /32 fractional divide, based on the module clock frequency
- Programmable 8-bit or 9-bit data format
- Programmable transmitter output polarity
- Programmable receive input polarity
- Up to 14-bit break character transmission.
- 11-bit break character detection option
- Two receiver wakeup methods with idle line or address mark wakeup
- Address match feature in the receiver to reduce address mark wakeup ISR overhead
- Ability to select MSB or LSB to be the first bit on wire
- UART0 supporting ISO-7816 protocol to interface with SIM cards and smart cards
- Receiver framing error detection
- Hardware parity generation and checking
- 1/16 bit-time noise detection
- DMA interface

## 2.2.12  LPUART

This device contains one Low-Power UART module, and can work in Stop and VLPS modes. The module also supports 4× to 32× data oversampling rate to meet different applications.

The LPUART module has the following features:
- Programmable baud rates (13-bit modulo divider) with configurable oversampling ratio from 4× to 32×
- Transmit and receive baud rate can operate asynchronous to the bus clock and can be configured independently of the bus clock frequency, support operation in Stop mode

- Interrupt, DMA or polled operation
- Hardware parity generation and checking
- Programmable 8-bit, 9-bit or 10-bit character length
- Programmable 1-bit or 2-bit stop bits
- Three receiver wakeup methods
  - Idle line wakeup
  - Address mark wakeup
  - Receive data match
- Automatic address matching to reduce ISR overhead:
  - Address mark matching
  - Idle line address matching
  - Address match start, address match end
- Optional 13-bit break character generation / 11-bit break character detection
- Configurable idle length detection supporting 1, 2, 4, 8, 16, 32, 64 or 128 idle characters
- Selectable transmitter output and receiver input polarity

## 2.2.13 SPI

This device contains two SPI modules. The SPI module provides a synchronous serial bus for communication between a chip and an external peripheral device.

The SPI modules have the following features:
- Full-duplex, three-wire synchronous transfers
- Master mode, or slave mode
- Data streaming operation in Slave mode with continuous slave selection
- Buffered transmit/receive operation using the transmit/receive first in first out (TX/RX FIFO) with depth of 4 entries
- Programmable transfer attributes on a per-frame basis
- Multiple peripheral chip select (PCS) (6 PCS available for SPI0 and 4 PCS for SPI1), expandable to 64 with external demultiplexer
- Deglitching support for up to 32 peripheral chip selects (PCSes) with external demultiplexer
- DMA support for adding entries to TX FIFO and removing entries from RX FIFO
- Global interrupt request line
- Modified SPI transfer formats for communication with slower peripheral devices
- Power-saving architectural features

## 2.2.14 FlexCAN

For KS22, the device contains two FlexCAN modules. For KS20, it has only one FlexCAN module. The FlexCAN module is a communication controller implementing the CAN protocol according to the ISO 11898-1 standard and CAN 2.0 B protocol specifications.

The FlexCAN module contains 16 message buffers. Each message buffer is 16 bytes.

The FlexCAN module has the following features:
- Flexible mailboxes of zero to eight bytes data length
- Each mailbox configurable as receive or transmit, all supporting standard and extended messages
- Individual Rx Mask registers per mailbox
- Full-featured Rx FIFO with storage capacity for up to six frames and automatic internal pointer handling with DMA support
- Transmission abort capability
- Programmable clock source to the CAN Protocol Interface, either peripheral clock or oscillator clock
- RAM not used by reception or transmission structures can be used as general purpose RAM space
- Listen-Only mode capability
- Programmable Loop-Back mode supporting self-test operation
- Programmable transmission priority scheme: lowest ID, lowest buffer number, or highest priority
- Time stamp based on 16-bit free-running timer
- Global network time, synchronized by a specific message
- Maskable interrupts
- Independence from the transmission medium (an external transceiver is assumed)
- Short latency time due to an arbitration scheme for high-priority messages
- Low power modes, with programmable wake up on bus activity
- Remote request frames may be handled automatically or by software
- CAN bit time settings and configuration bits can only be written in Freeze mode
- Tx mailbox status (Lowest priority buffer or empty buffer)
- Identifier Acceptance Filter Hit Indicator (IDHIT) register for received frames
- SYNCH bit available in Error in Status 1 register to inform that the module is synchronous with CAN bus
- CRC status for transmitted message
- Rx FIFO Global Mask register

- Selectable priority between mailboxes and Rx FIFO during matching process
- Powerful Rx FIFO ID filtering, capable of matching incoming IDs against either 128 extended, 256 standard, or 512 partial (8 bit) IDs, with up to 32 individual masking capability

## 2.2.15  LPI2C

This device contains two LPI2C modules. The LPI2C is a low power Inter-Integrated Circuit (I2C) module that supports an efficient interface to an I2C bus as a master and/or a slave. The LPI2C can continue operating in stop modes provided an appropriate clock is available and is designed for low CPU overhead with DMA offloading of FIFO register accesses. The LPI2C implements logic support for standard-mode, fast-mode, fast-mode plus and ultra-fast modes of operation. The LPI2C module also complies with the *System Management Bus (SMBus) Specification, version 2*.

The LPI2C modules have the following features:
- Standard, Fast, Fast+ and Ultra Fast modes are supported
- HS-mode supported in slave mode
- Multi-master support including synchronization and arbitration
- Clock stretching
- General call, 7-bit and 10-bit addressing
- Software reset, START byte and Device ID require software support
- For master mode:
    - command/transmit FIFO of 4 words
    - receive FIFO of 4 words
- For slave mode:
    - separate I2C slave registers to minimize software overhead due to master/slave switching
    - support for 7-bit or 10-bit addressing, address range, SMBus alert and general call address
    - transmit/receive data register supporting interrupt or DMA requests

## 2.2.16  USB

This device contains one USB module which implements a USB2.0 full-speed compliant peripheral and interfaces to the on-chip USBFS transceiver. It enables IRC48M to allow crystal-less USB operation.

The USBFS has the following features:

- USB 1.1 and 2.0 compliant full-speed device controller
- 16 bidirectional end points
- DMA or FIFO data stream interfaces
- Low-power consumption
- IRC48M with clock-recovery is supported to eliminate the 48 MHz crystal. It is used for USB device-only implementation.

### 2.2.17   I2S

The I2S module provides a synchronous audio interface (SAI), which can be clocked by bus clock, PLL/FLL output clock or external oscillator clock. The module supports asynchronous bit clocks (BCLKs) that can be generated internally from the audio master clock or supplied externally. And also supports the option for synchronous operation between the receiver and transmitter. And it can be functional in stop or very low power mode.

I2S module has the following features:
- Transmitter with independent bit clock and frame sync supporting 1 data channel
- Receiver with independent bit clock and frame sync supporting 1 data channel
- Maximum frame size of 16 words
- Word size of between 8-bits and 32-bits
- Word size configured separately for first word and remaining words in frame
- Asynchronous 8 × 32-bit FIFO for each transmit and receive channels
- Supports graceful restart after FIFO error
- Supports automatic restart after FIFO error without software intervention
- Supports packing of 8-bit and 16-bit data into each 32-bit FIFO word

### 2.2.18   FlexIO

The FlexIO is a highly configurable module providing a wide range of protocols including, but not limited to UART, I2C, SPI, I2S, and PWM/Waveform generation. The module supports programmable baud rates independent of bus clock frequency, with automatic start/stop bit generation.

The FlexIO module has the following features:
- Functional in VLPR/VLPW/Stop/VLPS mode provided the clock it is using remains enabled
- Four 32-bit double buffered shift registers with transmit, receive, and data match modes, and continuous data transfer

- The timing of the shifter's shift, load and store events are controlled by the highly flexible 16-bit timer assigned to the shifter
- Two or more shifters can be concatenated to support large data transfer sizes
- Each 16-bit timers operates independently, supports for reset, enable and disable on a variety of internal or external trigger conditions with programmable trigger polarity
- Flexible pin configuration supporting output disabled, open drain, bidirectional output data and output mode
- Supports interrupt, DMA or polled transmit/receive operation

## 2.2.19  Port control and GPIO

The Port Control and Interrupt (PORT) module provides support for port control, digital filtering, and external interrupt functions. The GPIO data direction and output data registers control the direction and output data of each pin when the pin is configured for the GPIO function. The GPIO input data register displays the logic value on each pin when the pin is configured for any digital function, provided the corresponding Port Control and Interrupt module for that pin is enabled.

The following figure shows the basic I/O pad structure. This diagram applies to all I/O pins except RESET_b and those configured as pseudo open-drain outputs. RESET_b is a true open-drain pin without p-channel output driver or diode to the ESD bus. Pseudo open-drain pins have the p-channel output driver disabled when configured for open-drain operation. None of the I/O pins, including open-drain and pseudo open-drain pins, are allowed to go above VDD.
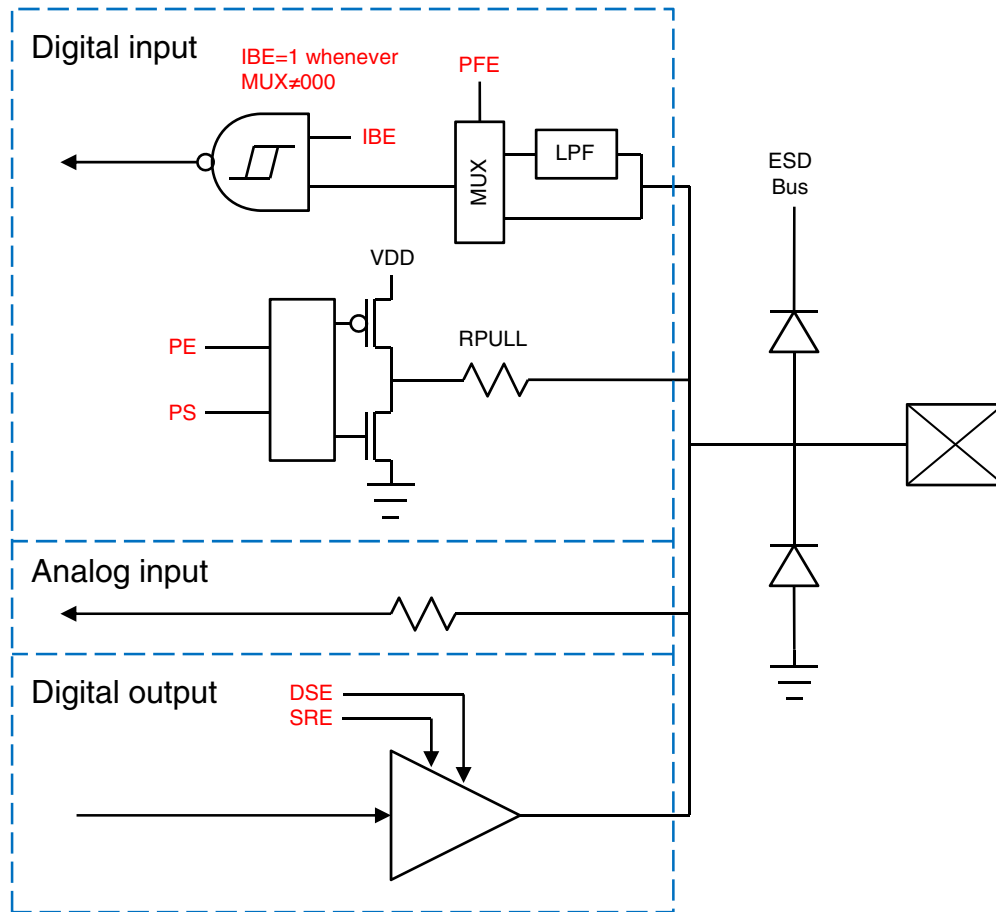
**Figure 4. I/O simplified block diagram**

The PORT module has the following features:
- all PIN support interrupt enable
- Configurable edge (rising, falling, or both) or level sensitive interrupt type
- Support DMA request
- Asynchronous wake-up in low-power modes
- Configurable pullup, pulldown, and pull-disable on select pins
- Configurable high and low drive strength on selected pins
- Configurable fast and slow slew rates on selected pins
- Configurable passive filter on selected pins
- Individual mux control field supporting analog or pin disabled, GPIO, and up to chip-specific digital functions
- Pad configuration fields are functional in all digital pin muxing modes.

The GPIO module has the following features:
- Port Data Input register visible in all digital pin-multiplexing modes
- Port Data Output register with corresponding set/clear/toggle registers

- Port Data Direction register
- GPIO support single-cycle access via fast GPIO.

# 3 Memory map

This device contains various memories and memory-mapped peripherals which are located in a 4 GB memory space. For more details of the system memory and peripheral locations, see the Memory Map chapter in the Reference Manual.
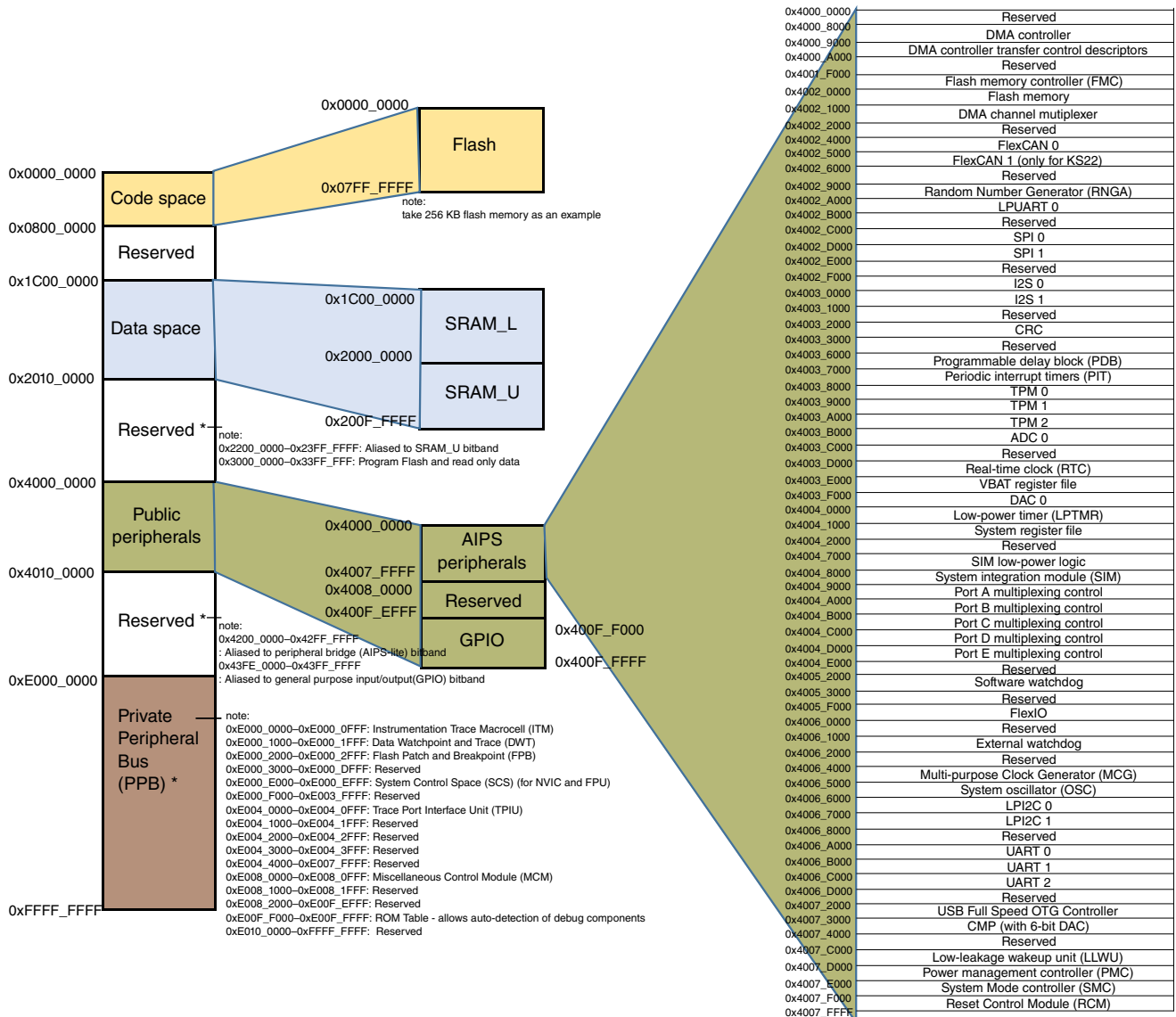


**Figure 5. Memory map**

# 4  Pinouts

## 4.1  Signal Multiplexing and Pin Assignments

The following table shows the signals available on each pin and the locations of these pins on the devices supported by this document. The Port Control Module is responsible for selecting which ALT functionality is available on each pin.

**NOTE**
For KS20, only CAN0 exists. For KS22, there are two instances of CAN module (CAN0 and CAN1).

| 100 LQFP | 64 LQFP | 48 QFN | Pin Name | Default | ALT0 | ALT1 | ALT2 | ALT3 | ALT4 | ALT5 | ALT6 | ALT7 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 1 | 1 | 1 | PTE0/ CLKOUT32K | ADC0_SE4a | ADC0_SE4a | PTE0/ CLKOUT32K | SPI1_PCS1 | UART1_TX | | | LPI2C1_SDA | RTC_ CLKOUT |
| 2 | 2 | 2 | PTE1/ LLWU_P0 | ADC0_SE5a | ADC0_SE5a | PTE1/ LLWU_P0 | SPI1_SOUT | UART1_RX | | | LPI2C1_SCL | SPI1_SIN |
| 3 | — | 3 | PTE2/ LLWU_P1 | ADC0_SE6a | ADC0_SE6a | PTE2/ LLWU_P1 | SPI1_SCK | UART1_ CTS_b | | | | |
| 4 | — | 4 | PTE3 | ADC0_SE7a | ADC0_SE7a | PTE3 | SPI1_SIN | UART1_ RTS_b | | | | SPI1_SOUT |
| 5 | — | 5 | PTE4/ LLWU_P2 | DISABLED | | PTE4/ LLWU_P2 | SPI1_PCS0 | LPUART0_ TX | | | | LPI2C1_SDA |
| 6 | — | 6 | PTE5 | DISABLED | | PTE5 | SPI1_PCS2 | LPUART0_ RX | | | | LPI2C1_SCL |
| 7 | — | — | PTE6 | DISABLED | | PTE6 | SPI1_PCS3 | LPUART0_ CTS_b | I2S0_MCLK | | | USB_SOF_ OUT |
| 8 | 3 | 7 | VDD | VDD | VDD | | | | | | | |
| 9 | 4 | 8 | VSS | VSS | VSS | | | | | | | |
| 10 | 5 | 9 | USB0_DP | USB0_DP | USB0_DP | | | | | | | |
| 11 | 6 | 10 | USB0_DM | USB0_DM | USB0_DM | | | | | | | |
| 12 | 7 | 11 | USBVDD | USBVDD | USBVDD | | | | | | | |
| 13 | — | — | NC | NC | NC | | | | | | | |
| 14 | 8 | — | ADC0_DP1 | ADC0_DP1 | ADC0_DP1 | | | | | | | |
| 15 | — | — | ADC0_DM1 | ADC0_DM1 | ADC0_DM1 | | | | | | | |
| 16 | — | — | ADC0_DP2 | ADC0_DP2 | ADC0_DP2 | | | | | | | |
| 17 | — | — | ADC0_DM2 | ADC0_DM2 | ADC0_DM2 | | | | | | | |
| 18 | 9 | — | ADC0_DP0 | ADC0_DP0 | ADC0_DP0 | | | | | | | |
| 19 | 10 | — | ADC0_DM0 | ADC0_DM0 | ADC0_DM0 | | | | | | | |
| 20 | 11 | — | ADC0_DP3 | ADC0_DP3 | ADC0_DP3 | | | | | | | |

| 100 LQFP | 64 LQFP | 48 QFN | Pin Name | Default | ALT0 | ALT1 | ALT2 | ALT3 | ALT4 | ALT5 | ALT6 | ALT7 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 21 | 12 | — | ADC0_DM3 | ADC0_DM3 | ADC0_DM3 | | | | | | | |
| 22 | 13 | 12 | VDDA | VDDA | VDDA | | | | | | | |
| 23 | 14 | 12 | VREFH | VREFH | VREFH | | | | | | | |
| 24 | 15 | 13 | VREFL | VREFL | VREFL | | | | | | | |
| 25 | 16 | 13 | VSSA | VSSA | VSSA | | | | | | | |
| 26 | 17 | — | CMP0_IN5 | CMP0_IN5 | CMP0_IN5 | | | | | | | |
| 27 | 18 | — | DAC0_OUT/ ADC0_SE23 | DAC0_OUT/ ADC0_SE23 | DAC0_OUT/ ADC0_SE23 | | | | | | | |
| 28 | 19 | 14 | XTAL32 | XTAL32 | XTAL32 | | | | | | | |
| 29 | 20 | 15 | EXTAL32 | EXTAL32 | EXTAL32 | | | | | | | |
| 30 | 21 | 16 | VBAT | VBAT | VBAT | | | | | | | |
| 31 | — | — | PTE24 | ADC0_SE17 | ADC0_SE17 | PTE24 | CAN1_TX | TPM0_CH0 | I2S1_TX_FS | LPI2C0_SCL | EWM_OUT_b | |
| 32 | — | — | PTE25 | ADC0_SE18 | ADC0_SE18 | PTE25 | CAN1_RX | TPM0_CH1 | I2S1_TX_ BCLK | LPI2C0_SDA | EWM_IN | |
| 33 | — | — | PTE26/ CLKOUT32K | DISABLED | | PTE26/ CLKOUT32K | | | I2S1_TXD0 | | RTC_ CLKOUT | USB_CLKIN |
| 34 | 22 | 17 | PTA0 | JTAG_TCLK/ SWD_CLK | | PTA0 | UART0_ CTS_b | TPM0_CH5 | | EWM_IN | | JTAG_TCLK/ SWD_CLK |
| 35 | 23 | 18 | PTA1 | JTAG_TDI | | PTA1 | UART0_RX | | CMP0_OUT | LPI2C1_ HREQ | TPM1_CH1 | JTAG_TDI |
| 36 | 24 | 19 | PTA2 | JTAG_TDO/ TRACE_ SWO | | PTA2 | UART0_TX | | | | TPM1_CH0 | JTAG_TDO/ TRACE_ SWO |
| 37 | 25 | 20 | PTA3 | JTAG_TMS/ SWD_DIO | | PTA3 | UART0_ RTS_b | TPM0_CH0 | | EWM_OUT_b | | JTAG_TMS/ SWD_DIO |
| 38 | 26 | 21 | PTA4/ LLWU_P3 | NMI_b | | PTA4/ LLWU_P3 | | TPM0_CH1 | | | I2S0_MCLK | NMI_b |
| 39 | 27 | — | PTA5 | DISABLED | | PTA5 | USB_CLKIN | TPM0_CH2 | | | I2S0_TX_ BCLK | JTAG_TRST_ b |
| 40 | — | — | VDD | VDD | VDD | | | | | | | |
| 41 | — | — | VSS | VSS | VSS | | | | | | | |
| 42 | 28 | — | PTA12 | DISABLED | | PTA12 | CAN0_TX | TPM1_CH0 | | | I2S0_TXD0 | |
| 43 | 29 | — | PTA13/ LLWU_P4 | DISABLED | | PTA13/ LLWU_P4 | CAN0_RX | TPM1_CH1 | | | I2S0_TX_FS | |
| 44 | — | — | PTA14 | DISABLED | | PTA14 | SPI0_PCS0 | UART0_TX | | | I2S0_RX_ BCLK | |
| 45 | — | — | PTA15 | DISABLED | | PTA15 | SPI0_SCK | UART0_RX | | | I2S0_RXD0 | |
| 46 | — | — | PTA16 | DISABLED | | PTA16 | SPI0_SOUT | UART0_ CTS_b | | | I2S0_RX_FS | |
| 47 | — | — | PTA17 | DISABLED | | PTA17 | SPI0_SIN | UART0_ RTS_b | | | I2S0_MCLK | |
| 48 | 30 | 22 | VDD | VDD | VDD | | | | | | | |
| 49 | 31 | 23 | VSS | VSS | VSS | | | | | | | |
| 50 | 32 | 24 | PTA18 | EXTAL0 | EXTAL0 | PTA18 | | | TPM_CLKIN0 | | | |

| 100 LQFP | 64 LQFP | 48 QFN | Pin Name | Default | ALT0 | ALT1 | ALT2 | ALT3 | ALT4 | ALT5 | ALT6 | ALT7 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 51 | 33 | 25 | PTA19 | XTAL0 | XTAL0 | PTA19 | | | TPM_CLKIN1 | | LPTMR0_ALT1 | |
| 52 | 34 | 26 | RESET_b | RESET_b | RESET_b | | | | | | | |
| 53 | 35 | 27 | PTB0/ LLWU_P5 | ADC0_SE8 | ADC0_SE8 | PTB0/ LLWU_P5 | LPI2C0_SCL | TPM1_CH0 | | | FXIO0_D4 | UART0_RX |
| 54 | 36 | 28 | PTB1 | ADC0_SE9 | ADC0_SE9 | PTB1 | LPI2C0_SDA | TPM1_CH1 | | EWM_IN | FXIO0_D5 | UART0_TX |
| 55 | 37 | 29 | PTB2 | ADC0_SE12 | ADC0_SE12 | PTB2 | LPI2C0_SCL | UART0_RTS_b | | | FXIO0_D6 | CAN1_RX |
| 56 | 38 | 30 | PTB3 | ADC0_SE13 | ADC0_SE13 | PTB3 | LPI2C0_SDA | UART0_CTS_b | | | FXIO0_D7 | CAN1_TX |
| 57 | — | — | PTB9 | DISABLED | | PTB9 | SPI1_PCS1 | LPUART0_CTS_b | | | | |
| 58 | — | — | PTB10 | DISABLED | | PTB10 | SPI1_PCS0 | LPUART0_RX | I2S1_TX_BCLK | | | |
| 59 | — | — | PTB11 | DISABLED | | PTB11 | SPI1_SCK | LPUART0_TX | I2S1_TX_FS | | | |
| 60 | — | — | VSS | VSS | VSS | | | | | | | |
| 61 | — | — | VDD | VDD | VDD | | | | | | | |
| 62 | 39 | 31 | PTB16 | DISABLED | | PTB16 | SPI1_SOUT | UART0_RX | TPM_CLKIN0 | | EWM_IN | I2S1_TXD0 (Note: 100LQFP only) |
| 63 | 40 | — | PTB17 | DISABLED | | PTB17 | SPI1_SIN | UART0_TX | TPM_CLKIN1 | | EWM_OUT_b | FXIO0_D0 |
| 64 | 41 | 32 | PTB18 | DISABLED | | PTB18 | CAN0_TX | TPM2_CH0 | I2S0_TX_BCLK | | | FXIO0_D1 |
| 65 | 42 | 33 | PTB19 | DISABLED | | PTB19 | CAN0_RX | TPM2_CH1 | I2S0_TX_FS | | | FXIO0_D2 |
| 66 | — | — | PTB20 | DISABLED | | PTB20 | | | | | CMP0_OUT | FXIO0_D4 |
| 67 | — | — | PTB21 | DISABLED | | PTB21 | | | | | FXIO0_D5 | |
| 68 | — | — | PTB22 | DISABLED | | PTB22 | | | | | FXIO0_D6 | |
| 69 | — | — | PTB23 | DISABLED | | PTB23 | | SPI0_PCS5 | | | FXIO0_D7 | |
| 70 | 43 | — | PTC0 | ADC0_SE14 | ADC0_SE14 | PTC0 | SPI0_PCS4 | PDB0_EXTRG | USB_SOF_OUT | | FXIO0_D3 | SPI0_PCS0 |
| 71 | 44 | 34 | PTC1/ LLWU_P6 | ADC0_SE15 | ADC0_SE15 | PTC1/ LLWU_P6 | SPI0_PCS3 | UART1_RTS_b | TPM0_CH0 | | I2S0_TXD0 | LPUART0_RTS_b |
| 72 | 45 | 35 | PTC2 | ADC0_SE4b | ADC0_SE4b | PTC2 | SPI0_PCS2 | UART1_CTS_b | TPM0_CH1 | | I2S0_TX_FS | LPUART0_CTS_b |
| 73 | 46 | 36 | PTC3/ LLWU_P7 | DISABLED | | PTC3/ LLWU_P7 | SPI0_PCS1 | UART1_RX | TPM0_CH2 | CLKOUT | I2S0_TX_BCLK | LPUART0_RX |
| 74 | 47 | — | VSS | VSS | VSS | | | | | | | |
| 75 | 48 | — | VDD | VDD | VDD | | | | | | | |
| 76 | 49 | 37 | PTC4/ LLWU_P8 | DISABLED | | PTC4/ LLWU_P8 | SPI0_PCS0 | UART1_TX | TPM0_CH3 | | LPI2C0_HREQ | LPUART0_TX |
| 77 | 50 | 38 | PTC5/ LLWU_P9 | DISABLED | | PTC5/ LLWU_P9 | SPI0_SCK | LPTMR0_ALT2 | I2S0_RXD0 | | CMP0_OUT | TPM0_CH2 |

| 100 LQFP | 64 LQFP | 48 QFN | Pin Name | Default | ALT0 | ALT1 | ALT2 | ALT3 | ALT4 | ALT5 | ALT6 | ALT7 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 78 | 51 | 39 | PTC6/ LLWU_P10 | CMP0_IN0 | CMP0_IN0 | PTC6/ LLWU_P10 | SPI0_SOUT | PDB0_ EXTRG | I2S0_RX_ BCLK | | I2S0_MCLK | LPI2C0_SCL |
| 79 | 52 | 40 | PTC7 | CMP0_IN1 | CMP0_IN1 | PTC7 | SPI0_SIN | USB_SOF_ OUT | I2S0_RX_FS | | | LPI2C0_SDA |
| 80 | 53 | — | PTC8 | CMP0_IN2 | CMP0_IN2 | PTC8 | LPI2C0_ SCLS | | I2S0_MCLK | | FXIO0_D0 | I2S1_RXD0 |
| 81 | 54 | — | PTC9 | CMP0_IN3 | CMP0_IN3 | PTC9 | LPI2C0_ SDAS | | I2S0_RX_ BCLK | | FXIO0_D1 | I2S1_RX_ BCLK |
| 82 | 55 | — | PTC10 | DISABLED | | PTC10 | LPI2C1_SCL | | I2S0_RX_FS | | FXIO0_D2 | I2S1_RX_FS |
| 83 | 56 | — | PTC11/ LLWU_P11 | DISABLED | | PTC11/ LLWU_P11 | LPI2C1_SDA | | | | FXIO0_D3 | I2S1_MCLK |
| 84 | — | — | PTC12 | DISABLED | | PTC12 | LPI2C1_ SCLS | | TPM_CLKIN0 | | | FXIO0_D0 |
| 85 | — | — | PTC13 | DISABLED | | PTC13 | LPI2C1_ SDAS | | TPM_CLKIN1 | | | FXIO0_D1 |
| 86 | — | — | PTC14 | DISABLED | | PTC14 | | | LPUART0_ RTS_b | | | FXIO0_D2 |
| 87 | — | — | PTC15 | DISABLED | | PTC15 | | | LPUART0_ CTS_b | | | FXIO0_D3 |
| 88 | — | — | VSS | VSS | VSS | | | | | | | |
| 89 | — | — | VDD | VDD | VDD | | | | | | | |
| 90 | — | — | PTC16 | DISABLED | | PTC16 | CAN1_RX | LPUART0_ RX | | | | FXIO0_D4 |
| 91 | — | — | PTC17 | DISABLED | | PTC17 | CAN1_TX | LPUART0_ TX | | | | FXIO0_D5 |
| 92 | — | — | PTC18 | DISABLED | | PTC18 | | LPUART0_ RTS_b | | | | |
| 93 | 57 | 41 | PTD0/ LLWU_P12 | DISABLED | | PTD0/ LLWU_P12 | SPI0_PCS0 | UART2_ RTS_b | | | LPUART0_ RTS_b | FXIO0_D6 |
| 94 | 58 | 42 | PTD1 | ADC0_SE5b | ADC0_SE5b | PTD1 | SPI0_SCK | UART2_ CTS_b | | | LPUART0_ CTS_b | FXIO0_D7 |
| 95 | 59 | 43 | PTD2/ LLWU_P13 | DISABLED | | PTD2/ LLWU_P13 | SPI0_SOUT | UART2_RX | | | LPUART0_ RX | LPI2C0_SCL |
| 96 | 60 | 44 | PTD3 | DISABLED | | PTD3 | SPI0_SIN | UART2_TX | | | LPUART0_ TX | LPI2C0_SDA |
| 97 | 61 | 45 | PTD4/ LLWU_P14 | DISABLED | | PTD4/ LLWU_P14 | SPI0_PCS1 | UART0_ RTS_b | TPM0_CH4 | | EWM_IN | SPI1_PCS0 |
| 98 | 62 | 46 | PTD5 | ADC0_SE6b | ADC0_SE6b | PTD5 | SPI0_PCS2 | UART0_ CTS_b | TPM0_CH5 | | EWM_OUT_b | SPI1_SCK |
| 99 | 63 | 47 | PTD6/ LLWU_P15 | ADC0_SE7b | ADC0_SE7b | PTD6/ LLWU_P15 | SPI0_PCS3 | UART0_RX | | | | SPI1_SOUT |
| 100 | 64 | 48 | PTD7 | DISABLED | | PTD7 | | UART0_TX | | | | SPI1_SIN |

## 4.2 Pin properties

The following table lists the pin properties.

| 100LQFP | 64LQFP | 48QFN | Pin Name | Driver Strength | Default Status after POR | Pull-up/ pull-down Setting after POR | Slew Rate after POR | Passive Pin Filter after POR | Open Drain | Pin Interrupt |
|---|---|---|---|---|---|---|---|---|---|---|
| 1 | 1 | 1 | PTE0/ CLKOUT 32K | ND | Hi-Z | - | FS | N | N | Y |
| 2 | 2 | 2 | PTE1/ LLWU_P 0 | ND | Hi-Z | - | FS | N | N | Y |
| 3 | | 3 | PTE2/ LLWU_P 1 | ND | Hi-Z | - | FS | N | N | Y |
| 4 | | 4 | PTE3 | ND | Hi-Z | - | FS | N | N | Y |
| 5 | | 5 | PTE4/ LLWU_P 2 | ND | Hi-Z | - | FS | N | N | Y |
| 6 | | 6 | PTE5 | ND | Hi-Z | - | FS | N | N | Y |
| 7 | | | PTE6 | ND | Hi-Z | - | FS | N | N | Y |
| 8 | 3 | 7 | VDD | - | - | - | - | - | - | - |
| 9 | 4 | 8 | VSS | - | - | - | - | - | - | - |
| 9 | 4 | 9 | VSS | - | - | - | - | - | - | - |
| 10 | 5 | 10 | USB0_D P | - | Hi-Z | - | - | - | - | - |
| 11 | 6 | 11 | USB0_D M | - | Hi-Z | - | - | - | - | - |
| 12 | 7 | | USBVDD | - | - | - | - | - | - | - |
| 13 | | | NC | - | - | - | - | - | - | - |
| 14 | 8 | | ADC0_D P1 | - | Hi-Z | - | - | - | - | - |
| 15 | | | ADC0_D M1 | - | Hi-Z | - | - | - | - | - |
| 16 | | | ADC0_D P2 | - | Hi-Z | - | - | - | - | - |
| 17 | | | ADC0_D M2 | - | Hi-Z | - | - | - | - | - |
| 18 | 9 | | ADC0_D P0 | - | Hi-Z | - | - | - | - | - |
| 19 | 10 | | ADC0_D M0 | - | Hi-Z | - | - | - | - | - |

*Table continues on the next page...*

| 100LQFP | 64LQFP | 48QFN | Pin Name | Driver Strength | Default Status after POR | Pull-up/ pull-down Setting after POR | Slew Rate after POR | Passive Pin Filter after POR | Open Drain | Pin Interrupt |
|---|---|---|---|---|---|---|---|---|---|---|
| 20 | 11 | | ADC0_DP3 | - | Hi-Z | - | - | - | - | - |
| 21 | 12 | | ADC0_DM3 | - | Hi-Z | - | - | - | - | - |
| 22 | 13 | 12 | VDDA | - | - | - | - | - | - | - |
| 23 | 14 | 12 | VREFH | - | Hi-Z | - | - | - | - | - |
| 24 | 15 | 13 | VREFL | - | Hi-Z | - | - | - | - | - |
| 25 | 16 | 13 | VSSA | - | Hi-Z | - | - | - | - | - |
| 26 | 17 | | CMP0_IN5 | - | Hi-Z | - | - | - | - | - |
| 27 | 18 | | DAC0_OUT/ ADC0_SE23 | - | Hi-Z | - | - | - | - | - |
| 28 | 19 | 14 | XTAL32 | - | Hi-Z | - | - | - | - | - |
| 29 | 20 | 15 | EXTAL32 | - | Hi-Z | - | - | - | - | - |
| 30 | 21 | 16 | VBAT | - | - | - | - | - | - | - |
| 31 | | | PTE24 | ND | Hi-Z | - | FS | N | N | Y |
| 32 | | | PTE25 | ND | Hi-Z | - | FS | N | N | Y |
| 33 | | | PTE26/ CLKOUT32K | ND | Hi-Z | - | FS | N | N | Y |
| 34 | 22 | 17 | PTA0 | ND | L | PD | FS | N | N | Y |
| 35 | 23 | 18 | PTA1 | ND | H | PU | FS | N | N | Y |
| 36 | 24 | 19 | PTA2 | ND | H | PU | FS | N | N | Y |
| 37 | 25 | 20 | PTA3 | ND | H | PU | FS | N | N | Y |
| 38 | 26 | 21 | PTA4/ LLWU_P3 | ND | H | PU | FS | N | N | Y |
| 39 | 27 | | PTA5 | ND | Hi-Z | - | FS | N | N | Y |
| 40 | | | VDD | - | - | - | - | - | - | - |
| 41 | | | VSS | - | - | - | - | - | - | - |
| 42 | 28 | | PTA12 | ND | Hi-Z | - | FS | N | N | Y |
| 43 | 29 | | PTA13/ LLWU_P4 | ND | Hi-Z | - | FS | N | N | Y |
| 44 | | | PTA14 | ND | Hi-Z | - | FS | N | N | Y |
| 45 | | | PTA15 | ND | Hi-Z | - | FS | N | N | Y |
| 46 | | | PTA16 | ND | Hi-Z | - | FS | N | N | Y |

*Table continues on the next page...*

| 100LQFP | 64LQFP | 48QFN | Pin Name | Driver Strength | Default Status after POR | Pull-up/ pull-down Setting after POR | Slew Rate after POR | Passive Pin Filter after POR | Open Drain | Pin Interrupt |
|---|---|---|---|---|---|---|---|---|---|---|
| 47 | | | PTA17 | ND | Hi-Z | - | FS | N | N | Y |
| 48 | 30 | 22 | VDD | - | - | - | - | - | - | - |
| 49 | 31 | 23 | VSS | - | - | - | - | - | - | - |
| 50 | 32 | 24 | PTA18 | ND | Hi-Z | - | FS | N | N | Y |
| 51 | 33 | 25 | PTA19 | ND | Hi-Z | - | FS | N | N | Y |
| 52 | 34 | 26 | RESET_b | - | H | PU | - | Y | N | - |
| 53 | 35 | 27 | PTB0/ LLWU_P5 | HD | Hi-Z | - | FS | N | N | Y |
| 54 | 36 | 28 | PTB1 | HD | Hi-Z | - | FS | N | N | Y |
| 55 | 37 | 29 | PTB2 | ND | Hi-Z | - | FS | N | N | Y |
| 56 | 38 | 30 | PTB3 | ND | Hi-Z | - | FS | N | N | Y |
| 57 | | | PTB9 | ND | Hi-Z | - | FS | N | N | Y |
| 58 | | | PTB10 | ND | Hi-Z | - | FS | N | N | Y |
| 59 | | | PTB11 | ND | Hi-Z | - | FS | N | N | Y |
| 60 | | | VSS | - | - | - | - | - | - | - |
| 61 | | | VDD | - | - | - | - | - | - | - |
| 62 | 39 | 31 | PTB16 | ND | Hi-Z | - | FS | N | N | Y |
| 63 | 40 | | PTB17 | ND | Hi-Z | - | FS | N | N | Y |
| 64 | 41 | 32 | PTB18 | ND | Hi-Z | - | FS | N | N | Y |
| 65 | 42 | 33 | PTB19 | ND | Hi-Z | - | FS | N | N | Y |
| 66 | | | PTB20 | ND | Hi-Z | - | FS | N | N | Y |
| 67 | | | PTB21 | ND | Hi-Z | - | FS | N | N | Y |
| 68 | | | PTB22 | ND | Hi-Z | - | FS | N | N | Y |
| 69 | | | PTB23 | ND | Hi-Z | - | FS | N | N | Y |
| 70 | 43 | | PTC0 | ND | Hi-Z | - | FS | N | N | Y |
| 71 | 44 | 34 | PTC1/ LLWU_P6 | ND | Hi-Z | - | FS | N | N | Y |
| 72 | 45 | 35 | PTC2 | ND | Hi-Z | - | FS | N | N | Y |
| 73 | 46 | 36 | PTC3/ LLWU_P7 | HD | Hi-Z | - | FS | N | N | Y |
| 74 | 47 | | VSS | - | - | - | - | - | - | - |
| 75 | 48 | | VDD | - | - | - | - | - | - | - |

*Table continues on the next page...*

| 100LQFP | 64LQFP | 48QFN | Pin Name | Driver Strength | Default Status after POR | Pull-up/ pull-down Setting after POR | Slew Rate after POR | Passive Pin Filter after POR | Open Drain | Pin Interrupt |
|---|---|---|---|---|---|---|---|---|---|---|
| 76 | 49 | 37 | PTC4/ LLWU_P 8 | HD | Hi-Z | - | FS | N | N | Y |
| 77 | 50 | 38 | PTC5/ LLWU_P 9 | ND | Hi-Z | - | FS | N | N | Y |
| 78 | 51 | 39 | PTC6/ LLWU_P 10 | ND | Hi-Z | - | FS | N | N | Y |
| 79 | 52 | 40 | PTC7 | ND | Hi-Z | - | FS | N | N | Y |
| 80 | 53 | | PTC8 | ND | Hi-Z | - | FS | N | N | Y |
| 81 | 54 | | PTC9 | ND | Hi-Z | - | FS | N | N | Y |
| 82 | 55 | | PTC10 | ND | Hi-Z | - | FS | N | N | Y |
| 83 | 56 | | PTC11/ LLWU_P 11 | ND | Hi-Z | - | FS | N | N | Y |
| 84 | | | PTC12 | ND | Hi-Z | - | FS | N | N | Y |
| 85 | | | PTC13 | ND | Hi-Z | - | FS | N | N | Y |
| 86 | | | PTC14 | ND | Hi-Z | - | FS | N | N | Y |
| 87 | | | PTC15 | ND | Hi-Z | - | FS | N | N | Y |
| 88 | | | VSS | - | - | - | - | - | - | - |
| 89 | | | VDD | - | - | - | - | - | - | - |
| 90 | | | PTC16 | ND | Hi-Z | - | FS | N | N | Y |
| 91 | | | PTC17 | ND | Hi-Z | - | FS | N | N | Y |
| 92 | | | PTC18 | ND | Hi-Z | - | FS | N | N | Y |
| 93 | 57 | 41 | PTD0/ LLWU_P 12 | ND | Hi-Z | - | FS | N | N | Y |
| 94 | 58 | 42 | PTD1 | ND | Hi-Z | - | FS | N | N | Y |
| 95 | 59 | 43 | PTD2/ LLWU_P 13 | ND | Hi-Z | - | FS | N | N | Y |
| 96 | 60 | 44 | PTD3 | ND | Hi-Z | - | FS | N | N | Y |
| 97 | 61 | 45 | PTD4/ LLWU_P 14 | HD | Hi-Z | - | FS | N | N | Y |
| 98 | 62 | 46 | PTD5 | HD | Hi-Z | - | FS | N | N | Y |
| 99 | 63 | 47 | PTD6/ LLWU_P 15 | HD | Hi-Z | - | FS | N | N | Y |

*Table continues on the next page...*

| 100LQFP | 64LQFP | 48QFN | Pin Name | Driver Strength | Default Status after POR | Pull-up/ pull- down Setting after POR | Slew Rate after POR | Passive Pin Filter after POR | Open Drain | Pin Interrupt |
|---|---|---|---|---|---|---|---|---|---|---|
| 100 | 64 | 48 | PTD7 | HD | Hi-Z | - | FS | N | N | Y |

| Properties | Abbreviation | Descriptions |
|---|---|---|
| Driver strength | ND | Normal drive |
| | HD | High drive |
| Default status after POR | Hi-Z | High impendence |
| | H | High level |
| | L | Low level |
| Pull-up/pull-down setting after POR | PU | Pull-up |
| | PD | Pull-down |
| Slew rate after POR | FS | Fast slew rate |
| | SS | Slow slew rate |
| Passive Pin Filter after POR | N | Disabled |
| | Y | Enabled |
| Open drain | N | Disabled[1] |
| | Y | Enabled |
| Pin interrupt | Y | Yes |

1. When UART or LPUART module is enabled and a pin is functional for UART or LPUART, this pin is (pseudo-) open drain configurable.

# 4.3   Module Signal Description Tables

The following sections correlate the chip-level signal name with the signal name used in the module's chapter. They also briefly describe the signal function and direction.

## 4.3.1   Core Modules

**Table 9.   JTAG Signal Descriptions**

| Chip signal name | Module signal name | Description | I/O |
|---|---|---|---|
| JTAG_TMS | JTAG_TMS/ SWD_DIO | JTAG Test Mode Selection | I |

*Table continues on the next page...*

### Table 9. JTAG Signal Descriptions (continued)

| Chip signal name | Module signal name | Description | I/O |
|---|---|---|---|
| JTAG_TCLK | JTAG_TCLK/ SWD_CLK | JTAG Test Clock | I |
| JTAG_TDI | JTAG_TDI | JTAG Test Data Input | I |
| JTAG_TDO | JTAG_TDO/ TRACE_SWO | JTAG Test Data Output | O |
| JTAG_TRST | JTAG_TRST_b | JTAG Reset | I |

### Table 10. SWD Signal Descriptions

| Chip signal name | Module signal name | Description | I/O |
|---|---|---|---|
| SWD_DIO | JTAG_TMS/ SWD_DIO | Serial Wire Data | I |
| SWD_CLK | JTAG_TCLK/ SWD_CLK | Serial Wire Clock | I |

### Table 11. TPIU Signal Descriptions

| Chip signal name | Module signal name | Description | I/O |
|---|---|---|---|
| TRACE_SWO | JTAG_TDO/ TRACE_SWO | Trace output data from the ARM CoreSight debug block over a single pin | O |

## 4.3.2 System Modules

### Table 12. EWM Signal Descriptions

| Chip signal name | Module signal name | Description | I/O |
|---|---|---|---|
| EWM_IN | EWM_in | EWM input for safety status of external safety circuits. The polarity of EWM_in is programmable using the EWM_CTRL[ASSIN] bit. The default polarity is active-low. | I |
| EWM_OUT | EWM_out | EWM reset out signal | O |

## 4.3.3   Clock Modules

**Table 13.   OSC Signal Descriptions**

| Chip signal name | Module signal name | Description | I/O |
|---|---|---|---|
| EXTAL0 | EXTAL | External clock/Oscillator input | I |
| XTAL0 | XTAL | Oscillator output | O |

**Table 14.   RTC OSC Signal Descriptions**

| Chip signal name | Module signal name | Description | I/O |
|---|---|---|---|
| EXTAL32 | EXTAL32 | 32.768 kHz oscillator input | I |
| XTAL32 | XTAL32 | 32.768 kHz oscillator output | O |

## 4.3.4   Analog

**Table 15.   ADC 0 Signal Descriptions**

| Chip signal name | Module signal name | Description | I/O |
|---|---|---|---|
| ADC0_DP[3:0] | DADP3–DADP0 | Differential Analog Channel Inputs | I |
| ADC0_DM[3:0] | DADM3–DADM0 | Differential Analog Channel Inputs | I |
| ADC0_SEn | AD$n$ | Single-Ended Analog Channel Inputs | I |
| VREFH | $V_{REFSH}$ | Voltage Reference Select High | I |
| VREFL | $V_{REFSL}$ | Voltage Reference Select Low | I |
| VDDA | $V_{DDA}$ | Analog Power Supply | I |
| VSSA | $V_{SSA}$ | Analog Ground | I |

**Table 16.   CMP 0 Signal Descriptions**

| Chip signal name | Module signal name | Description | I/O |
|---|---|---|---|
| CMP0_IN[5:0] | IN[5:0] | Analog voltage inputs | I |
| CMP0_OUT | CMPO | Comparator output | O |

**Table 17.   DAC 0 Signal Descriptions**

| Chip signal name | Module signal name | Description | I/O |
|---|---|---|---|
| DAC0_OUT | — | DAC output | O |

## 4.3.5   Timer Modules

**Table 18.   PDB 0 Signal Descriptions**

| Chip signal name | Module signal name | Description | I/O |
|---|---|---|---|
| PDB0_EXTRG | EXTRG | External Trigger Input Source<br><br>If the PDB is enabled and external trigger input source is selected, a positive edge on the EXTRG signal resets and starts the counter. | I |

**Table 19.   LPTMR 0 Signal Descriptions**

| Chip signal name | Module signal name | Description | I/O |
|---|---|---|---|
| LPTMR0_ALT[2:1] | LPTMR0_ALT*n* | Pulse Counter Input pin | I |

**Table 20.   RTC Signal Descriptions**

| Chip signal name | Module signal name | Description | I/O |
|---|---|---|---|
| VBAT | — | Backup battery supply for RTC and VBAT register file | I |
| RTC_CLKOUT | RTC_CLKOUT | 1 Hz square-wave output or OSCERCLK | O |

**Table 21.   TPM 0 Signal Descriptions**

| Chip signal name | Module signal name | Description | I/O |
|---|---|---|---|
| TPM_CLKIN[1:0] | TPM_EXTCLK | External clock. TPM external clock can be selected to increment the TPM counter on every rising edge synchronized to the counter clock. | I |
| TPM0_CH[5:0] | TPM_CHn | TPM channel (n = 5 to 0). A TPM channel pin is configured as output when configured in an output compare or PWM mode and the TPM counter is enabled, otherwise the TPM channel pin is an input. | I/O |

**Table 22.   TPM 1 Signal Descriptions**

| Chip signal name | Module signal name | Description | I/O |
|---|---|---|---|
| TPM_CLKIN[1:0] | TPM_EXTCLK | External clock. TPM external clock can be selected to increment the TPM counter on every rising edge synchronized to the counter clock. | I |

*Table continues on the next page...*

**Table 22. TPM 1 Signal Descriptions (continued)**

| Chip signal name | Module signal name | Description | I/O |
|---|---|---|---|
| TPM1_CH[1:0] | TPM_CHn | TPM channel (n = 5 to 0). A TPM channel pin is configured as output when configured in an output compare or PWM mode and the TPM counter is enabled, otherwise the TPM channel pin is an input. | I/O |

**Table 23. TPM 2 Signal Descriptions**

| Chip signal name | Module signal name | Description | I/O |
|---|---|---|---|
| TPM_CLKIN[1:0] | TPM_EXTCLK | External clock. TPM external clock can be selected to increment the TPM counter on every rising edge synchronized to the counter clock. | I |
| TPM2_CH[1:0] | TPM_CHn | TPM channel (n = 5 to 0). A TPM channel pin is configured as output when configured in an output compare or PWM mode and the TPM counter is enabled, otherwise the TPM channel pin is an input. | I/O |

## 4.3.6 Communication Interfaces

**Table 24. USB FS OTG Signal Descriptions**

| Chip signal name | Module signal name | Description | I/O |
|---|---|---|---|
| USB0_DM | usb_dm | USB D- analog data signal on the USB bus. | I/O |
| USB0_DP | usb_dp | USB D+ analog data signal on the USB bus. | I/O |
| USB_CLKIN | — | Alternate USB clock input | I |
| USB_SOF_OUT | — | USB start of frame signal. Can be used to make the USB start of frame available for external synchronization. | O |

**Table 25. CAN 0 Signal Descriptions**

| Chip signal name | Module signal name | Description | I/O |
|---|---|---|---|
| CAN0_RX | CAN Rx | CAN Receive Pin | Input |
| CAN0_TX | CAN Tx | CAN Transmit Pin | Output |

### Table 26. CAN 1 (for KS22 only) Signal Descriptions

| Chip signal name | Module signal name | Description | I/O |
|---|---|---|---|
| CAN1_RX | CAN Rx | CAN Receive Pin | Input |
| CAN1_TX | CAN Tx | CAN Transmit Pin | Output |

### Table 27. SPI 0 Signal Descriptions

| Chip signal name | Module signal name | Description | I/O |
|---|---|---|---|
| SPI0_PCS0 | PCS0/$\overline{SS}$ | Peripheral Chip Select 0 (O) | I/O |
| SPI0_PCS[3:1] | PCS[1:3] | Peripheral Chip Selects 1–3 | O |
| SPI0_PCS4 | PCS4 | Peripheral Chip Select 4 | O |
| SPI0_PCS5 | PCS5/ $\overline{PCSS}$ | Peripheral Chip Select 5 /Peripheral Chip Select Strobe | O |
| SPI0_SIN | SIN | Serial Data In | I |
| SPI0_SOUT | SOUT | Serial Data Out | O |
| SPI0_SCK | SCK | Serial Clock (O) | I/O |

### Table 28. SPI 1 Signal Descriptions

| Chip signal name | Module signal name | Description | I/O |
|---|---|---|---|
| SPI1_PCS0 | PCS0/$\overline{SS}$ | Peripheral Chip Select 0 (O) | I/O |
| SPI1_PCS[3:1] | PCS[1:3] | Peripheral Chip Selects 1–3 | O |
| SPI1_SIN | SIN | Serial Data In | I |
| SPI1_SOUT | SOUT | Serial Data Out | O |
| SPI1_SCK | SCK | Serial Clock (O) | I/O |

### Table 29. LPI$^2$C 0 Signal Descriptions

| Chip signal name | Module signal name | Description | I/O |
|---|---|---|---|
| LPI2C0_SCL | SCL | LPI2C clock line. | I/O |
| LPI2C0_SDA | SDA | LPI2C data line. | I/O |
| LPI2C0_HREQ | HREQ | Host request, can initiate an LPI2C master transfer if asserted and the I2C bus is idle. | I |
| LPI2C0_SCLS | SCLS | Secondary I2C clock line. If LPI2C master/slave are configured to use separate pins, this the LPI2C slave SCL pin. | I/O |
| LPI2C0_SDAS | SDAS | Secondary I2C data line. If LPI2C master/slave are configured to use separate pins, this the LPI2C slave SDA pin. | I/O |

## Table 30. LPI²C 1 Signal Descriptions

| Chip signal name | Module signal name | Description | I/O |
|---|---|---|---|
| LPI2C1_SCL | SCL | LPI2C clock line. | I/O |
| LPI2C1_SDA | SDA | LPI2C data line. | I/O |
| LPI2C1_HREQ | HREQ | Host request, can initiate an LPI2C master transfer if asserted and the I2C bus is idle. | I |
| LPI2C1_SCLS | SCLS | Secondary I2C clock line. If LPI2C master/slave are configured to use separate pins, this the LPI2C slave SCL pin. | I/O |
| LPI2C1_SDAS | SDAS | Secondary I2C data line. If LPI2C master/slave are configured to use separate pins, this the LPI2C slave SDA pin. | I/O |

## Table 31. LPUART Signal Descriptions

| Chip signal name | Module signal name | Description | I/O |
|---|---|---|---|
| LPUART0_TX | LPUART_TX | Transmit data. This pin is normally an output, but is an input (tristated) in single wire mode whenever the transmitter is disabled or transmit direction is configured for receive data. | O/I |
| LPUART0_RX | LPUART_RX | Receive data | I |
| $\overline{\text{LPUART0\_CTS}}$ | LPUART_CTS | Clear to send | I |
| $\overline{\text{LPUART0\_CTS}}$ | LPUART_RTS | Request to send | I |

## Table 32. UART 0 Signal Descriptions

| Chip signal name | Module signal name | Description | I/O |
|---|---|---|---|
| $\overline{\text{UART0\_CTS}}$ | $\overline{\text{CTS}}$ | Clear to send | I |
| $\overline{\text{UART0\_RTS}}$ | $\overline{\text{RTS}}$ | Request to send | O |
| UART0_TX | TXD | Transmit data | O |
| UART0_RX | RXD | Receive data | I |

## Table 33. UART 1 Signal Descriptions

| Chip signal name | Module signal name | Description | I/O |
|---|---|---|---|
| $\overline{\text{UART1\_CTS}}$ | $\overline{\text{CTS}}$ | Clear to send | I |
| $\overline{\text{UART1\_RTS}}$ | $\overline{\text{RTS}}$ | Request to send | O |
| UART1_TX | TXD | Transmit data | O |
| UART1_RX | RXD | Receive data | I |

**Table 34.   UART 2 Signal Descriptions**

| Chip signal name | Module signal name | Description | I/O |
|---|---|---|---|
| UART2_CTS | CTS | Clear to send | I |
| UART2_RTS | RTS | Request to send | O |
| UART2_TX | TXD | Transmit data | O |
| UART2_RX | RXD | Receive data | I |

**Table 35.   I$^2$S0 Signal Descriptions**

| Chip signal name | Module signal name | Description | I/O |
|---|---|---|---|
| I2S0_MCLK | SAI_MCLK | Audio Master Clock. The master clock is an input when externally generated and an output when internally generated. | I/O |
| I2S0_RX_BCLK | SAI_RX_BCLK | Receive Bit Clock. The bit clock is an input when externally generated and an output when internally generated. | I/O |
| I2S0_RX_FS | SAI_RX_SYNC | Receive Frame Sync. The frame sync is an input sampled synchronously by the bit clock when externally generated and an output generated synchronously by the bit clock when internally generated. | I/O |
| I2S0_RXD | SAI_RX_DATA | Receive Data. The receive data is sampled synchronously by the bit clock. | I |
| I2S0_TX_BCLK | SAI_TX_BCLK | Transmit Bit Clock. The bit clock is an input when externally generated and an output when internally generated. | I/O |
| I2S0_TX_FS | SAI_TX_SYNC | Transmit Frame Sync. The frame sync is an input sampled synchronously by the bit clock when externally generated and an output generated synchronously by the bit clock when internally generated. | I/O |
| I2S0_TXD | SAI_TX_DATA | Transmit Data. The transmit data is generated synchronously by the bit clock and is tristated whenever not transmitting a word. | O |

**Table 36.   I$^2$S1 Signal Descriptions**

| Chip signal name | Module signal name | Description | I/O |
|---|---|---|---|
| I2S1_MCLK | SAI_MCLK | Audio Master Clock. The master clock is an input when externally generated and an output when internally generated. | I/O |
| I2S1_RX_BCLK | SAI_RX_BCLK | Receive Bit Clock. The bit clock is an input when externally generated and an output when internally generated. | I/O |
| I2S1_RX_FS | SAI_RX_SYNC | Receive Frame Sync. The frame sync is an input sampled synchronously by the bit clock when externally generated and an output generated synchronously by the bit clock when internally generated. | I/O |
| I2S1_RXD | SAI_RX_DATA | Receive Data. The receive data is sampled synchronously by the bit clock. | I |

*Table continues on the next page...*

**Table 36. I²S1 Signal Descriptions (continued)**

| Chip signal name | Module signal name | Description | I/O |
|---|---|---|---|
| I2S1_TX_BCLK | SAI_TX_BCLK | Transmit Bit Clock. The bit clock is an input when externally generated and an output when internally generated. | I/O |
| I2S1_TX_FS | SAI_TX_SYNC | Transmit Frame Sync. The frame sync is an input sampled synchronously by the bit clock when externally generated and an output generated synchronously by the bit clock when internally generated. | I/O |
| I2S1_TXD | SAI_TX_DATA | Transmit Data. The transmit data is generated synchronously by the bit clock and is tristated whenever not transmitting a word. | O |

**Table 37. FlexIO Signal Descriptions**

| Chip signal name | Module signal name | Description | I/O |
|---|---|---|---|
| FXIO0_D*n* | FXIO_D*n* (*n*=0...7) | Bidirectional FlexIO Shifter and Timer pin inputs/outputs | I/O |

## 4.3.7  Human-Machine Interfaces (HMI)

**Table 38. GPIO Signal Descriptions**

| Chip signal name | Module signal name | Description | I/O |
|---|---|---|---|
| PTA[31:0][1] | PORTA31–PORTA0 | General-purpose input/output | I/O |
| PTB[31:0][1] | PORTB31–PORTB0 | General-purpose input/output | I/O |
| PTC[31:0][1] | PORTC31–PORTC0 | General-purpose input/output | I/O |
| PTD[31:0][1] | PORTD31–PORTD0 | General-purpose input/output | I/O |
| PTE[31:0][1] | PORTE31–PORTE0 | General-purpose input/output | I/O |

1. The available GPIO pins depends on the specific package. See the signal multiplexing section for which exact GPIO signals are available.

## 4.4  Pinouts

The following figure shows the pinout diagram for the devices supported by this document. Many signals may be multiplexed onto a single pin. To determine what signals can be used on which pin, see the previous "signal multiplexing and pin assignments" section.

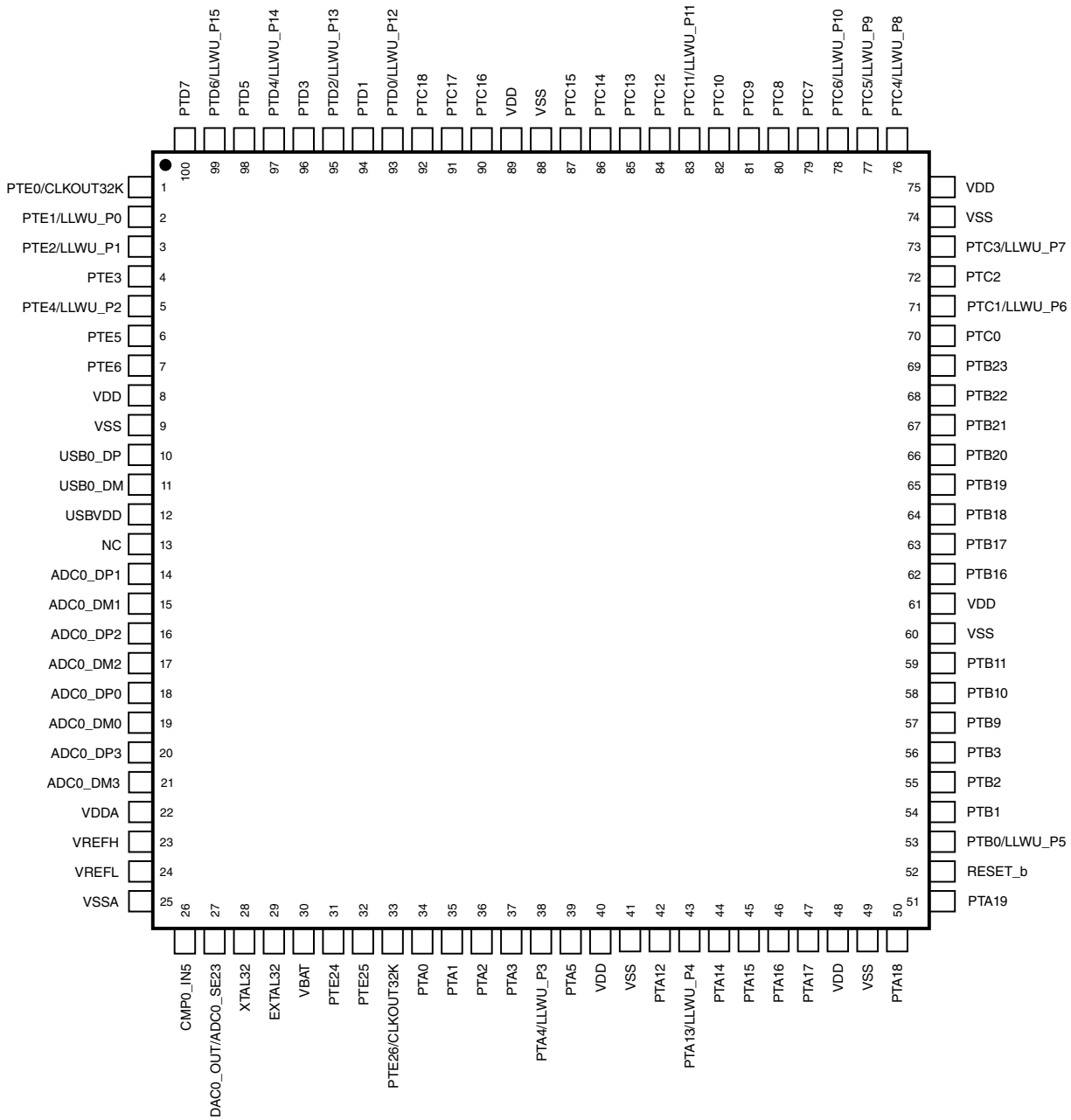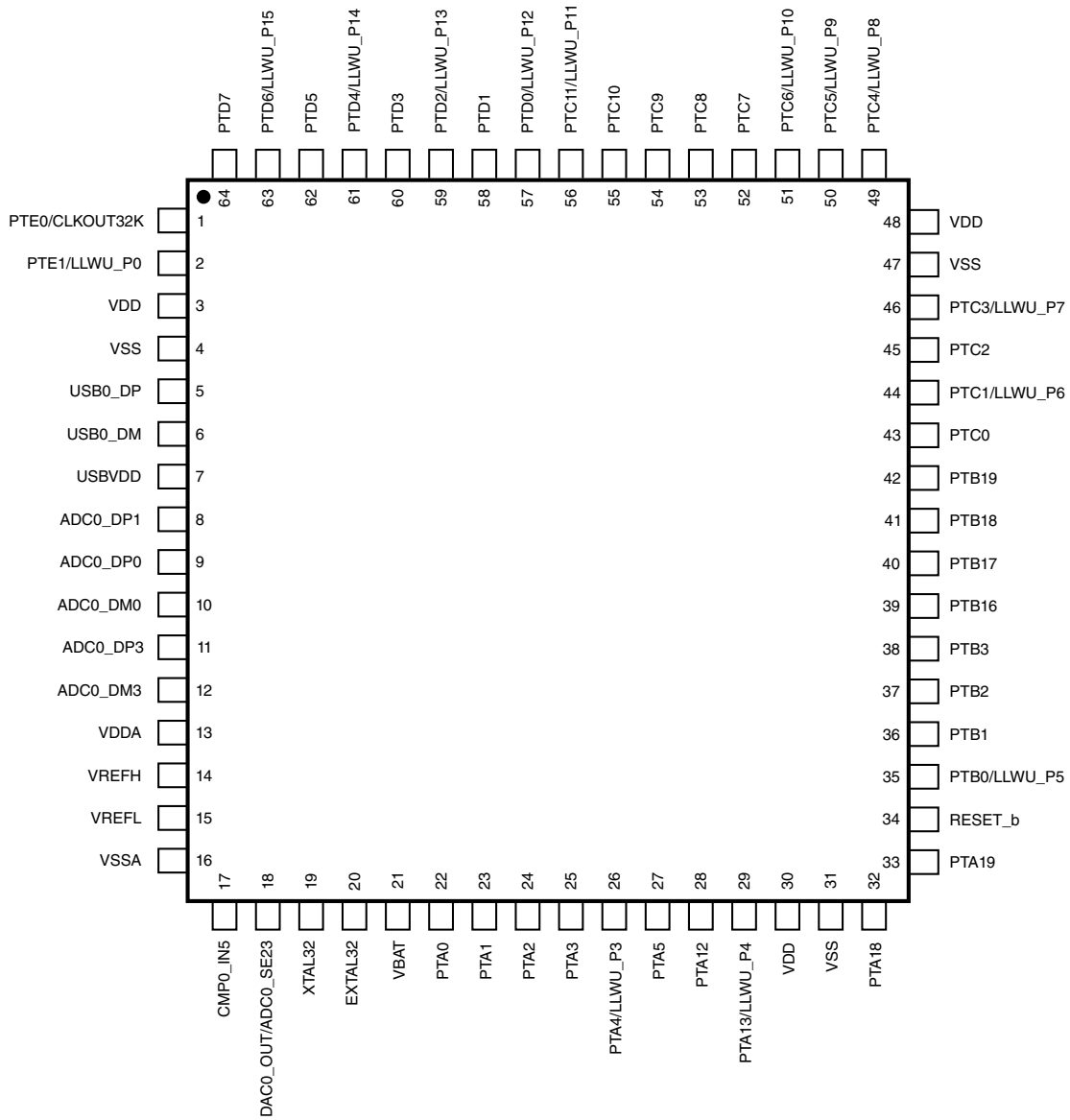**Figure 6. 100 LQFP Pinout Diagram**
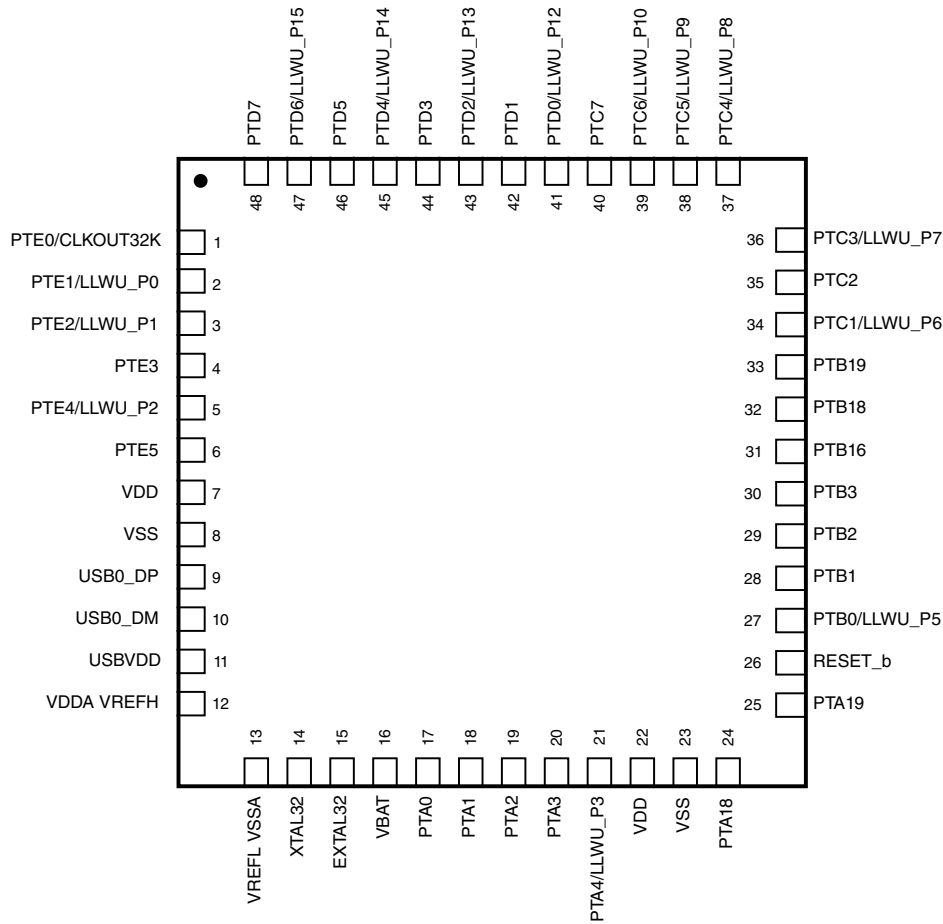
**Figure 7. 64 LQFP Pinout Diagram**

**Figure 8. 48 QFN Pinout Diagram**

## 4.5  Package dimensions

The following figures show the dimensions of the package options for the devices supported by this document.
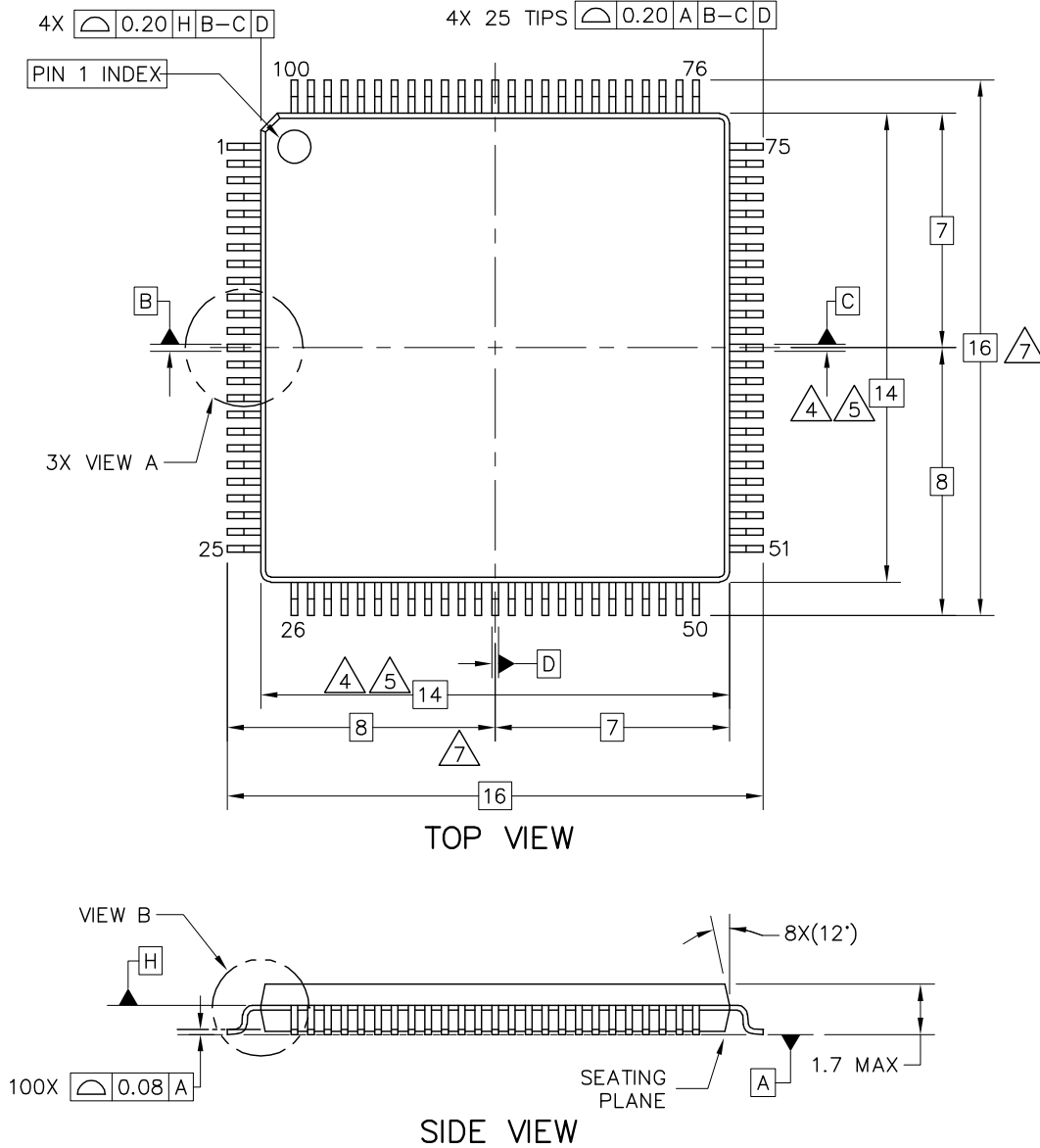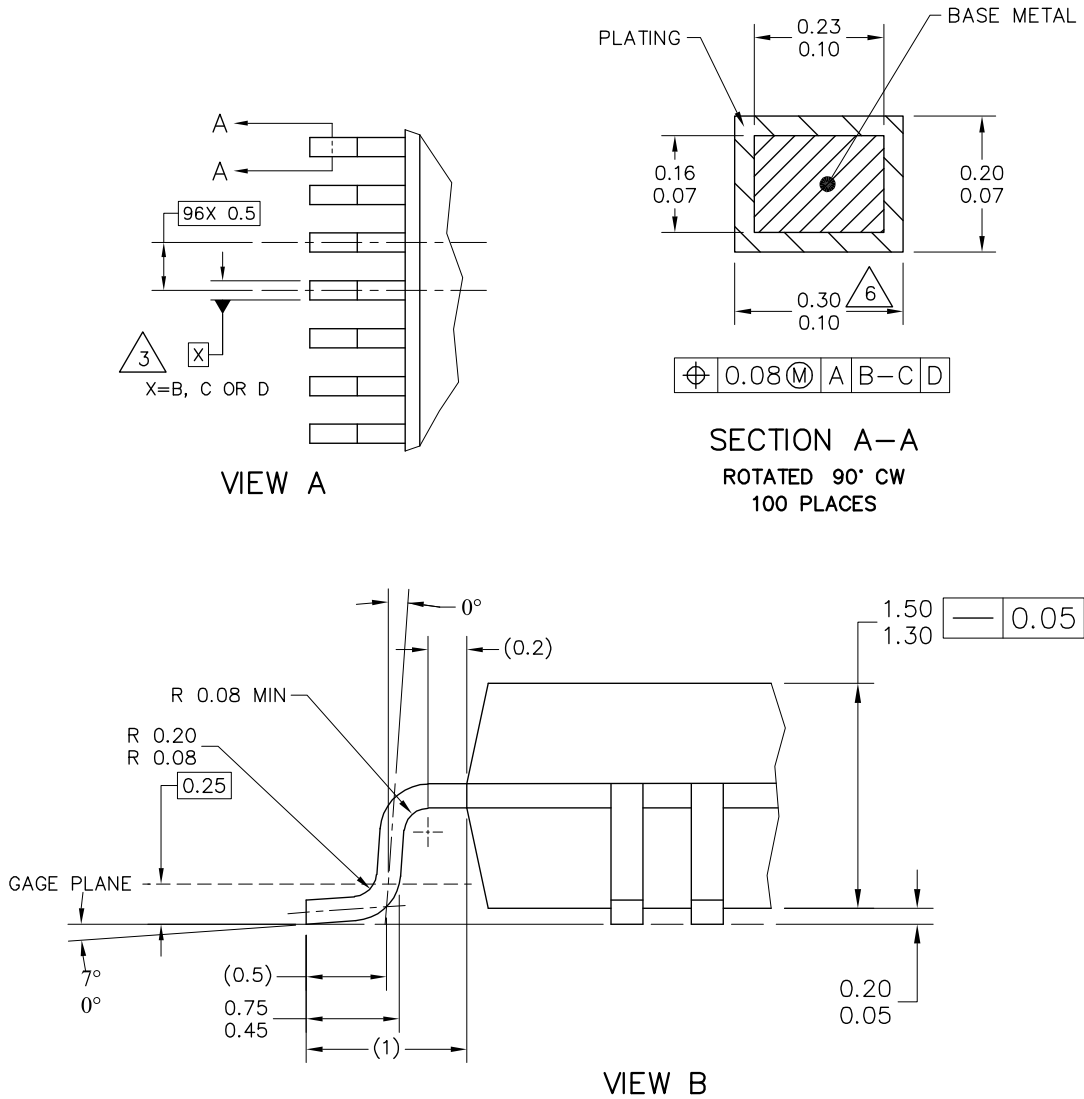
**Figure 9. 100-pin LQFP package dimensions 1**

PLATING — 0.23 / 0.10 — BASE METAL

0.16 / 0.07

0.20 / 0.07

0.30 / 0.10 △6

⊕ | 0.08 Ⓜ | A | B-C | D

**SECTION A-A**
ROTATED 90° CW
100 PLACES

A ←
A ←

96X 0.5

△3
X
X=B, C OR D

**VIEW A**

0°

(0.2)

R 0.08 MIN

R 0.20
R 0.08

0.25

GAGE PLANE

7°
0°

(0.5)
0.75
0.45

(1)

1.50 / 1.30 — | 0.05

0.20 / 0.05

**VIEW B**

NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.

2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M-1994.

△3. DATUMS B, C AND D TO BE DETERMINED AT DATUM PLANE H.

△4. THE TOP PACKAGE BODY SIZE MAY BE SMALLER THAN THE BOTTOM PACKAGE SIZE BY A MAXIMUM OF 0.1 MM.

△5. DIMENSIONS DO NOT INCLUDE MOLD PROTRUSIONS. THE MAXIMUM ALLOWABLE PROTRUSION IS 0.25 mm PER SIDE. THE DIMENSIONS ARE MAXIMUM BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.

△6. DIMENSION DOES NOT INCLUDE DAM BAR PROTRUSION. PROTRUSIONS SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 0.35. MINIMUM SPACE BETWEEN PROTRUSION AND AN ADJACENT LEAD SHALL BE 0.07 MM.

△7. DIMENSIONS ARE DETERMINED AT THE SEATING PLANE, DATUM A.

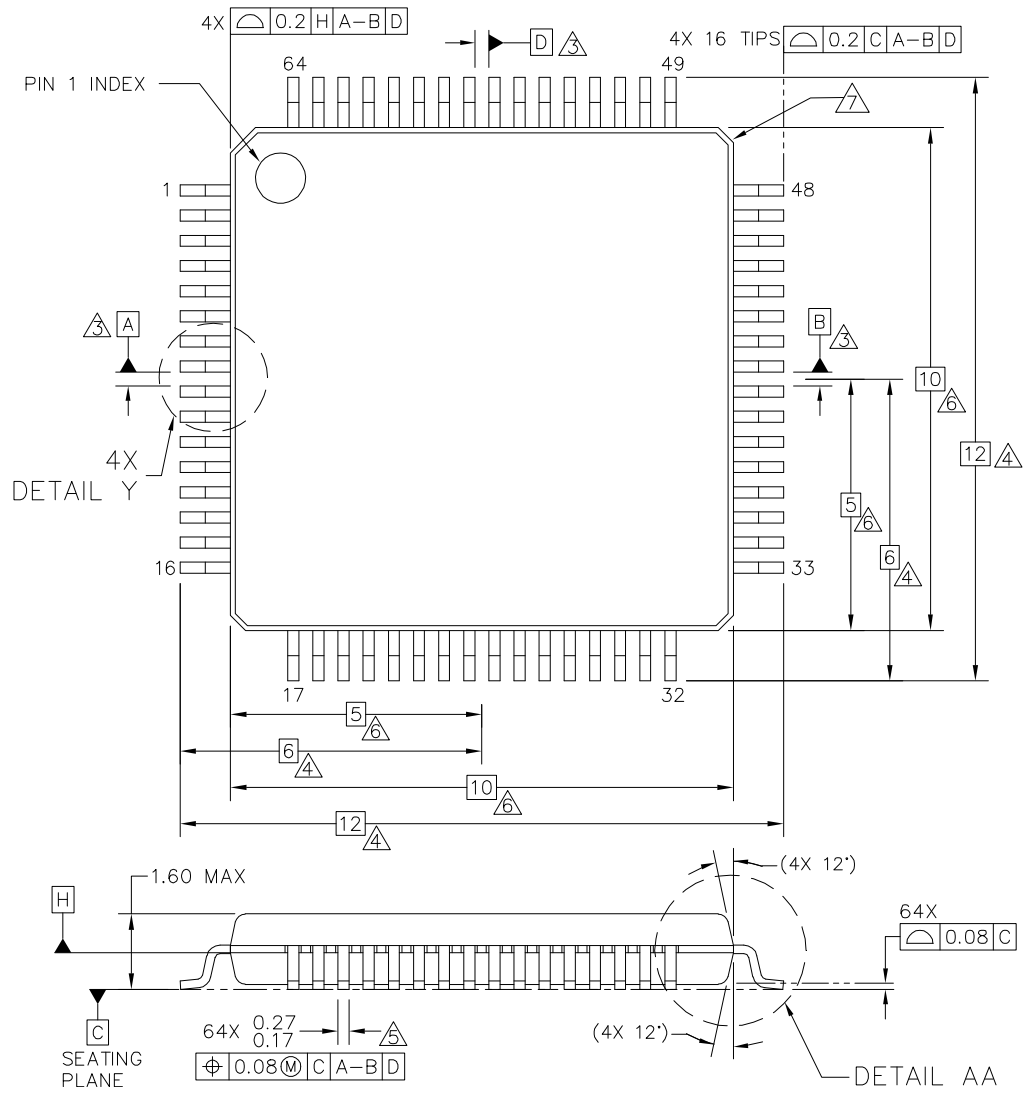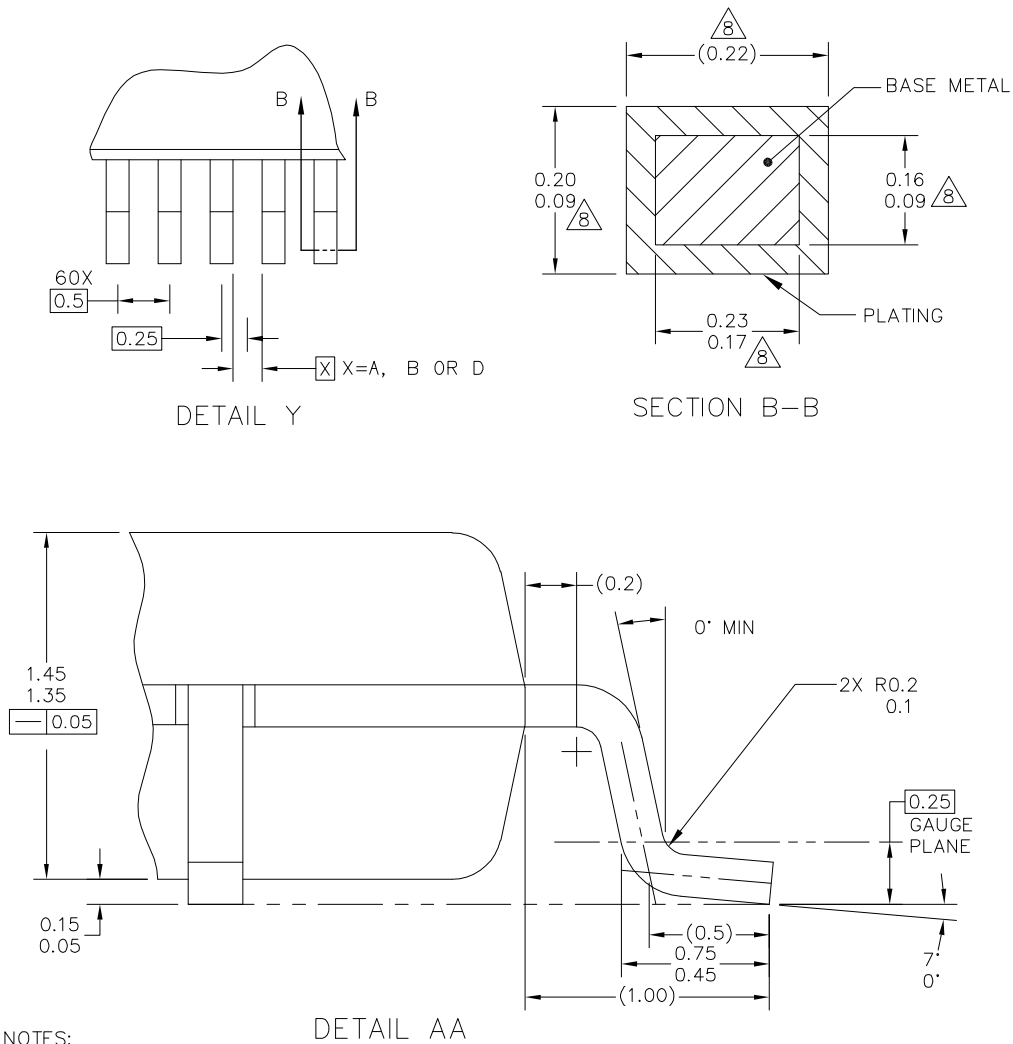**Figure 10. 100-pin LQFP package dimensions 2**

**Figure 11. 64-pin LQFP package dimensions 1**

DETAIL Y

SECTION B-B



DETAIL AA

NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.

2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.

3. DATUMS A, B AND D TO BE DETERMINED AT DATUM PLANE H.

4. DIMENSIONS TO BE DETERMINED AT SEATING PLANE C.

5. THIS DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE UPPER LIMIT BY MORE THAN 0.08 MM AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD SHALL NOT BE LESS THAN 0.07 MM.

6. THIS DIMENSION DOES NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 MM PER SIDE. THIS DIMENSION IS MAXIMUM PLASTIC BODY SIZE DIMENSION INCLUDING MOLD MISMATCH.

7. EXACT SHAPE OF EACH CORNER IS OPTIONAL.

8. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.1 MM AND 0.25 MM FROM THE LEAD TIP.
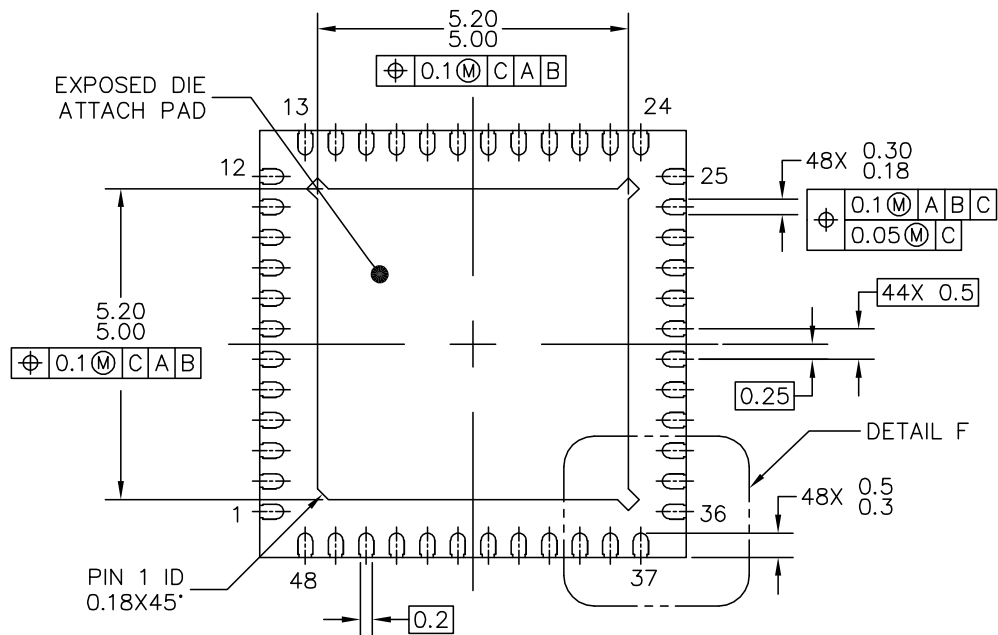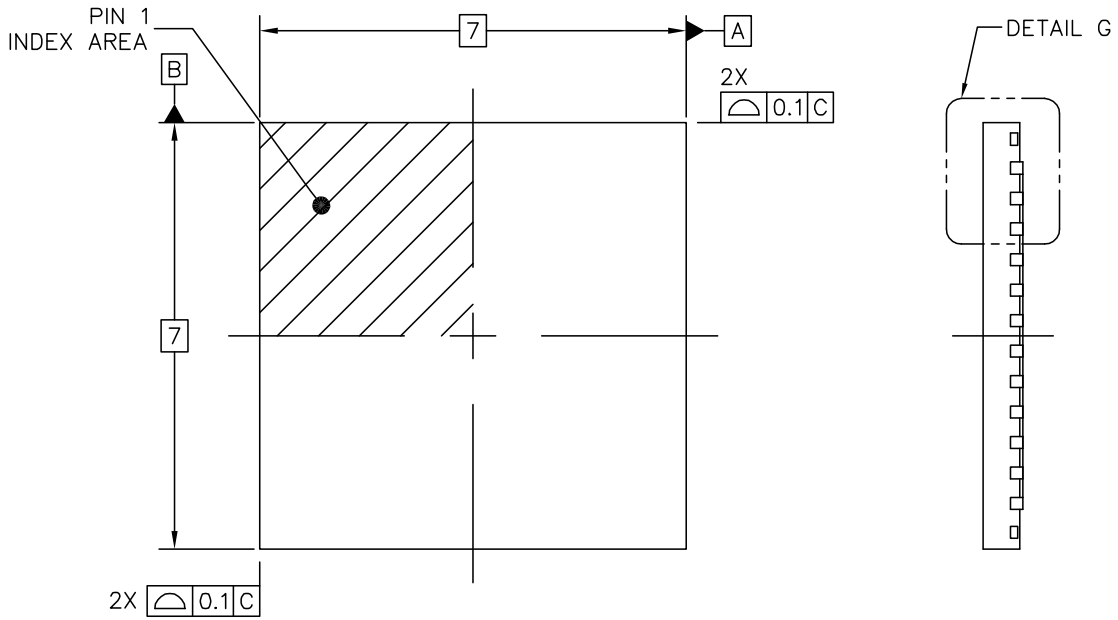
**Figure 12. 64-pin LQFP package dimensions 2**

**Figure 13. 48-pin QFN package dimension 1**
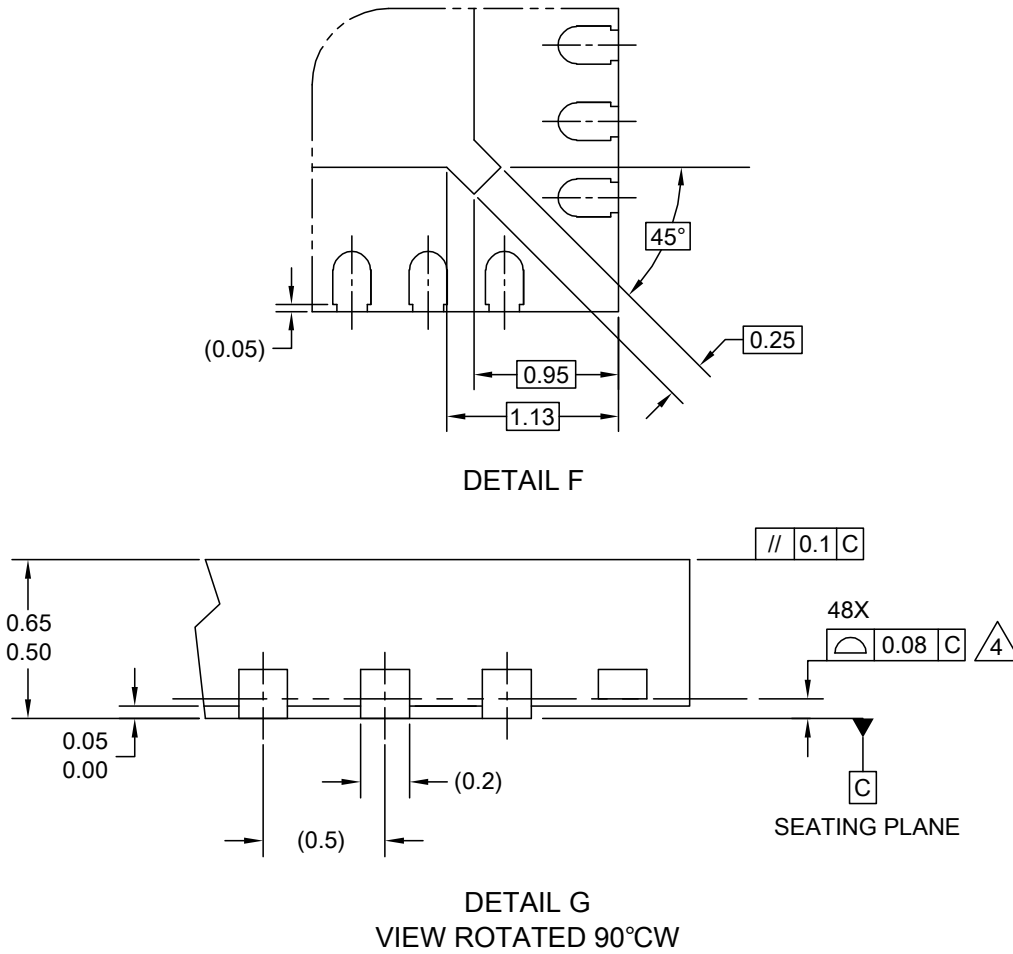
DETAIL F



DETAIL G
VIEW ROTATED 90°CW

NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.

2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.

3. THIS IS A NON-JEDEC REGISTERED PACKAGE.

4. COPLANARITY APPLIES TO LEADS AND DIE ATTACH FLAG.

5. MIN. METAL GAP SHOULD BE 0.2 MM.

**Figure 14. 48-pin QFN package dimension 2**

# 5  Electrical characteristics

## 5.1  Terminology and guidelines

## 5.1.1 Definitions

Key terms are defined in the following table:

| Term | Definition |
|---|---|
| Rating | A minimum or maximum value of a technical characteristic that, if exceeded, may cause permanent chip failure:<br><br>• *Operating ratings* apply during operation of the chip.<br>• *Handling ratings* apply when the chip is not powered.<br><br>NOTE: The likelihood of permanent chip failure increases rapidly as soon as a characteristic begins to exceed one of its operating ratings. |
| Operating requirement | A specified value or range of values for a technical characteristic that you must guarantee during operation to avoid incorrect operation and possibly decreasing the useful life of the chip |
| Operating behavior | A specified value or range of values for a technical characteristic that are guaranteed during operation if you meet the operating requirements and any other specified conditions |
| Typical value | A specified value for a technical characteristic that:<br><br>• Lies within the range of values specified by the operating behavior<br>• Is representative of that characteristic during operation when you meet the typical-value conditions or other specified conditions<br><br>NOTE: Typical values are provided as design guidelines and are neither tested nor guaranteed. |

## 5.1.2 Examples

*Operating rating*:

| Symbol | Description | Min. | Max. | Unit |
|--------|-------------|------|------|------|
| $V_{DD}$ | 1.0 V core supply voltage | −0.3 | 1.2 | V |

*Operating requirement*:

| Symbol | Description | Min. | Max. | Unit |
|--------|-------------|------|------|------|
| $V_{DD}$ | 1.0 V core supply voltage | 0.9 | 1.1 | V |

*Operating behavior* that includes a *typical value*:

| Symbol | Description | Min. | Typ. | Max. | Unit |
|--------|-------------|------|------|------|------|
| $I_{WP}$ | Digital I/O weak pullup/pulldown current | 10 | 70 | 130 | µA |

## 5.1.3 Typical-value conditions

Typical values assume you meet the following conditions (or other conditions as specified):

| Symbol | Description | Value | Unit |
|--------|-------------|-------|------|
| $T_A$ | Ambient temperature | 25 | °C |
| $V_{DD}$ | Supply voltage | 3.3 | V |

## 5.1.4  Relationship between ratings and operating requirements



Operating (power on)



Handling (power off)
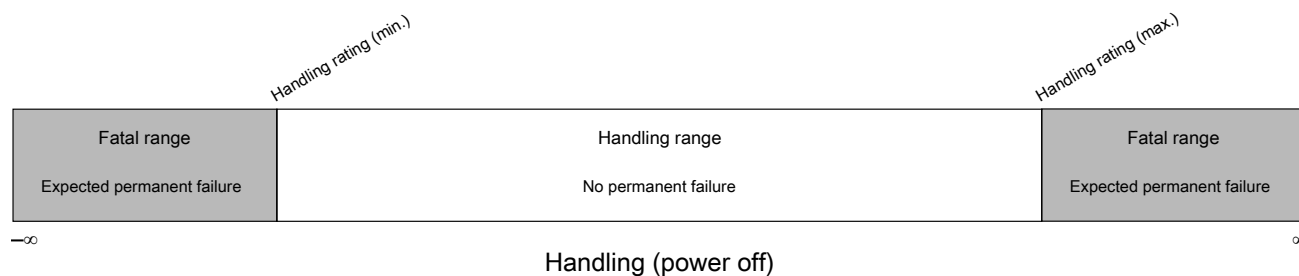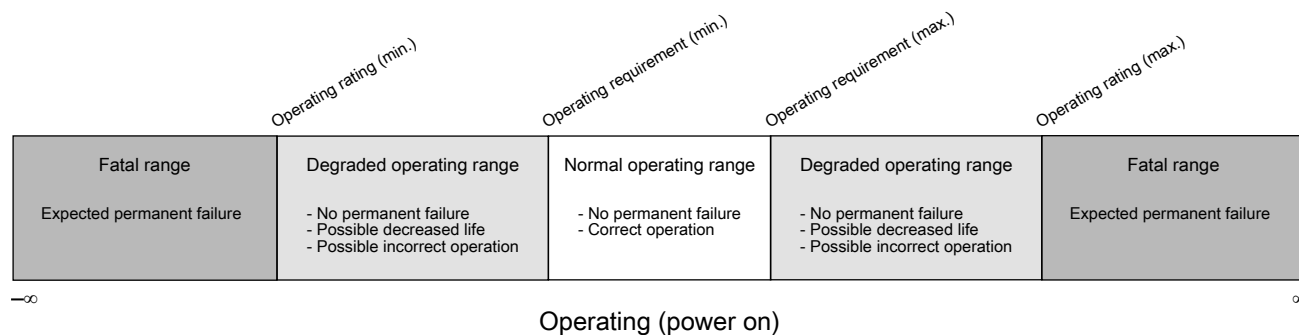
## 5.1.5  Guidelines for ratings and operating requirements

Follow these guidelines for ratings and operating requirements:

- Never exceed any of the chip's ratings.
- During normal operation, don't exceed any of the chip's operating requirements.
- If you must exceed an operating requirement at times other than during normal operation (for example, during power sequencing), limit the duration as much as possible.

## 5.2  Ratings

### 5.2.1  Thermal handling ratings

| Symbol | Description | Min. | Max. | Unit | Notes |
|--------|-------------|------|------|------|-------|
| $T_{STG}$ | Storage temperature | −55 | 150 | °C | 1 |
| $T_{SDR}$ | Solder temperature, lead-free | — | 260 | °C | 2 |

1. Determined according to JEDEC Standard JESD22-A103, *High Temperature Storage Life*.
2. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

## 5.2.2   Moisture handling ratings

| Symbol | Description | Min. | Max. | Unit | Notes |
|--------|-------------|------|------|------|-------|
| MSL | Moisture sensitivity level | — | 3 | — | 1 |

1. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

## 5.2.3   ESD handling ratings

| Symbol | Description | Min. | Max. | Unit | Notes |
|--------|-------------|------|------|------|-------|
| $V_{HBM}$ | Electrostatic discharge voltage, human body model | -2000 | +2000 | V | 1 |
| $V_{CDM}$ | Electrostatic discharge voltage, charged-device model | -500 | +500 | V | 2 |
| $I_{LAT}$ | Latch-up current at ambient temperature of 105°C | -100 | +100 | mA | 3 |

1. Determined according to JEDEC Standard JESD22-A114, *Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)*.
2. Determined according to JEDEC Standard JESD22-C101, *Field-Induced Charged-Device Model Test Method for Electrostatic-Discharge-Withstand Thresholds of Microelectronic Components*.
3. Determined according to JEDEC Standard JESD78, *IC Latch-Up Test*.

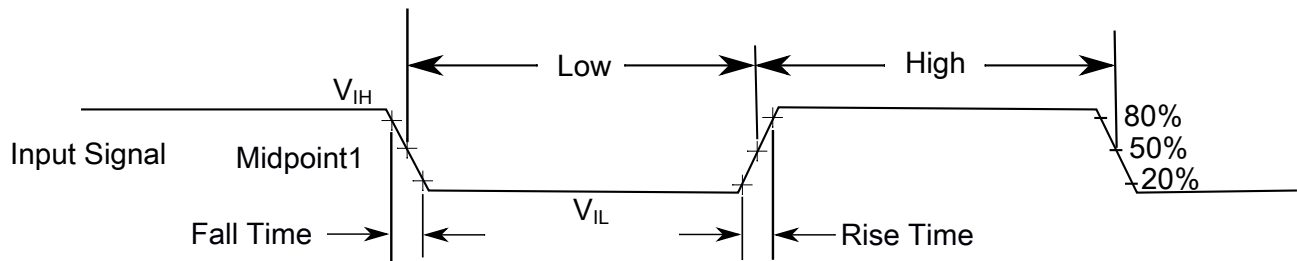## 5.2.4   Voltage and current operating ratings

### Table 39.   Voltage and current operating ratings

| Symbol | Description | Min. | Max. | Unit |
|--------|-------------|------|------|------|
| $V_{DD}$ | Digital supply voltage | −0.3 | 3.8 | V |
| $I_{DD}$ | Digital supply current | — | 120 | mA |
| $V_{IO}$ | IO pin input voltage | −0.3 | $V_{DD} + 0.3$ | V |
| $I_D$ | Instantaneous maximum current single pin limit (applies to all port pins) | −25 | 25 | mA |
| $V_{DDA}$ | Analog supply voltage | $V_{DD} - 0.3$ | $V_{DD} + 0.3$ | V |
| $V_{USB\_DP}$ | USB_DP input voltage | −0.3 | 3.63 | V |
| $V_{USB\_DM}$ | USB_DM input voltage | −0.3 | 3.63 | V |
| $V_{BAT}$ | RTC battery supply voltage | −0.3 | 3.8 | V |

# 5.3   General

## 5.3.1 AC electrical characteristics

Unless otherwise specified, propagation delays are measured from the 50% to the 50% point, and rise and fall times are measured at the 20% and 80% points, as shown in the following figure.



The midpoint is $V_{IL} + (V_{IH} - V_{IL}) / 2$

**Figure 15. Input signal measurement reference**

All digital I/O switching characteristics, unless otherwise specified, assume that the output pins have the following characteristics.

- $C_L$=30 pF loads
- Slew rate disabled
- Normal drive strength

## 5.3.2 Nonswitching electrical specifications

### 5.3.2.1 Voltage and current operating requirements

**Table 40. Voltage and current operating requirements**

| Symbol | Description | Min. | Max. | Unit | Notes |
|---|---|---|---|---|---|
| $V_{DD}$ | Supply voltage | 1.71 | 3.6 | V | |
| $V_{DDA}$ | Analog supply voltage | 1.71 | 3.6 | V | |
| $V_{DD} - V_{DDA}$ | $V_{DD}$-to-$V_{DDA}$ differential voltage | −0.1 | 0.1 | V | |
| $V_{SS} - V_{SSA}$ | $V_{SS}$-to-$V_{SSA}$ differential voltage | −0.1 | 0.1 | V | |
| $V_{BAT}$ | RTC battery supply voltage | 1.71 | 3.6 | V | |
| $USBV_{DD}$ | USB Transceiver supply voltage | 3.0 | 3.6 | V | 1 |
| $V_{IH}$ | Input high voltage | $0.7 \times V_{DD}$ | — | V | |
| | • 2.7 V ≤ $V_{DD}$ ≤ 3.6 V | $0.75 \times V_{DD}$ | — | V | |
| | • 1.7 V ≤ $V_{DD}$ ≤ 2.7 V | | | | |

*Table continues on the next page...*

**Table 40. Voltage and current operating requirements (continued)**

| Symbol | Description | Min. | Max. | Unit | Notes |
|---|---|---|---|---|---|
| $V_{IL}$ | Input low voltage | — | $0.35 \times V_{DD}$ | V | |
| | • $2.7\ V \leq V_{DD} \leq 3.6\ V$ | — | $0.3 \times V_{DD}$ | V | |
| | • $1.7\ V \leq V_{DD} \leq 2.7\ V$ | | | | |
| $V_{HYS}$ | Input hysteresis | $0.06 \times V_{DD}$ | — | V | |
| $I_{ICIO}$ | Analog and I/O pin DC injection current — single pin | | | | 2 |
| | • $V_{IN} < V_{SS}$-0.3V (Negative current injection) | -3 | — | mA | |
| $I_{ICcont}$ | Contiguous pin DC injection current —regional limit, includes sum of negative injection currents or sum of positive injection currents of 16 contiguous pins | | | | |
| | • Negative current injection | -25 | — | mA | |
| $V_{ODPU}$ | Open drain pullup voltage level | $V_{DD}$ | $V_{DD}$ | V | 3 |
| $V_{RAM}$ | $V_{DD}$ voltage required to retain RAM | 1.2 | — | V | |
| $V_{RFVBAT}$ | $V_{BAT}$ voltage required to retain the VBAT register file | $V_{POR\_VBAT}$ | — | V | |

1. USB nominal operating voltage is 3.3 V.
2. All analog and I/O pins are internally clamped to $V_{SS}$ through ESD protection diodes. If $V_{IN}$ is less than $V_{IO\_MIN}$ or greater than $V_{IO\_MAX}$, a current limiting resistor is required. The negative DC injection current limiting resistor is calculated as $R=(V_{IO\_MIN}-V_{IN})/|I_{ICIO}|$.
3. Open drain outputs must be pulled to VDD.

## 5.3.2.2 HVD, LVD and POR operating requirements
**Table 41. $V_{DD}$ supply HVD, LVD and POR operating requirements**

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| $V_{HVDH}$ | High Voltage Detect (High Trip Point) | — | 3.72 | — | V | |
| $V_{HVDL}$ | High Voltage Detect (Low Trip Point) | — | 3.46 | — | V | |
| $V_{POR}$ | Falling VDD POR detect voltage | 0.8 | 1.1 | 1.5 | V | |
| $V_{LVDH}$ | Falling low-voltage detect threshold — high range (LVDV=01) | 2.48 | 2.56 | 2.64 | V | |
| | Low-voltage warning thresholds — high range | | | | | 1 |
| $V_{LVW1H}$ | • Level 1 falling (LVWV=00) | 2.62 | 2.70 | 2.78 | V | |
| $V_{LVW2H}$ | • Level 2 falling (LVWV=01) | 2.72 | 2.80 | 2.88 | V | |
| $V_{LVW3H}$ | • Level 3 falling (LVWV=10) | 2.82 | 2.90 | 2.98 | V | |
| $V_{LVW4H}$ | • Level 4 falling (LVWV=11) | 2.92 | 3.00 | 3.08 | V | |
| $V_{HYSH}$ | Low-voltage inhibit reset/recover hysteresis — high range | — | 80 | — | mV | |
| $V_{LVDL}$ | Falling low-voltage detect threshold — low range (LVDV=00) | 1.54 | 1.60 | 1.66 | V | |
| | Low-voltage warning thresholds — low range | | | | | 1 |

*Table continues on the next page...*

**Table 41. V$_{DD}$ supply HVD, LVD and POR operating requirements (continued)**

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| V$_{LVW1L}$ | • Level 1 falling (LVWV=00) | 1.74 | 1.80 | 1.86 | V | |
| V$_{LVW2L}$ | • Level 2 falling (LVWV=01) | 1.84 | 1.90 | 1.96 | V | |
| V$_{LVW3L}$ | • Level 3 falling (LVWV=10) | 1.94 | 2.00 | 2.06 | V | |
| V$_{LVW4L}$ | • Level 4 falling (LVWV=11) | 2.04 | 2.10 | 2.16 | V | |
| V$_{HYSL}$ | Low-voltage inhibit reset/recover hysteresis — low range | — | 60 | — | mV | |
| V$_{BG}$ | Bandgap voltage reference | 0.97 | 1.00 | 1.03 | V | |
| t$_{LPO}$ | Internal low power oscillator period — factory trimmed | 900 | 1000 | 1100 | µs | |

1. Rising threshold is the sum of falling threshold and hysteresis voltage

**Table 42. VBAT power operating requirements**

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| V$_{POR\_VBAT}$ | Falling VBAT supply POR detect voltage | 0.8 | 1.1 | 1.5 | V | |

## 5.3.2.3  Voltage and current operating behaviors

**Table 43. Voltage and current operating behaviors**

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| V$_{OH}$ | Output high voltage — Normal drive pad except RESET_B | | | | | |
| | 2.7 V ≤ V$_{DD}$ ≤ 3.6 V, I$_{OH}$ = -5 mA | V$_{DD}$ – 0.5 | — | — | V | 1 |
| | 1.71 V ≤ V$_{DD}$ ≤ 2.7 V, I$_{OH}$ = -2.5 mA | V$_{DD}$ – 0.5 | — | — | V | |
| V$_{OH}$ | Output high voltage — High drive pad except RESET_B | | | | | |
| | 2.7 V ≤ V$_{DD}$ ≤ 3.6 V, I$_{OH}$ = -20 mA | V$_{DD}$ – 0.5 | — | — | V | 1 |
| | 1.71 V ≤ V$_{DD}$ ≤ 2.7 V, I$_{OH}$ = -10 mA | V$_{DD}$ – 0.5 | — | — | V | |
| I$_{OHT}$ | Output high current total for all ports | — | — | 100 | mA | |
| V$_{OL}$ | Output low voltage — Normal drive pad except RESET_B | | | | | |
| | 2.7 V ≤ V$_{DD}$ ≤ 3.6 V, I$_{OL}$ = 5 mA | — | — | 0.5 | V | 1 |
| | 1.71 V ≤ V$_{DD}$ ≤ 2.7 V, I$_{OL}$ = 2.5 mA | — | — | 0.5 | V | |
| V$_{OL}$ | Output low voltage — High drive pad except RESET_B | | | | | |
| | 2.7 V ≤ V$_{DD}$ ≤ 3.6 V, I$_{OL}$ = 20 mA | — | — | 0.5 | V | 1 |
| | 1.71 V ≤ V$_{DD}$ ≤ 2.7 V, I$_{OL}$ = 10 mA | — | — | 0.5 | V | |
| V$_{OL}$ | Output low voltage — RESET_B | | | | | |
| | 2.7 V ≤ V$_{DD}$ ≤ 3.6 V, I$_{OL}$ = 3 mA | — | — | 0.5 | V | |

*Table continues on the next page...*

**Table 43.   Voltage and current operating behaviors (continued)**

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| | $1.71\text{ V} \le V_{DD} \le 2.7\text{ V}$, $I_{OL} = 1.5\text{ mA}$ | — | — | 0.5 | V | |
| $I_{OLT}$ | Output low current total for all ports | — | — | 100 | mA | |
| $I_{IN}$ | Input leakage current (per pin) for full temperature range | | | | | |
| | All pins other than high drive port pins | — | 0.002 | 0.5 | µA | 1, 2 |
| | High drive port pins | — | 0.004 | 0.5 | µA | |
| $I_{IN}$ | Input leakage current (total all pins) for full temperature range | — | — | 1.0 | µA | 2 |
| $R_{PU}$ | Internal pullup resistors | 20 | — | 50 | kΩ | 3 |
| $R_{PD}$ | Internal pulldown resistors | 20 | — | 50 | kΩ | 4 |

1.  PTB0, PTB1, PTD4, PTD5, PTD6, PTD7, PTC3, and PTC4 I/O have both high drive and normal drive capability selected by the associated PTx_PCRn[DSE] control bit. All other GPIOs are normal drive only.
2.  Measured at VDD=3.6V
3.  Measured at $V_{DD}$ supply voltage = $V_{DD}$ min and Vinput = $V_{SS}$
4.  Measured at $V_{DD}$ supply voltage = $V_{DD}$ min and Vinput = $V_{DD}$

## 5.3.2.4   Power mode transition operating behaviors

All specifications except $t_{POR}$ and VLLSx → RUN recovery times in the following table assume this clock configuration:

- CPU and system clocks = 80 MHz
- Bus clock = 40 MHz
- Flash clock = 20 MHz
- MCG mode: FEI

**Table 44.   Power mode transition operating behaviors**

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| $t_{POR}$ | After a POR event, amount of time from the point $V_{DD}$ reaches 1.71 V to execution of the first instruction across the operating temperature range of the chip. | — | — | 300 | µs | 1 |
| | • VLLS0 → RUN | — | — | 140 | µs | |
| | • VLLS1 → RUN | — | — | 140 | µs | |
| | • VLLS2 → RUN | — | — | 80 | µs | |
| | • VLLS3 → RUN | — | — | 80 | µs | |

*Table continues on the next page...*

**Table 44. Power mode transition operating behaviors (continued)**

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|--------|-------------|------|------|------|------|-------|
| | • LLS2 → RUN | — | — | 6 | µs | |
| | • LLS3 → RUN | — | — | 6 | µs | |
| | • VLPS → RUN | — | — | 5.7 | µs | |
| | • STOP → RUN | — | — | 5.7 | µs | |

1. Normal boot (FTFA_FOPT[LPBOOT]=1)

## 5.3.2.5  Power consumption operating behaviors

The maximum values stated in the following table represent the characterized results equivalent to the mean plus three times the standard deviation (mean + 3 sigma).

**NOTE**

The while(1) test is executed with flash cache enabled.

**Table 45. Power consumption operating behaviors**

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|--------|-------------|------|------|------|------|-------|
| $I_{DDA}$ | Analog supply current | — | — | See note | mA | 1 |
| $I_{DD\_HSRUN}$ | High Speed Run mode current - all peripheral clocks disabled, CoreMark benchmark code executing from flash | | | | | 2, 3, 4 |
| | @ 1.8V | — | 24.17 | 26.215 | mA | |
| | @ 3.0V | — | 24.20 | 26.292 | mA | |
| $I_{DD\_HSRUN}$ | High Speed Run mode current - all peripheral clocks disabled, code executing from flash | | | | | 2 |
| | @ 1.8V | — | 20.97 | 23.015 | mA | |
| | @ 3.0V | — | 20.97 | 23.062 | mA | |
| $I_{DD\_HSRUN}$ | High Speed Run mode current — all peripheral clocks enabled, code executing from flash | | | | | 5 |
| | @ 1.8V | — | 27.77 | 30.028 | mA | |
| | @ 3.0V | — | 27.79 | 30.083 | mA | |
| $I_{DD\_RUN}$ | Run mode current in Compute operation — CoreMark benchmark code executing from flash | | | | | 3, 4, 6 |
| | @ 1.8V | — | 15.58 | 16.790 | mA | |
| | @ 3.0V | — | 16.19 | 17.457 | mA | |

*Table continues on the next page...*

**Table 45. Power consumption operating behaviors (continued)**

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| $I_{DD\_RUN}$ | Run mode current in Compute operation — code executing from flash | | | | | 6 |
| | @ 1.8V | — | 13.38 | 14.590 | mA | |
| | @ 3.0V | — | 13.42 | 14.687 | mA | |
| $I_{DD\_RUN}$ | Run mode current — all peripheral clocks disabled, code executing from flash | | | | | 7 |
| | @ 1.8V | — | 13.81 | 15.087 | mA | |
| | @ 3.0V | | | | | |
| | • @ 25°C | — | 13.87 | 15.158 | mA | |
| | • @ -40°C | — | 13.72 | 15.050 | mA | |
| | • @ 70°C | — | 14.03 | 15.267 | mA | |
| | • @ 85°C | — | 14.12 | 15.347 | mA | |
| | • @ 105°C | — | 14.31 | 15.529 | mA | |
| $I_{DD\_RUN}$ | Run mode current — all peripheral clocks enabled, code executing from flash | | | | | 8 |
| | @ 1.8V | — | 18.00 | 20.042 | mA | |
| | @ 3.0V | | | | | |
| | • @ 25°C | — | 18.08 | 20.145 | mA | |
| | • @ -40°C | — | 17.88 | 20.022 | mA | |
| | • @ 70°C | — | 18.27 | 20.229 | mA | |
| | • @ 85°C | — | 18.35 | 20.321 | mA | |
| | • @ 105°C | — | 18.55 | 20.544 | mA | |
| $I_{DD\_RUN}$ | Run mode current — Compute operation, code executing from flash | | | | | 9 |
| | @ 1.8V | — | 12.68 | 13.763 | mA | |
| | @ 3.0V | | | | | |
| | • @ 25°C | — | 12.62 | 13.714 | mA | |
| | • @ -40°C | — | 12.53 | 13.652 | mA | |
| | • @ 70°C | — | 12.76 | 13.827 | mA | |
| | • @ 85°C | — | 12.84 | 13.895 | mA | |
| | • @ 105°C | — | 13.02 | 14.078 | mA | |
| $I_{DD\_WAIT}$ | Wait mode high frequency current at 3.0 V — all peripheral clocks disabled | — | 6.56 | 7.022 | mA | 7 |
| $I_{DD\_WAIT}$ | Wait mode reduced frequency current at 3.0 V — all peripheral clocks disabled | — | 3.80 | 4.118 | mA | 10 |

*Table continues on the next page...*

**Table 45. Power consumption operating behaviors (continued)**

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| $I_{DD\_VLPR}$ | Very-low-power run mode current in Compute operation — CoreMark benchmark code executing from flash | | | | | |
| | @ 1.8V | — | 967.09 | 1031.341 | µA | 3, 4, 11 |
| | @ 3.0V | — | 973.06 | 1040.294 | µA | |
| $I_{DD\_VLPR}$ | Very-low-power run mode current in Compute operation, code executing from flash | | | | | |
| | @ 1.8V | — | 449.10 | 513.351 | µA | 11 |
| | @ 3.0V | — | 462.61 | 529.844 | µA | |
| $I_{DD\_VLPR}$ | Very-low-power run mode current at 3.0 V — all peripheral clocks disabled | — | 520.34 | 592.022 | µA | 12 |
| $I_{DD\_VLPR}$ | Very-low-power run mode current at 3.0 V — all peripheral clocks enabled | — | 845.46 | 1005.706 | µA | 13 |
| $I_{DD\_VLPW}$ | Very-low-power wait mode current at 3.0 V — all peripheral clocks disabled | — | 240.81 | 269.275 | µA | 14 |
| $I_{DD\_STOP}$ | Stop mode current at 3.0 V | | | | | |
| | @ 25°C | — | 269.63 | 292.223 | µA | |
| | @ -40°C | — | 253.73 | 280.001 | µA | |
| | @ 70°C | — | 309.98 | 346.335 | µA | |
| | @ 85°C | — | 347.88 | 401.693 | µA | |
| | @ 105°C | — | 450.05 | 565.013 | µA | |
| $I_{DD\_VLPS}$ | Very-low-power stop mode current at 3.0 V | | | | | |
| | @ 25°C | — | 3.48 | 6.005 | µA | |
| | @ -40°C | — | 2.47 | 3.740 | µA | |
| | @ 70°C | — | 15.20 | 30.384 | µA | |
| | @ 85°C | — | 28.62 | 52.396 | µA | |
| | @ 105°C | — | 65.48 | 115.129 | µA | |
| $I_{DD\_LLS3}$ | Low leakage stop mode 3 current at 3.0 V | | | | | |
| | @ 25°C | — | 2.78 | 3.778 | µA | |
| | @ -40°C | — | 2.14 | 2.881 | µA | |
| | @ 70°C | — | 7.72 | 12.481 | µA | |
| | @ 85°C | — | 13.30 | 21.607 | µA | |
| | @ 105°C | — | 29.50 | 47.202 | µA | |
| $I_{DD\_LLS2}$ | Low leakage stop mode 2 current at 3.0 V | | | | | |
| | @ 25°C | — | 2.56 | 3.293 | µA | |
| | @ -40°C | — | 2.10 | 2.802 | µA | |
| | @ 70°C | — | 6.14 | 8.758 | µA | |
| | @ 85°C | — | 10.34 | 15.242 | µA | |
| | @ 105°C | — | 22.68 | 33.393 | µA | |
| $I_{DD\_VLLS3}$ | Very low-leakage stop mode 3 current at 3.0 V | | | | | |
| | @ 25°C | — | 2.01 | 2.769 | µA | |

*Table continues on the next page...*

## Table 45. Power consumption operating behaviors (continued)

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| | @ -40°C | — | 1.55 | 2.485 | μA | |
| | @ 70°C | — | 5.81 | 9.658 | μA | |
| | @ 85°C | — | 10.06 | 16.695 | μA | |
| | @ 105°C | — | 22.30 | 35.783 | μA | |
| $I_{DD\_VLLS2}$ | Very low-leakage stop mode 2 current at 3.0 V | | | | | |
| | @ 25°C | — | 1.76 | 2.298 | μA | |
| | @ -40°C | — | 1.51 | 1.963 | μA | |
| | @ 70°C | — | 3.73 | 5.221 | μA | |
| | @ 85°C | — | 6.12 | 8.624 | μA | |
| | @ 105°C | — | 13.22 | 18.408 | μA | |
| $I_{DD\_VLLS1}$ | Very low-leakage stop mode 1 current at 3.0 V | | | | | |
| | @ 25°C | — | 0.64 | 0.835 | μA | |
| | @ -40°C | — | 0.55 | 0.795 | μA | |
| | @ 70°C | — | 1.88 | 2.427 | μA | |
| | @ 85°C | — | 3.52 | 4.640 | μA | |
| | @ 105°C | — | 8.62 | 11.273 | μA | |
| $I_{DD\_VLLS0}$ | Very low-leakage stop mode 0 current at 3.0 V with POR detect circuit enabled | | | | | |
| | @ 25°C | — | 0.36 | 0.525 | μA | |
| | @ -40°C | — | 0.29 | 0.513 | μA | |
| | @ 70°C | — | 1.58 | 2.108 | μA | |
| | @ 85°C | — | 3.19 | 4.289 | μA | |
| | @ 105°C | — | 8.20 | 10.838 | μA | |
| $I_{DD\_VLLS0}$ | Very low-leakage stop mode 0 current at 3.0 V with POR detect circuit disabled | | | | | |
| | @ 25°C | — | 0.093 | 0.249 | μA | |
| | @ -40°C | — | 0.016 | 0.145 | μA | |
| | @ 70°C | — | 1.30 | 1.821 | μA | |
| | @ 85°C | — | 2.91 | 3.994 | μA | |
| | @ 105°C | — | 7.92 | 10.501 | μA | |
| $I_{DD\_VBAT}$ | Average current with RTC and 32kHz disabled at 3.0 V | | | | | $V_{DD}$ is off. |
| | @ 25°C | — | 0.21 | 0.245 | μA | |
| | @ -40°C | — | 0.14 | 0.163 | μA | |
| | @ 70°C | — | 1.15 | 1.498 | μA | |
| | @ 85°C | — | 2.44 | 3.596 | μA | |
| | @ 105°C | — | 6.49 | 9.557 | μA | |
| $I_{DD\_VBAT}$ | Average current when CPU is not accessing RTC registers at 3.0 V | | | | | $V_{DD}$ is off. |
| | • @ 25°C | — | 0.76 | 0.899 | μA | |

*Table continues on the next page...*

**Table 45.  Power consumption operating behaviors (continued)**

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|--------|-------------|------|------|------|------|-------|
|        | • @ -40°C   | —    | 0.63 | 0.745 | µA  |       |
|        | • @ 70°C    | —    | 1.80 | 2.346 | µA  |       |
|        | • @ 85°C    | —    | 3.11 | 4.575 | µA  |       |
|        | • @ 105°C   | —    | 7.24 | 10.653 | µA |       |

1. The analog supply current is the sum of the active or disabled current for each of the analog modules on the device. See each module's specification for its supply current.
2. 120MHz core and system clock, 60MHz bus clock, and 24MHz flash clock. MCG configured for PEE mode. All peripheral clocks disabled.
3. Cache on and prefetch on, low compiler optimization.
4. Coremark benchmark compiled using IAR 7.2 with optimization level high.
5. 120MHz core and system clock, 60MHz bus clock, and 24MHz flash clock. MCG configured for PEE mode. All peripheral clocks enabled.
6. 80 MHz core and system clock, 40 MHz bus clock, and 26.67 MHz flash clock. MCG configured for PEE mode. Compute operation.
7. 80MHz core and system clock, 40MHz bus clock, and 26.67MHz flash clock. MCG configured for FEI mode. All peripheral clocks disabled.
8. 80MHz core and system clock, 40MHz bus clock, and 26.67MHz flash clock. MCG configured for FEI mode. All peripheral clocks enabled.
9. 80MHz core and system clock, 40MHz bus clock, and 26.67MHz flash clock. MCG configured for FEI mode. Compute operation.
10. 25MHz core and system clock, 25MHz bus clock, and 25MHz flash clock. MCG configured for FEI mode.
11. 4 MHz core, system, and bus clock and 1MHz flash clock. MCG configured for BLPE mode. Compute operation. Code executing from flash.
12. 4 MHz core, system, and bus clock and 1MHz flash clock. MCG configured for BLPE mode. All peripheral clocks disabled. Code executing from flash.
13. 4 MHz core, system, and bus clock and 1MHz flash clock. MCG configured for BLPE mode. All peripheral clocks enabled but peripherals are not in active operation. Code executing from flash.
14. 4 MHz core, system, and bus clock and 1MHz flash clock. MCG configured for BLPE mode. All peripheral clocks disabled.

### 5.3.2.5.1  Diagram: Typical IDD_RUN operating behavior

The following data was measured under these conditions:

- MCG in FBE mode for 50 MHz and lower frequencies. MCG in FEE mode at frequencies between 50 MHz and 100MHz.
- No GPIOs toggled
- Code execution from flash with cache enabled
- For the ALLOFF curve, all peripheral clocks are disabled except FTFA
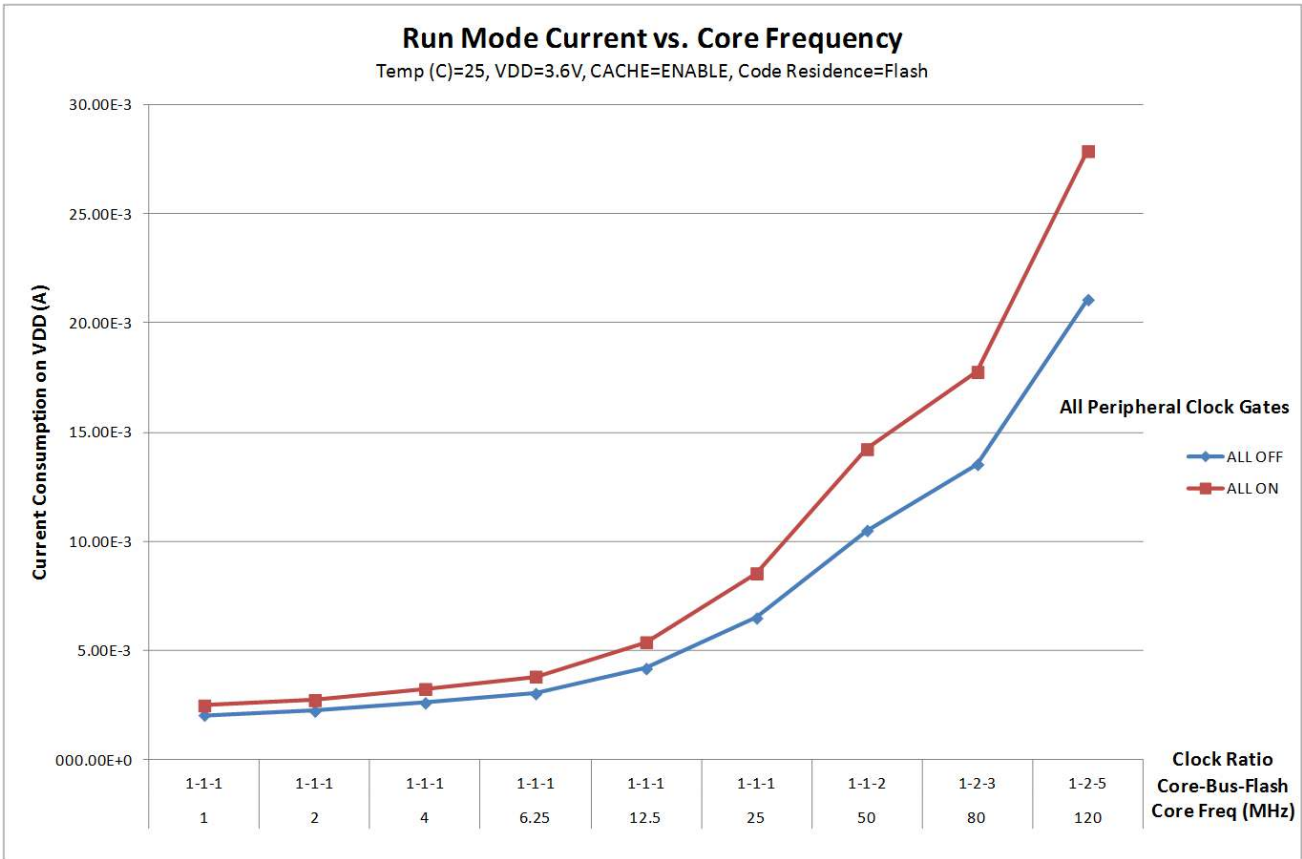
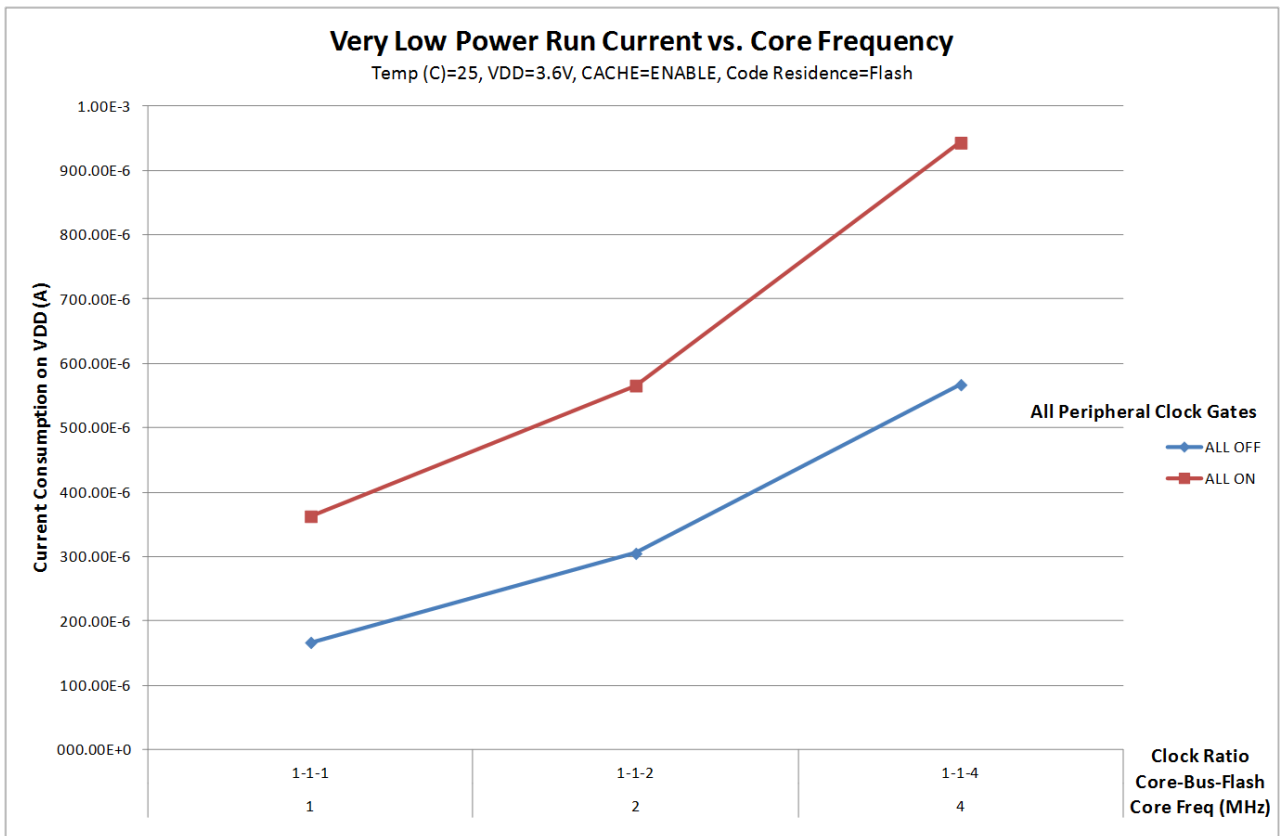**Figure 16. Run mode supply current vs. core frequency**

**Figure 17. VLPR mode supply current vs. core frequency**

## 5.3.2.6   EMC performance

Electromagnetic compatibility (EMC) performance is highly dependent on the environment in which the MCU resides. Board design and layout, circuit topology choices, location and characteristics of external components, and MCU software operation play a significant role in the EMC performance. The system designer can consult the following Freescale applications notes, available on freescale.com for advice and guidance specifically targeted at optimizing EMC performance.

- AN2321: Designing for Board Level Electromagnetic Compatibility
- AN1050: Designing for Electromagnetic Compatibility (EMC) with HCMOS Microcontrollers
- AN1263: Designing for Electromagnetic Compatibility with Single-Chip Microcontrollers

- AN2764: Improving the Transient Immunity Performance of Microcontroller-Based Applications
- AN1259: System Design and Layout Techniques for Noise Reduction in MCU-Based Systems

#### 5.3.2.6.1 EMC radiated emissions operating behaviors

**Table 46. EMC radiated emissions operating behaviors for 64 LQFP package**

| Parameter | Conditions | Clocks | Frequency range | Level (Typ.) | Unit | Notes |
|---|---|---|---|---|---|---|
| $V_{EME}$ | Device configuration, test conditions and EM testing per standard IEC 61967-2.<br><br>Supply voltages:<br>• VDD = 3.3 V<br><br>Temp = 25°C | FSYS = 120 MHz<br><br>FBUS = 60 MHz<br><br>External crystal = 8 MHz | 150 kHz–50 MHz | 14 | dBuV | 1, 2 |
| | | | 50 MHz–150 MHz | 23 | | |
| | | | 150 MHz–500 MHz | 23 | | |
| | | | 500 MHz–1000 MHz | 9 | | |
| | | | IEC level | L | | 3 |

1. Measurements were made per IEC 61967-2 while the device was running typical application code.
2. The reported emission level is the value of the maximum measured emission, rounded up to the next whole number, from among the measured orientations in each frequency range.
3. IEC Level Maximums: M ≤ 18dBmV, L ≤ 24dBmV, K ≤ 30dBmV, I ≤ 36dBmV, H ≤ 42dBmV .

#### 5.3.2.6.2 Designing with radiated emissions in mind

To find application notes that provide guidance on designing your system to minimize interference from radiated emissions:
1. Go to www.freescale.com.
2. Perform a keyword search for "EMC design."

### 5.3.2.7 Capacitance attributes

**Table 47. Capacitance attributes**

| Symbol | Description | Min. | Max. | Unit |
|---|---|---|---|---|
| $C_{IN\_A}$ | Input capacitance: analog pins | — | 7 | pF |
| $C_{IN\_D}$ | Input capacitance: digital pins | — | 7 | pF |

## 5.3.3 Switching specifications

## 5.3.3.1  Device clock specifications

**Table 48.   Device clock specifications**

| Symbol | Description | Min. | Max. | Unit |
|--------|-------------|------|------|------|
| High Speed run mode ||||||
| $f_{SYS}$ | System and core clock | — | 120 | MHz |
| $f_{BUS}$ | Bus clock | — | 60 | MHz |
| Normal run mode |||||
| $f_{SYS}$ | System and core clock | — | 80 | MHz |
| $f_{SYS\_USB}$ | System and core clock when Full Speed USB in operation | 20 | — | MHz |
| $f_{BUS}$ | Bus clock | — | 50 | MHz |
| $f_{FLASH}$ | Flash clock | — | 26.67 | MHz |
| $f_{LPTMR}$ | LPTMR clock | — | 25 | MHz |
| VLPR and VLPS modes[1] |||||
| $f_{SYS}$ | System and core clock | — | 4 | MHz |
| $f_{BUS}$ | Bus clock | — | 4 | MHz |
| $f_{FLASH}$ | Flash clock | — | 1 | MHz |
| $f_{ERCLK}$ | External reference clock | — | 16 | MHz |
| $f_{LPTMR\_pin}$ | LPTMR clock | — | 25 | MHz |
| $f_{LPTMR\_ERCLK}$ | LPTMR external reference clock | — | 16 | MHz |
| $f_{I2S\_MCLK}$ | I2S master clock | — | 12.5 | MHz |
| $f_{I2S\_BCLK}$ | I2S bit clock | — | 4 | MHz |
| $f_{FlexIO}$ | FlexIO clock | — | 16 | MHz |
| $f_{LPI2C}$ | LPI2C clock | — | 16 | MHz |
| $f_{FlexCAN}$ | FlexCAN clock | — | 4 | MHz |

1. The frequency limitations in VLPR and VLPS modes here override any frequency specification listed in the timing specification for any other module. These same frequency limits apply to VLPS, whether VLPS was entered from RUN or from VLPR.

## 5.3.3.2  General switching specifications

These general purpose specifications apply to all signals configured for GPIO, UART, and timers.

**Table 49.   General switching specifications**

| Symbol | Description | Min. | Max. | Unit | Notes |
|--------|-------------|------|------|------|-------|
| | GPIO pin interrupt pulse width (digital glitch filter disabled) — Synchronous path | 1.5 | — | Bus clock cycles | 1, 2 |
| | External RESET and NMI pin interrupt pulse width — Asynchronous path | 100 | — | ns | 3 |

*Table continues on the next page...*

**Table 49. General switching specifications (continued)**

| Symbol | Description | Min. | Max. | Unit | Notes |
|---|---|---|---|---|---|
| | GPIO pin interrupt pulse width (digital glitch filter disabled, passive filter disabled) — Asynchronous path | 50 | — | ns | 4 |
| | Port rise and fall time | | | | 5 |
| | • Slew disabled | — | | | |
| |     • $1.71 \leq V_{DD} \leq 2.7V$ | — | 10 | ns | |
| |     • $2.7 \leq V_{DD} \leq 3.6V$ | | 5 | ns | |
| | • Slew enabled | — | | | |
| |     • $1.71 \leq V_{DD} \leq 2.7V$ | — | 30 | ns | |
| |     • $2.7 \leq V_{DD} \leq 3.6V$ | | 16 | ns | |

1. This is the minimum pulse width that is guaranteed to pass through the pin synchronization circuitry. Shorter pulses may or may not be recognized. In Stop, VLPS, LLS, and VLLSx modes, the synchronizer is bypassed so shorter pulses can be recognized in that case.
2. The greater of synchronous and asynchronous timing must be met.
3. These pins have a passive filter enabled on the inputs. This is the shortest pulse width that is guaranteed to be recognized.
4. These pins do not have a passive filter on the inputs. This is the shortest pulse width that is guaranteed to be recognized.
5. 25 pF load

## 5.3.4 Thermal specification

### 5.3.4.1 Thermal operating requirements

**Table 50. Thermal operating requirements**

| Symbol | Description | Min. | Max. | Unit | Notes |
|---|---|---|---|---|---|
| $T_J$ | Die junction temperature | −40 | 125 | °C | |
| $T_A$ | Ambient temperature | −40 | 105 | °C | 1 |

1. Maximum $T_A$ can be exceeded only if the user ensures that $T_J$ does not exceed maximum $T_J$. The simplest method to determine $T_J$ is: $T_J = T_A + R_{\Theta JA} \times$ chip power dissipation.

### 5.3.4.2 Thermal attributes

**Table 51. Thermal attributes**

| Board type | Symbol | Description | 100 LQFP | 64 LQFP | 48 QFN | Unit | Notes |
|---|---|---|---|---|---|---|---|
| Single-layer (1s) | $R_{\Theta JA}$ | Thermal resistance, junction to ambient (natural convection) | 58 | 61 | 81 | °C/W | 1, 2, 3 |

*Table continues on the next page...*

**Table 51.  Thermal attributes (continued)**

| Board type | Symbol | Description | 100 LQFP | 64 LQFP | 48 QFN | Unit | Notes |
|---|---|---|---|---|---|---|---|
| Four-layer (2s2p) | $R_{\theta JA}$ | Thermal resistance, junction to ambient (natural convection) | 46 | 43 | 28 | °C/W | 1, 2, 3,4 |
| Single-layer (1s) | $R_{\theta JMA}$ | Thermal resistance, junction to ambient (200 ft./min. air speed) | 48 | 49 | 66 | °C/W | 1, 4, 5 |
| Four-layer (2s2p) | $R_{\theta JMA}$ | Thermal resistance, junction to ambient (200 ft./min. air speed) | 40 | 36 | 23 | °C/W | 1, 4, 5 |
| — | $R_{\theta JB}$ | Thermal resistance, junction to board | 31 | 25 | 11 | °C/W | 6 |
| — | $R_{\theta JC}$ | Thermal resistance, junction to case | 16 | 13 | 1.3 | °C/W | 7 |
| — | $\Psi_{JT}$ | Thermal characterization parameter, junction to package top outside center (natural convection) | 2 | 2 | 2 | °C/W | 8 |
| — | $\Psi_{JB}$ | Thermal characterization parameter, junction to package bottom (natural convection) | - | - | - | °C/W | 9 |

1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Per SEMI G38-87 and JEDEC JESD51-2 with the single layer board horizontal.
3. Per JEDEC JESD51-2 with natural convection for horizontally oriented board. Board meets JESD51-9 specification for 1s or 2s2p board, respectively.
4. Per JEDEC JESD51-6 with the board horizontal.
5. Per JEDEC JESD51-6 with forced convection for horizontally oriented board. Board meets JESD51-9 specification for 1s or 2s2p board, respectively.
6. Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
7. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).
8. Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.
9. Thermal characterization parameter indicating the temperature difference between package bottom center and the junction temperature per JEDEC JESD51-12. When Greek letters are not available, the thermal characterization parameter is written as Psi-JB.

# 5.4  Peripheral operating requirements and behaviors

## 5.4.1  Debug modules

## 5.4.1.1  SWD electricals

### Table 52.  SWD full voltage range electricals

| Symbol | Description | Min. | Max. | Unit |
|---|---|---|---|---|
| | Operating voltage | 1.71 | 3.6 | V |
| S1 | SWD_CLK frequency of operation<br><br>• Serial wire debug | <br><br>0 | <br><br>33 | <br><br>MHz |
| S2 | SWD_CLK cycle period | 1/S1 | — | ns |
| S3 | SWD_CLK clock pulse width<br><br>• Serial wire debug | <br><br>15 | <br><br>— | <br><br>ns |
| S4 | SWD_CLK rise and fall times | — | 3 | ns |
| S9 | SWD_DIO input data setup time to SWD_CLK rise | 8 | — | ns |
| S10 | SWD_DIO input data hold time after SWD_CLK rise | 1.4 | — | ns |
| S11 | SWD_CLK high to SWD_DIO data valid | — | 25 | ns |
| S12 | SWD_CLK high to SWD_DIO high-Z | 5 | — | ns |
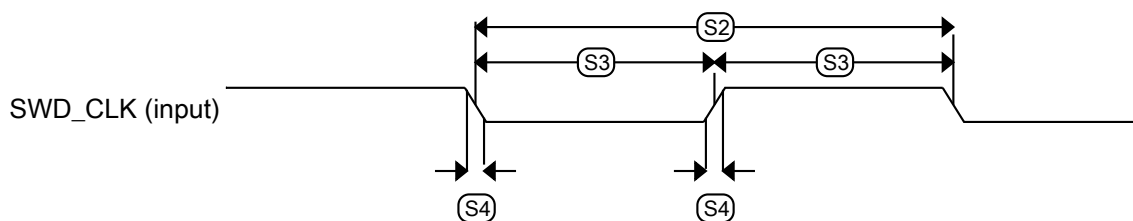


**Figure 18. Serial wire clock input timing**
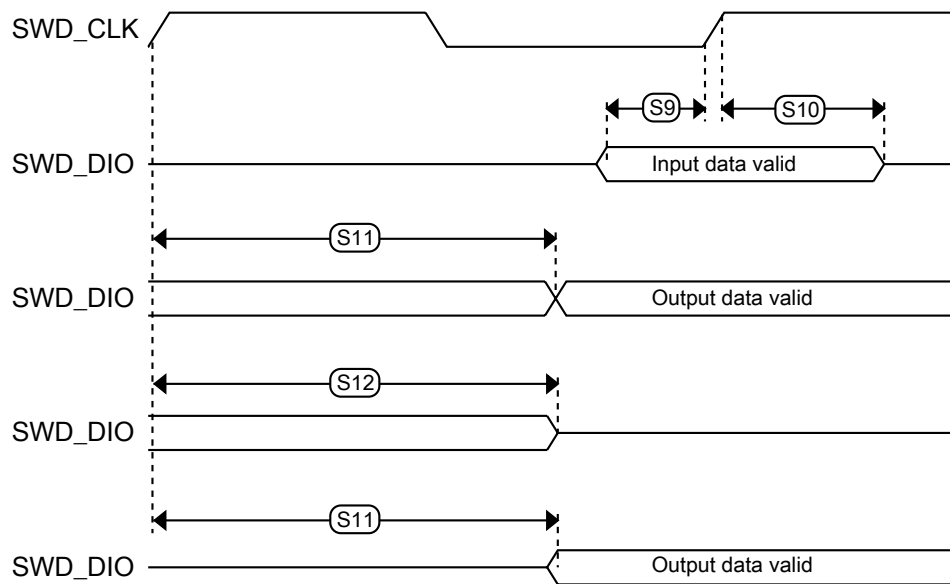
**Figure 19. Serial wire data timing**

## 5.4.1.2 JTAG electricals
### Table 53. JTAG limited voltage range electricals

| Symbol | Description | Min. | Max. | Unit |
|--------|-------------|------|------|------|
| | Operating voltage | 2.7 | 3.6 | V |
| J1 | TCLK frequency of operation | | | MHz |
| | • Boundary Scan | 0 | 10 | |
| | • JTAG and CJTAG | 0 | 20 | |
| J2 | TCLK cycle period | 1/J1 | — | ns |
| J3 | TCLK clock pulse width | | | |
| | • Boundary Scan | 50 | — | ns |
| | • JTAG and CJTAG | 25 | — | ns |
| J4 | TCLK rise and fall times | — | 3 | ns |
| J5 | Boundary scan input data setup time to TCLK rise | 20 | — | ns |
| J6 | Boundary scan input data hold time after TCLK rise | 1 | — | ns |
| J7 | TCLK low to boundary scan output data valid | — | 25 | ns |
| J8 | TCLK low to boundary scan output high-Z | — | 25 | ns |
| J9 | TMS, TDI input data setup time to TCLK rise | 8 | — | ns |
| J10 | TMS, TDI input data hold time after TCLK rise | 1 | — | ns |

*Table continues on the next page...*

**Table 53.   JTAG limited voltage range electricals (continued)**

| Symbol | Description | Min. | Max. | Unit |
|--------|-------------|------|------|------|
| J11 | TCLK low to TDO data valid | — | 19 | ns |
| J12 | TCLK low to TDO high-Z | — | 19 | ns |
| J13 | TRST assert time | 100 | — | ns |
| J14 | TRST setup time (negation) to TCLK high | 8 | — | ns |

**Table 54.   JTAG full voltage range electricals**

| Symbol | Description | Min. | Max. | Unit |
|--------|-------------|------|------|------|
|  | Operating voltage | 1.71 | 3.6 | V |
| J1 | TCLK frequency of operation |  |  | MHz |
|  | • Boundary Scan | 0 | 10 |  |
|  | • JTAG and CJTAG | 0 | 15 |  |
| J2 | TCLK cycle period | 1/J1 | — | ns |
| J3 | TCLK clock pulse width |  |  |  |
|  | • Boundary Scan | 50 | — | ns |
|  | • JTAG and CJTAG | 33 | — | ns |
| J4 | TCLK rise and fall times | — | 3 | ns |
| J5 | Boundary scan input data setup time to TCLK rise | 20 | — | ns |
| J6 | Boundary scan input data hold time after TCLK rise | 1.4 | — | ns |
| J7 | TCLK low to boundary scan output data valid | — | 27 | ns |
| J8 | TCLK low to boundary scan output high-Z | — | 27 | ns |
| J9 | TMS, TDI input data setup time to TCLK rise | 8 | — | ns |
| J10 | TMS, TDI input data hold time after TCLK rise | 1.4 | — | ns |
| J11 | TCLK low to TDO data valid | — | 26.2 | ns |
| J12 | TCLK low to TDO high-Z | — | 26.2 | ns |
| J13 | TRST assert time | 100 | — | ns |
| J14 | TRST setup time (negation) to TCLK high | 8 | — | ns |
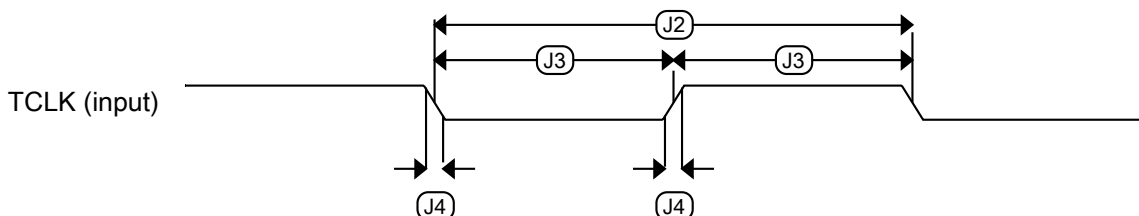


**Figure 20. Test clock input timing**

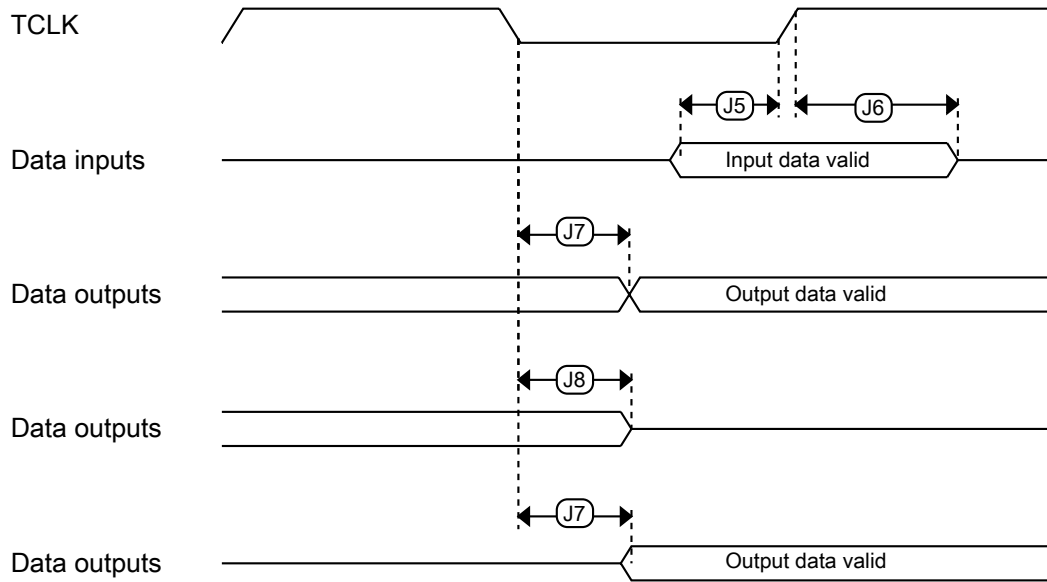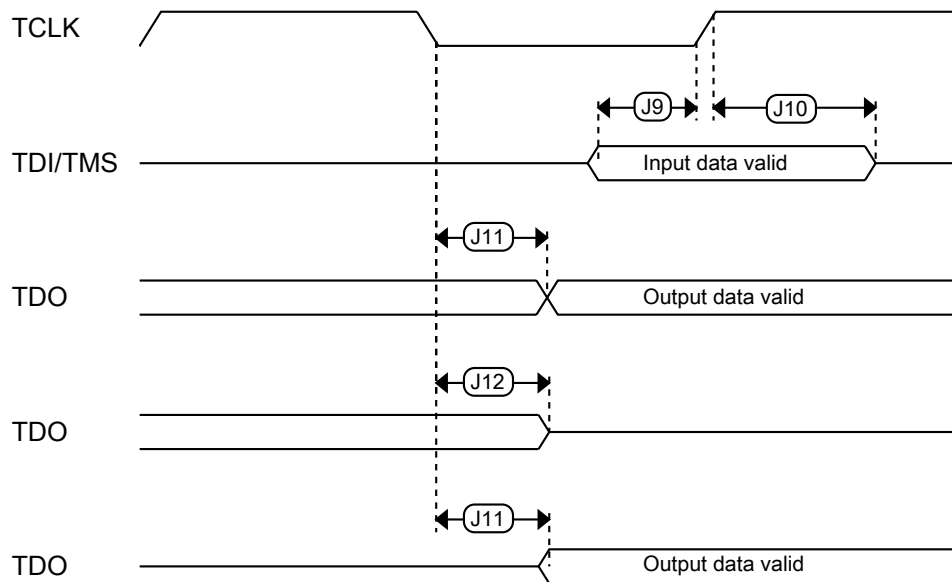**Figure 21. Boundary scan (JTAG) timing**
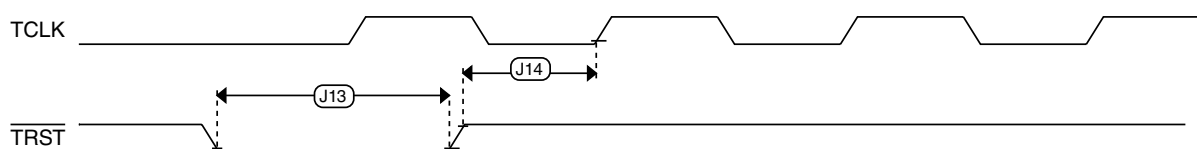


**Figure 22. Test Access Port timing**

**Figure 23. $\overline{\text{TRST}}$ timing**

## 5.4.2 System modules

There are no specifications necessary for the device's system modules.

## 5.4.3 Clock modules

### 5.4.3.1 MCG specifications

**Table 55. MCG specifications**

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| $f_{ints\_ft}$ | Internal reference frequency (slow clock) — factory trimmed at nominal VDD and 25 °C | — | 32.768 | — | kHz | |
| $\Delta f_{ints\_t}$ | Total deviation of internal reference frequency (slow clock) over voltage and temperature | — | +0.5/-0.7 | ± 2 | % | |
| $f_{ints\_t}$ | Internal reference frequency (slow clock) — user trimmed | 31.25 | — | 39.0625 | kHz | |
| $\Delta_{fdco\_res\_t}$ | Resolution of trimmed average DCO output frequency at fixed voltage and temperature — using SCTRIM and SCFTRIM | — | ± 0.3 | ± 0.6 | %$f_{dco}$ | 1 |
| $\Delta f_{dco\_t}$ | Total deviation of trimmed average DCO output frequency over voltage and temperature | — | +0.5/-0.7 | ± 2 | %$f_{dco}$ | 1, 2 |
| $\Delta f_{dco\_t}$ | Total deviation of trimmed average DCO output frequency over fixed voltage and temperature range of 0–70°C | — | ± 0.3 | ± 1.5 | %$f_{dco}$ | 1 |
| $f_{intf\_ft}$ | Internal reference frequency (fast clock) — factory trimmed at nominal VDD and 25°C | — | 4 | — | MHz | |
| $\Delta f_{intf\_ft}$ | Frequency deviation of internal reference clock (fast clock) over temperature and voltage — factory trimmed at nominal VDD and 25 °C | — | +1/-2 | ± 5 | %$f_{intf\_ft}$ | |
| $f_{intf\_t}$ | Internal reference frequency (fast clock) — user trimmed at nominal VDD and 25 °C | 3 | — | 5 | MHz | |
| $f_{loc\_low}$ | Loss of external clock minimum frequency — RANGE = 00 | (3/5) x $f_{ints\_t}$ | — | — | kHz | |

*Table continues on the next page...*

## Table 55.  MCG specifications (continued)

| Symbol | Description | | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|---|
| $f_{loc\_high}$ | Loss of external clock minimum frequency — RANGE = 01, 10, or 11 | | (16/5) x $f_{ints\_t}$ | — | — | kHz | |
| FLL | | | | | | | |
| $f_{fll\_ref}$ | FLL reference frequency range | | 31.25 | — | 39.0625 | kHz | |
| $f_{dco}$ | DCO output frequency range | Low range (DRS=00) $640 \times f_{fll\_ref}$ | 20 | 20.97 | 25 | MHz | 3, 4 |
| | | Mid range (DRS=01) $1280 \times f_{fll\_ref}$ | 40 | 41.94 | 50 | MHz | |
| | | Mid-high range (DRS=10) $1920 \times f_{fll\_ref}$ | 60 | 62.91 | 75 | MHz | |
| | | High range (DRS=11) $2560 \times f_{fll\_ref}$ | 80 | 83.89 | 100 | MHz | |
| $f_{dco\_t\_DMX32}$ | DCO output frequency | Low range (DRS=00) $732 \times f_{fll\_ref}$ | — | 23.99 | — | MHz | 5, 6 |
| | | Mid range (DRS=01) $1464 \times f_{fll\_ref}$ | — | 47.97 | — | MHz | |
| | | Mid-high range (DRS=10) $2197 \times f_{fll\_ref}$ | — | 71.99 | — | MHz | |
| | | High range (DRS=11) $2929 \times f_{fll\_ref}$ | — | 95.98 | — | MHz | |
| $J_{cyc\_fll}$ | FLL period jitter <br> • $f_{VCO}$ = 48 MHz <br> • $f_{VCO}$ = 98 MHz | | — <br> — | — <br> 180 <br> 150 | — <br> — | ps | |
| $t_{fll\_acquire}$ | FLL target frequency acquisition time | | — | — | 1 | ms | 7 |
| PLL | | | | | | | |
| $f_{vco}$ | VCO operating frequency | | 48.0 | — | 120 | MHz | |
| $I_{pll}$ | PLL operating current <br> • PLL @ 96 MHz ($f_{osc\_hi\_1}$ = 8 MHz, $f_{pll\_ref}$ = 2 MHz, VDIV multiplier = 48) | | — | 1060 | — | µA | 8 |
| $I_{pll}$ | PLL operating current <br> • PLL @ 48 MHz ($f_{osc\_hi\_1}$ = 8 MHz, $f_{pll\_ref}$ = 2 MHz, VDIV multiplier = 24) | | — | 600 | — | µA | 8 |
| $f_{pll\_ref}$ | PLL reference frequency range | | 2.0 | — | 4.0 | MHz | |
| $J_{cyc\_pll}$ | PLL period jitter (RMS) <br> • $f_{vco}$ = 48 MHz <br> • $f_{vco}$ = 100 MHz | | — <br> — | 120 <br> 75 | — <br> — | ps <br> ps | 9 |
| $J_{acc\_pll}$ | PLL accumulated jitter over 1µs (RMS) | | — <br> — | 1350 <br> 600 | — <br> — | ps <br> ps | 9 |

*Table continues on the next page...*

**Table 55. MCG specifications (continued)**

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|--------|-------------|------|------|------|------|-------|
| | • $f_{vco}$ = 48 MHz | | | | | |
| | • $f_{vco}$ = 100 MHz | | | | | |
| $D_{lock}$ | Lock entry frequency tolerance | ± 1.49 | — | ± 2.98 | % | |
| $D_{unl}$ | Lock exit frequency tolerance | ± 4.47 | — | ± 5.97 | % | |
| $t_{pll\_lock}$ | Lock detector detection time | — | — | $150 \times 10^{-6}$ + 1075(1/ $f_{pll\_ref}$) | s | 10 |

1. This parameter is measured with the internal reference (slow clock) being used as a reference to the FLL (FEI clock mode).
2. 2.0 V <= VDD <= 3.6 V.
3. These typical values listed are with the slow internal reference clock (FEI) using factory trim and DMX32=0.
4. The resulting system clock frequencies should not exceed their maximum specified values. The DCO frequency deviation ($\Delta f_{dco\_t}$) over voltage and temperature should be considered.
5. These typical values listed are with the slow internal reference clock (FEI) using factory trim and DMX32=1.
6. The resulting clock frequency must not exceed the maximum specified clock frequency of the device.
7. This specification applies to any time the FLL reference source or reference divider is changed, trim value is changed, DMX32 bit is changed, DRS bits are changed, or changing from FLL disabled (BLPE, BLPI) to FLL enabled (FEI, FEE, FBE, FBI). If a crystal/resonator is being used as the reference, this specification assumes it is already running.
8. Excludes any oscillator currents that are also consuming power while PLL is in operation.
9. This specification was obtained using a NXP developed PCB. PLL jitter is dependent on the noise characteristics of each PCB and results will vary.
10. This specification applies to any time the PLL VCO divider or reference divider is changed, or changing from PLL disabled (BLPE, BLPI) to PLL enabled (PBE, PEE). If a crystal/resonator is being used as the reference, this specification assumes it is already running.

## 5.4.3.2 IRC48M specifications

**Table 56. IRC48M specifications**

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|--------|-------------|------|------|------|------|-------|
| $V_{DD}$ | Supply voltage | 1.71 | — | 3.6 | V | |
| $I_{DD48M}$ | Supply current | — | 400 | 500 | µA | |
| $f_{irc48m}$ | Internal reference frequency | — | 48 | — | MHz | |
| $\Delta f_{irc48m\_ol\_hv}$ | Open loop total deviation of IRC48M frequency at high voltage (VDD=1.89V-3.6V) over 0°C to 70°C | — | | | | |
| | Regulator enable (USB_CLK_RECOVER_IRC_EN[REG_EN]=1) | — | ± 0.2 | ± 0.5 | %$f_{irc48m}$ | 1 |
| $\Delta f_{irc48m\_ol\_hv}$ | Open loop total deviation of IRC48M frequency at high voltage (VDD=1.89V-3.6V) over full temperature | | | | | |
| | Regulator enable (USB_CLK_RECOVER_IRC_EN[REG_EN]=1) | — | ± 0.4 | ± 1.0 | %$f_{irc48m}$ | 1 |
| $\Delta f_{irc48m\_ol\_lv}$ | Open loop total deviation of IRC48M frequency at low voltage (VDD=1.71V-1.89V) over full temperature | | | | | 1 |
| | Regulator disable (USB_CLK_RECOVER_IRC_EN[REG_EN]=0) | — | ± 0.4 | ± 1.0 | %$f_{irc48m}$ | |

*Table continues on the next page...*

## Table 56. IRC48M specifications (continued)

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| | Regulator enable (USB_CLK_RECOVER_IRC_EN[REG_EN]=1) | — | ± 0.5 | ± 1.5 | | |
| $\Delta f_{irc48m\_cl}$ | Closed loop total deviation of IRC48M frequency over voltage and temperature | — | — | ± 0.1 | %$f_{host}$ | 2 |
| $J_{cyc\_irc48m}$ | Period Jitter (RMS) | — | 35 | 150 | ps | |
| $t_{irc48mst}$ | Startup time | — | 2 | 3 | µs | 3 |

1. The maximum value represents characterized results equivalent to the mean plus or minus three times the standard deviation (mean ± 3 sigma).
2. Closed loop operation of the IRC48M is only feasible for USB device operation; it is not usable for USB host operation. It is enabled by configuring for USB Device, selecting IRC48M as USB clock source, and enabling the clock recover function (USB_CLK_RECOVER_IRC_CTRL[CLOCK_RECOVER_EN]=1, USB_CLK_RECOVER_IRC_EN[IRC_EN]=1).
3. IRC48M startup time is defined as the time between clock enablement and clock availability for system use. Enable the clock by one of the following settings:
   - USB_CLK_RECOVER_IRC_EN[IRC_EN]=1 or
   - MCG operating in an external clocking mode and MCG_C7[OSCSEL]=10 or MCG_C5[PLLCLKEN0]=1, or
   - SIM_SOPT2[PLLFLLSEL]=11

## 5.4.3.3 Oscillator electrical specifications

### 5.4.3.3.1 Oscillator DC electrical specifications
#### Table 57. Oscillator DC electrical specifications

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| $V_{DD}$ | Supply voltage | 1.71 | — | 3.6 | V | |
| $I_{DDOSC}$ | Supply current — low-power mode (HGO=0) | | | | | 1 |
| | • 32 kHz | — | 500 | — | nA | |
| | • 4 MHz | — | 200 | — | µA | |
| | • 8 MHz (RANGE=01) | — | 300 | — | µA | |
| | • 16 MHz | — | 950 | — | µA | |
| | • 24 MHz | — | 1.2 | — | mA | |
| | • 32 MHz | — | 1.5 | — | mA | |
| $I_{DDOSC}$ | Supply current — high-gain mode (HGO=1) | | | | | 1 |
| | • 32 kHz | — | 25 | — | µA | |
| | • 4 MHz | — | 400 | — | µA | |
| | • 8 MHz (RANGE=01) | — | 500 | — | µA | |
| | • 16 MHz | — | 2.5 | — | mA | |
| | | — | 3 | — | mA | |

*Table continues on the next page...*

## Table 57.  Oscillator DC electrical specifications (continued)

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| | • 24 MHz | — | 4 | — | mA | |
| | • 32 MHz | | | | | |
| $C_x$ | EXTAL load capacitance | — | — | — | | 2, 3 |
| $C_y$ | XTAL load capacitance | — | — | — | | 2, 3 |
| $R_F$ | Feedback resistor — low-frequency, low-power mode (HGO=0) | — | — | — | MΩ | 2, 4 |
| | Feedback resistor — low-frequency, high-gain mode (HGO=1) | — | 10 | — | MΩ | |
| | Feedback resistor — high-frequency, low-power mode (HGO=0) | — | — | — | MΩ | |
| | Feedback resistor — high-frequency, high-gain mode (HGO=1) | — | 1 | — | MΩ | |
| $R_S$ | Series resistor — low-frequency, low-power mode (HGO=0) | — | — | — | kΩ | |
| | Series resistor — low-frequency, high-gain mode (HGO=1) | — | 200 | — | kΩ | |
| | Series resistor — high-frequency, low-power mode (HGO=0) | — | — | — | kΩ | |
| | Series resistor — high-frequency, high-gain mode (HGO=1) | — | 0 | — | kΩ | |
| $V_{pp}$[5] | Peak-to-peak amplitude of oscillation (oscillator mode) — low-frequency, low-power mode (HGO=0) | — | 0.6 | — | V | |
| | Peak-to-peak amplitude of oscillation (oscillator mode) — low-frequency, high-gain mode (HGO=1) | — | $V_{DD}$ | — | V | |
| | Peak-to-peak amplitude of oscillation (oscillator mode) — high-frequency, low-power mode (HGO=0) | — | 0.6 | — | V | |
| | Peak-to-peak amplitude of oscillation (oscillator mode) — high-frequency, high-gain mode (HGO=1) | — | $V_{DD}$ | — | V | |

1.  $V_{DD}$=3.3 V, Temperature =25 °C
2.  See crystal or resonator manufacturer's recommendation
3.  $C_x$ and $C_y$ can be provided by using either integrated capacitors or external components.
4.  When low-power mode is selected, $R_F$ is integrated and must not be attached externally.
5.  The EXTAL and XTAL pins should only be connected to required oscillator components and must not be connected to any other device.

### 5.4.3.3.2 Oscillator frequency specifications

**Table 58. Oscillator frequency specifications**

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| $f_{osc\_lo}$ | Oscillator crystal or resonator frequency — low-frequency mode (MCG_C2[RANGE]=00) | 32 | — | 40 | kHz | |
| $f_{osc\_hi\_1}$ | Oscillator crystal or resonator frequency — high-frequency mode (low range) (MCG_C2[RANGE]=01) | 3 | — | 8 | MHz | |
| $f_{osc\_hi\_2}$ | Oscillator crystal or resonator frequency — high frequency mode (high range) (MCG_C2[RANGE]=1x) | 8 | — | 32 | MHz | |
| $f_{ec\_extal}$ | Input clock frequency (external clock mode) | — | — | 50 | MHz | 1, 2 |
| $t_{dc\_extal}$ | Input clock duty cycle (external clock mode) | 40 | 50 | 60 | % | |
| $t_{cst}$ | Crystal startup time — 32 kHz low-frequency, low-power mode (HGO=0) | — | 750 | — | ms | 3, 4 |
| | Crystal startup time — 32 kHz low-frequency, high-gain mode (HGO=1) | — | 250 | — | ms | |
| | Crystal startup time — 8 MHz high-frequency (MCG_C2[RANGE]=01), low-power mode (HGO=0) | — | 0.6 | — | ms | |
| | Crystal startup time — 8 MHz high-frequency (MCG_C2[RANGE]=01), high-gain mode (HGO=1) | — | 1 | — | ms | |

1. Other frequency limits may apply when external clock is being used as a reference for the FLL or PLL.
2. When transitioning from FEI or FBI to FBE mode, restrict the frequency of the input clock so that, when it is divided by FRDIV, it remains within the limits of the DCO input clock frequency.
3. Proper PC board layout procedures must be followed to achieve specifications.
4. Crystal startup time is defined as the time between the oscillator being enabled and the OSCINIT bit in the MCG_S register being set.

## 5.4.3.4 32 kHz oscillator electrical characteristics

### 5.4.3.4.1 32 kHz oscillator DC electrical specifications

**Table 59. 32kHz oscillator DC electrical specifications**

| Symbol | Description | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| $V_{BAT}$ | Supply voltage | 1.71 | — | 3.6 | V |
| $R_F$ | Internal feedback resistor | — | 100 | — | MΩ |
| $C_{para}$ | Parasitical capacitance of EXTAL32 and XTAL32 | — | 5 | 7 | pF |
| $V_{pp}$[1] | Peak-to-peak amplitude of oscillation | — | 0.6 | — | V |

1. When a crystal is being used with the 32 kHz oscillator, the EXTAL32 and XTAL32 pins should only be connected to required oscillator components and must not be connected to any other devices.

### 5.4.3.4.2  32 kHz oscillator frequency specifications

**Table 60.  32 kHz oscillator frequency specifications**

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| $f_{osc\_lo}$ | Oscillator crystal | — | 32.768 | — | kHz | |
| $t_{start}$ | Crystal start-up time | — | 1000 | — | ms | 1 |
| $f_{ec\_extal32}$ | Externally provided input clock frequency | — | 32.768 | — | kHz | 2 |
| $v_{ec\_extal32}$ | Externally provided input clock amplitude | 700 | — | $V_{BAT}$ | mV | 2, 3 |

1. Proper PC board layout procedures must be followed to achieve specifications.
2. This specification is for an externally supplied clock driven to EXTAL32 and does not apply to any other clock input. The oscillator remains enabled and XTAL32 must be left unconnected.
3. The parameter specified is a peak-to-peak value and $V_{IH}$ and $V_{IL}$ specifications do not apply. The voltage of the applied clock must be within the range of $V_{SS}$ to $V_{BAT}$.

## 5.4.4   Memories and memory interfaces

## 5.4.4.1   Flash electrical specifications

This section describes the electrical characteristics of the flash memory module.

### 5.4.4.1.1   Flash timing specifications — program and erase

The following specifications represent the amount of time the internal charge pumps are active and do not include command overhead.

**Table 61.  NVM program/erase timing specifications**

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| $t_{hvpgm4}$ | Longword Program high-voltage time | — | 7.5 | 18 | µs | — |
| $t_{hversscr}$ | Sector Erase high-voltage time | — | 13 | 113 | ms | 1 |
| $t_{hversall}$ | Erase All high-voltage time | — | 104 | 904 | ms | 1 |

1. Maximum time based on expectations at cycling end-of-life.

### 5.4.4.1.2   Flash timing specifications — commands

**Table 62.  Flash command timing specifications**

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| $t_{rd1sec2k}$ | Read 1s Section execution time (flash sector) | — | — | 60 | µs | 1 |
| $t_{pgmchk}$ | Program Check execution time | — | — | 45 | µs | 1 |
| $t_{rdrsrc}$ | Read Resource execution time | — | — | 30 | µs | 1 |

*Table continues on the next page...*

**Table 62. Flash command timing specifications (continued)**

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|--------|-------------|------|------|------|------|-------|
| $t_{pgm4}$ | Program Longword execution time | — | 65 | 145 | µs | — |
| $t_{ersscr}$ | Erase Flash Sector execution time | — | 14 | 114 | ms | 2 |
| $t_{rd1all}$ | Read 1s All Blocks execution time | — | — | 1.8 | ms | 1 |
| $t_{rdonce}$ | Read Once execution time | — | — | 30 | µs | 1 |
| $t_{pgmonce}$ | Program Once execution time | — | 100 | — | µs | — |
| $t_{ersall}$ | Erase All Blocks execution time | — | 175 | 1300 | ms | 2 |
| $t_{vfykey}$ | Verify Backdoor Access Key execution time | — | — | 30 | µs | 1 |

1. Assumes 25 MHz flash clock frequency.
2. Maximum times for erase parameters based on expectations at cycling end-of-life.

### 5.4.4.1.3  Flash high voltage current behaviors
**Table 63. Flash high voltage current behaviors**

| Symbol | Description | Min. | Typ. | Max. | Unit |
|--------|-------------|------|------|------|------|
| $I_{DD\_PGM}$ | Average current adder during high voltage flash programming operation | — | 2.5 | 6.0 | mA |
| $I_{DD\_ERS}$ | Average current adder during high voltage flash erase operation | — | 1.5 | 4.0 | mA |

### 5.4.4.1.4  Reliability specifications
**Table 64. NVM reliability specifications**

| Symbol | Description | Min. | Typ.[1] | Max. | Unit | Notes |
|--------|-------------|------|------|------|------|-------|
| Program Flash | | | | | | |
| $t_{nvmretp10k}$ | Data retention after up to 10 K cycles | 5 | 50 | — | years | — |
| $t_{nvmretp1k}$ | Data retention after up to 1 K cycles | 20 | 100 | — | years | — |
| $n_{nvmcycp}$ | Cycling endurance | 10 K | 50 K | — | cycles | 2 |

1. Typical data retention values are based on measured response accelerated at high temperature and derated to a constant 25 °C use profile. Engineering Bulletin EB618 does not apply to this technology. Typical endurance defined in Engineering Bulletin EB619.
2. Cycling endurance represents number of program/erase cycles at $-40\ °C \le T_j \le 125\ °C$.

## 5.4.5  Security and integrity modules

There are no specifications necessary for the device's security and integrity modules.

## 5.4.6   Analog

### 5.4.6.1   ADC electrical specifications

The 16-bit accuracy specifications listed in Table 65 and Table 66 are achievable on the differential pins ADCx_DPx, ADCx_DMx.

All other ADC channels meet the 13-bit differential/12-bit single-ended accuracy specifications.

#### 5.4.6.1.1   16-bit ADC operating conditions
**Table 65.   16-bit ADC operating conditions**

| Symbol | Description | Conditions | Min. | Typ.[1] | Max. | Unit | Notes |
|---|---|---|---|---|---|---|---|
| $V_{DDA}$ | Supply voltage | Absolute | 1.71 | — | 3.6 | V | |
| $\Delta V_{DDA}$ | Supply voltage | Delta to $V_{DD}$ ($V_{DD} - V_{DDA}$) | -100 | 0 | +100 | mV | 2 |
| $\Delta V_{SSA}$ | Ground voltage | Delta to $V_{SS}$ ($V_{SS} - V_{SSA}$) | -100 | 0 | +100 | mV | 2 |
| $V_{REFH}$ | ADC reference voltage high | | 1.13 | $V_{DDA}$ | $V_{DDA}$ | V | |
| $V_{REFL}$ | ADC reference voltage low | | $V_{SSA}$ | $V_{SSA}$ | $V_{SSA}$ | V | |
| $V_{ADIN}$ | Input voltage | • 16-bit differential mode<br><br>• All other modes | VREFL<br><br>VREFL | —<br><br>— | 31/32 * VREFH<br><br>VREFH | V | |
| $C_{ADIN}$ | Input capacitance | • 16-bit mode<br><br>• 8-bit / 10-bit / 12-bit modes | —<br><br>— | 8<br><br>4 | 10<br><br>5 | pF | |
| $R_{ADIN}$ | Input series resistance | | — | 2 | 5 | kΩ | |
| $R_{AS}$ | Analog source resistance (external) | 13-bit / 12-bit modes<br>$f_{ADCK}$ < 4 MHz | — | — | 5 | kΩ | 3 |
| $f_{ADCK}$ | ADC conversion clock frequency | ≤ 13-bit mode | 1.0 | — | 24.0 | MHz | 4 |
| $f_{ADCK}$ | ADC conversion clock frequency | 16-bit mode | 2.0 | — | 12.0 | MHz | 4 |
| $C_{rate}$ | ADC conversion rate | ≤ 13-bit modes<br><br>No ADC hardware averaging<br><br>Continuous conversions enabled, subsequent conversion time | 20 | — | 1200 | Ksps | 5 |
| $C_{rate}$ | ADC conversion rate | 16-bit mode<br><br>No ADC hardware averaging | 37 | — | 461 | Ksps | 5 |

### Table 65.  16-bit ADC operating conditions

| Symbol | Description | Conditions | Min. | Typ.[1] | Max. | Unit | Notes |
|--------|-------------|-----------|------|---------|------|------|-------|
|        |             | Continuous conversions enabled, subsequent conversion time |  |  |  |  |  |

1. Typical values assume $V_{DDA}$ = 3.0 V, Temp = 25 °C, $f_{ADCK}$ = 1.0 MHz, unless otherwise stated. Typical values are for reference only, and are not tested in production.
2. DC potential difference.
3. This resistance is external to MCU. To achieve the best results, the analog source resistance must be kept as low as possible. The results in this data sheet were derived from a system that had < 8 Ω analog source resistance. The $R_{AS}/C_{AS}$ time constant should be kept to < 1 ns.
4. To use the maximum ADC conversion clock frequency, CFG2[ADHSC] must be set and CFG1[ADLPC] must be clear.
5. For guidelines and examples of conversion rate calculation, download the ADC calculator tool.
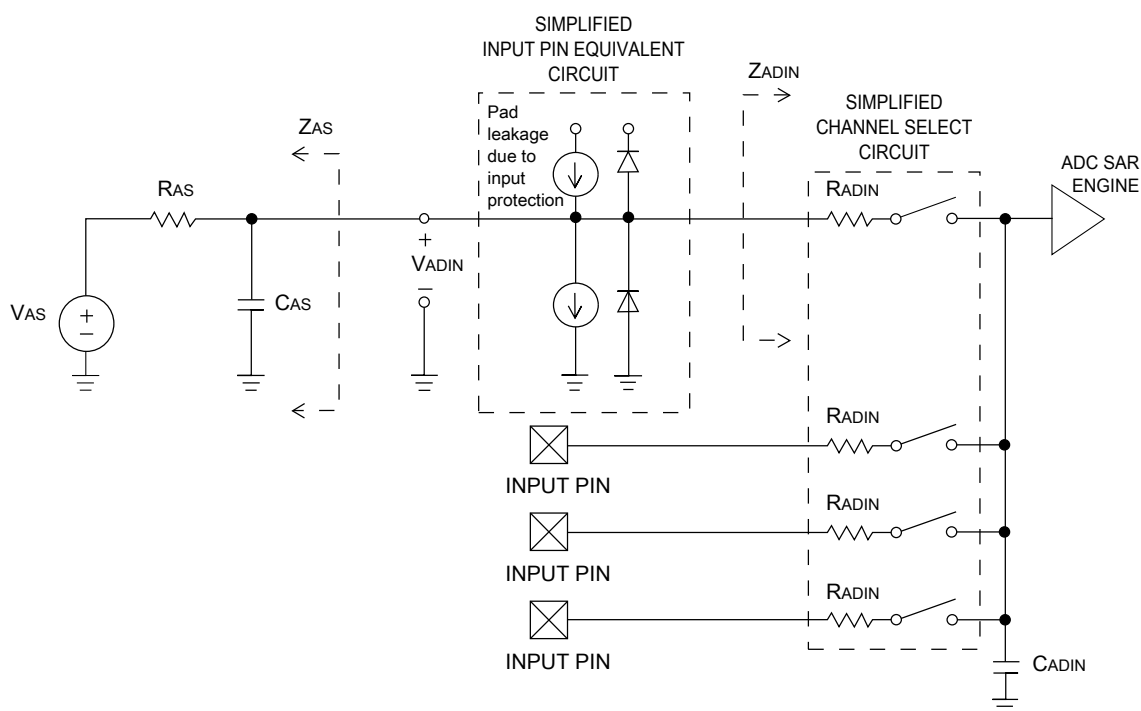


**Figure 24. ADC input impedance equivalency diagram**

## 5.4.6.1.2   16-bit ADC electrical characteristics

### Table 66.  16-bit ADC characteristics ($V_{REFH}$ = $V_{DDA}$, $V_{REFL}$ = $V_{SSA}$)

| Symbol | Description | Conditions[1] | Min. | Typ.[2] | Max. | Unit | Notes |
|--------|-------------|---------------|------|---------|------|------|-------|
| $I_{DDA\_ADC}$ | Supply current |  | 0.215 | — | 1.7 | mA | 3 |
| $f_{ADACK}$ | ADC asynchronous clock source | • ADLPC = 1, ADHSC = 0 | 1.2 | 2.4 | 3.9 | MHz | $t_{ADACK}$ = 1/ $f_{ADACK}$ |

*Table continues on the next page...*

### Table 66.   16-bit ADC characteristics (V$_{REFH}$ = V$_{DDA}$, V$_{REFL}$ = V$_{SSA}$) (continued)

| Symbol | Description | Conditions[1] | Min. | Typ.[2] | Max. | Unit | Notes |
|--------|-------------|---------------|------|---------|------|------|-------|
| | | • ADLPC = 1, ADHSC = 1 | 2.4 | 4.0 | 6.1 | MHz | |
| | | • ADLPC = 0, ADHSC = 0 | 3.0 | 5.2 | 7.3 | MHz | |
| | | • ADLPC = 0, ADHSC = 1 | 4.4 | 6.2 | 9.5 | MHz | |
| | Sample Time | See Reference Manual chapter for sample times | | | | | |
| TUE | Total unadjusted error | • 12-bit modes | — | ±4 | ±6.8 | LSB[4] | 5 |
| | | • <12-bit modes | — | ±1.4 | ±2.1 | | |
| DNL | Differential non-linearity | • 12-bit modes | — | ±0.7 | −1.1 to +1.9 | LSB[4] | 5 |
| | | • <12-bit modes | — | ±0.2 | −0.3 to 0.5 | | |
| INL | Integral non-linearity | • 12-bit modes | — | ±1.0 | −2.7 to +1.9 | LSB[4] | 5 |
| | | • <12-bit modes | — | ±0.5 | −0.7 to +0.5 | | |
| E$_{FS}$ | Full-scale error | • 12-bit modes | — | −4 | −5.4 | LSB[4] | V$_{ADIN}$ = V$_{DDA}$[5] |
| | | • <12-bit modes | — | −1.4 | −1.8 | | |
| E$_Q$ | Quantization error | • 16-bit modes | — | −1 to 0 | — | LSB[4] | |
| | | • ≤13-bit modes | — | — | ±0.5 | | |
| ENOB | Effective number of bits | 16-bit differential mode | | | | | 6 |
| | | • Avg = 32 | 12.8 | 14.5 | — | bits | |
| | | • Avg = 4 | 11.9 | 13.8 | — | bits | |
| | | 16-bit single-ended mode | | | | | |
| | | • Avg = 32 | 12.2 | 13.9 | — | bits | |
| | | • Avg = 4 | 11.4 | 13.1 | — | bits | |
| SINAD | Signal-to-noise plus distortion | See ENOB | 6.02 × ENOB + 1.76 | | | dB | |
| THD | Total harmonic distortion | 16-bit differential mode | | | | dB | 7 |
| | | • Avg = 32 | — | -94 | — | dB | |
| | | 16-bit single-ended mode | | | | | |
| | | • Avg = 32 | — | -85 | — | | |
| SFDR | Spurious free dynamic range | 16-bit differential mode | | | | dB | 7 |
| | | • Avg = 32 | 82 | 95 | — | dB | |
| | | 16-bit single-ended mode | | | | | |
| | | • Avg = 32 | 78 | 90 | — | | |

*Table continues on the next page...*

### Table 66. 16-bit ADC characteristics ($V_{REFH}$ = $V_{DDA}$, $V_{REFL}$ = $V_{SSA}$) (continued)

| Symbol | Description | Conditions[1] | Min. | Typ.[2] | Max. | Unit | Notes |
|---|---|---|---|---|---|---|---|
| $E_{IL}$ | Input leakage error | | | $I_{In} \times R_{AS}$ | | mV | $I_{In}$ = leakage current (refer to the MCU's voltage and current operating ratings) |
| | Temp sensor slope | Across the full temperature range of the device | 1.55 | 1.62 | 1.69 | mV/°C | 8 |
| $V_{TEMP25}$ | Temp sensor voltage | 25 °C | 706 | 716 | 726 | mV | 8 |

1. All accuracy numbers assume the ADC is calibrated with $V_{REFH}$ = $V_{DDA}$
2. Typical values assume $V_{DDA}$ = 3.0 V, Temp = 25 °C, $f_{ADCK}$ = 2.0 MHz unless otherwise stated. Typical values are for reference only and are not tested in production.
3. The ADC supply current depends on the ADC conversion clock speed, conversion rate and ADC_CFG1[ADLPC] (low power). For lowest power operation, ADC_CFG1[ADLPC] must be set, the ADC_CFG2[ADHSC] bit must be clear with 1 MHz ADC conversion clock speed.
4. 1 LSB = ($V_{REFH}$ - $V_{REFL}$)/$2^N$
5. ADC conversion clock < 16 MHz, Max hardware averaging (AVGE = %1, AVGS = %11)
6. Input data is 100 Hz sine wave. ADC conversion clock < 12 MHz.
7. Input data is 1 kHz sine wave. ADC conversion clock < 12 MHz.
8. ADC conversion clock < 3 MHz



Typical ADC 16-bit Differential ENOB vs ADC Clock
100Hz, 90% FS Sine Input
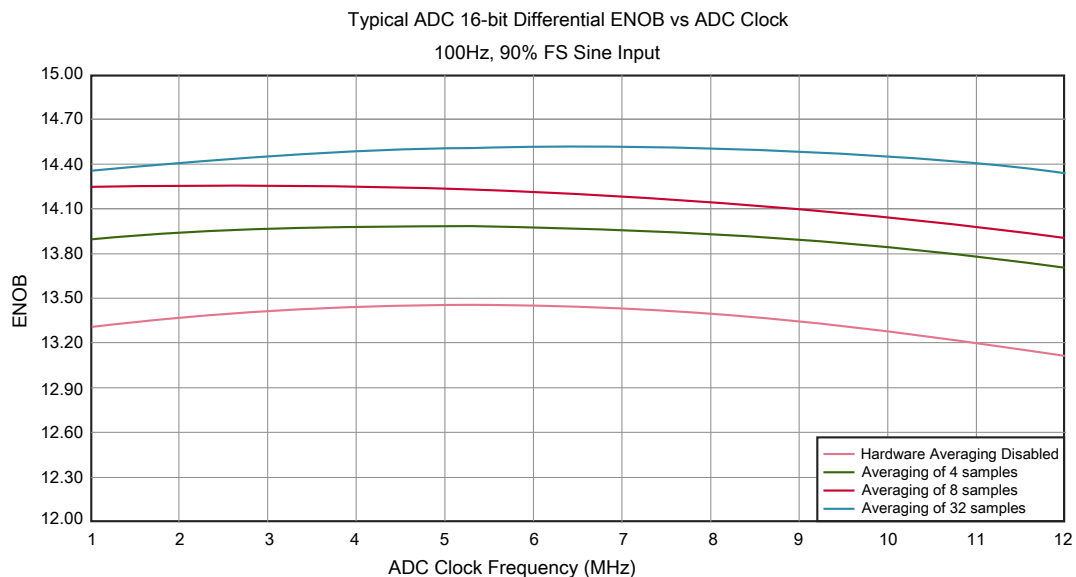
**Figure 25. Typical ENOB vs. ADC_CLK for 16-bit differential mode**
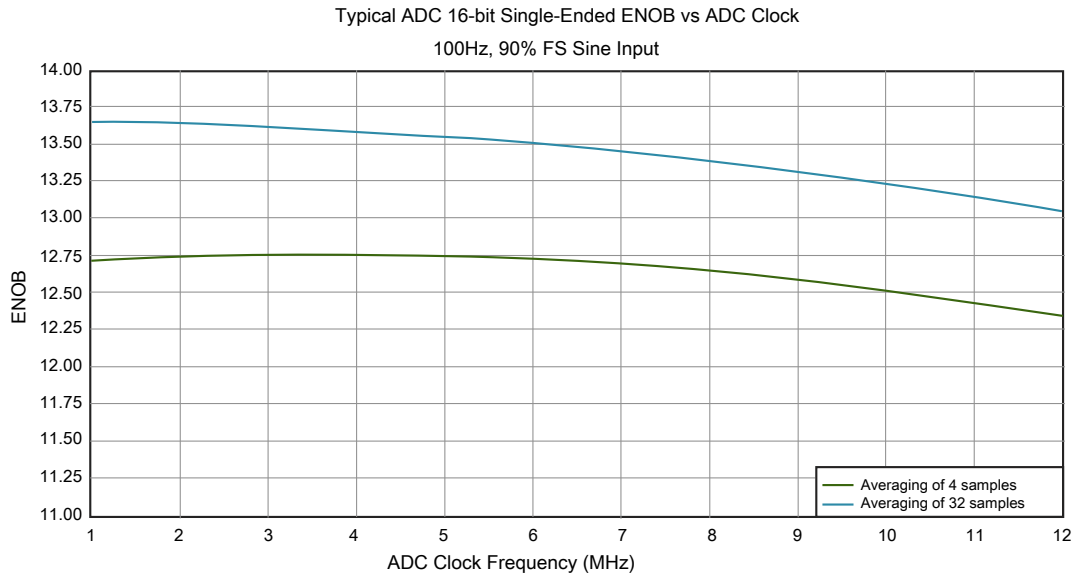
**Figure 26. Typical ENOB vs. ADC_CLK for 16-bit single-ended mode**

## 5.4.6.2 CMP and 6-bit DAC electrical specifications

### Table 67. Comparator and 6-bit DAC electrical specifications

| Symbol | Description | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| $V_{DD}$ | Supply voltage | 1.71 | — | 3.6 | V |
| $I_{DDHS}$ | Supply current, High-speed mode (EN=1, PMODE=1) | — | — | 200 | µA |
| $I_{DDLS}$ | Supply current, low-speed mode (EN=1, PMODE=0) | — | — | 20 | µA |
| $V_{AIN}$ | Analog input voltage | $V_{SS} - 0.3$ | — | $V_{DD}$ | V |
| $V_{AIO}$ | Analog input offset voltage | — | — | 20 | mV |
| $V_H$ | Analog comparator hysteresis[1] | | | | |
| | • CR0[HYSTCTR] = 00 | — | 5 | — | mV |
| | • CR0[HYSTCTR] = 01 | — | 10 | — | mV |
| | • CR0[HYSTCTR] = 10 | — | 20 | — | mV |
| | • CR0[HYSTCTR] = 11 | — | 30 | — | mV |
| $V_{CMPOh}$ | Output high | $V_{DD} - 0.5$ | — | — | V |
| $V_{CMPOl}$ | Output low | — | — | 0.5 | V |
| $t_{DHS}$ | Propagation delay, high-speed mode (EN=1, PMODE=1) | 20 | 50 | 200 | ns |
| $t_{DLS}$ | Propagation delay, low-speed mode (EN=1, PMODE=0) | 80 | 250 | 600 | ns |
| | Analog comparator initialization delay[2] | — | — | 40 | µs |
| $I_{DAC6b}$ | 6-bit DAC current adder (enabled) | — | 7 | — | µA |
| INL | 6-bit DAC integral non-linearity | −0.5 | — | 0.5 | LSB[3] |
| DNL | 6-bit DAC differential non-linearity | −0.3 | — | 0.3 | LSB |

1. Typical hysteresis is measured with input voltage range limited to 0.6 to $V_{DD}$–0.6 V.

2. Comparator initialization delay is defined as the time between software writes to change control inputs (Writes to CMP_DACCR[DACEN], CMP_DACCR[VRSEL], CMP_DACCR[VOSEL], CMP_MUXCR[PSEL], and CMP_MUXCR[MSEL]) and the comparator output settling to a stable level.

3. 1 LSB = $V_{reference}/64$
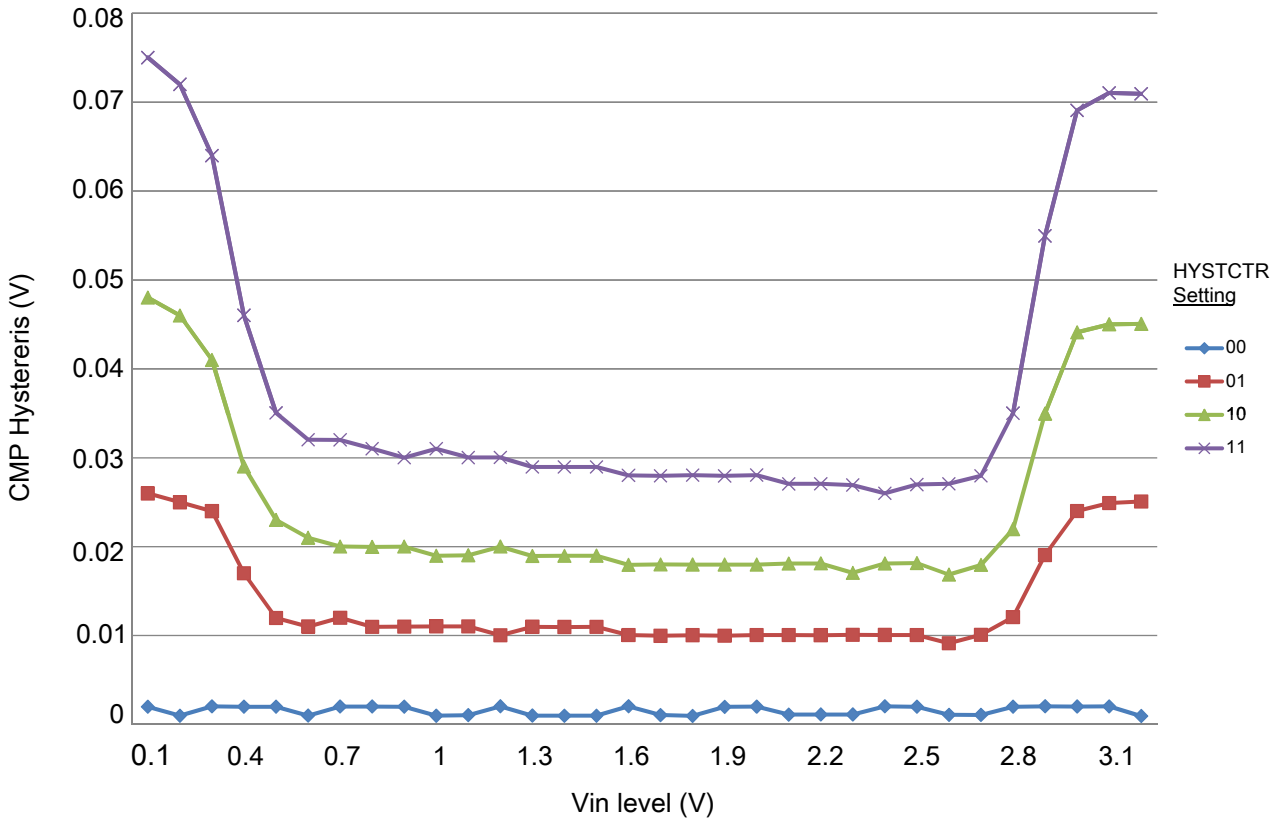


**Figure 27. Typical hysteresis vs. Vin level (VDD = 3.3 V, PMODE = 0)**
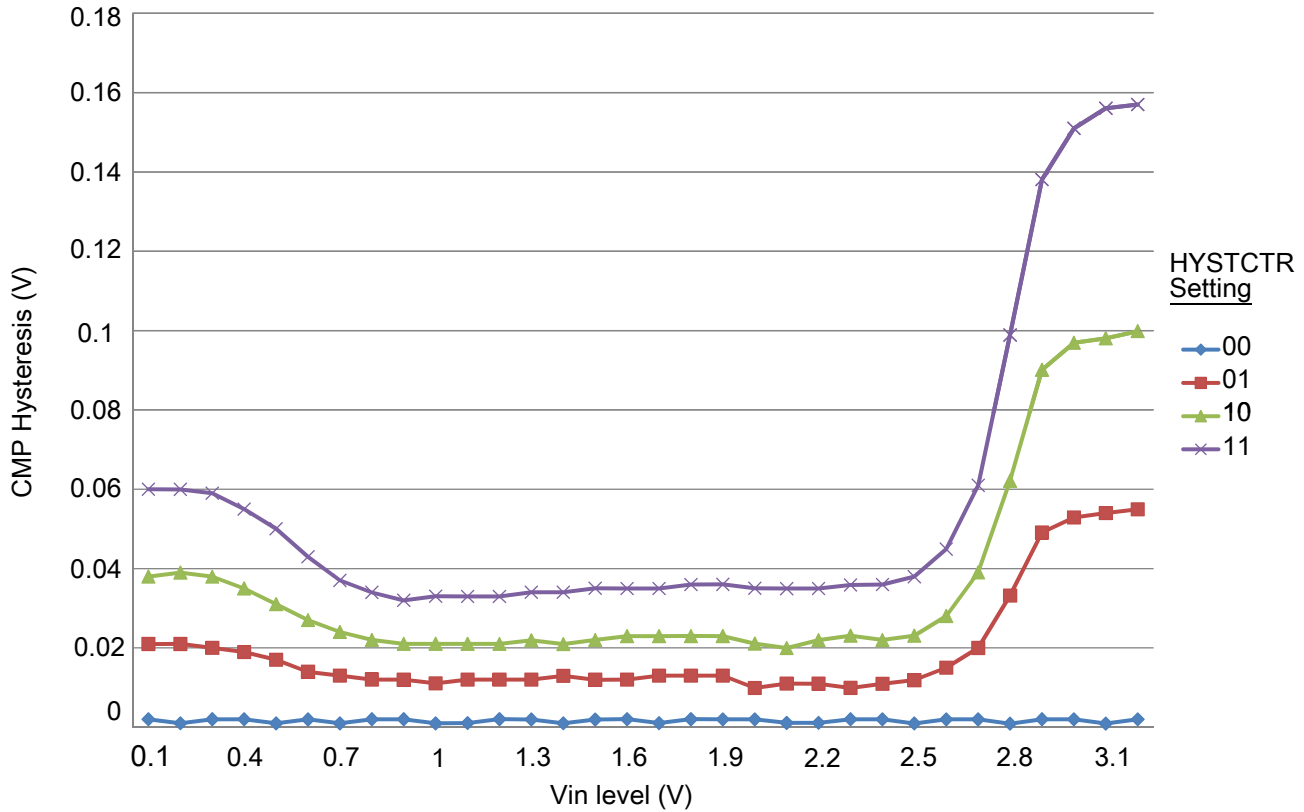
**Figure 28. Typical hysteresis vs. Vin level (VDD = 3.3 V, PMODE = 1)**

## 5.4.6.3   12-bit DAC electrical characteristics

### 5.4.6.3.1   12-bit DAC operating requirements
**Table 68.   12-bit DAC operating requirements**

| Symbol | Desciption | Min. | Max. | Unit | Notes |
|--------|------------|------|------|------|-------|
| $V_{DDA}$ | Supply voltage | 1.71 | 3.6 | V | |
| $V_{DACR}$ | Reference voltage | 1.13 | 3.6 | V | 1 |
| $C_L$ | Output load capacitance | — | 100 | pF | 2 |
| $I_L$ | Output load current | — | 1 | mA | |

1. The DAC reference can be selected to be $V_{DDA}$ or VREFH.
2. A small load capacitance (47 pF) can improve the bandwidth performance of the DAC

## 5.4.6.3.2  12-bit DAC operating behaviors
### Table 69.  12-bit DAC operating behaviors

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| $I_{DDA\_DACLP}$ | Supply current — low-power mode | — | — | 330 | µA | |
| $I_{DDA\_DACHP}$ | Supply current — high-speed mode | — | — | 1200 | µA | |
| $t_{DACLP}$ | Full-scale settling time (0x080 to 0xF7F) — low-power mode | — | 100 | 200 | µs | 1 |
| $t_{DACHP}$ | Full-scale settling time (0x080 to 0xF7F) — high-power mode | — | 15 | 30 | µs | 1 |
| $t_{CCDACLP}$ | Code-to-code settling time (0xBF8 to 0xC08) — low-power mode and high-speed mode | — | 0.7 | 1 | µs | 1 |
| $V_{dacoutl}$ | DAC output voltage range low — high-speed mode, no load, DAC set to 0x000 | — | — | 100 | mV | |
| $V_{dacouth}$ | DAC output voltage range high — high-speed mode, no load, DAC set to 0xFFF | $V_{DACR}$ −100 | — | $V_{DACR}$ | mV | |
| INL | Integral non-linearity error — high speed mode | — | — | ±8 | LSB | 2 |
| DNL | Differential non-linearity error — $V_{DACR}$ > 2 V | — | — | ±1 | LSB | 3 |
| DNL | Differential non-linearity error — $V_{DACR}$ = VREF_OUT | — | — | ±1 | LSB | 4 |
| $V_{OFFSET}$ | Offset error | — | ±0.4 | ±0.8 | %FSR | 5 |
| $E_G$ | Gain error | — | ±0.1 | ±0.6 | %FSR | 5 |
| PSRR | Power supply rejection ratio, $V_{DDA}$ ≥ 2.4 V | 60 | — | 90 | dB | |
| $T_{CO}$ | Temperature coefficient offset voltage | — | 3.7 | — | µV/C | 6 |
| $T_{GE}$ | Temperature coefficient gain error | — | 0.000421 | — | %FSR/C | |
| Rop | Output resistance (load = 3 kΩ) | — | — | 250 | Ω | |
| SR | Slew rate -80h→ F7Fh→ 80h | | | | V/µs | |
| | • High power ($SP_{HP}$) | 1.2 | 1.7 | — | | |
| | • Low power ($SP_{LP}$) | 0.05 | 0.12 | — | | |
| BW | 3dB bandwidth | | | | kHz | |
| | • High power ($SP_{HP}$) | 550 | — | — | | |
| | • Low power ($SP_{LP}$) | 40 | — | — | | |

1. Settling within ±1 LSB
2. The INL is measured for 0 + 100 mV to $V_{DACR}$ −100 mV
3. The DNL is measured for 0 + 100 mV to $V_{DACR}$ −100 mV
4. The DNL is measured for 0 + 100 mV to $V_{DACR}$ −100 mV with $V_{DDA}$ > 2.4 V
5. Calculated by a best fit curve from $V_{SS}$ + 100 mV to $V_{DACR}$ − 100 mV
6. $V_{DDA}$ = 3.0 V, reference select set for $V_{DDA}$ (DACx_CO:DACRFS = 1), high power mode (DACx_C0:LPEN = 0), DAC set to 0x800, temperature range is across the full range of the device
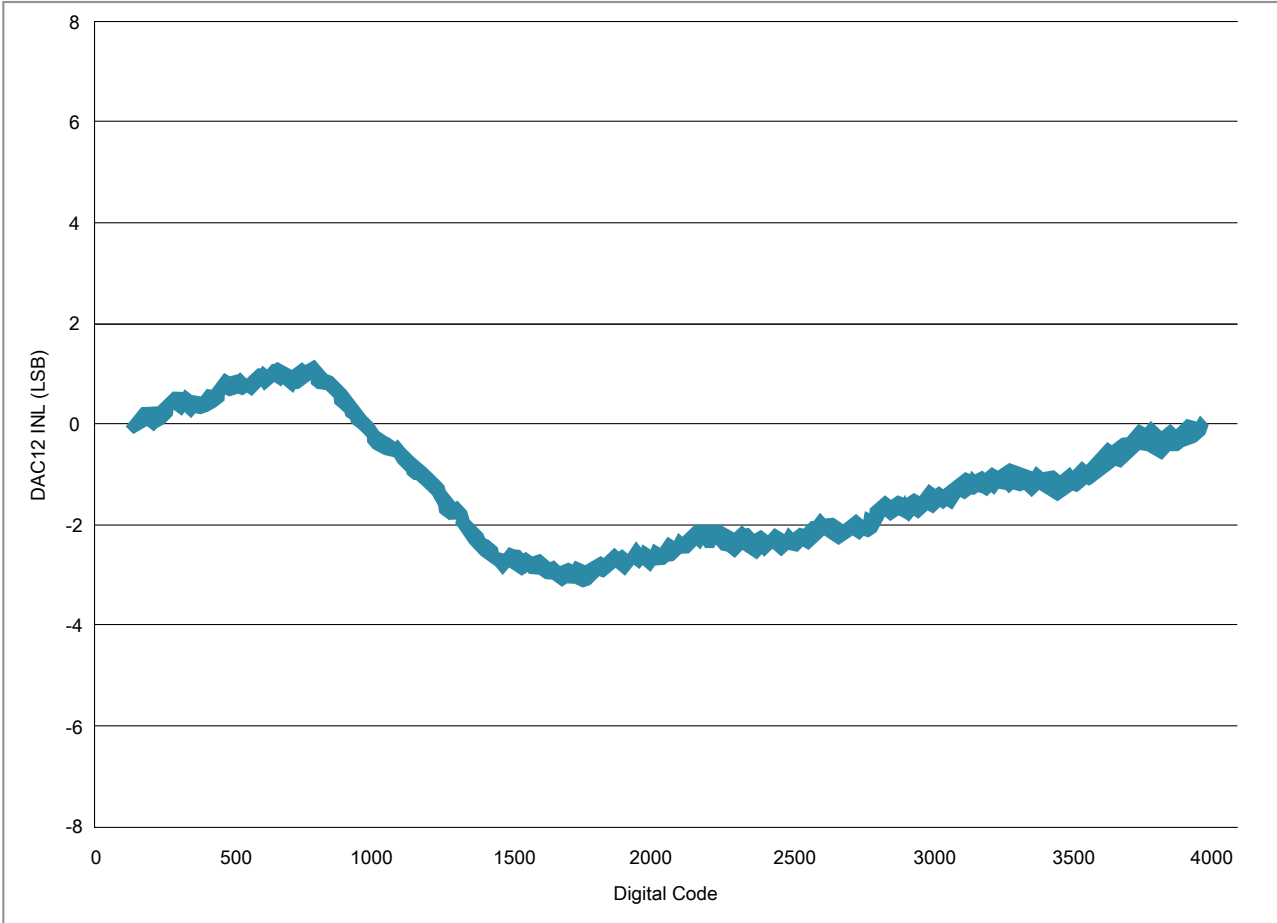
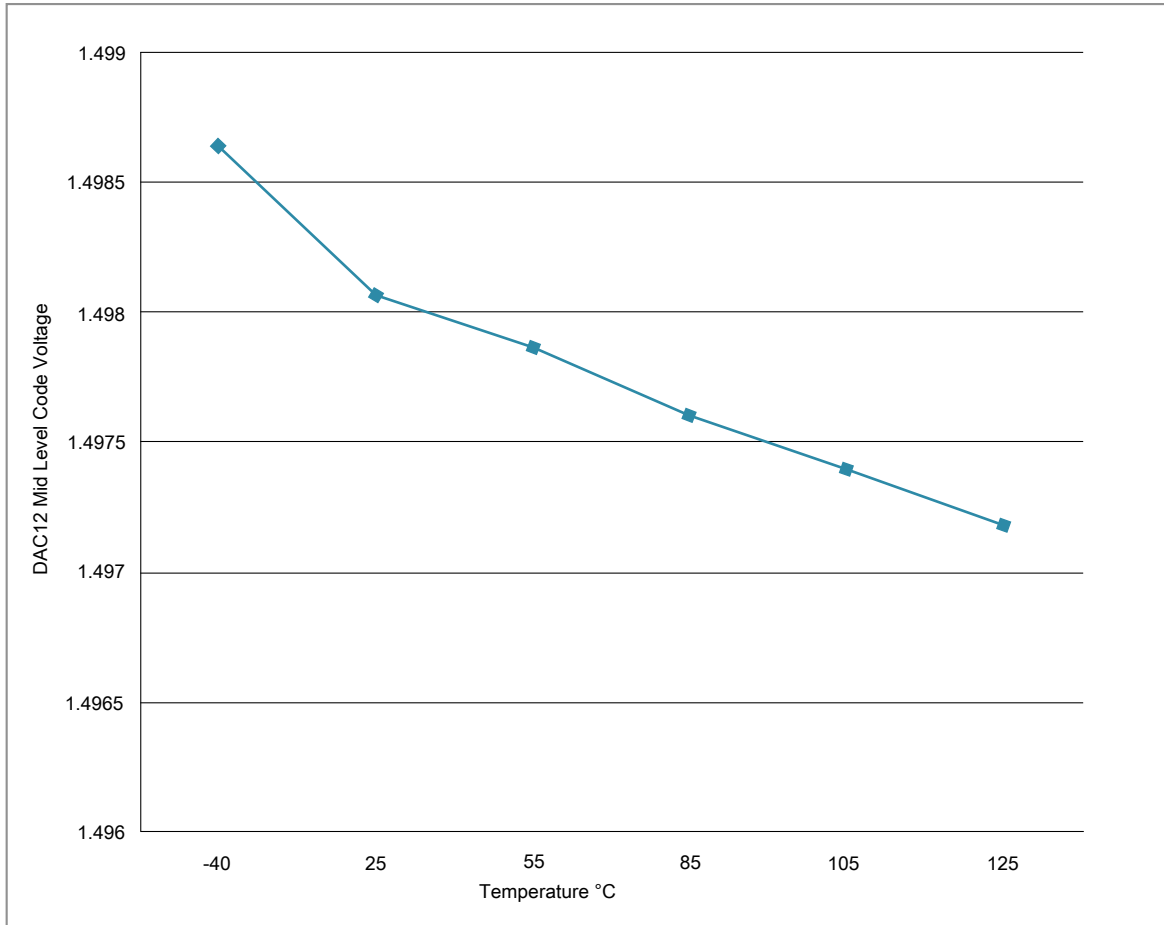**Figure 29. Typical INL error vs. digital code**

**Figure 30. Offset at half scale vs. temperature**

## 5.4.7   Timers

See General switching specifications.

## 5.4.8   Communication interfaces

### 5.4.8.1   USB electrical specifications

The USB electricals for the USB On-the-Go module conform to the standards documented by the Universal Serial Bus Implementers Forum. For the most up-to-date standards, visit **usb.org**.

**NOTE**

The MCGPLLCLK meets the USB jitter and signaling rate specifications for certification with the use of an external clock/crystal for both Device and Host modes.

The MCGFLLCLK does not meet the USB jitter or signaling rate specifications for certification.

The IRC48M meets the USB jitter and signaling rate specifications for certification in Device mode when the USB clock recovery mode is enabled. It does not meet the USB signaling rate specifications for certification in Host mode operation.

## 5.4.8.2  DSPI switching specifications (limited voltage range)

The Deserial Serial Peripheral Interface (DSPI) provides a synchronous serial bus with master and slave operations. Many of the transfer attributes are programmable. The tables below provide DSPI timing characteristics for classic SPI timing modes. Refer to the SPI chapter of the Reference Manual for information on the modified transfer formats used for communicating with slower peripheral devices.

**Table 70.  Master mode DSPI timing (limited voltage range)**

| Num | Description | Min. | Max. | Unit | Notes |
|---|---|---|---|---|---|
|  | Operating voltage | 2.7 | 3.6 | V |  |
|  | Frequency of operation | — | 30 | MHz |  |
| DS1 | DSPI_SCK output cycle time | $2 \times t_{BUS}$ | — | ns |  |
| DS2 | DSPI_SCK output high/low time | $(t_{SCK}/2) - 2$ | $(t_{SCK}/2) + 2$ | ns |  |
| DS3 | DSPI_PCS*n* valid to DSPI_SCK delay | $(t_{BUS} \times 2) - 2$ | — | ns | 1 |
| DS4 | DSPI_SCK to DSPI_PCS*n* invalid delay | $(t_{BUS} \times 2) - 2$ | — | ns | 2 |
| DS5 | DSPI_SCK to DSPI_SOUT valid | — | 8.5 | ns |  |
| DS6 | DSPI_SCK to DSPI_SOUT invalid | -2 | — | ns |  |
| DS7 | DSPI_SIN to DSPI_SCK input setup | 16.2 | — | ns |  |
| DS8 | DSPI_SCK to DSPI_SIN input hold | 0 | — | ns |  |

1.  The delay is programmable in SPIx_CTARn[PSSCK] and SPIx_CTARn[CSSCK].
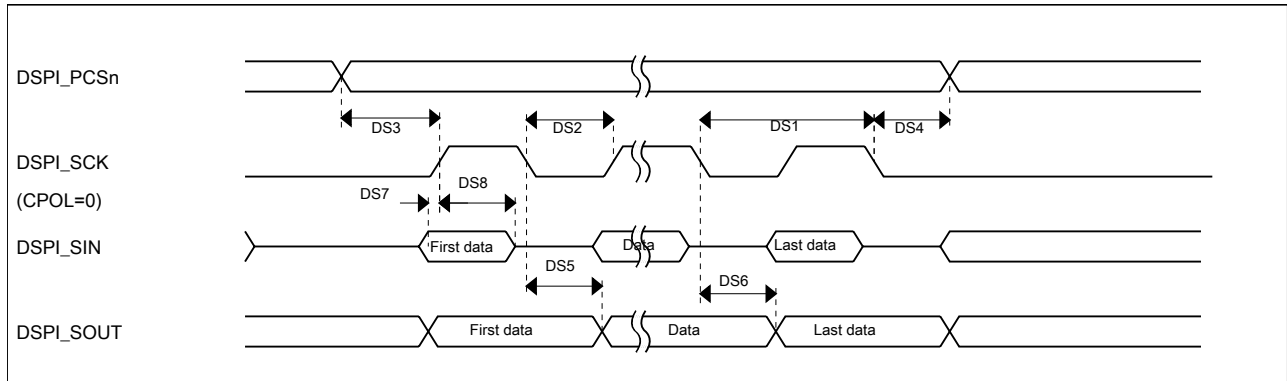2.  The delay is programmable in SPIx_CTARn[PASC] and SPIx_CTARn[ASC].

**Figure 31. DSPI classic SPI timing — master mode**

**Table 71.  Slave mode DSPI timing (limited voltage range)**

| Num | Description | Min. | Max. | Unit | Notes |
|---|---|---|---|---|---|
| | Operating voltage | 2.7 | 3.6 | V | |
| | Frequency of operation | — | 15 | MHz | [1] |
| DS9 | DSPI_SCK input cycle time | 4 x $t_{BUS}$ | — | ns | |
| DS10 | DSPI_SCK input high/low time | $(t_{SCK}/2) - 2$ | $(t_{SCK}/2) + 2$ | ns | |
| DS11 | DSPI_SCK to DSPI_SOUT valid | — | 21.4 | ns | |
| DS12 | DSPI_SCK to DSPI_SOUT invalid | 0 | — | ns | |
| DS13 | DSPI_SIN to DSPI_SCK input setup | 2.6 | — | ns | |
| DS14 | DSPI_SCK to DSPI_SIN input hold | 7 | — | ns | |
| DS15 | $\overline{DSPI\_SS}$ active to DSPI_SOUT driven | — | 17 | ns | |
| DS16 | $\overline{DSPI\_SS}$ inactive to DSPI_SOUT not driven | — | 17 | ns | |

1.  The maximum operating frequency is measured with noncontinuous CS and SCK. When DSPI is configured with continuous CS and SCK, the SPI clock must not be greater than 1/6 of the bus clock. For example, when the bus clock is 60 MHz, the SPI clock must not be greater than 10 MHz.
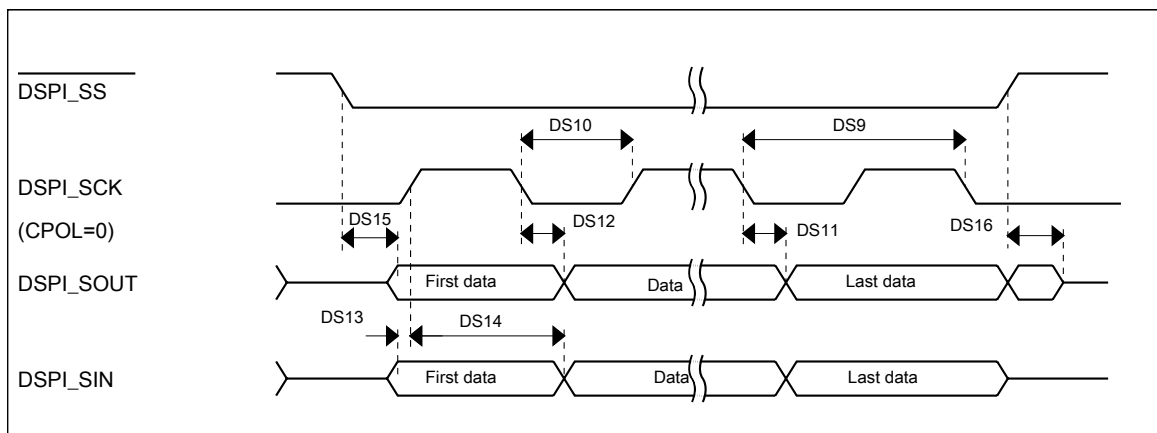


**Figure 32. DSPI classic SPI timing — slave mode**

## 5.4.8.3 DSPI switching specifications (full voltage range)

The Deserial Serial Peripheral Interface (DSPI) provides a synchronous serial bus with master and slave operations. Many of the transfer attributes are programmable. The tables below provides DSPI timing characteristics for classic SPI timing modes. Refer to the SPI chapter of the Reference Manual for information on the modified transfer formats used for communicating with slower peripheral devices.

**Table 72.   Master mode DSPI timing (full voltage range)**

| Num | Description | Min. | Max. | Unit | Notes |
|-----|-------------|------|------|------|-------|
|  | Operating voltage | 1.71 | 3.6 | V | 1 |
|  | Frequency of operation | — | 15 | MHz |  |
| DS1 | DSPI_SCK output cycle time | $4 \times t_{BUS}$ | — | ns |  |
| DS2 | DSPI_SCK output high/low time | $(t_{SCK}/2) - 4$ | $(t_{SCK/2}) + 4$ | ns |  |
| DS3 | DSPI_PCS$n$ valid to DSPI_SCK delay | $(t_{BUS} \times 2) - 4$ | — | ns | 2 |
| DS4 | DSPI_SCK to DSPI_PCS$n$ invalid delay | $(t_{BUS} \times 2) - 4$ | — | ns | 3 |
| DS5 | DSPI_SCK to DSPI_SOUT valid | — | 10 | ns |  |
| DS6 | DSPI_SCK to DSPI_SOUT invalid | -4.5 | — | ns |  |
| DS7 | DSPI_SIN to DSPI_SCK input setup | 24.6 | — | ns |  |
| DS8 | DSPI_SCK to DSPI_SIN input hold | 0 | — | ns |  |

1. The DSPI module can operate across the entire operating voltage for the processor, but to run across the full voltage range the maximum frequency of operation is reduced.
2. The delay is programmable in SPIx_CTARn[PSSCK] and SPIx_CTARn[CSSCK].
3. The delay is programmable in SPIx_CTARn[PASC] and SPIx_CTARn[ASC].
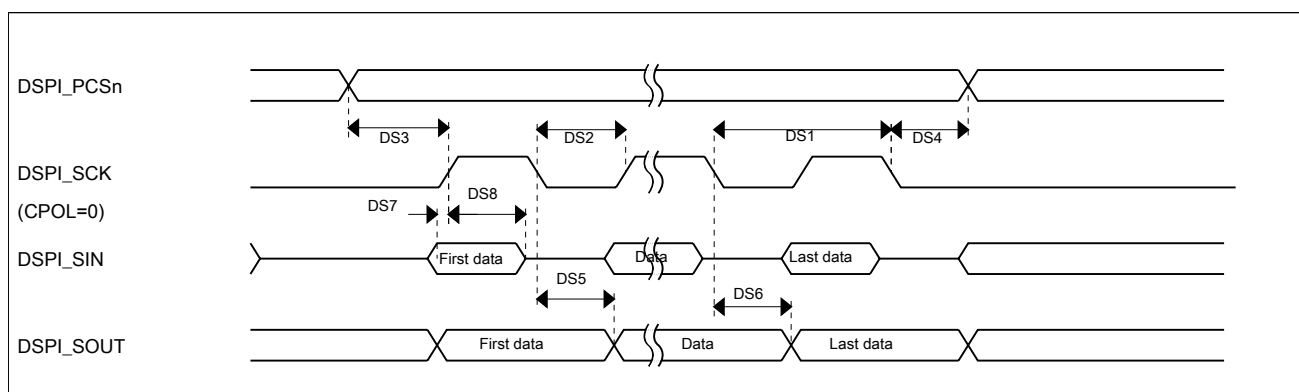


**Figure 33. DSPI classic SPI timing — master mode**

**Table 73. Slave mode DSPI timing (full voltage range)**

| Num | Description | Min. | Max. | Unit |
|-----|-------------|------|------|------|
| | Operating voltage | 1.71 | 3.6 | V |
| | Frequency of operation | — | 7.5 | MHz |
| DS9 | DSPI_SCK input cycle time | 8 x $t_{BUS}$ | — | ns |
| DS10 | DSPI_SCK input high/low time | $(t_{SCK}/2)$ - 4 | $(t_{SCK/2})$ + 4 | ns |
| DS11 | DSPI_SCK to DSPI_SOUT valid | — | 29.5 | ns |
| DS12 | DSPI_SCK to DSPI_SOUT invalid | 0 | — | ns |
| DS13 | DSPI_SIN to DSPI_SCK input setup | 3.2 | — | ns |
| DS14 | DSPI_SCK to DSPI_SIN input hold | 7 | — | ns |
| DS15 | $\overline{DSPI\_SS}$ active to DSPI_SOUT driven | — | 25 | ns |
| DS16 | $\overline{DSPI\_SS}$ inactive to DSPI_SOUT not driven | — | 25 | ns |
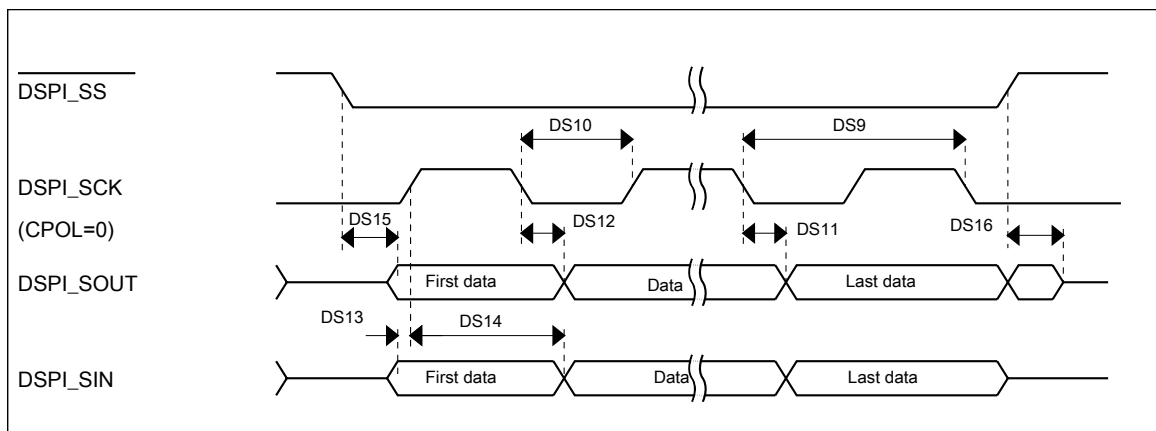


**Figure 34. DSPI classic SPI timing — slave mode**

## 5.4.8.4   LPI$^2$C

**Table 74.  LPI$^2$C specifications**

| Symbol | Description | | Min. | Max. | Unit | Notes |
|--------|-------------|--|------|------|------|-------|
| $f_{SCL}$ | SCL clock frequency | Standard mode (Sm) | 0 | 100 | kHz | 1 |
| | | Fast mode (Fm) | 0 | 400 | | 1, 2 |
| | | Fast mode Plus (Fm+) | 0 | 1000 | | 1, 3 |
| | | Ultra Fast mode (UFm) | 0 | 5000 | | 1, 4 |
| | | High speed mode (Hs-mode) | 0 | 3400 | | 1, 5 |

1.  See General switching specifications, measured at room temperature.
2.  Measured with the maximum bus loading of 400pF at 3.3V VDD with pull-up Rp = 220Ω , and at 1.8V VDD with Rp = 880Ω. For all other cases, select appropriate Rp per I2C Bus Specification and the pin drive capability.
3.  Fm+ is only supported on high drive pin with high drive enabled. It is measured with the maximum bus loading of 400pF at 3.3V VDD with Rp = 220Ω. For all other cases, select appropriate Rp per I2C Bus Specification and the pin drive capability.

4. UFm is only supported on high drive pin with high drive enabled and push-pull output only mode. It is measured at 3.3V VDD with the maximum bus loading of 400pF. For 1.8V VDD, the maximum speed is 4Mbps.
5. Hs-mode is only supported in slave mode and on the high drive pins with high drive enabled.

## 5.4.8.5  UART switching specifications

See General switching specifications.

## 5.4.8.6  I2S/SAI switching specifications

This section provides the AC timing for the I2S/SAI module in master mode (clocks are driven) and slave mode (clocks are input). All timing is given for noninverted serial clock polarity (TCR2[BCP] is 0, RCR2[BCP] is 0) and a noninverted frame sync (TCR4[FSP] is 0, RCR4[FSP] is 0). If the polarity of the clock and/or the frame sync have been inverted, all the timing remains valid by inverting the bit clock signal (BCLK) and/or the frame sync (FS) signal shown in the following figures.

### 5.4.8.6.1  Normal Run, Wait and Stop mode performance over a limited operating voltage range

This section provides the operating performance over a limited operating voltage for the device in Normal Run, Wait and Stop modes.

**Table 75.  I2S/SAI master mode timing in Normal Run, Wait and Stop modes (limited voltage range)**

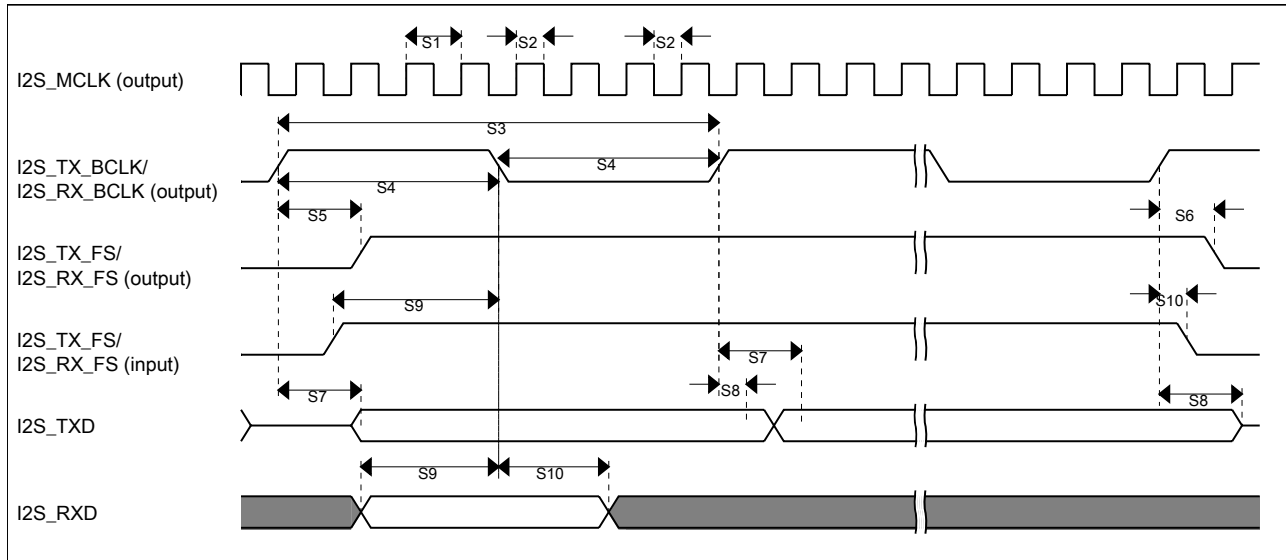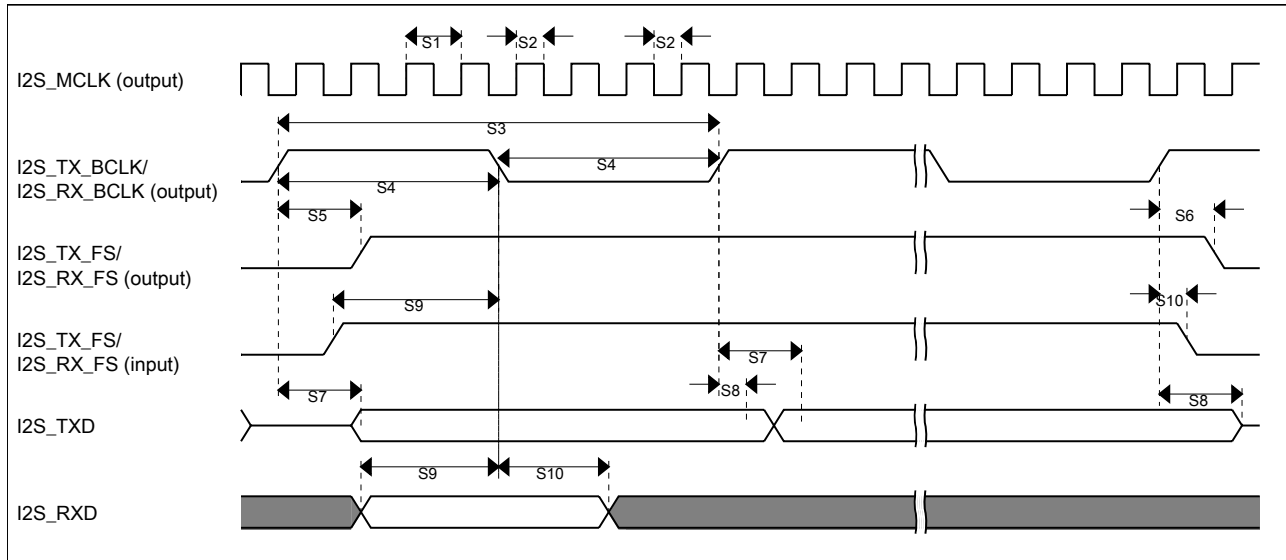| Num. | Characteristic | Min. | Max. | Unit |
|------|----------------|------|------|------|
|  | Operating voltage | 2.7 | 3.6 | V |
| S1 | I2S_MCLK cycle time | 40 | — | ns |
| S2 | I2S_MCLK pulse width high/low | 45% | 55% | MCLK period |
| S3 | I2S_TX_BCLK/I2S_RX_BCLK cycle time (output) | 80 | — | ns |
| S4 | I2S_TX_BCLK/I2S_RX_BCLK pulse width high/low | 45% | 55% | BCLK period |
| S5 | I2S_TX_BCLK/I2S_RX_BCLK to I2S_TX_FS/I2S_RX_FS output valid | — | 15 | ns |
| S6 | I2S_TX_BCLK/I2S_RX_BCLK to I2S_TX_FS/I2S_RX_FS output invalid | 0 | — | ns |
| S7 | I2S_TX_BCLK to I2S_TXD valid | — | 15 | ns |
| S8 | I2S_TX_BCLK to I2S_TXD invalid | 0 | — | ns |
| S9 | I2S_RXD/I2S_RX_FS input setup before I2S_RX_BCLK | 18 | — | ns |
| S10 | I2S_RXD/I2S_RX_FS input hold after I2S_RX_BCLK | 0 | — | ns |

**Figure 35. I2S/SAI timing — master modes**

**Table 76.   I2S/SAI slave mode timing in Normal Run, Wait and Stop modes (limited voltage range)**

| Num. | Characteristic | Min. | Max. | Unit |
|---|---|---|---|---|
| | Operating voltage | 2.7 | 3.6 | V |
| S11 | I2S_TX_BCLK/I2S_RX_BCLK cycle time (input) | 80 | — | ns |
| S12 | I2S_TX_BCLK/I2S_RX_BCLK pulse width high/low (input) | 45% | 55% | MCLK period |
| S13 | I2S_TX_FS/I2S_RX_FS input setup before I2S_TX_BCLK/I2S_RX_BCLK | 4.5 | — | ns |
| S14 | I2S_TX_FS/I2S_RX_FS input hold after I2S_TX_BCLK/I2S_RX_BCLK | 2 | — | ns |
| S15 | I2S_TX_BCLK to I2S_TXD/I2S_TX_FS output valid | — | 20 | ns |
| S16 | I2S_TX_BCLK to I2S_TXD/I2S_TX_FS output invalid | 0 | — | ns |
| S17 | I2S_RXD setup before I2S_RX_BCLK | 4.5 | — | ns |
| S18 | I2S_RXD hold after I2S_RX_BCLK | 2 | — | ns |
| S19 | I2S_TX_FS input assertion to I2S_TXD output valid[1] | — | 25 | ns |

1. Applies to first bit in each frame and only if the TCR4[FSE] bit is clear
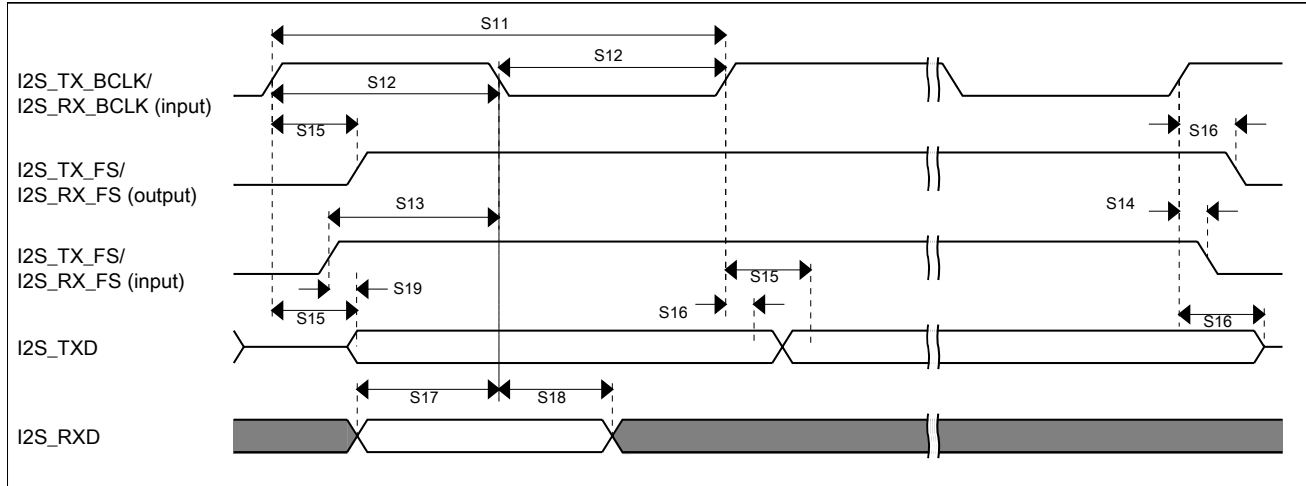
**Figure 36. I2S/SAI timing — slave modes**
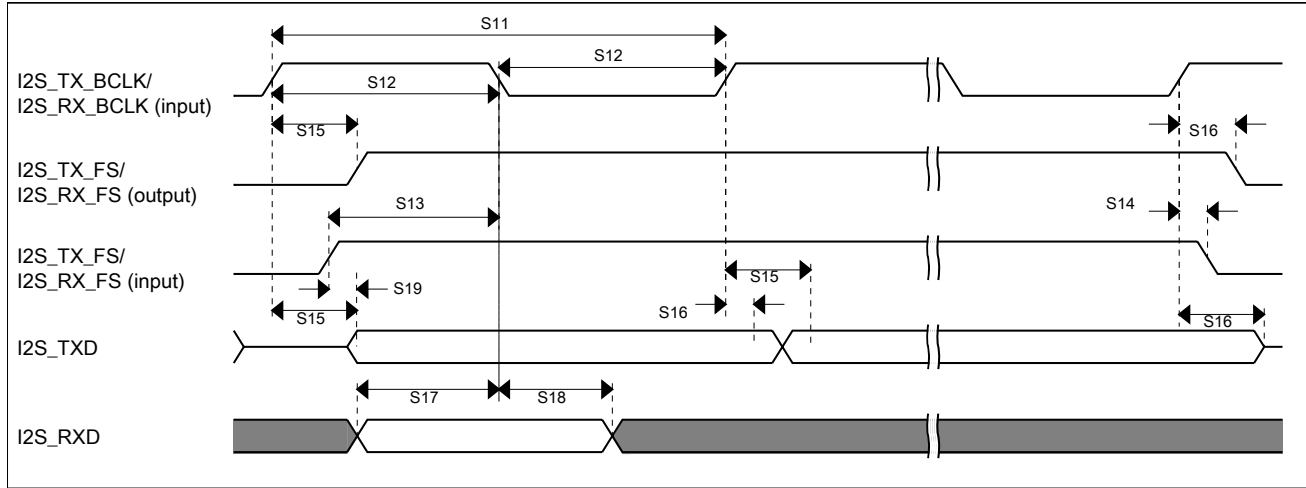
### 5.4.8.6.2   Normal Run, Wait and Stop mode performance over the full operating voltage range

This section provides the operating performance over the full operating voltage for the device in Normal Run, Wait and Stop modes.

**Table 77.  I2S/SAI master mode timing in Normal Run, Wait and Stop modes (full voltage range)**

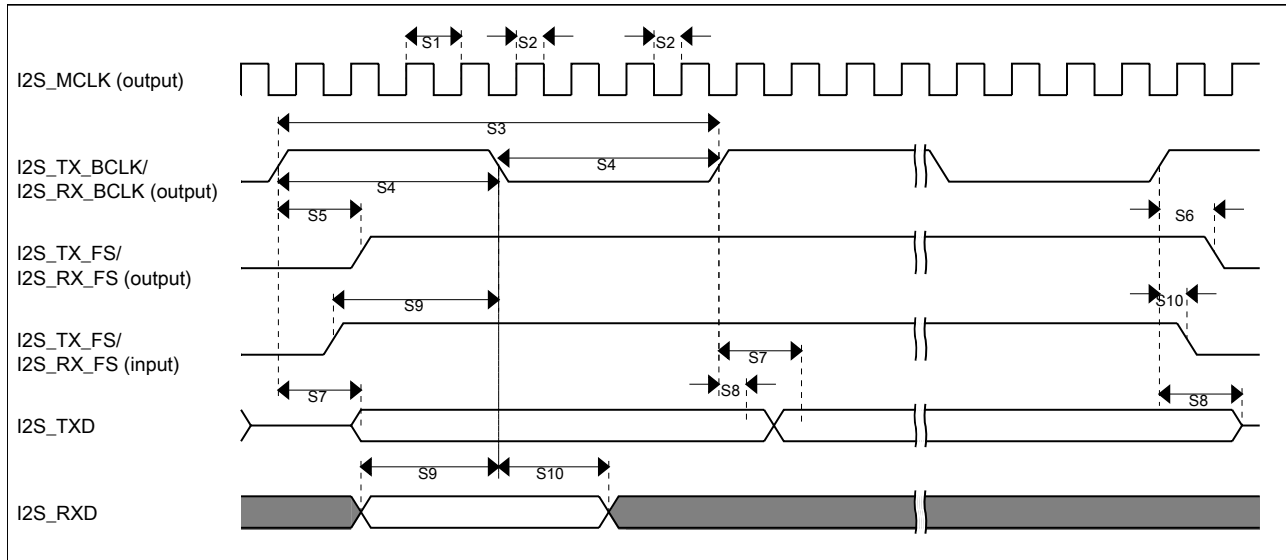| Num. | Characteristic | Min. | Max. | Unit |
|---|---|---|---|---|
|  | Operating voltage | 1.71 | 3.6 | V |
| S1 | I2S_MCLK cycle time | 40 | — | ns |
| S2 | I2S_MCLK pulse width high/low | 45% | 55% | MCLK period |
| S3 | I2S_TX_BCLK/I2S_RX_BCLK cycle time (output) | 80 | — | ns |
| S4 | I2S_TX_BCLK/I2S_RX_BCLK pulse width high/low | 45% | 55% | BCLK period |
| S5 | I2S_TX_BCLK/I2S_RX_BCLK to I2S_TX_FS/I2S_RX_FS output valid | — | 15 | ns |
| S6 | I2S_TX_BCLK/I2S_RX_BCLK to I2S_TX_FS/I2S_RX_FS output invalid | -1.0 | — | ns |
| S7 | I2S_TX_BCLK to I2S_TXD valid | — | 15 | ns |
| S8 | I2S_TX_BCLK to I2S_TXD invalid | 0 | — | ns |
| S9 | I2S_RXD/I2S_RX_FS input setup before I2S_RX_BCLK | 27 | — | ns |
| S10 | I2S_RXD/I2S_RX_FS input hold after I2S_RX_BCLK | 0 | — | ns |

**Figure 37. I2S/SAI timing — master modes**

**Table 78. I2S/SAI slave mode timing in Normal Run, Wait and Stop modes (full voltage range)**

| Num. | Characteristic | Min. | Max. | Unit |
|------|----------------|------|------|------|
|  | Operating voltage | 1.71 | 3.6 | V |
| S11 | I2S_TX_BCLK/I2S_RX_BCLK cycle time (input) | 80 | — | ns |
| S12 | I2S_TX_BCLK/I2S_RX_BCLK pulse width high/low (input) | 45% | 55% | MCLK period |
| S13 | I2S_TX_FS/I2S_RX_FS input setup before I2S_TX_BCLK/I2S_RX_BCLK | 5.8 | — | ns |
| S14 | I2S_TX_FS/I2S_RX_FS input hold after I2S_TX_BCLK/I2S_RX_BCLK | 2 | — | ns |
| S15 | I2S_TX_BCLK to I2S_TXD/I2S_TX_FS output valid | — | 28.5 | ns |
| S16 | I2S_TX_BCLK to I2S_TXD/I2S_TX_FS output invalid | 0 | — | ns |
| S17 | I2S_RXD setup before I2S_RX_BCLK | 5.8 | — | ns |
| S18 | I2S_RXD hold after I2S_RX_BCLK | 2 | — | ns |
| S19 | I2S_TX_FS input assertion to I2S_TXD output valid[1] | — | 26.3 | ns |

1. Applies to first bit in each frame and only if the TCR4[FSE] bit is clear

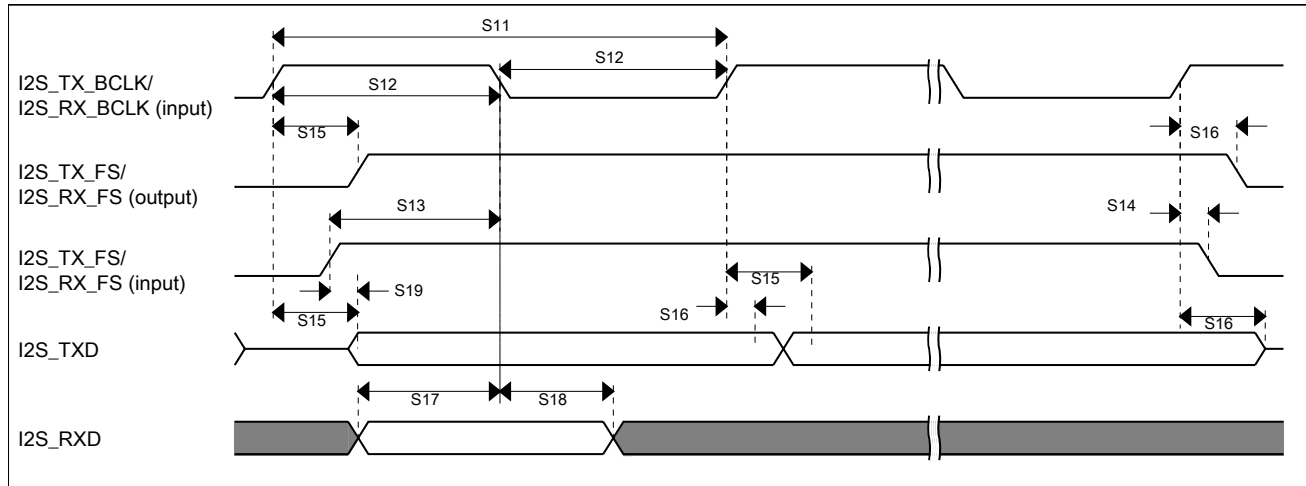**Figure 38. I2S/SAI timing — slave modes**

### 5.4.8.6.3 VLPR, VLPW, and VLPS mode performance over the full operating voltage range

This section provides the operating performance over the full operating voltage for the device in VLPR, VLPW, and VLPS modes.

**Table 79. I2S/SAI master mode timing in VLPR, VLPW, and VLPS modes (full voltage range)**

| Num. | Characteristic | Min. | Max. | Unit |
|------|----------------|------|------|------|
| | Operating voltage | 1.71 | 3.6 | V |
| S1 | I2S_MCLK cycle time | 62.5 | — | ns |
| S2 | I2S_MCLK pulse width high/low | 45% | 55% | MCLK period |
| S3 | I2S_TX_BCLK/I2S_RX_BCLK cycle time (output) | 250 | — | ns |
| S4 | I2S_TX_BCLK/I2S_RX_BCLK pulse width high/low | 45% | 55% | BCLK period |
| S5 | I2S_TX_BCLK/I2S_RX_BCLK to I2S_TX_FS/ I2S_RX_FS output valid | — | 45 | ns |
| S6 | I2S_TX_BCLK/I2S_RX_BCLK to I2S_TX_FS/ I2S_RX_FS output invalid | -1 | — | ns |
| S7 | I2S_TX_BCLK to I2S_TXD valid | — | 45 | ns |
| S8 | I2S_TX_BCLK to I2S_TXD invalid | | — | ns |
| S9 | I2S_RXD/I2S_RX_FS input setup before I2S_RX_BCLK | | — | ns |
| S10 | I2S_RXD/I2S_RX_FS input hold after I2S_RX_BCLK | 0 | — | ns |

**Figure 39. I2S/SAI timing — master modes**

**Table 80.   I2S/SAI slave mode timing in VLPR, VLPW, and VLPS modes (full voltage range)**

| Num. | Characteristic | Min. | Max. | Unit |
|------|----------------|------|------|------|
| | Operating voltage | 1.71 | 3.6 | V |
| S11 | I2S_TX_BCLK/I2S_RX_BCLK cycle time (input) | 250 | — | ns |
| S12 | I2S_TX_BCLK/I2S_RX_BCLK pulse width high/low (input) | 45% | 55% | MCLK period |
| S13 | I2S_TX_FS/I2S_RX_FS input setup before I2S_TX_BCLK/I2S_RX_BCLK | 30 | — | ns |
| S14 | I2S_TX_FS/I2S_RX_FS input hold after I2S_TX_BCLK/I2S_RX_BCLK | 7 | — | ns |
| S15 | I2S_TX_BCLK to I2S_TXD/I2S_TX_FS output valid | — | | ns |
| S16 | I2S_TX_BCLK to I2S_TXD/I2S_TX_FS output invalid | 0 | — | ns |
| S17 | I2S_RXD setup before I2S_RX_BCLK | 30 | — | ns |
| S18 | I2S_RXD hold after I2S_RX_BCLK | 4 | — | ns |
| S19 | I2S_TX_FS input assertion to I2S_TXD output valid[1] | — | 72 | ns |

1.   Applies to first bit in each frame and only if the TCR4[FSE] bit is clear

**Figure 40. I2S/SAI timing — slave modes**

# 6  Design considerations

## 6.1  Hardware design considerations

This device contains protective circuitry to guard against damage due to high static voltage or electric fields. However, take normal precautions to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit.

### 6.1.1  Printed circuit board recommendations

- Place connectors or cables on one edge of the board and do not place digital circuits between connectors.
- Drivers and filters for I/O functions must be placed as close to the connectors as possible. Connect TVS devices at the connector to a good ground. Connect filter capacitors at the connector to a good ground.
- Physically isolate analog circuits from digital circuits if possible.
- Place input filter capacitors as close to the MCU as possible.
- For best EMC performance, route signals as transmission lines; use a ground plane directly under LQFP packages; and solder the exposed pad (EP) to ground directly under QFN packages.

## 6.1.2  Power delivery system

Consider the following items in the power delivery system:
- Use a plane for ground.
- Use a plane for MCU VDD supply if possible.
- Always route ground first, as a plane or continuous surface, and never as sequential segments.
- Route power next, as a plane or traces that are parallel to ground traces.
- Place bulk capacitance, 10 µF or more, at the entrance of the power plane.
- Place bypass capacitors for MCU power domain as close as possible to each VDD/VSS pair, including VDDA/VSSA and VREFH/VREFL.
- The minimum bypass requirement is to place 0.1 µF capacitors positioned as near as possible to the package supply pins.
- The USB_VDD voltage range is 3.0 V to 3.6 V. It is recommended to include a filter circuit with one bulk capacitor (no less than 2.2 µF) and one 0.1 µF capacitor at the USB_VDD pin to improve USB performance.

## 6.1.3  Analog design

Each ADC input must have an RC filter as shown in the following figure. The maximum value of R must be RAS max if fast sampling and high resolution are required. The value of C must be chosen to ensure that the RC time constant is very small compared to the sample period.
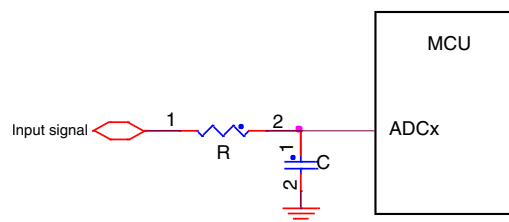


**Figure 41. RC circuit for ADC input**

High voltage measurement circuits require voltage division, current limiting, and over-voltage protection as shown the following figure. The voltage divider formed by R1 – R4 must yield a voltage less than or equal to VREFH. The current must be limited to less than the injection current limit. Since the ADC pins do not have diodes to VDD, external clamp diodes must be included to protect against transient over-voltages.
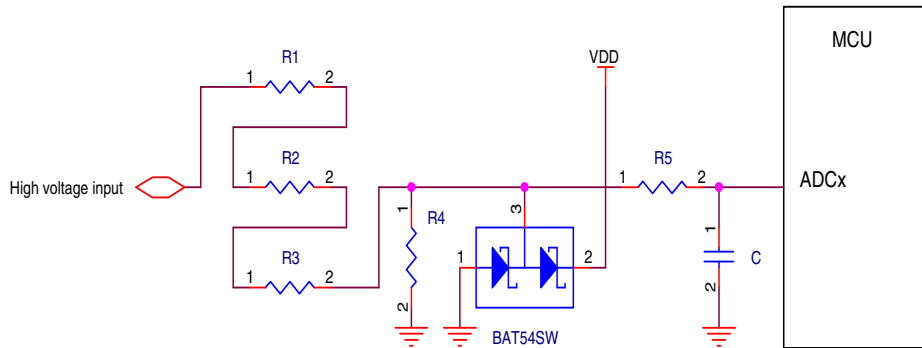
**Figure 42. High voltage measurement with an ADC input**

## 6.1.4   Digital design

Ensure that all I/O pins cannot get pulled above VDD (Max I/O is VDD+0.3V).

### CAUTION
Do not provide power to I/O pins prior to VDD, especially the RESET_b pin.

• RESET_b pin

The RESET_b pin is an open-drain I/O pin that has an internal pullup resistor. An external RC circuit is recommended to filter noise as shown in the following figure. The resistor value must be in the range of 4.7 kΩ to 10 kΩ; the recommended capacitance value is 0.1 µF. The RESET_b pin also has a selectable digital filter to reject spurious noise.
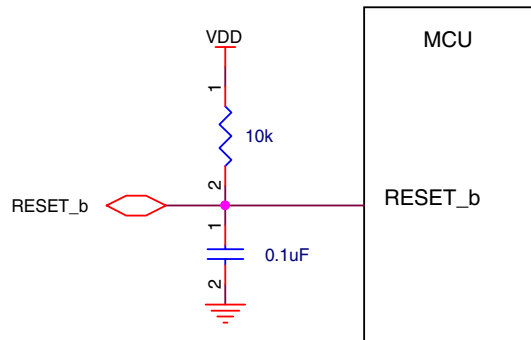


**Figure 43. Reset circuit**

When an external supervisor chip is connected to the RESET_b pin, a series resistor must be used to avoid damaging the supervisor chip or the RESET_b pin, as shown in the following figure. The series resistor value (RS below) must be in the range of 100 Ω to 1 kΩ depending on the external reset chip drive strength. The supervisor chip must have an active high, open-drain output.
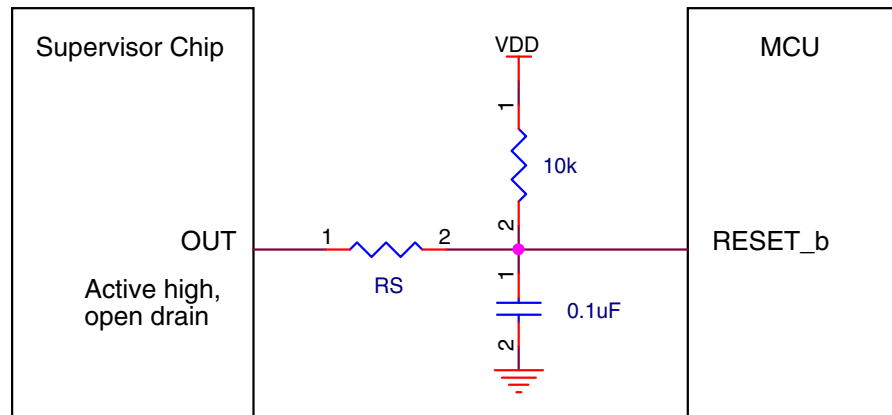


**Figure 44. Reset signal connection to external reset chip**

• NMI pin

Do not add a pull-down resistor or capacitor on the NMI_b pin, because a low level on this pin will trigger non-maskable interrupt. When this pin is enabled as the NMI function, an external pull-up resistor (10 kΩ) as shown in the following figure is recommended for robustness.

If the NMI_b pin is used as an I/O pin, the non-maskable interrupt handler is required to disable the NMI function by remapping to another function. The NMI function is disabled by programming the FOPT[NMI_DIS] bit to zero.
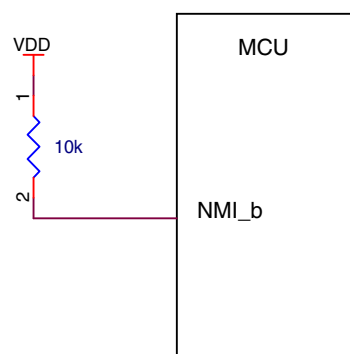


**Figure 45. NMI pin biasing**

• Debug interface

This MCU uses the standard ARM SWD interface protocol as shown in the following figure. While pull-up or pull-down resistors are not required (SWD_DIO has an internal pull-up and SWD_CLK has an internal pull-down), external 10 kΩ pull resistors are recommended for system robustness. The RESET_b pin recommendations mentioned above must also be considered.
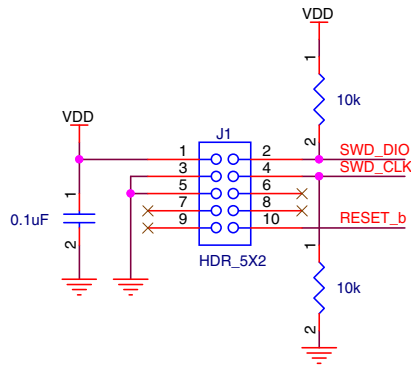


**Figure 46. SWD debug interface**

- Low leakage stop mode wakeup

  Select low leakage wakeup pins (LLWU_Px) to wake the MCU from one of the low leakage stop modes (LLS/VLLSx). See the pinout table for pin selection.

- Unused pin

  Unused GPIO pins must be left floating (no electrical connections) with the MUX field of the pin's PORTx_PCRn register equal to 0:0:0. This disables the digital input path to the MCU.

  If the USB module is not used, leave the USB data pins (USB0_DP, USB0_DM) floating. Connect USB_VDD to ground through a 10 kΩ resistor if the USB module is not used.

## 6.1.5  Crystal oscillator

When using an external crystal or ceramic resonator as the frequency reference for the MCU clock system, refer to the following table and diagrams.

The feedback resistor, RF, is incorporated internally with the low power oscillators. An external feedback is required when using high gain (HGO=1) mode.

Internal load capacitors (Cx, Cy) are provided in the low frequency (32.786 kHz) mode. Use the SCxP bits in the OSC0_CR register to adjust the load capacitance for the crystal. Typically, values of 10pf to 16 pF are sufficient for 32.768 kHz crystals that have a 12.5 pF CL specification. The internal load capacitor selection must not be used for high frequency crystals and resonators.

**Table 81.  External crystal/resonator connections**

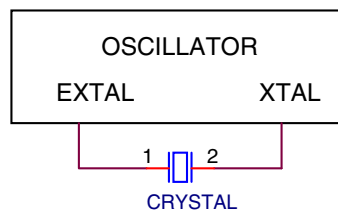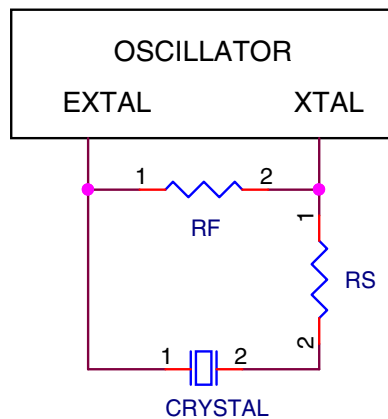| Oscillator mode | Oscillator mode |
|---|---|
| Low frequency (32.768 kHz), low power | Diagram 1 |
| Low frequency (32.768 kHz), high gain | Diagram 2, Diagram 4 |
| High frequency (3-32 MHz), low power | Diagram 3 |
| High frequency (3-32 MHz), high gain | Diagram 4 |



**Figure 47. Crystal connection – Diagram 1**



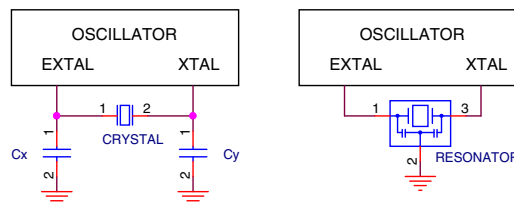**Figure 48. Crystal connection – Diagram 2**



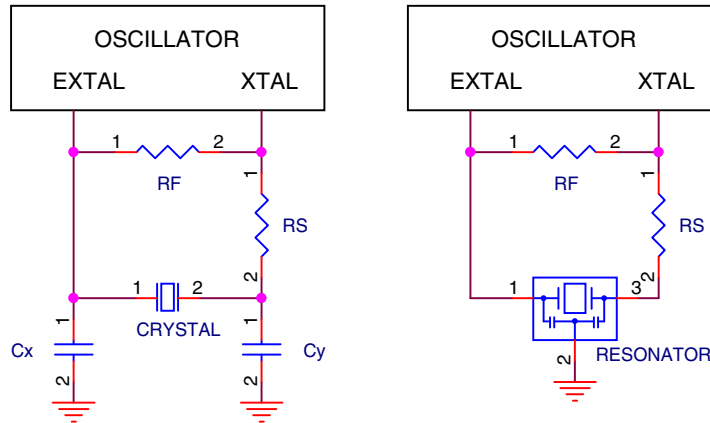**Figure 49. Crystal connection – Diagram 3**

**Figure 50. Crystal connection – Diagram 4**

## 6.2 Software considerations

All Kinetis MCUs are supported by comprehensive Freescale and third-party hardware and software enablement solutions, which can reduce development costs and time to market. Featured software and tools are listed below. Visit http://www.freescale.com/kinetis/sw for more information and supporting collateral.

Evaluation and Prototyping Hardware

- MAPS Development Kit: http://www.freescale.com/KS

IDEs for Kinetis MCUs

- Kinetis Design Studio IDE: http://www.freescale.com/kds
- Partner IDEs: http://www.freescale.com/kide

Run-time Software

- Kinetis SDK: http://www.freescale.com/ksdk
- Kinetis Bootloader: http://www.freescale.com/kboot
- ARM mbed Development Platform: http://www.freescale.com/mbed

For all other partner-developed software and tools, visit http://www.freescale.com/partners.

## 7 Part identification

## 7.1  Description

Part numbers for the chip have fields that identify the specific part. You can use the values of these fields to determine the specific part you have received.

## 7.2  Format

Part numbers for this device have the following format:

Q KS## A FFF R T PP CC N

## 7.3  Fields

This table lists the possible values for each field in the part number (not all combinations are valid):

**Table 82.  Part number fields description**

| Field | Description | Values |
|---|---|---|
| Q | Qualification status | • M = Fully qualified, general market flow<br>• P = Prequalification |
| KS## | Kinetis family | • KS20<br>• KS22 |
| A | Key attribute | • F = Cortex-M4 with DSP and FPU |
| FFF | Program flash memory size | • 128 = 128 KB<br>• 256 = 256 KB |
| R | Silicon revision | • (Blank) = Main<br>• A = Revision after main |
| T | Temperature range (°C) | • V = –40 to 105 |
| PP | Package identifier | • FT = 48 QFN (7 mm x 7 mm)<br>• LH = 64 LQFP (10 mm x 10 mm)<br>• LL = 100 LQFP (14 mm x 14 mm) |
| CC | Maximum CPU frequency (MHz) | • 12 = 120 MHz |
| N | Packaging type | • R = Tape and reel<br>• (Blank) = Trays |

## 7.4  Example

This is an example part number:

MKS22FN256VLL12

# 8  Revision history

The following table provides a revision history for this document.

**Table 83.  Revision history**

| Rev. No. | Date | Substantial Changes |
|:---:|:---:|---|
| 2 | 12/2015 | Initial public release. |
| 3 | 04/2016 | Added 48-pin QFN package. |

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