

N-channel 600 V, 0.110 Ω typ., 24 A MDmesh™ DM2 Power MOSFET in TO-220FP package

Datasheet - production data

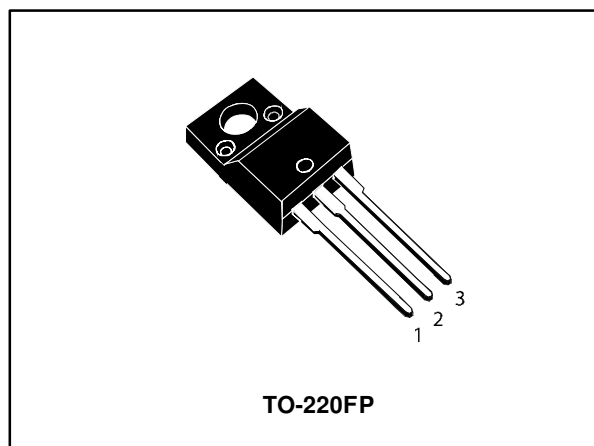
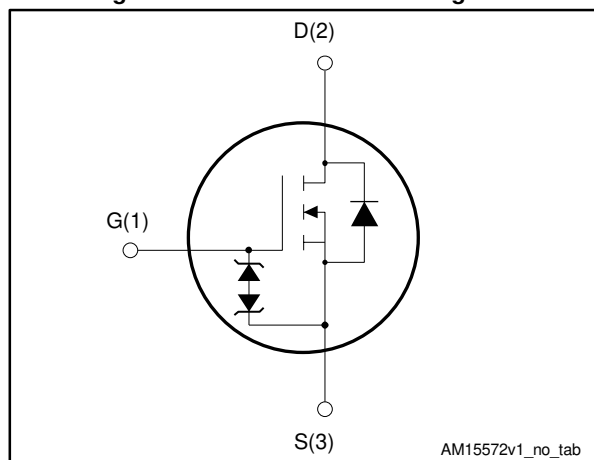


Figure 1: Internal schematic diagram



Features

Order code	V _{DS} @ T _{Jmax.}	R _{DS(on)} max.	I _D
STF33N60DM2	650 V	0.130 Ω	24 A

- Fast-recovery body diode
- Extremely low gate charge and input capacitance
- Low on-resistance
- 100% avalanche tested
- Extremely high dv/dt ruggedness
- Zener-protected

Applications

- Switching applications

Description

This high voltage N-channel Power MOSFET is part of the MDmesh™ DM2 fast recovery diode series. It offers very low recovery charge (Q_{rr}) and time (t_{rr}) combined with low $R_{DS(on)}$, rendering it suitable for the most demanding high efficiency converters and ideal for bridge topologies and ZVS phase-shift converters.

Table 1: Device summary

Order code	Marking	Package	Packing
STF33N60DM2	33N60DM2	TO-220FP	Tube

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1 Electrical ratings

Table 2: Absolute maximum ratings

Symbol	Parameter	Value	Unit
V _{GS}	Gate-source voltage	±25	V
I _D	Drain current (continuous) at T _{case} = 25 °C	24	A
	Drain current (continuous) at T _{case} = 100 °C	15.5	
I _{DM} ⁽¹⁾	Drain current (pulsed)	96	A
P _{TOT}	Total dissipation at T _{case} = 25 °C	35	W
dv/dt ⁽²⁾	Peak diode recovery voltage slope	50	V/ns
dv/dt ⁽³⁾	MOSFET dv/dt ruggedness	50	
V _{ISO}	Insulation withstand voltage (RMS) from all three leads to external heat sink (t = 1 s; T _C = 25 °C)	2500	V
T _{stg}	Storage temperature range	-55 to 150	°C
T _j	Operating junction temperature range		

Notes:

(1) Pulse width is limited by safe operating area.

(2) I_{SD} ≤ 24 A, di/dt=900 A/μs; V_{DS peak} < V_{(BR)DSS}, V_{DD} = 400 V.

(3) V_{DS} ≤ 480 V.

Table 3: Thermal data

Symbol	Parameter	Value	Unit
R _{thj-case}	Thermal resistance junction-case	3.6	°C/W
R _{thj-amb}	Thermal resistance junction-ambient	62.5	

Table 4: Avalanche characteristics

Symbol	Parameter	Value	Unit
I _{AR}	Avalanche current, repetitive or not repetitive (Pulse width limited by T _{jmax})	5.5	A
E _{AS}	Single pulse avalanche energy (starting T _j = 25 °C, I _D = I _{AR} , V _{DD} = 50 V)	570	mJ

2 Electrical characteristics

($T_{\text{case}} = 25\text{ °C}$ unless otherwise specified)

Table 5: Static

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0\text{ V}$, $I_D = 1\text{ mA}$	600			V
I_{DSS}	Zero gate voltage drain current	$V_{GS} = 0\text{ V}$, $V_{DS} = 600\text{ V}$			1	μA
		$V_{GS} = 0\text{ V}$, $V_{DS} = 600\text{ V}$, $T_{\text{case}} = 125\text{ °C}^{(1)}$			100	
I_{GSS}	Gate-body leakage current	$V_{DS} = 0\text{ V}$, $V_{GS} = \pm 25\text{ V}$			± 10	μA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$, $I_D = 250\text{ }\mu\text{A}$	3	4	5	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\text{ V}$, $I_D = 12\text{ A}$		0.110	0.130	Ω

Notes:

⁽¹⁾Defined by design, not subject to production test.

Table 6: Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	$V_{DS} = 100\text{ V}$, $f = 1\text{ MHz}$, $V_{GS} = 0\text{ V}$	-	1870	-	μF
C_{oss}	Output capacitance		-	87	-	
C_{rss}	Reverse transfer capacitance		-	2	-	
$C_{oss\text{ eq.}}^{(1)}$	Equivalent output capacitance	$V_{DD} = 480\text{ V}$, $V_{GS} = 0\text{ V}$	-	157	-	μF
R_G	Intrinsic gate resistance	$f = 1\text{ MHz}$, $I_D = 0\text{ A}$	-	4.5	-	Ω
Q_g	Total gate charge	$V_{DD} = 480\text{ V}$, $I_D = 24\text{ A}$, $V_{GS} = 10\text{ V}$ (see Figure 15: "Test circuit for gate charge behavior")	-	43	-	nC
Q_{gs}	Gate-source charge		-	9.8	-	
Q_{gd}	Gate-drain charge		-	21	-	

Notes:

⁽¹⁾ $C_{oss\text{ eq.}}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS} .

Table 7: Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 300\text{ V}$, $I_D = 12\text{ A}$ $R_G = 4.7\text{ }\Omega$, $V_{GS} = 10\text{ V}$ (see Figure 14: "Test circuit for resistive load switching times" and Figure 19: "Switching time waveform")	-	17	-	ns
t_r	Rise time		-	8	-	
$t_{d(off)}$	Turn-off delay time		-	62	-	
t_f	Fall time		-	9	-	

Table 8: Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		24	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		96	A
$V_{SD}^{(2)}$	Forward on voltage	$V_{GS} = 0\text{ V}$, $I_{SD} = 24\text{ A}$	-		1.6	V
t_{rr}	Reverse recovery time	$I_{SD} = 24\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$, $V_{DD} = 60\text{ V}$ (see Figure 16 : "Test circuit for inductive load switching and diode recovery times")	-	120		ns
Q_{rr}	Reverse recovery charge		-	0.53		μC
I_{RRM}	Reverse recovery current		-	8.8		A
t_{rr}	Reverse recovery time	$I_{SD} = 24\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$, $V_{DD} = 60\text{ V}$, $T_j = 150\text{ }^\circ\text{C}$ (see Figure 16 : "Test circuit for inductive load switching and diode recovery times")	-	316		ns
Q_{rr}	Reverse recovery charge		-	2.85		μC
I_{RRM}	Reverse recovery current		-	18		A

Notes:

(1) Pulse width is limited by safe operating area.

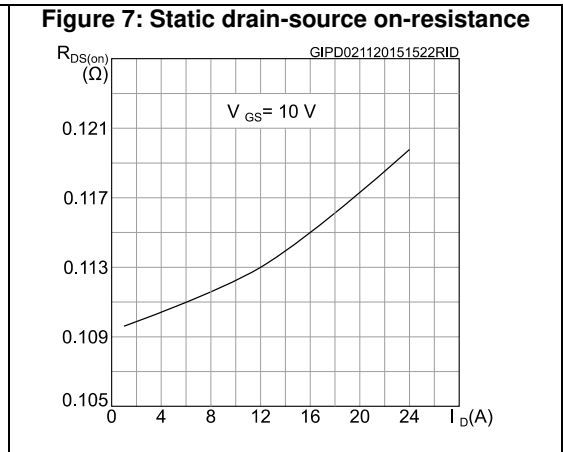
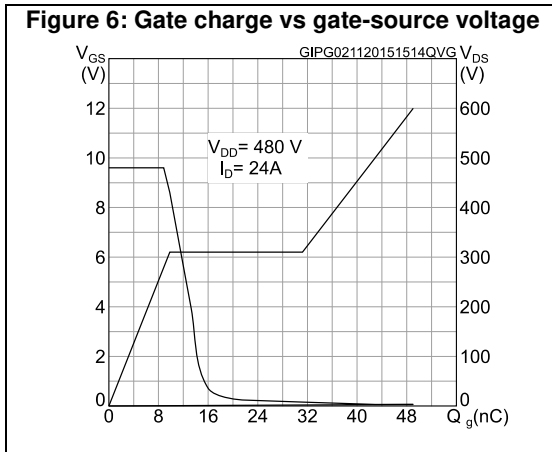
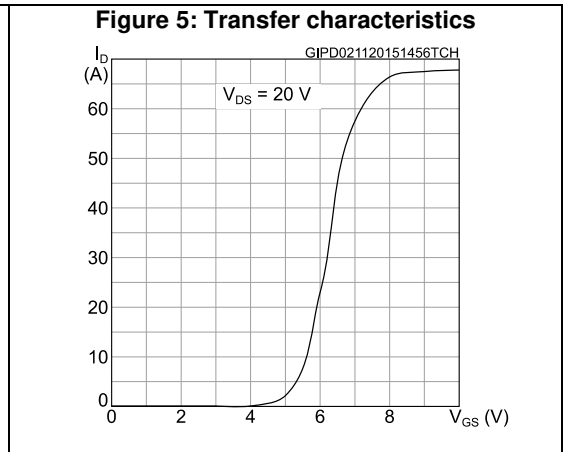
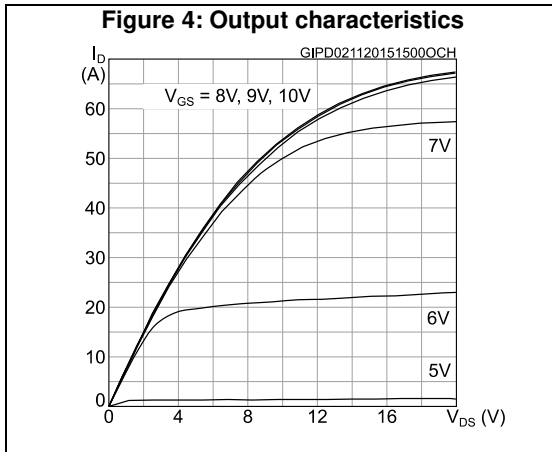
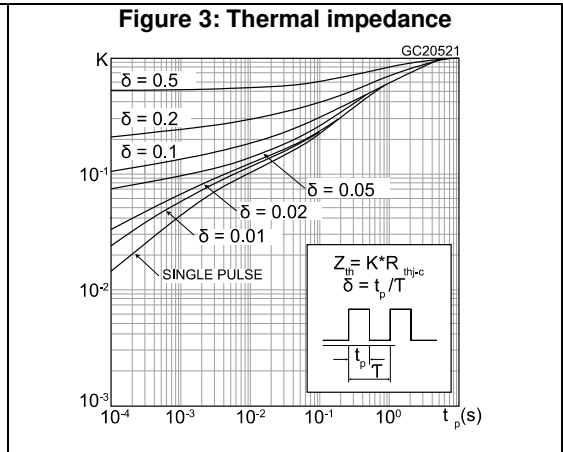
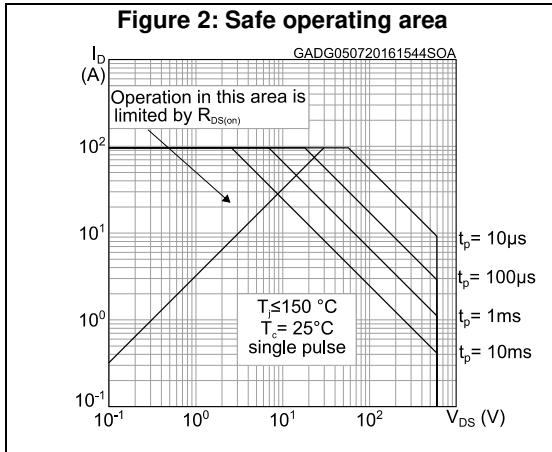
(2) Pulse test: pulse duration = 300 μs , duty cycle 1.5%.

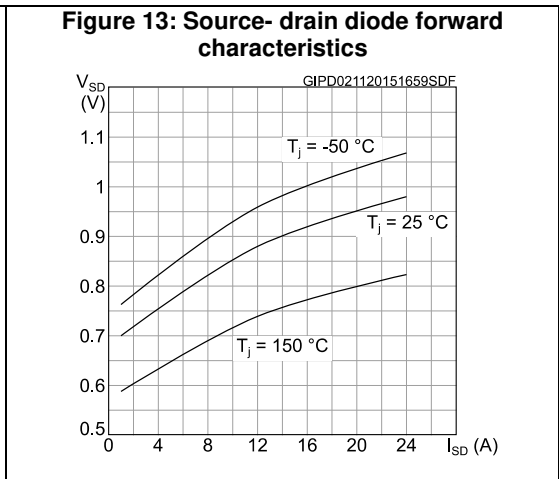
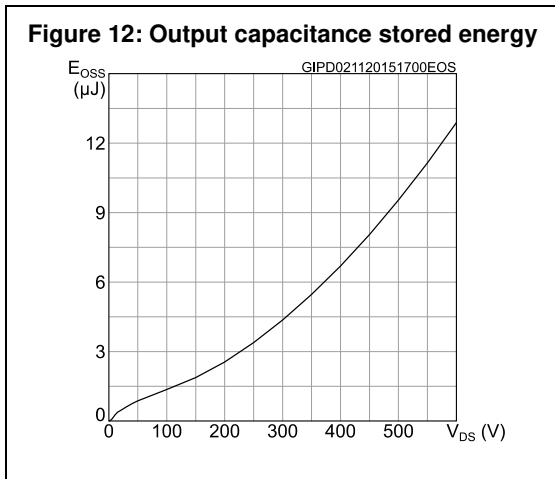
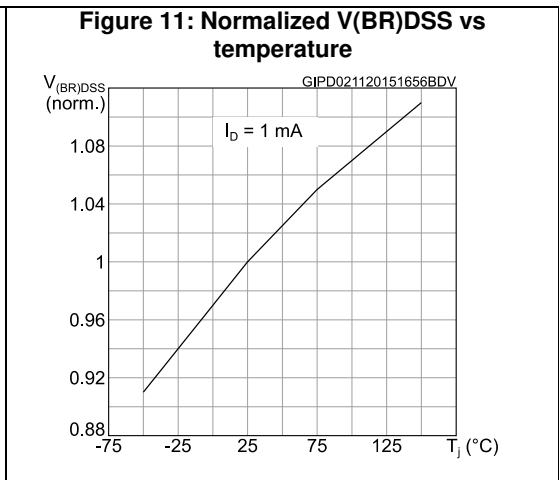
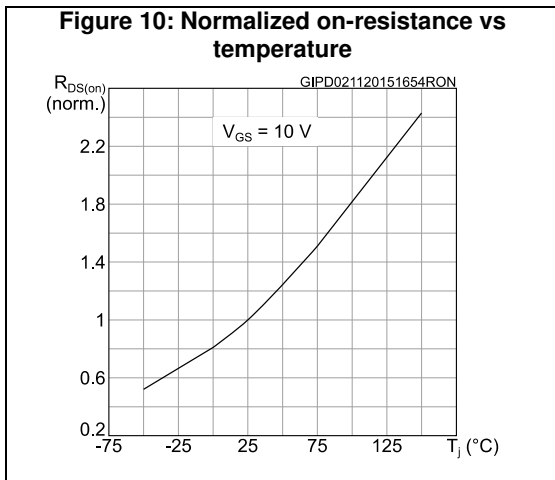
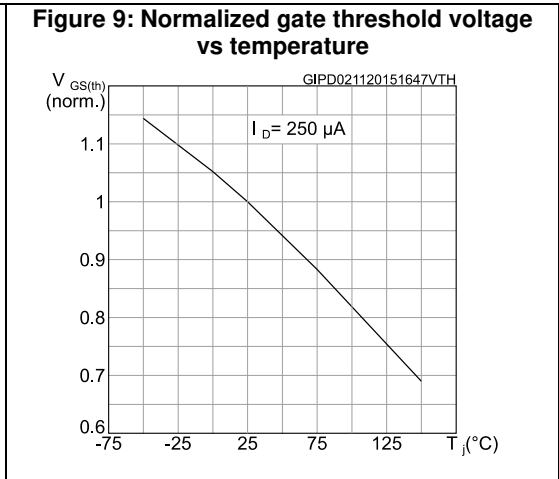
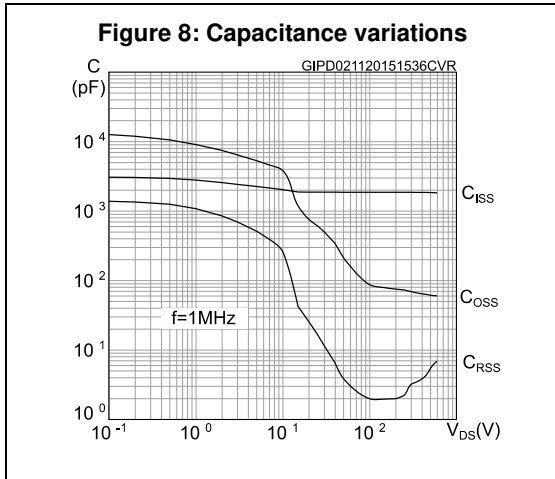
Table 9: Gate-source Zener diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)GSO}$	Gate-source breakdown voltage	$I_{GS} = \pm 250\text{ }\mu\text{A}$, $I_D = 0\text{ A}$	± 30	-	-	V

The built-in back-to-back Zener diodes are specifically designed to enhance the ESD performance of the device. The Zener voltage facilitates efficient and cost-effective device integrity protection, thus eliminating the need for additional external componentry.

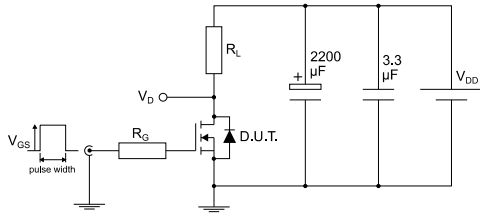
2.1 Electrical characteristics (curves)





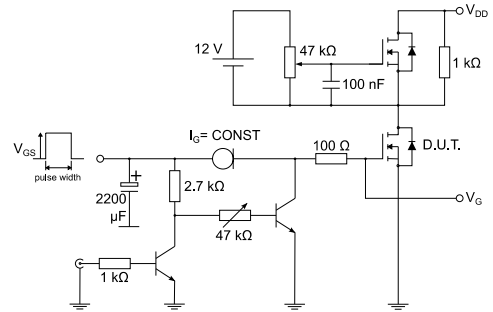
3 Test circuits

Figure 14: Test circuit for resistive load switching times



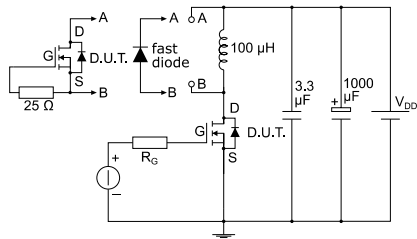
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Figure 15: Test circuit for gate charge behavior



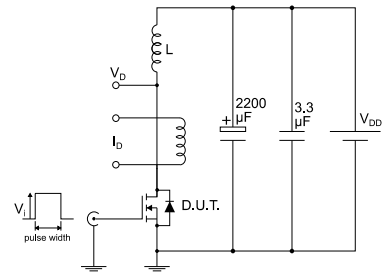
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Figure 16: Test circuit for inductive load switching and diode recovery times



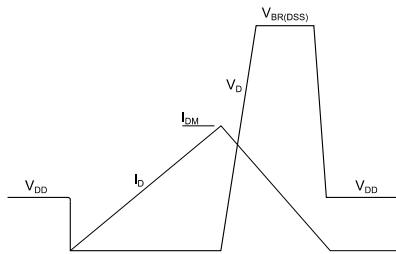
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Figure 17: Unclamped inductive load test circuit



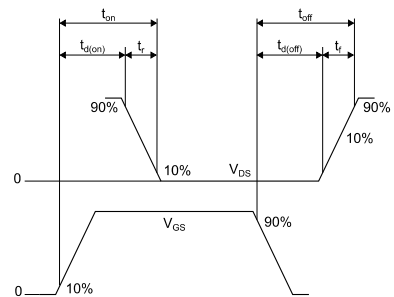
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Figure 18: Unclamped inductive waveform



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Figure 19: Switching time waveform



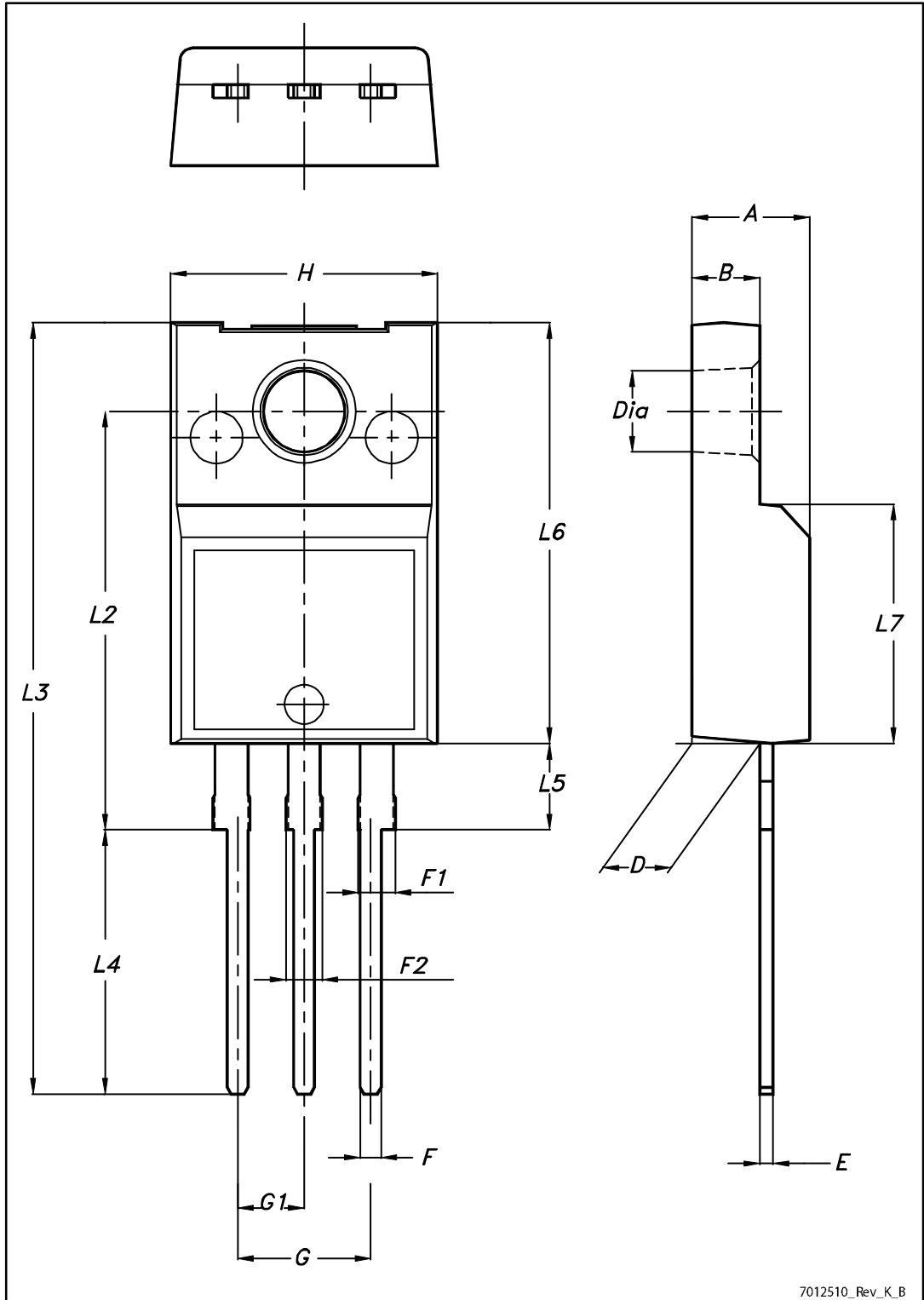
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4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

4.1 TO-220FP package information

Figure 20: TO-220FP package outline



7012510_Rev_K.B

Table 10: TO-220FP package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.4		4.6
B	2.5		2.7
D	2.5		2.75
E	0.45		0.7
F	0.75		1
F1	1.15		1.70
F2	1.15		1.70
G	4.95		5.2
G1	2.4		2.7
H	10		10.4
L2		16	
L3	28.6		30.6
L4	9.8		10.6
L5	2.9		3.6
L6	15.9		16.4
L7	9		9.3
Dia	3		3.2

5 Revision history

Table 11: Document revision history

Date	Revision	Changes
04-Sep-2014	1	First release.
05-Jul-2016	2	Document status promoted from preliminary to production data. Updated title and features in cover page. Updated <i>Section 1: "Electrical ratings"</i> and <i>Section 2: "Electrical characteristics"</i> . Added <i>Section 2.1: "Electrical characteristics (curves)"</i> . Minor text changes.

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