August 2002

FAIRCHILD

SEMICONDUCTOR®

FDS8333C

## 30V N & P-Channel PowerTrench® MOSFETs

General Description

These N & P-Channel MOSFETs are produced using Fairchild Semiconductor's advanced PowerTrench process that has been especially tailored to minimize on-state resistance and yet maintain superior switching performance.

These devices are well suited for low voltage and battery powered applications where low in-line power loss and fast switching are required.

Features

- **Q1** 4.1 A, 30V. $R_{DS(ON)}$ = 80 mΩ @ V_{GS} = 10 V
  $R_{DS(ON)}$ = 130 mΩ @ V_{GS} = 4.5 V

- **Q2** −3.4 A, 30V. $R_{DS(ON)}$ = 130 mΩ @ V_{GS} = −10 V
  $R_{DS(ON)}$ = 200 mΩ @ V_{GS} = −4.5 V

- Low gate charge

- High performance trench technology for extremely low $R_{DS(ON)}$.

- High power and handling capability in a widely used surface mount package.

SO-8

Pin 1
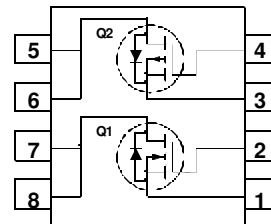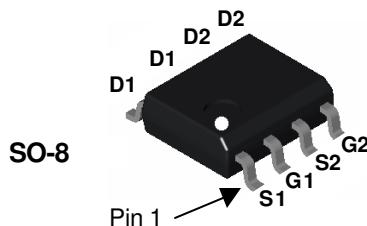
Absolute Maximum Ratings $T_A=25^oC$ unless otherwise noted

Symbol	Parameter		Q1	Q2	Units
V_{DSS}	Drain-Source Voltage		30	−30	V
V_{GSS}	Gate-Source Voltage		±16	±20	
I_D	Drain Current – Continuous	(Note 1a)	4.1	−3.4	A
	– Pulsed		20	−20	
P_D	Power Dissipation for Dual Operation		2		
	Power Dissipation for Single Operation	(Note 1a)	1.6		W
		(Note 1b)	1		
		(Note 1c)	0.9		
T_J, T_{STG}	Operating and Storage Junction Temperature Range		−55 to +150		°C

Thermal Characteristics

$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1a)	78		°C/W
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	(Note 1)	40		

Package Marking and Ordering Information

Device Marking	Device	Reel Size	Tape width	Quantity
FDS8333C	FDS8333C	7"	12mm	2500 units

Electrical Characteristics $T_A = 25°C$ unless otherwise noted

Symbol	Parameter	Test Conditions		Min	Typ	Max	Units
Off Characteristics							
BV_{DSS}	Drain–Source Breakdown Voltage	$V_{GS} = 0$ V, $I_D = 250$ μA / $V_{GS} = 0$ V, $I_D = -250$ μA	**Q1** / **Q2**	30 / −30			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250$ μA, Ref. to 25°C / $I_D = -250$ μA, Ref. to 25°C	**Q1** / **Q2**		25 / −22		mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 24$ V, $V_{GS} = 0$ V / $V_{DS} = -24$ V, $V_{GS} = 0$ V	**Q1** / **Q2**			1 / −1	μA
I_{GSSF} / I_{GSSR}	Gate–Body Leakage, Forward	$V_{GS} = \pm 16$ V, $V_{DS} = 0$ V				±100	nA
I_{GSSF} / I_{GSSR}	Gate–Body Leakage, Reverse	$V_{GS} = \pm 20$V, $V_{DS} = 0$ V				±100	nA
On Characteristics (Note 2)							
$V_{GS(th)}$	Gate Threshold Voltage	**Q1**	$V_{DS} = V_{GS}$, $I_D = 250$ μA	1	1.7	3	V
		Q2	$V_{DS} = V_{GS}$, $I_D = -250$ μA	−1	−1.8	−3	
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate Threshold Voltage Temperature Coefficient	$I_D = 250$ μA, Ref. To 25°C **Q1** / $I_D = -250$ μA, Ref. to 25°C **Q2**			−4.2 / 3.7		mV/°C
$R_{DS(on)}$	Static Drain–Source On–Resistance	**Q1**	$V_{GS} = 10$ V, $I_D = 4.1$ A / $V_{GS} = 4.5$ V, $I_D = 3.2$ A / $V_{GS} = 10$ V, $I_D = 4.1$ A $T_J = 125°C$		67 / 81 / 103	80 / 130 / 145	mΩ
		Q2	$V_{GS} = -10$ V, $I_D = -3.4$ A / $V_{GS} = -4.5$ V, $I_D = -2.5$ A / $V_{GS} = -10$V, $I_D = -3.4$A, $T_J = 125°C$		105 / 167 / 147	130 / 200 / 220	
$I_{D(on)}$	On–State Drain Current	**Q1**	$V_{GS} = 10$ V, $V_{DS} = 5$ V	10			A
		Q2	$V_{GS} = -10$ V, $V_{DS} = -5$ V	−5			
g_{FS}	Forward Transconductance	**Q1**	$V_{DS} = 5$ V $I_D = 4.1$ A		9		S
		Q2	$V_{DS} = -5$ V $I_D = -3.4$A		5		
Dynamic Characteristics							
C_{iss}	Input Capacitance	**Q1**	$V_{DS} = 10$ V, $V_{GS} = 0$ V, $f = 1.0$MHz		282		pF
		Q2	$V_{DS} = -10$ V, $V_{GS} = 0$ V, $f = 1.0$MHz		185		
C_{oss}	Output Capacitance	**Q1**	$V_{DS} = 10$ V, $V_{GS} = 0$ V, $f = 1.0$MHz		49		pF
		Q2	$V_{DS} = -10$ V, $V_{GS} = 0$ V, $f = 1.0$MHz		56		
C_{rss}	Reverse Transfer Capacitance	**Q1**	$V_{DS} = 10$ V, $V_{GS} = 0$ V, $f = 1.0$MHz		20		pF
		Q2	$V_{DS} = -10$ V, $V_{GS} = 0$ V, $f = 1.0$MHz		26		
R_G	Gate Resistance	**Q1**	$V_{GS} = 15$ mV, $f = 1.0$MHz		2.3		Ω
		Q2	$V_{GS} = -15$ mV, $f = 1.0$MHz		−9.6		
Switching Characteristics (Note 2)							
$t_{d(on)}$	Turn–On Delay Time	**Q1**	For **Q1**: $V_{DS} = 10$ V, $I_{DS} = 1$ A, $V_{GS} = 4.5$ V, $R_{GEN} = 6$ Ω		4.5	9	ns
		Q2			4.5	9	
t_r	Turn–On Rise Time	**Q1**			6	12	ns
		Q2	For **Q2**: $V_{DS} = -10$ V, $I_{DS} = -1$ A, $V_{GS} = -4.5$ V, $R_{GEN} = 6$ Ω		13	23	
$t_{d(off)}$	Turn–Off Delay Time	**Q1**			19	34	ns
		Q2			11	20	
t_f	Turn–Off Fall Time	**Q1**			1.5	3	ns
		Q2			2	4	
Q_g	Total Gate Charge	**Q1**	For **Q1**: $V_{DS} = 10$ V, $I_{DS} = 4.1$ A, $V_{GS} = 4.5$ V, $R_{GEN} = 6$ Ω		4.7	6.6	nC
		Q2			4.1	5.7	
Q_{gs}	Gate–Source Charge	**Q1**			0.9		nC
		Q2	For **Q2**: $V_{DS} = -10$ V, $I_{DS} = -3.4$ A, $V_{GS} = -4.5$ V,		0.8		
Q_{gd}	Gate–Drain Charge	**Q1**			0.6		nC
		Q2			0.4		

Electrical Characteristics $T_A = 25°C$ unless otherwise noted

Symbol	Parameter	Test Conditions		Min	Typ	Max	Units
Drain–Source Diode Characteristics and Maximum Ratings							
V_{SD}	Drain–Source Diode Forward Voltage	**Q1**	$V_{GS} = 0$ V, $I_S = 1.3$ A (Note 2)		0.8	1.2	V
		Q2	$V_{GS} = 0$ V, $I_S = -1.3$ A (Note 2)		0.8	−1.2	
t_{rr}	Diode Reverse Recovery Time	**Q1**	$I_F = 4.1$ A, $di_F/d_t = 100$ A/μs		16.3		nS
		Q2	$I_F = -3.4$ A, $di_F/d_t = 100$ A/μs		14.5		
Q_{rr}	Diode Reverse Recovery Charge	**Q1**	$I_F = 4.1$ A, $di_F/d_t = 100$ A/μs		26.7		nC
		Q2	$I_F = -3.4$ A, $di_F/d_t = 100$ A/μs		21.1		

Notes:

1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.
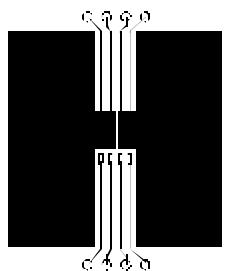
a) 78°C/W when mounted on a 0.5in² pad of 2 oz copper
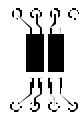
b) 125°C/W when mounted on a 0.02 in² pad of 2 oz copper
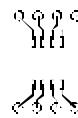
c) 135°C/W when mounted on a minimum pad.

Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width < 300μs, Duty Cycle < 2.0%

Typical Characteristics: N-Channel
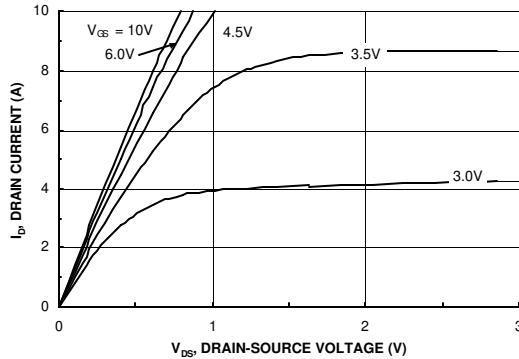
Figure 1. On-Region Characteristics.
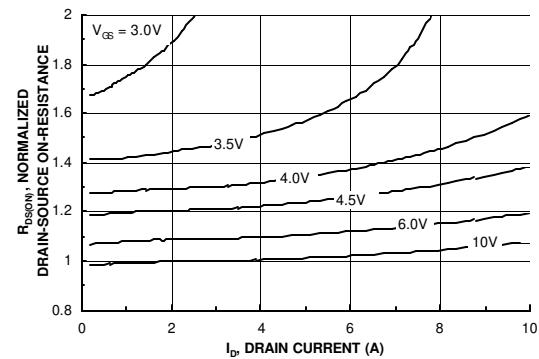
Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.
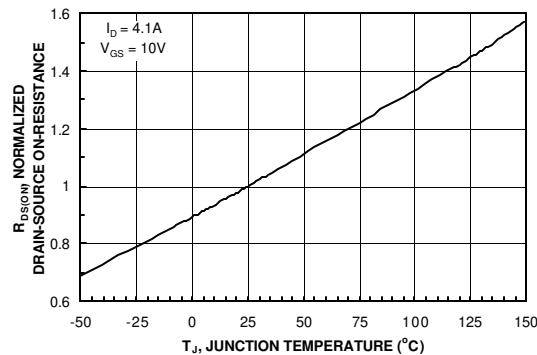

Figure 3. On-Resistance Variation withTemperature.
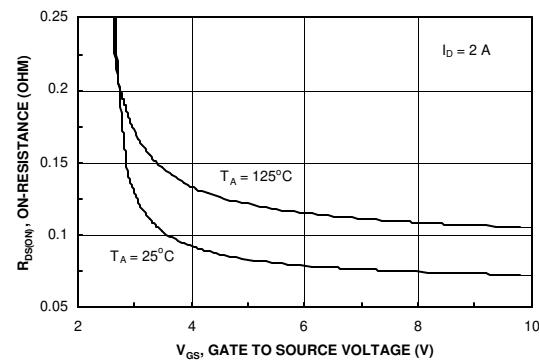

**Figure 4. On-Resistance Variation with Gate-to-Source Voltage.**
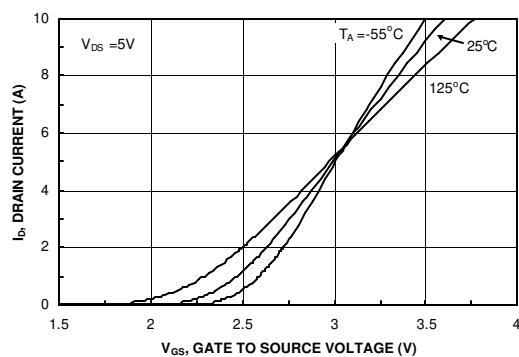

Figure 5. Transfer Characteristics.
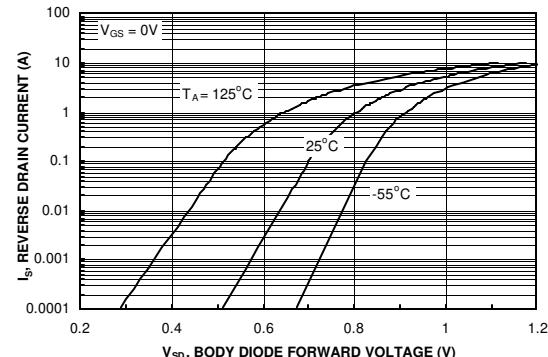
Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.

Typical Characteristics: N-Channel (continued)
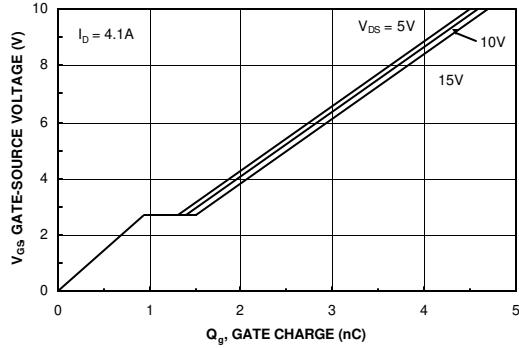
Figure 7. Gate Charge Characteristics.
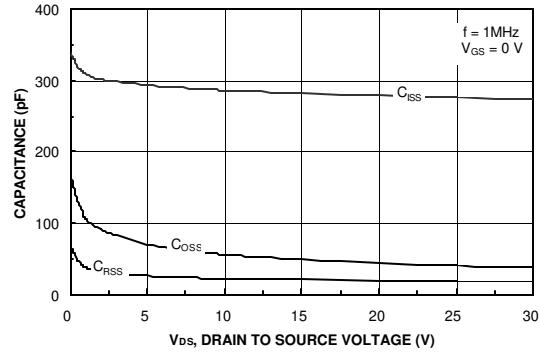
Figure 8. Capacitance Characteristics.
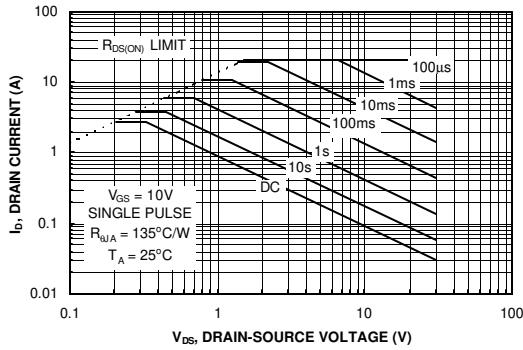
Figure 9. Maximum Safe Operating Area.
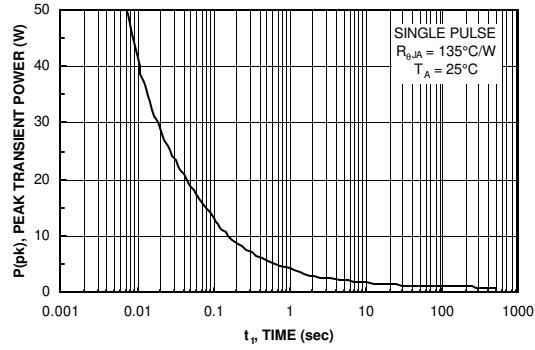
Figure 10. Single Pulse Maximum Power Dissipation.

Typical Characteristics: P-Channel
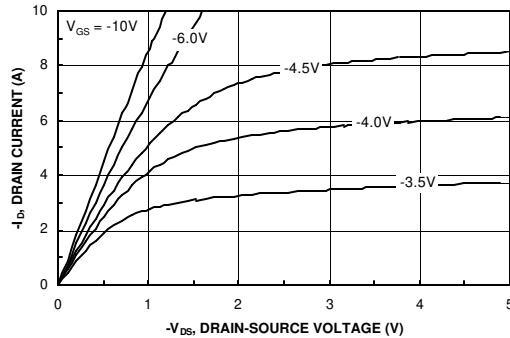

Figure 11. On-Region Characteristics.
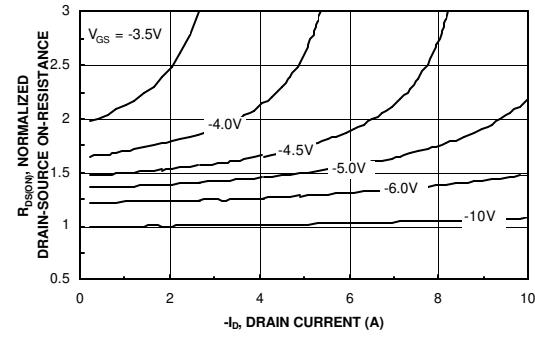
Figure 12. On-Resistance Variation with Drain Current and Gate Voltage.
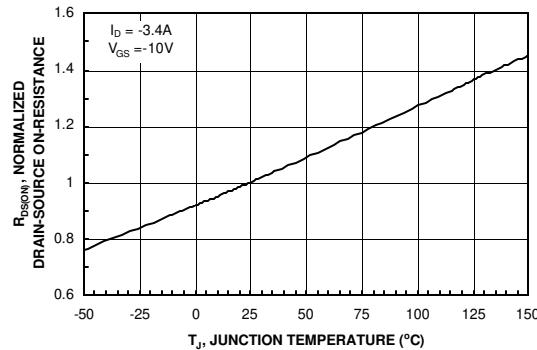
Figure 13. On-Resistance Variation withTemperature.
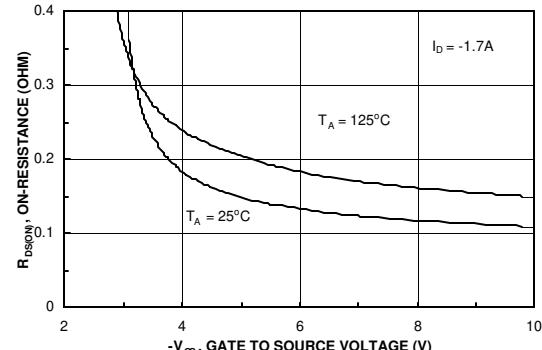
Figure 14. On-Resistance Variation with Gate-to-Source Voltage.
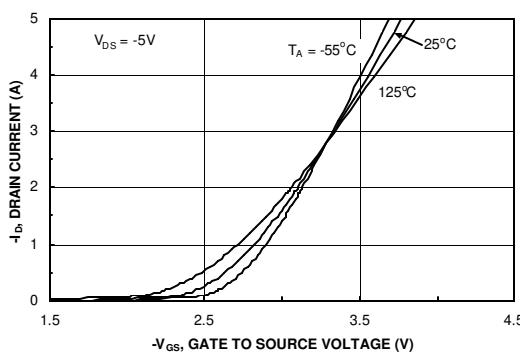

Figure 15. Transfer Characteristics.
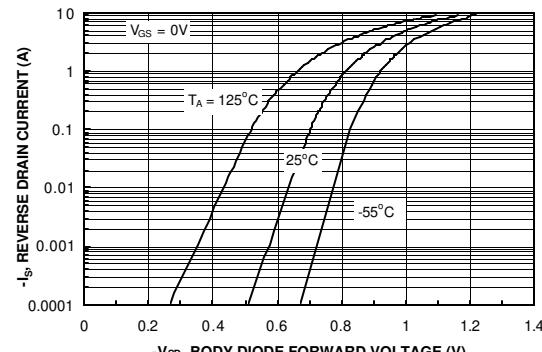
Figure 16. Body Diode Forward Voltage Variation with Source Current and Temperature.

# Typical Characteristics: P-Channel (continued)
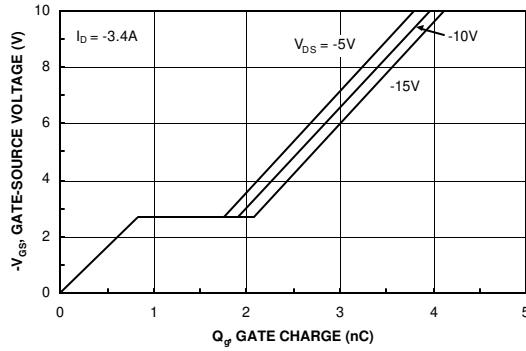

Figure 17. Gate Charge Characteristics.
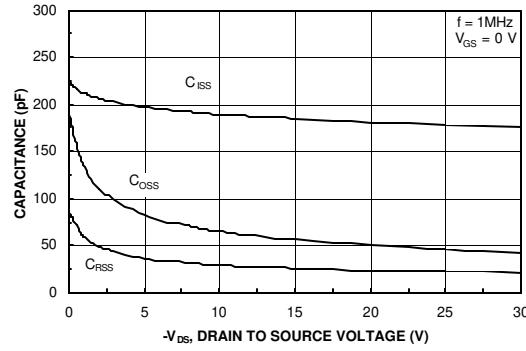
Figure 18. Capacitance Characteristics.
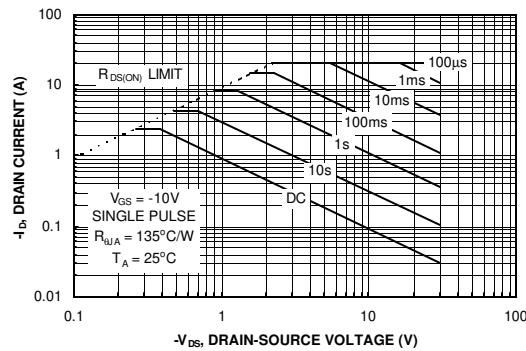

Figure 19. Maximum Safe Operating Area.
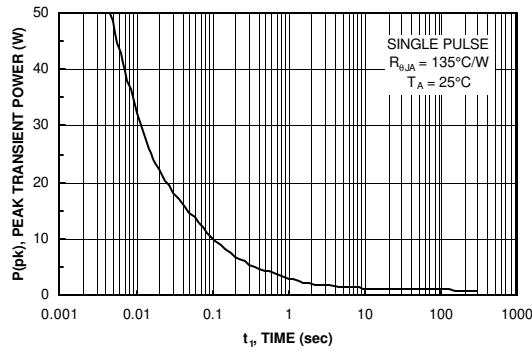
Figure 20. Single Pulse Maximum
Power Dissipation.
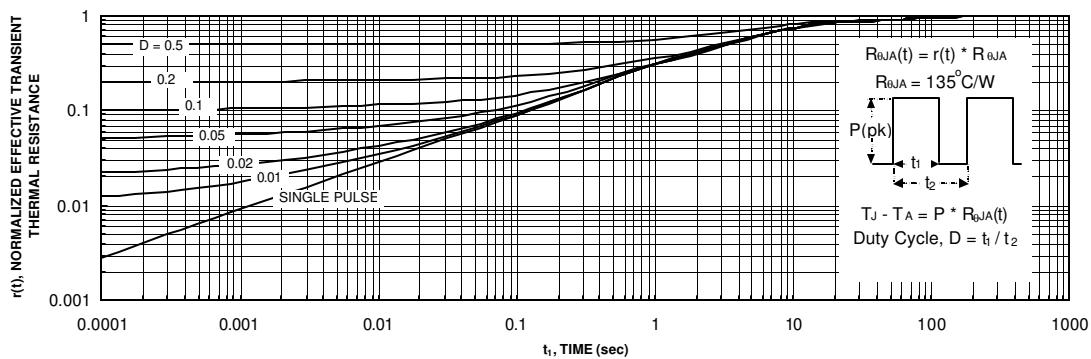
Figure 21. Transient Thermal Response Curve.

**Thermal characterization performed using the conditions described in Note 1c.
Transient thermal response will change depending on the circuit board design.**

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Programmable Active Droop™		OPTOPLANAR™	SMART START™	

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