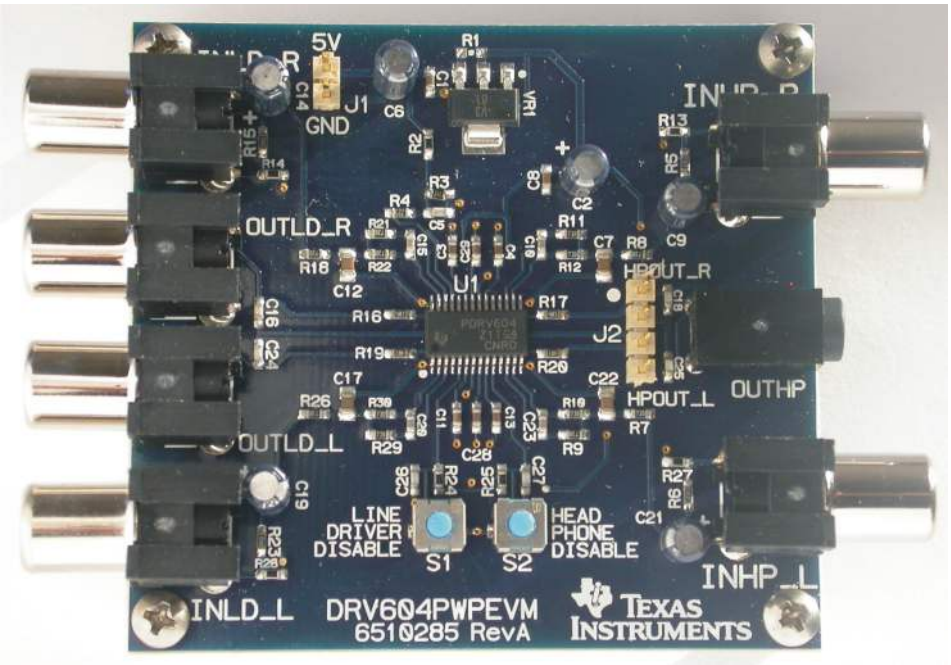
DRV604PWPEVM



DRV604PWPEVM

This user's guide describes the operation of the evaluation module for the DRV604. The user's guide also provides measurement data and design information like schematic, BOM and PCB layout.

Contents

List of Figures

DRV604PWPEVM (continued)

List of Tables

1 Overview

The DRV604PWPEVM customer evaluation module demonstrates the DRV604PWP integrated circuit (IC) from Texas Instruments (TI).

The DRV604PWP is a 2Vrms Pop-Free stereo line driver with a stereo headphone driver designed to allow the removal of the output DC-blocking capacitors for reduced component count and cost. The device is ideal for single supply electronics where size and cost are critical design parameters.

Designed using TI's patented DirectPath™ technology, The DRV604 is capable of driving 2 Vrms into a 5kΩ load and a clean 40mW into a 32Ω headphone with a single 3.3V supply voltage. The device has differential inputs and uses external gain setting resistors, that supports a gain range of ±1V/V to ±10V/V, and line and headphone outputs have ±8kV IEC ESD protection. The DRV604 (occasionally referred to as the '604) has built-in shutdown control for pop-free on/off control.

Using the DRV604 in audio products can reduce component count considerably compared to traditional methods of generating a 2Vrms output. The DRV604 does not require a power supply greater than 3.3V to generate its 5.6Vpp output, nor does it require a split rail power supply. The DRV604 integrates its own charge pump to generate a negative supply rail that provides a clean, pop-free ground biased 2Vrms output.

The DRV604 is available in a 28-pin HTSSOP.

This EVM is configured with single ended RCA input connectors for analog input, and RCA's for the line output and a 3.5mm mini-jack for the HP output. Power supply is connected via a two pin 2.54mm pin header.

Table 1. DRV604PWPEVM Specification

Key Parameters	
Supply Voltage	5 V
Number of Channels	4
Load Impedance: Line	Min 5 kΩ
Load Impedance: HP	Min 32 Ω
Output Voltage: Line	2Vrms
Output Power: Head Phone	40 mW
Dynamic Range	> 103 dB

This EVM is designed for applications such as Set-top boxes, LCD/PDP TV's, Blu-ray DVD receivers, DVD mini-component systems, home theater in a box (HTIB) or soundcards

This document covers EVM specifications, audio performance measurements graphs, and design documentation that includes schematics, parts list and layout design.

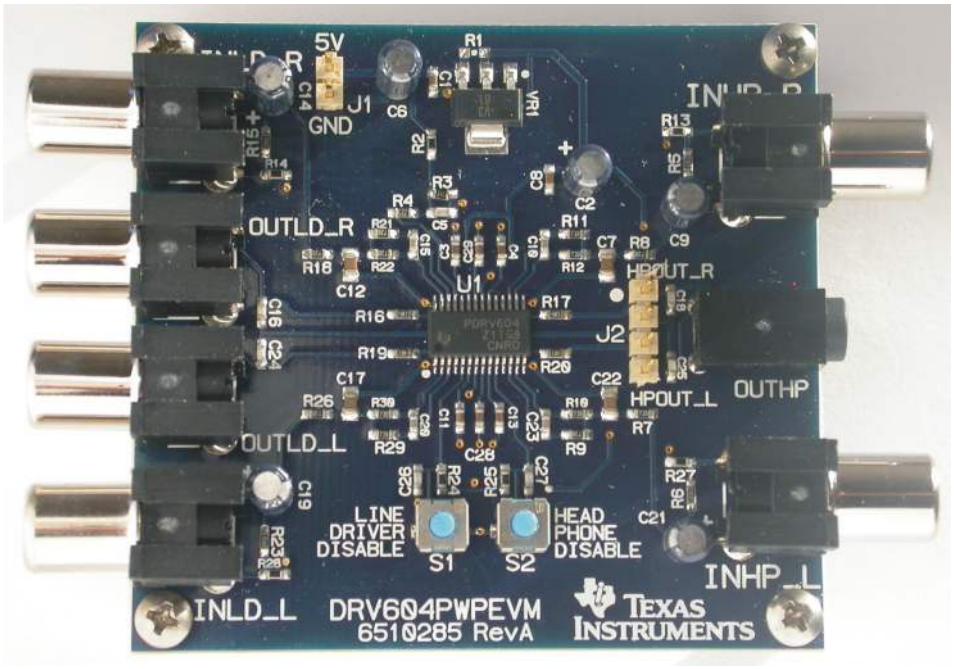


Figure 1. DRV604PWPEVM EVM Photo

Gerber (layout) files are available at www.ti.com.

1.1 DRV604PWPEVM Features

The DRV604PWPEVM has these features:

- 4-channel evaluation module (double-sided, plated-through PCB layout)
- Up to 2-Vrms line output
- Single-ended analog input and output
- Output capacitor less
- Shutdown button

2 Quick Setup Guide

This chapter describes the DRV604PWPEVM board in regards to power supply and system interfaces. The chapter provides information regarding handling and unpacking, absolute operating conditions, and a description of the factory default switch and jumper configuration.

The following is a step-by-step guide to configuring the DRV604PWPEVM for device evaluation.

2.1 Electrostatic Discharge Notice

CAUTION

Failure to observe proper ESD handling procedures may result in damage to EVM components.

2.2 Unpacking the EVM

On opening the DRV604PWPEVM package, ensure that the following items are included:

- 1 pc. DRV604PWPEVM board using one DRV604PWP.

If either of these items is missing, contact the Texas Instruments Product Information Center nearest you to inquire about a replacement.

2.3 Power-Supply Setup

To power up the EVM one power supply is needed. The power supply is connected to the EVM using a 2pin 2.54mm pin header, J1.

Table 2. Recommended Supply Voltage

Description	Voltage Limitations	Current Requirement	Cable
Power supply	5 V	0.1 A	—

CAUTION

Applying voltages above the limitations given in Table 2 may cause permanent damage to your hardware.

3 On/Off Sequence

For minimum click and pop during power on and power off, the DRV604 Enable inputs, pin 5 and pin 10, should be kept low. The preferred power-up/down sequence is shown in Figure 2.

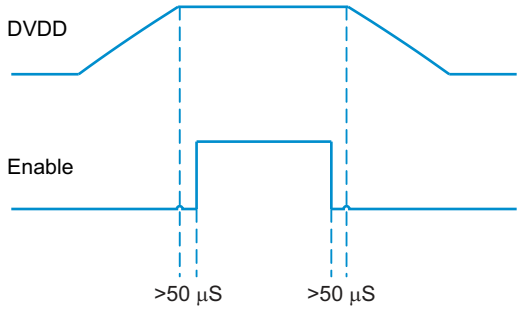


Figure 2. Power-Up/-Down Sequence

4 Component Selection

4.1 Charge Pump

The charge pump flying capacitors, C28 and C29, serves to transfer charge during the generation of the negative supply voltage. The PVSS capacitors, C11 and C13, must be at least equal to the charge pump capacitor in order to allow maximum charge transfer. Low ESR capacitors are an ideal selection, and a value of 1µF is typical. Capacitor values smaller than 1µF can be used, but the maximum output can be reduced, it is therefore recommended to validate the design with thorough testing.

4.2 Decoupling Capacitors

The DRV604 is a DirectPath™ Line Driver amplifier that requires adequate power supply decoupling to ensure that the noise and total harmonic distortion (THD) are low. Good low equivalent-series-resistance (ESR) ceramic capacitors, C3 and C4 typical 1µF, placed as close as possible to the device V_{DD} leads works best. Placing this decoupling capacitor close to the DRV604 is important for the performance of the amplifier. For filtering lower frequency noise signals, a 10µF or greater capacitors placed near the audio amplifier would also help, but is not required in most applications because of the high PSRR of this device.

The charge pump circuit does apply ripple current on the V_{DD} line, and an LC or RC filter may be needed if noise-sensitive audio devices share the V_{DD} supply.

4.3 Using the DRV604 as a 2nd Order Low-Pass Filter

Several audio DACs used today require an external low-pass filter to remove out of band noise. This is possible with the DRV604 and the EVM is configured as a 50kHz 2nd order active Butterworth filter. The topology chosen is the MFB with single ended input. Further the DRV604 needs an AC-coupling capacitor to remove dc-content from the source.

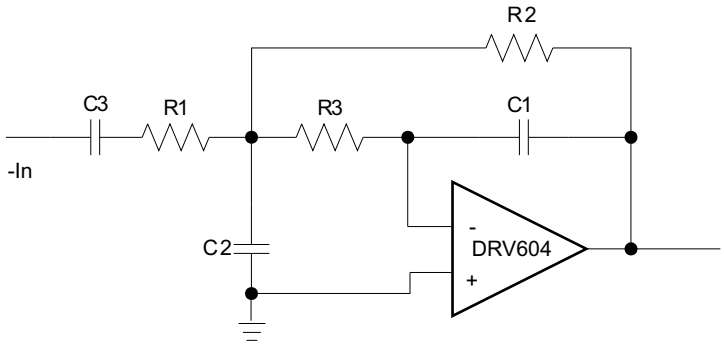


Figure 3. 2nd Order Active Low-Pass Filter, SE Input

This topology demands a unity gain stable opamp, if that's not the case, a capacitor from inverting input to GND of the same value as C1 is used. That increases the high frequency gain to 2.

The component values can be calculated with the help of the TI FilterPro™ program available on:

http://focus.ti.com/docs/toolsw/folders/print/filterpro.html

In Table 3 various proposals for the filter and gain settings can be found.

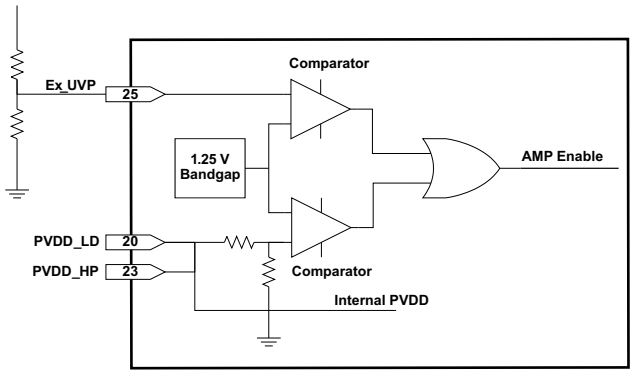
Table 3. DRV604PWPEVM Filter Specifications

EVM Reference Designators			C10, C15, C20, C23	C7, C12 C17, C22	C9, C14, C19, C21	R8, R18 R26, R7	R11, R21 R29, R9	R12, R22 R30, R10
Gain	High Pass	Low Pass	C1	C2	C3	R1	R2	R3
–1 V/V	1.6 Hz	40 kHz	100 pF	680 pF	10 μF	10 kΩ	10 kΩ	24 kΩ
–1.5 V/V	1.3 Hz	40 kHz	68 pF	680 pF	15 μF	8.2 kΩ	12 kΩ	30 kΩ
–2 V/V	1.6 Hz	40 kHz	33 pF	330 pF	6.8 μF	15 kΩ	30 kΩ	47 kΩ
–2 V/V	1.6 Hz	30 kHz	47 pF	470 pF	6.8 μF	15 kΩ	30 kΩ	43 kΩ
–3.33 V/V	1.2 Hz	40 kHz	33 pF	470 pF	10 μF	13 kΩ	43 kΩ	43 kΩ
–10 V/V	0.6 Hz	30 kHz	22 pF	1 nF	22 μF	4.7 kΩ	47 kΩ	27 kΩ

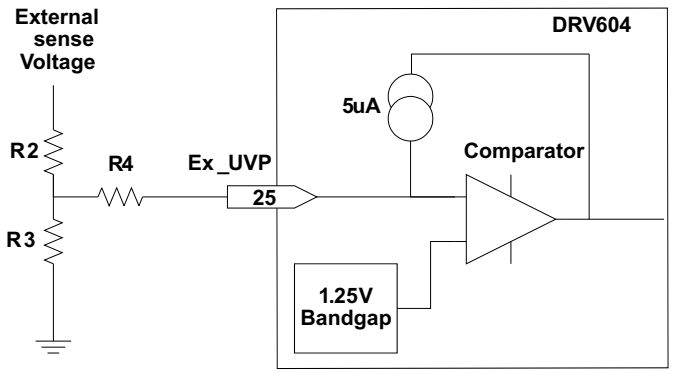
The resistor values should be low value to achieve low noise, but should be of high enough value to obtain a small size ac-coupling capacitor.

4.4 Internal and External Under Voltage Detection and RESET Output

The DRV604 contains an internal precession band gap reference voltage and 2 comparators, one is used to monitor the supply voltage, PVDD_AB and PVDD_CD, the other to monitor an external user selectable voltage on pin 25. The internal PVDD monitor is set at 2.8V with 200mV hysteresis.



The external under voltage detection can be used to shutdown the DRV604 before an input device can make a pop. The shutdown threshold at the UVP pin is 1.25V. A resistor divider is used to obtain the shutdown threshold and hysteresis desired for the application.



The selected thresholds can be determined as follows:

$$V_{UVP} = 1.25\ V \times \frac{(R2 + R3)}{R3}$$

$$V_{Hysteresis} = 5\ \mu A \times R4 \left(\frac{R2}{R3} + 1\right)$$

With the condition R4 >> R2||R3

For example, to obtain V_{UVP} = 4.5V and 400mV hysteresis, we can use R2=10k, R3=3k9 and R4 = 22k.

To filter supply spikes and noise a capacitor across R3 can be added.

5 Layout Recommendations

The charge pump capacitors, C28 and C29, should be routed with as short a track as possible, the same goes for the supply decoupling caps, C3, C4 and C11, C13. To avoid ground loop induced hum, the AGND, PGND and the audio input GND tracks should be routed as star ground connections – this is the concept used on DRV604PWPEVM.

6 DRV604PWPEVM Performance

Table 4. General Test Conditions[(1)]

General Test Conditions		Notes
Supply voltage	5.0 V	
Load impedance	5 kΩ	
Input signal	1 kHz Sine	
Measurement filter	AES17	

(1) These test conditions are used for all tests, unless otherwise specified.

Table 5. Electrical Data

Electrical Data		Notes/Conditions
Output voltage, 5 kΩ	2.1 Vrms	1 kHz, 1% THD+N, T_A = 25°C
Output voltage, 100 kΩ	2.2 Vrms	1 kHz, 1% THD+N, T_A = 25°C
Supply current	< 30 mA	1 kHz, 40mW at 32 Ω and 2Vrms at 5 kΩ

Table 6. Audio Performance Line Output

Audio Performance Analog Input			Notes/Conditions
THD+N, 5 kΩ	0.02 Vrms	< 0.070 %	1 kHz (Noise limited)
THD+N, 5 kΩ	0.2 Vrms	< 0.007 %	1 kHz (Noise limited)
THD+N, 5 kΩ	2 Vrms	< 0.002 %	1 kHz
Dynamic range		> 109 dB	Ref: 2Vrms, A-weighted, AES17 filter
Noise voltage		< 7 μV_{RMS}	A-weighted, AES17 filter
DC offset		< 1 mV	No signal, 2.5-kΩ load
Channel separation		> 100 dB	1 kHz, 2 Vrms
Frequency response: 20 Hz to 20 kHz		±0.5 dB	2 Vrms / 2.5 kΩ

Table 7. Audio Performance Headphone Output

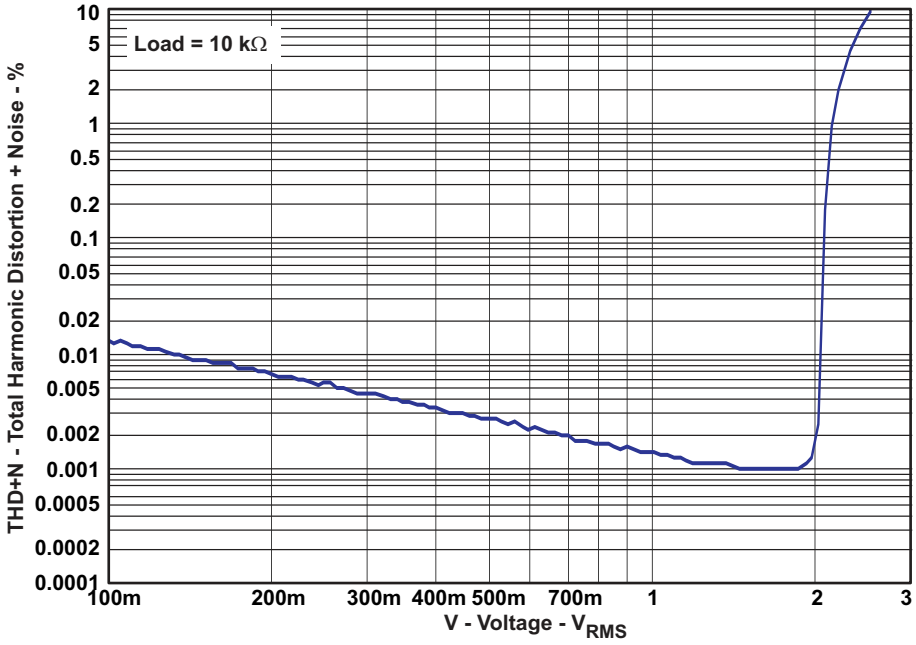
Audio Performance Analog Input			Notes/Conditions
THD+N, 32 Ω	0.4 mWrms	< 0.005 %	1 kHz (Noise limited)
THD+N, 32 Ω	4.0 mWrms	< 0.010 %	1 kHz (Noise limited)
THD+N, 32 Ω	40 mWrms	< 0.030 %	1 kHz
Dynamic range		> 103 dB	Ref: 40mWrms at 32 Ω, A-weighted, AES17 filter
Noise voltage		< 9 μV_{rms}	A-weighted, AES17 filter
DC offset		< 1 mV	No signal, 32 Ω load
Channel separation		> 70 dB	1 kHz, 2 V_{RMS}
Frequency response: 20 Hz to 20 kHz		±0.5 dB	40mWrms / 32 Ω

Table 8. Physical Specifications

Physical Specifications		Notes/Conditions
PCB dimensions	65 × 60 × 25 mm	Width × Length × Height (mm)
Total weight	34 gr	Components + PCB + Mechanics

Note: All electrical and audio specifications are typical values

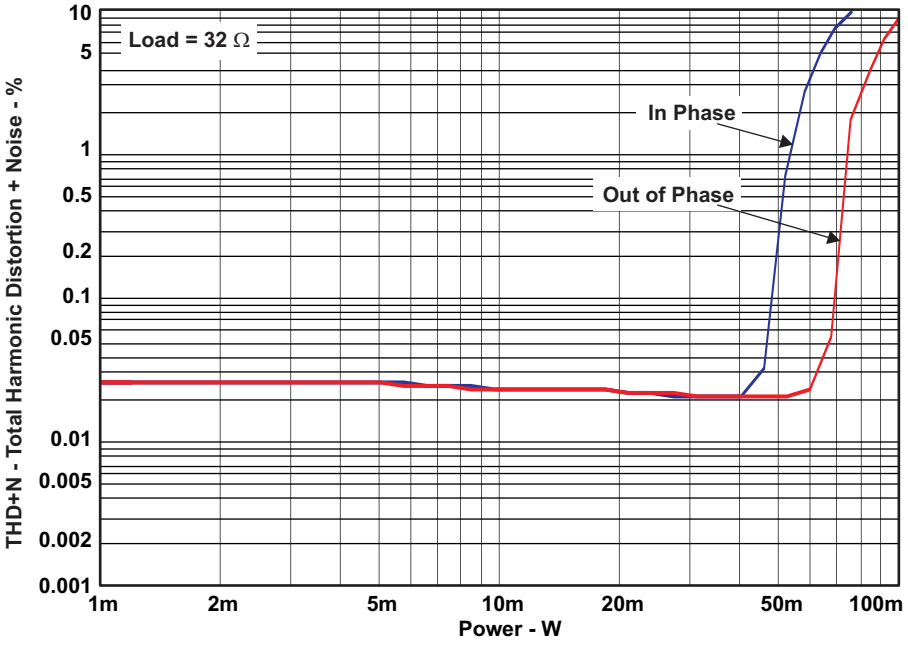
6.1 THD+N vs Voltage and Power



Blue: 10 kΩ

Figure 4. THD+N vs Voltage (Line Output)

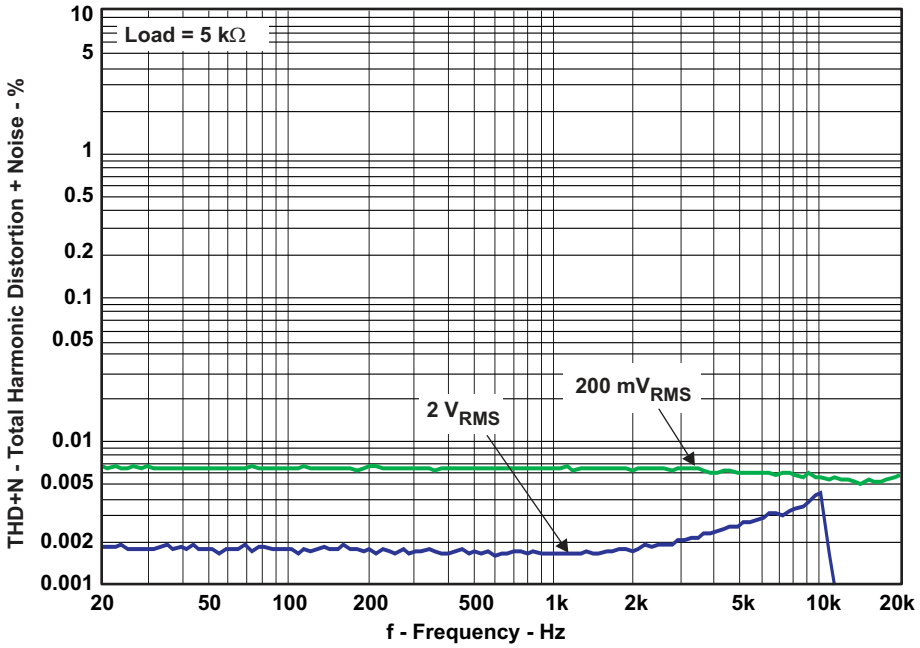
The THD+N up to over 1Vrms are dominated by noise. 0.001% equals –100dB !



Blue: 32 Ω

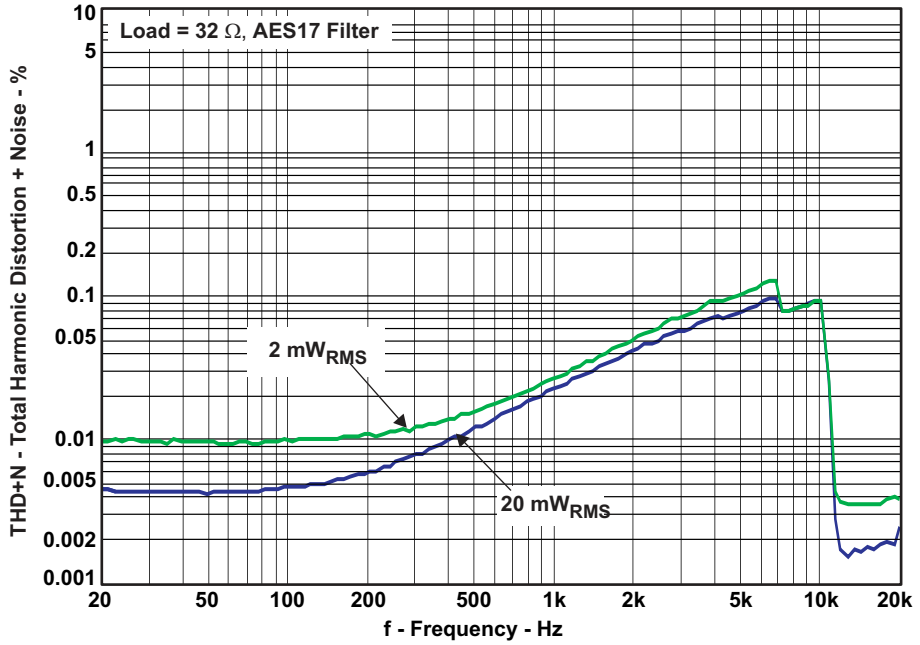
Figure 5. THD+N vs Power (HeadPhone Output)

6.2 THD+N vs Frequency



Green 200mVrms Blue: 2Vrms Load Impedance 5kΩ

Figure 6. THD+N vs Frequency (Line Output)



Green 2mWrms Blue: 20mWrms Load Impedance is 32Ω

Figure 7. THD+N vs Frequency (HeadPhone Output)

6.3 FFT Spectrum with –60dBFS Tone

Reference voltage is 2Vrms. FFT size 16k.

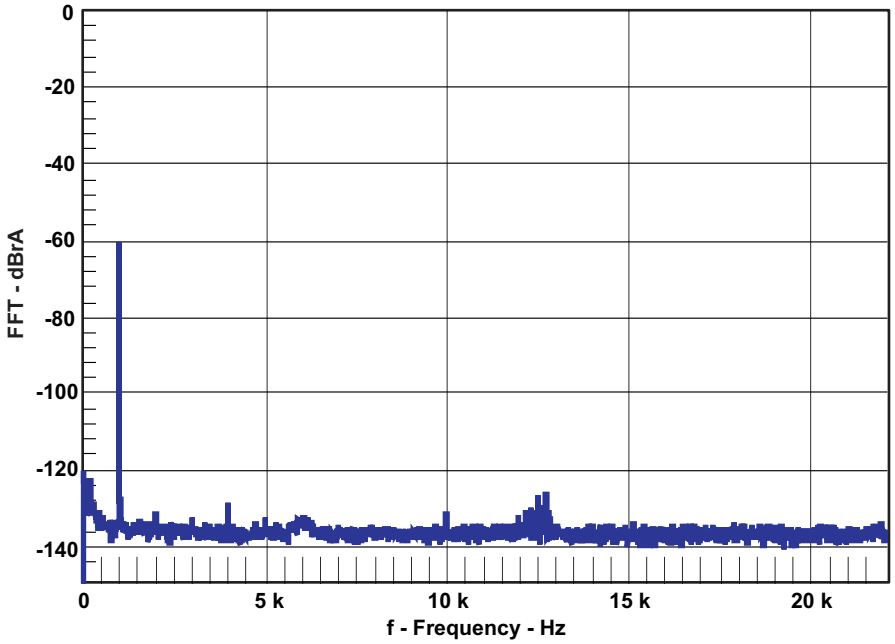


Figure 8. FFT Spectrum with –60-dBFS Tone (Line Output)

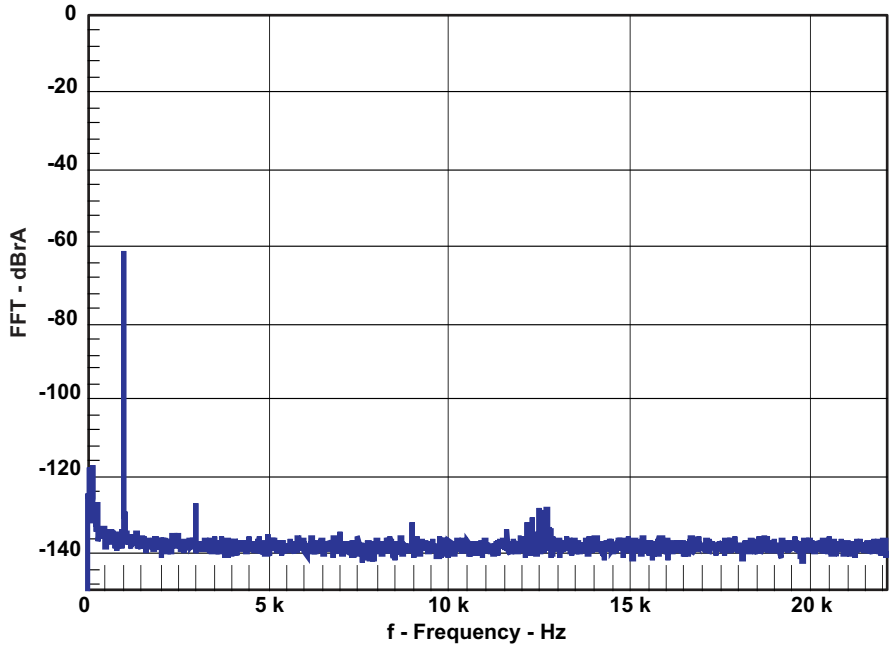
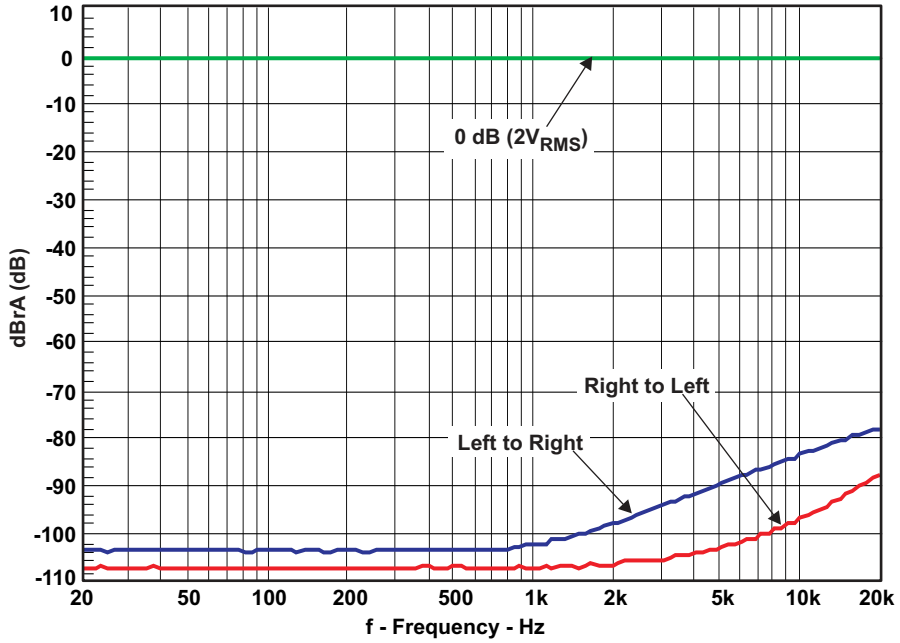


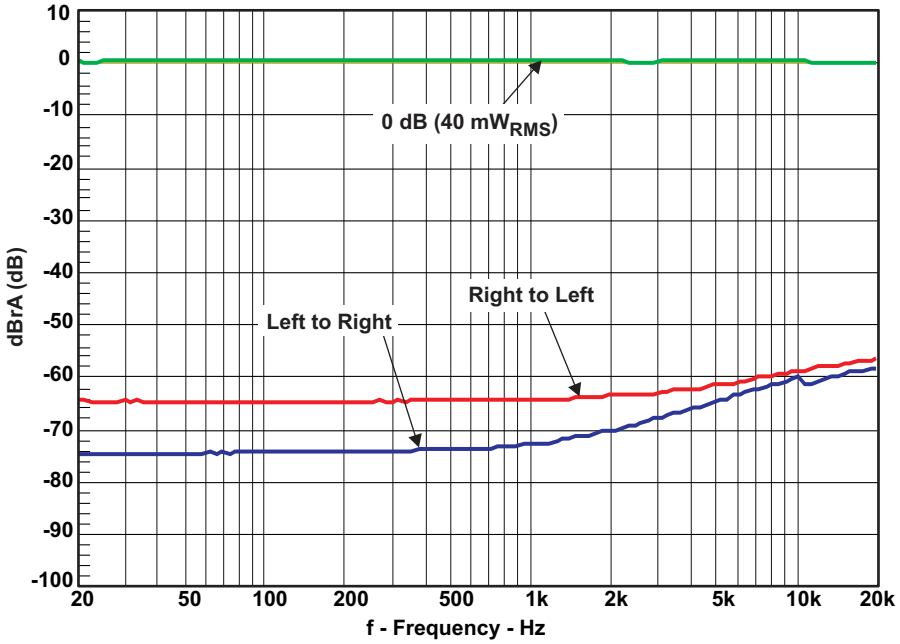
Figure 9. FFT Spectrum with –60-dBFS Tone (Head-Phone Output)

6.4 Channel Separation



Comments: Green: 0dB (2vrms) Blue: Left to right Red: Right to left

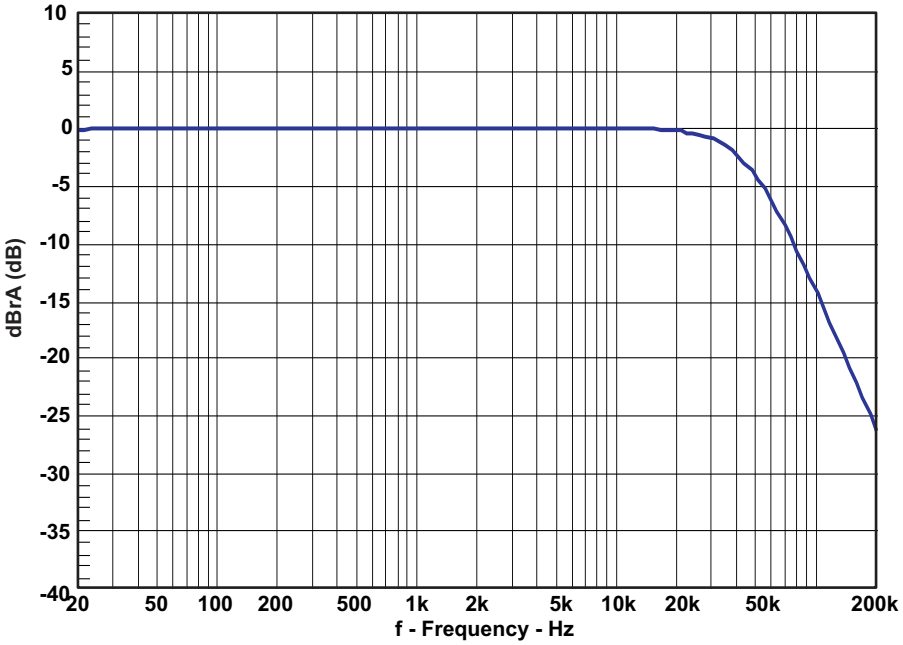
Figure 10. Channel Separation, Line Output



Comments: Green: 0dB (40mWrms) Blue: Left to right Red: Right to left

Figure 11. Channel Separation, Headphone Output

6.5 Frequency Response



1Vrms output, 10kΩ load, 500kHz measurement filter, 2Vrms reference

Figure 12. Frequency Response, Line Output

6.6 Pop/Click (Enable)

Shown with and without input signal applied. The measurement results are presented in time domain. Load 5 kΩ.

Power supply is applied, and then the shutdown signal is released. The enable signal is used to trigger the measuring system.

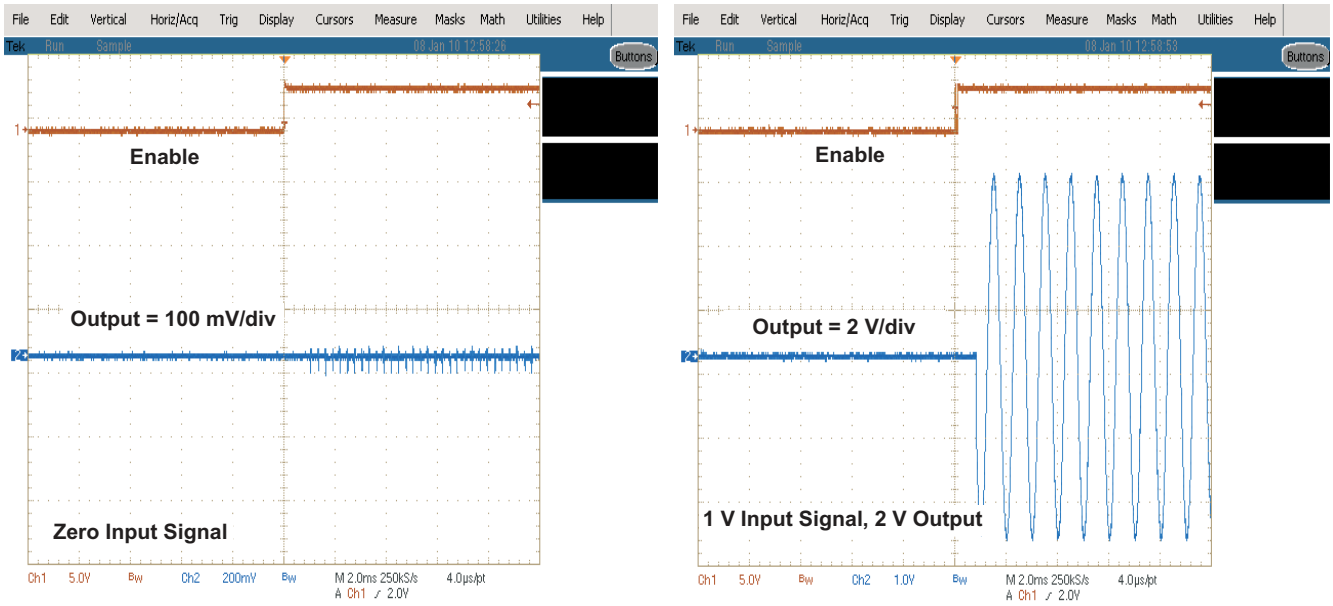


Figure 13. Pop/Click (Enable)

6.7 Pop/Click (Disable)

Shown with and without input signal applied. The measurement results are presented in time domain. Load 5 kΩ

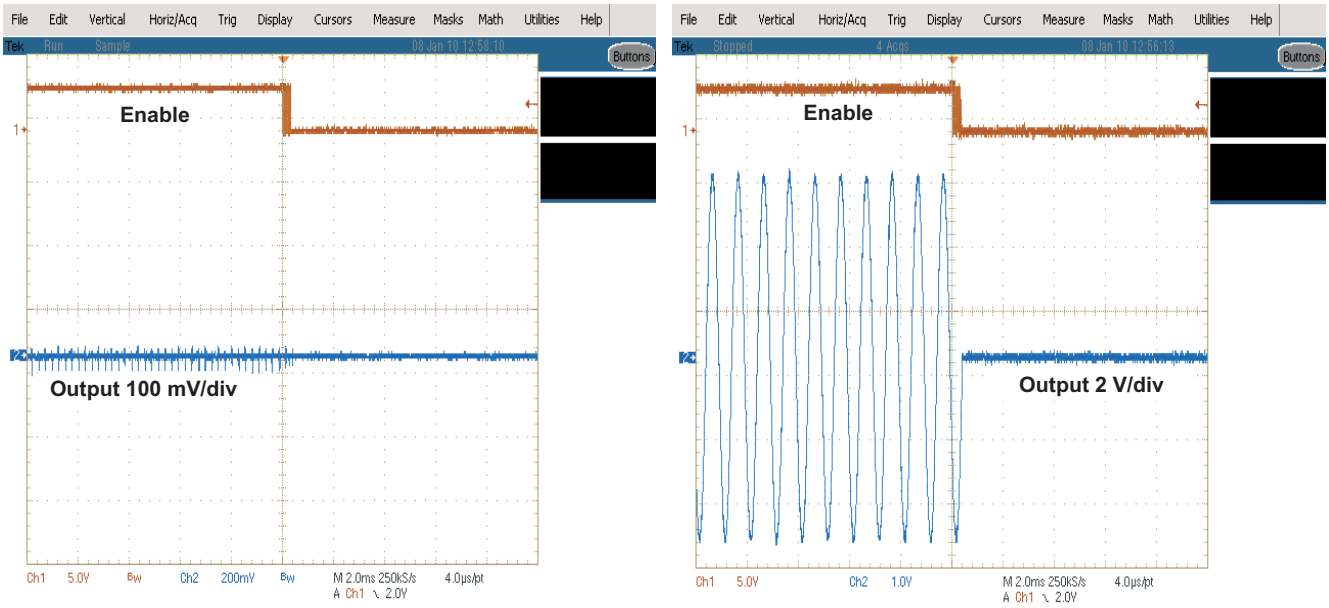


Figure 14. Pop/Click (Disable)

7 Related Documentation from Texas Instruments

Table 9 contains a list of data manuals that have detailed descriptions of the integrated circuits used in the design of the DRV604PWPEVM. The data manuals can be obtained at the URL http://www.ti.com.

Table 9. Related Documentation

Part Number	Literature Number
DRV604	SLOS659
TLV1117-33	SLVS561I

8 Design Documentation

8.1 Schematics

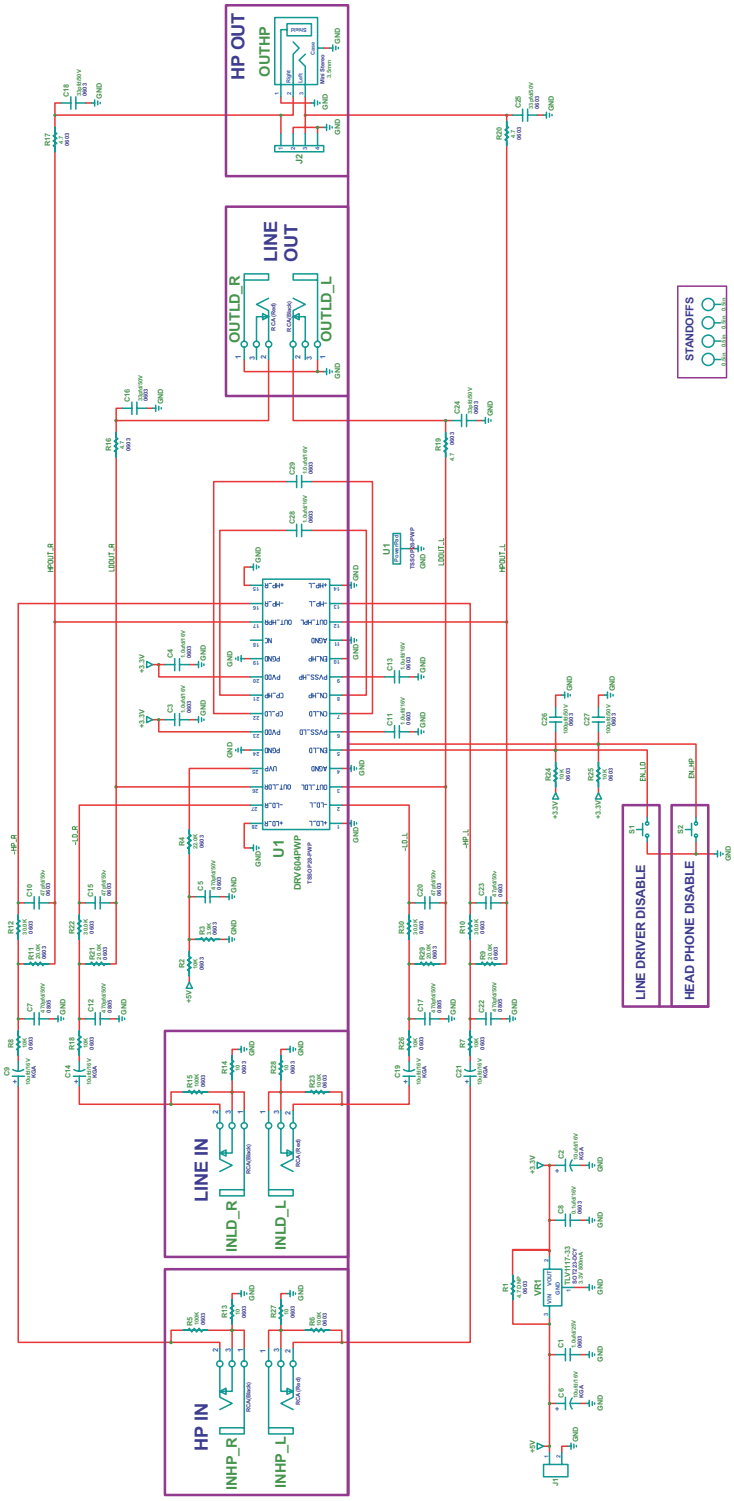


Figure 15. DRV604PWPEVM Schematic: DRV604

8.2 Parts List

Table 10. Bill of Materials

MANU Part No.	QTY	Ref Des	Vendor Part No.	Description	Vendor	MANU
TI-SEMICONDUCTORS						
DRV604PWP	1	U1	DRV604PWP	NEED DATA, TSSOP28-PWP ROHS	TI	TI
TLV1117-33CDCYR	1	VR1	296-21112-1	VOLT REG LDO 3.3V 800mA SOT223-DCY ROHS	DIGI-KEY	TI
CAPACITORS						
ECJ-1VC1H330J	4	C16, C18, C24, C25	PCC330ACVCT	CAP SMD0603 CERM 33PFD 50V 5% NPO ROHS	DIGI-KEY	PANASONIC
ECJ-1VC1H470J	4	C10, C15, C20, C23	PCC470ACVCT	CAP SMD0603 CERM 47PFD 50V 5% NPO ROHS	DIGI-KEY	MURATA
ECJ-1VC1H101J	2	C26, C27	PCC101ACVCT	CAP SMD0603 CERM 100PFD 50V 5% NPO ROHS	DIGI-KEY	PANASONIC
ECJ-1VC1H471J	1	C5	PCC2147CT	CAP SMD0603 CERM 470PFD 50V 5% NPO ROHS	DIGI-KEY	PANASONIC
08055A471JAT2A	4	C7, C12, C17, C22	478-1324-1	CAP SMD0805 CERM 470PFD 50V 5% NPO ROHS	DIGI-KEY	AVX
ECJ-1VB1C104K	1	C8	PCC1762CT	CAP SMD0603 CERM 0.1UFD 16V 10% X7R ROHS	DIGI-KEY	PANASONIC
C1608X7R1C105K	6	C3, C4, C11, C13, C28, C29	445-1604-1	CAP SMD0603 CERM 1.0UFD 16V 5% X7R ROHS	DIGI-KEY	TDK
TMK107BJ105KA	1	C1	587-1248-1	CAP SMD0603 CERM 1.0UFD 25V 10% X5R ROHS	DIGI-KEY	TAIYO YUDEN
ECE-A1CKG100	6	C2, C6, C9, C14, C19, C21	P910	CAP 10UFD 16V RAD ALUM ELEC KGA ROHS	DIGI-KEY	PANASONIC
RESISTORS						
RC0603JR-074R7L	4	R16, R17, R19, R20	311-4.7GRCT	RESISTOR SMD0603 4.7 R 5% THICK FILM 1/10W	DIGI-KEY	YAGEO
RC0603JR-0710RL	4	R13, R14, R27, R28	311-10GRCT	RESISTOR SMD0603 THICK FILM 10 R 5% 1/10W	DIGI-KEY	YAGEO
ERJ-3GEYJ392V	1	R3	P3.9KGCT	RESISTOR SMD0603 3.9K Ω 5% 1/10W ROHS	DIGI-KEY	PANASONIC
ERJ-3GEYJ103V	7	R2, R7, R8, R18, R24, R25, R26	P10KGCT	RESISTOR SMD0603 10K 5% 1/10W ROHS	DIGI-KEY	PANASONIC
ERJ-3EKF2002V	4	R9, R11, R21, R29	P20.0KHCT	RESISTOR SDM0603 20.0kΩ 1% 1/16W ROHS	DIGI-KEY	PANASONIC
ERJ-3EKF2202V	1	R4	P22.0KHCT	RESISTOR SMD0603 22.0k 1% THICK FILM 1/10W	DIGI-KEY	PANASONIC
RC0603FR-0730KL	4	R10, R12, R22, R30	311-30.0KHRCT	RESISTOR SMD0603 THICK FILM 30.0k 1% 1/10W	DIGI-KEY	PANASONIC
HEADERS AND JACKS						
PBC02SAAN	1	J1	S1011E-02	HEADER THRU MALE 2 PIN 100LS GOLD ROHS	DIGI-KEY	SULLINS
PBC04SAAN	1	J2	S1011E-04	HEADER THRU MALE 4 PIN 100LS GOLD ROHS	DIGI-KEY	SULLINS
PJRAN1X1U03X	3	INHP_L, INLD_L, OUTLD_R	89K7617	JACK, RCA 3-PIN PCB-RA RED ROHS	NEWARK	SWITCHCRAFT
PJRAN1X1U01X	3	INHP_R, INLD_R, OUTLD_L	65K7770	JACK, RCA 3-PIN PCB-RA BLACK ROHS	NEWARK	SWITCHCRAFT
STX-3000	1	OUTHP	806-STX-3000	JACK,MINI-STEREO,ROHS	MOUSER	KYCON
SWITCHES						
TL1015AF160QG	2	S1, S2	EG4344CT	SWITCH, MOM, 160G SMT 4×3MM ROHS	DIGI-KEY	E-SWITCH
COMPONENTS NOT ASSEMBLED						
R1						

8.3 PCB Layers

Gerber files are available on the EVM page for download

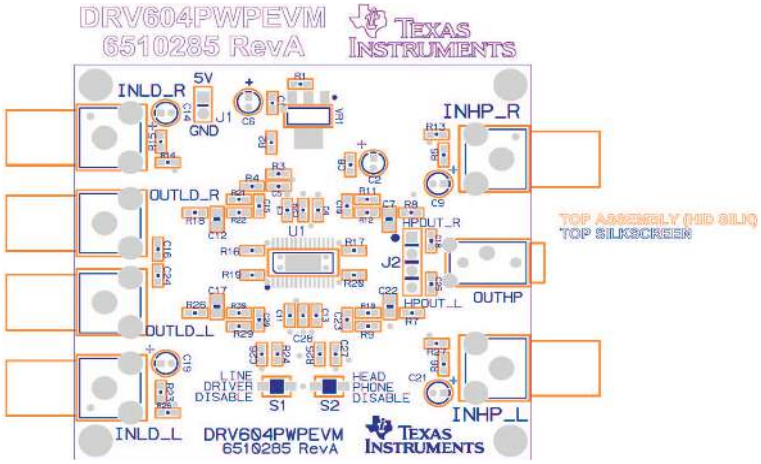


Figure 16. DRV604PWPEVM PCB Component Placement

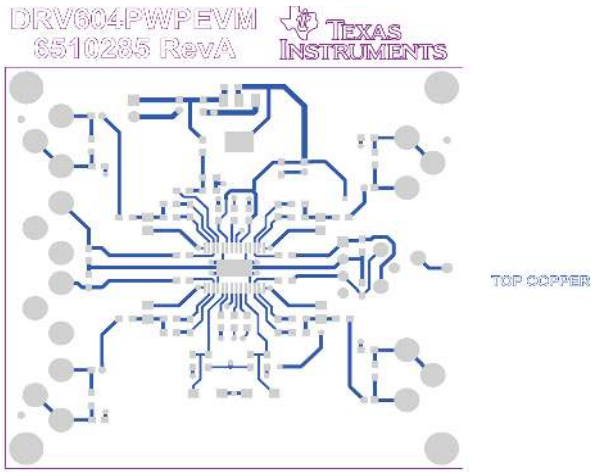


Figure 17. DRV604PWPEVM PCB Top Layer

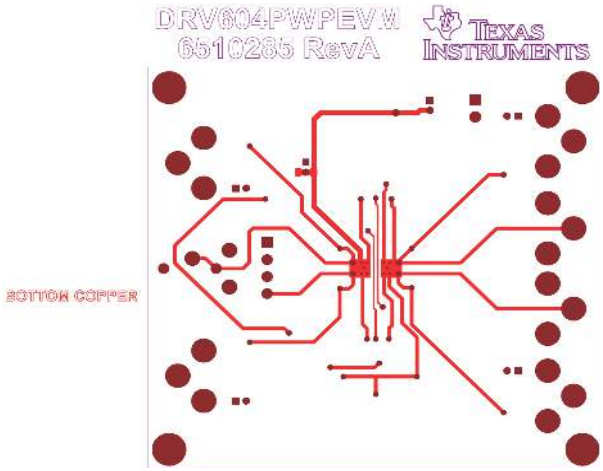


Figure 18. DRV604PWPEVM PCB Bottom Layer

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EVM WARNINGS AND RESTRICTIONS

It is important to operate this EVM within the input voltage range of 0 V to 3 V_{RMS} and the output voltage range of 0 V to 3.3 V.

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than +60°C. The EVM is designed to operate properly with certain components above +40°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

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