

## ***LMR50410EVM User's Guide***

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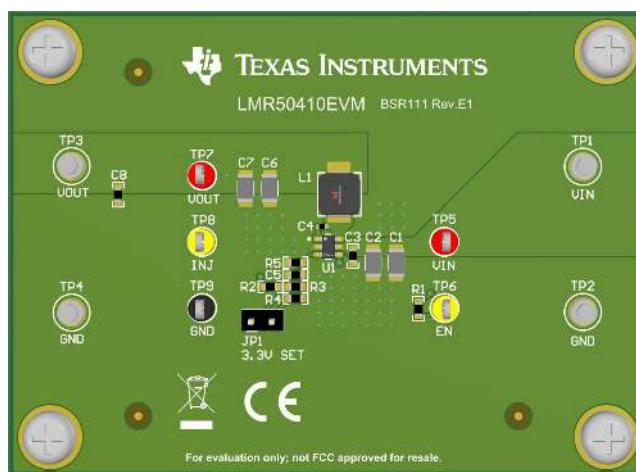
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The Texas Instruments LMR50410EVM evaluation module (EVM) helps designers evaluate the operation and performance of the PLMR50410 wide-input synchronous buck regulator. This document describes the setup and the input/output connections of the EVM. The included are the board layout, schematic, and bill of materials.

## 1 Introduction

The Texas Instruments LMR50410EVM evaluation module (EVM) helps designers evaluate the operation and performance of the PLMR50410 wide-input buck regulator.



**Figure 1. LMR50410EVM Board**

### EVM Features

- 4-V to 36-V input voltage range
- Default 5-V output
- Up to 1-A output current
- 700-kHz switching frequency
- Hiccup mode short current protection
- Internal compensation

The EVM contains one DC/DC converter (see [Table 1](#)).

**Table 1. Device and Package Configurations**

CONVERTER	EVM	DEVICE	PACKAGE
U1	LMR50410EVM	PLMR50410	SOT23-6

## 2 Setup

This section describes the jumpers and connectors on the EVM and how to properly connect, set up, and use the LMR50410EVM.

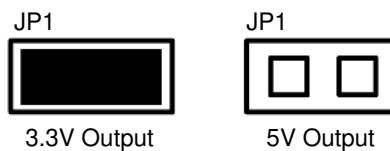
### 2.1 Input/Output Connector Description

**VIN — Terminal TP1** – Power input terminal for the converter. Adjacent to it is the GND reference ground. Use this terminal to attach the EVM to a cable harness.

**VOUT — Terminal TP3** – Regulated output voltage for the converter. Adjacent to it is the GND reference ground.

**GND — Terminal TP2, TP4** – Ground reference for the converter. Use these terminals to attach the EVM to a cable harness.

**VOUT SETTING — Jumper JP1** – Used to set output voltage to 5-V or 3.3-V output



**Figure 2. Vout Jumper Setting**

**Testpoint — TP7, TP8, TP9** – Test points used for loop response measurements

### 2.2 Adjusting the Output Voltage

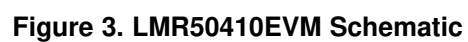
If other outputs need to be configured, leave jumper J1 unconnected and adjust the feedback resistors using [Equation 1](#).

$$V_{OUT} = V_{REF} \times ( 1 + ( R3 / R5 ) )$$

where

- $V_{REF}$  is 1.0 V

(1)



## 4 Board Layout

Figure 4 and Figure 5 show the board layout for the LMR50410EVM. The PCB consists of a 2-layer design. The board size is 57 mm x 79 mm, 1-oz copper planes are applied on both layers.

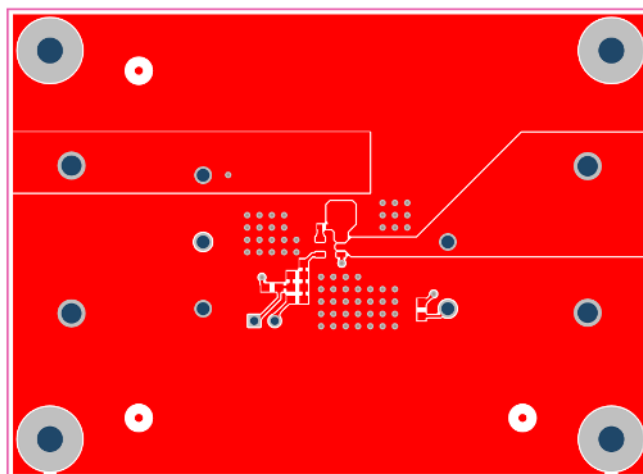


Figure 4. Top Layer

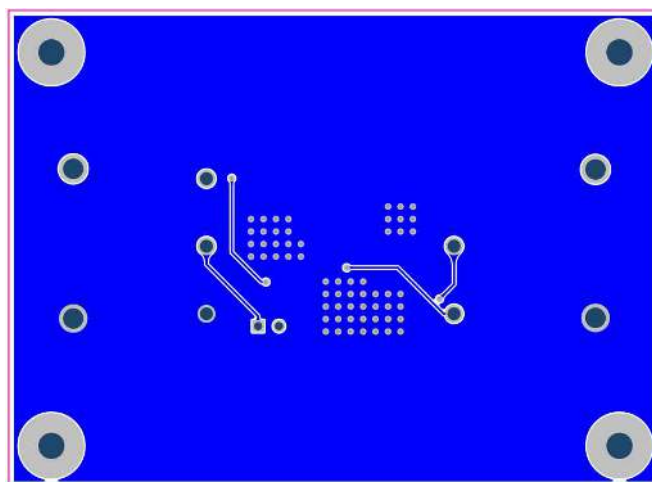


Figure 5. Bottom Layer

## 5 Bill of Materials

**Table 2. LMR50410EVM Bill of Materials**

DESIGNATOR	QUANTITY	VALUE	DESCRIPTION	PACKAGE REFERENCE	PART NUMBER	MANUFACTURER
C1, C2	2	4.7 $\mu$ F	CAP, CERM, 4.7 $\mu$ F, 50 V, $\pm$ 10%, X7R, 1206	1206		
C3	1	0.1 $\mu$ F	CAP, CERM, 0.1 $\mu$ F, 50 V, $\pm$ 10%, X7R, 0603	0603		
C4	1	0.1 $\mu$ F	CAP, CERM, 0.1 $\mu$ F, 25 V, $\pm$ 10%, X7R, 0402	0402		
C5	1	22 pF	CAP, CERM, 22 pF, 50 V, $\pm$ 5%, C0G/NP0, 0603	0603		
C6, C7	2	10 $\mu$ F	CAP, CERM, 10 $\mu$ F, 25 V, $\pm$ 10%, X7R, 1206	1206		
C8	1	0.1 $\mu$ F	CAP, CERM, 0.1 $\mu$ F, 25 V, $\pm$ 10%, X7R, 0603	0603		
JP1	1		Header, 100 mil, 2x1, Tin, TH	Header, 2 PIN, 100mil, Tin		
L1	1		10- $\mu$ H Shielded Molded Inductor 1.8-A 199 m $\Omega$ Max	5020	74437334100	Würth Electronics
R1	1	100 k	RES, 100 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	0603		
R2	1	51	RES, 51, 5%, 0.1 W, AEC-Q200 Grade 0, 0603	0603		
R3	1	115 k	RES, 115 k, 1%, 0.1 W, 0603	0603		
R4	1	154 k	RES, 154 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	0603		
R5	1	28.7 k	RES, 28.7 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	0603		
TP1, TP2, TP3, TP4	4		Terminal, Turret, TH, Double	Keystone1502-2		
TP5, TP7	2		Test Point, Multipurpose, Red, TH	Red Multipurpose Testpoint		
TP6, TP8	2		Test Point, Multipurpose, Yellow, TH	Yellow Multipurpose Testpoint		
TP9	1		Test Point, Multipurpose, Black, TH	Black Multipurpose Testpoint		
U1	1		Synchronous step-down converter	SOT23-6	PLMR50410XDVBR	Texas Instruments

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