MJ15001 (NPN), MJ15002 (PNP)

Complementary Silicon Power Transistors

The MJ15001 and MJ15002 are power transistors designed for high power audio, disk head positioners and other linear applications.

Features

- High Safe Operating Area
- For Low Distortion Complementary Designs
- High DC Current Gain
- These Devices are Pb−Free and are RoHS Compliant*

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector−Emitter Voltage	V_{CEO}	140	Vdc
Collector−Base Voltage	V_{CBO}	140	Vdc
Emitter−Base Voltage	V_{EBO}	5	Vdc
Collector Current − Continuous	I_C	15	Adc
Base Current − Continuous	I_B	5	Adc
Emitter Current − Continuous	I_E	20	Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	200 1.14	W W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to +200	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction−to−Case	$R_{\theta JC}$	0.875	°C/W
Maximum Lead Temperature for Soldering Purposes 1/16″ from Case for ≤ 10 secs	T_L	265	°C

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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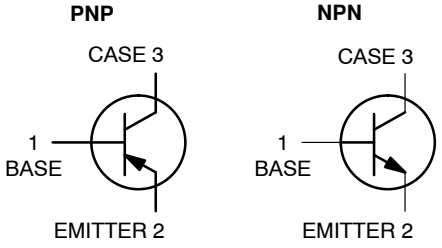
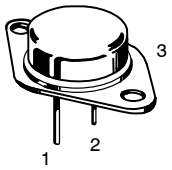
20 AMPERE POWER TRANSISTORS COMPLEMENTARY SILICON 140 VOLTS, 250 WATTS

SCHEMATIC





TO−204AA (TO−3)
CASE 1−07
STYLE 1

MARKING DIAGRAM

MJ1500x	=	Device Code x = 1 or 2
G	=	Pb−Free Package
A	=	Location Code
YY	=	Year
WW	=	Work Week
MEX	=	Country of Orgin

ORDERING INFORMATION

Device	Package	Shipping
MJ15001G	TO−204AA (Pb−Free)	100 Units/Tray
MJ15002G	TO−204AA (Pb−Free)	100 Units/Tray

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector−Emitter Sustaining Voltage (Note 1) (I_C, = 200 mAdc, I_B = 0)	$V_{CEO(sus)}$	140	–	Vdc
Collector Cutoff Current (V_{CE} = 140 Vdc, $V_{BE(off)}$ = 1.5 Vdc) (V_{CE} = 140 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 150°C)	I_{CEX}	 – –	 100 2.0	 μAdc mAdc
Collector Cutoff Current (V_{CE} = 140 Vdc, I_B = 0)	I_{CEO}	–	250	μAdc
Emitter Cutoff Current (V_{EB} = 5 Vdc, I_C = 0)	I_{EBO}	–	100	μAdc
SECOND BREAKDOWN				
Second Breakdown Collector Current with Base Forward Biased (V_{CE} = 40 Vdc, t = 1 s (non−repetitive)) (V_{CE} = 100 Vdc, t = 1 s (non−repetitive))	$I_{S/b}$	 5.0 0.5	 – –	Adc
ON CHARACTERISTICS				
DC Current Gain (I_C = 4 Adc, V_{CE} = 2 Vdc)	h_{FE}	25	150	–
Collector−Emitter Saturation Voltage (I_C = 4 Adc, I_B = 0.4 Adc)	$V_{CE(sat)}$	–	1.0	Vdc
Base−Emitter On Voltage (I_C = 4 Adc, V_{CE} = 2 Vdc)	$V_{BE(on)}$	–	2.0	Vdc
DYNAMIC CHARACTERISTICS				
Current−Gain — Bandwidth Product (I_C = 0.5 Adc, V_{CE} = 10 Vdc, f_{test} = 0.5 MHz)	f_T	2.0	–	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f_{test} = 1 MHz)	C_{ob}	–	1000	pF

1. Pulse Test: Pulse Width = 300 μs, Duty Cycle ≤ 2%.

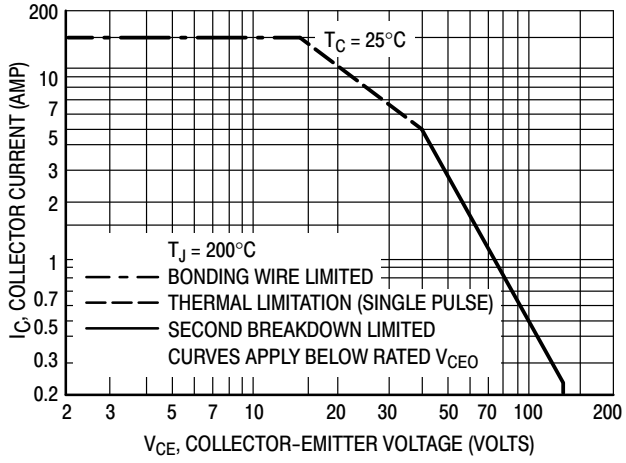


Figure 1. Active−Region Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 1 is based on $T_{J\,(pk)}$ = 200°C; T_C is variable depending on conditions. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

TYPICAL CHARACTERISTICS

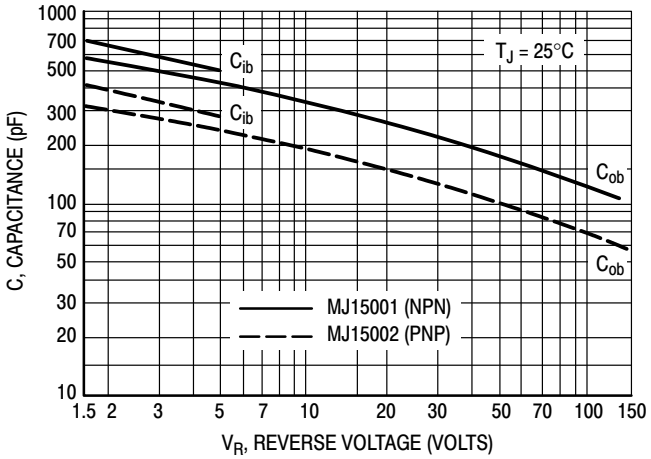


Figure 2. Capacitances

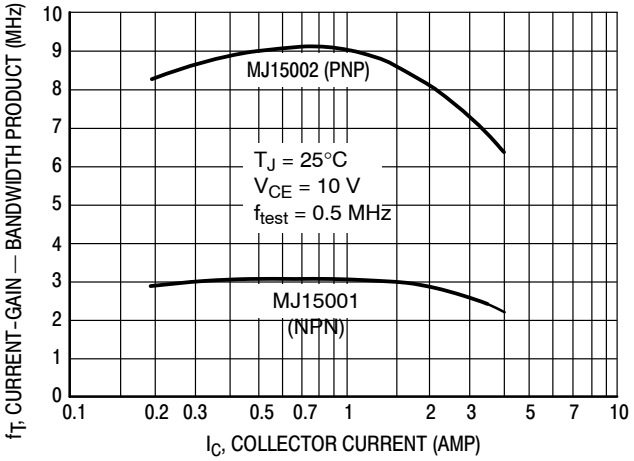


Figure 3. Current−Gain — Bandwidth Product

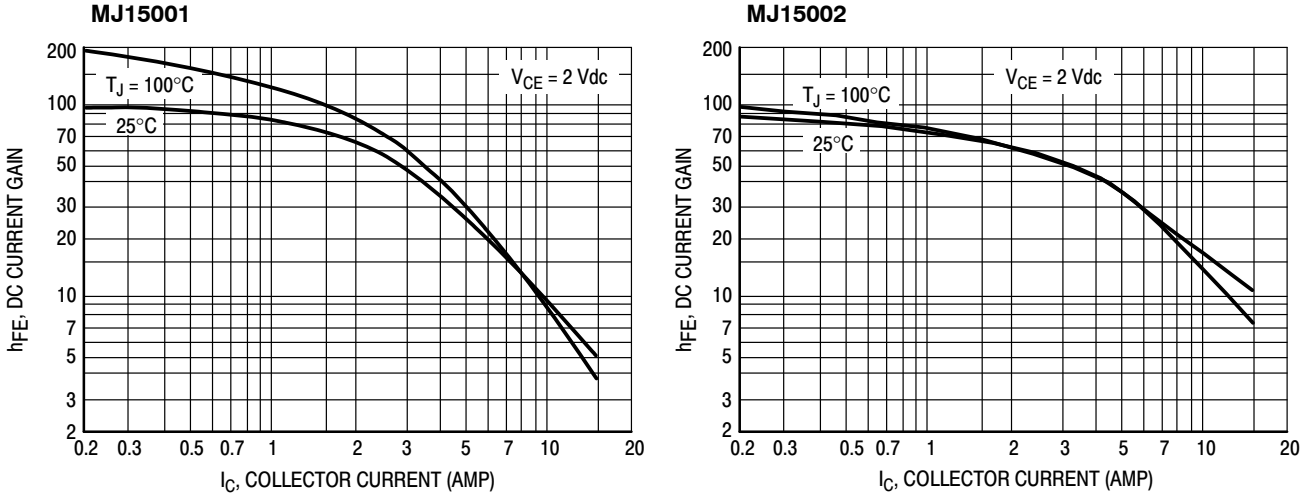


Figure 4. DC Current Gain

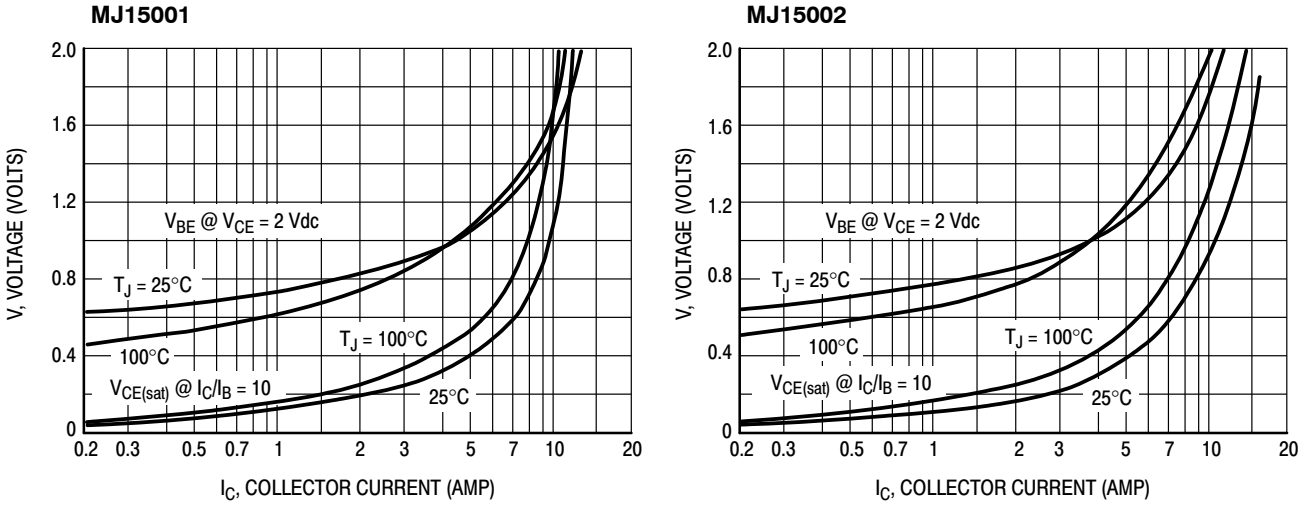
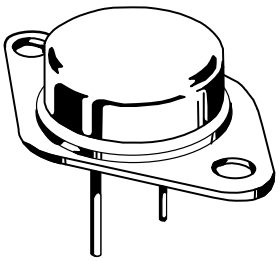


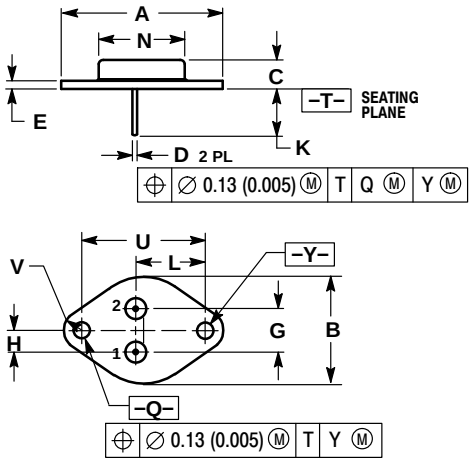
Figure 5. “On” Voltages



SCALE 1:1

TO−204 (TO−3)
CASE 1−07
ISSUE Z

DATE 05/18/1988



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. ALL RULES AND NOTES ASSOCIATED WITH REFERENCED TO−204AA OUTLINE SHALL APPLY.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	1.550 REF		39.37 REF	
B	---	1.050	---	26.67
C	0.250	0.335	6.35	8.51
D	0.038	0.043	0.97	1.09
E	0.055	0.070	1.40	1.77
G	0.430 BSC		10.92 BSC	
H	0.215 BSC		5.46 BSC	
K	0.440	0.480	11.18	12.19
L	0.665 BSC		16.89 BSC	
N	---	0.830	---	21.08
Q	0.151	0.165	3.84	4.19
U	1.187 BSC		30.15 BSC	
V	0.131	0.188	3.33	4.77

STYLE 1:
PIN 1. BASE
2. EMITTER
CASE: COLLECTOR

STYLE 2:
PIN 1. BASE
2. COLLECTOR
CASE: EMITTER

STYLE 3:
PIN 1. GATE
2. SOURCE
CASE: DRAIN

STYLE 4:
PIN 1. GROUND
2. INPUT
CASE: OUTPUT

STYLE 5:
PIN 1. CATHODE
2. EXTERNAL TRIP/DELAY
CASE: ANODE

STYLE 6:
PIN 1. GATE
2. EMITTER
CASE: COLLECTOR

STYLE 7:
PIN 1. ANODE
2. OPEN
CASE: CATHODE

STYLE 8:
PIN 1. CATHODE #1
2. CATHODE #2
CASE: ANODE

STYLE 9:
PIN 1. ANODE #1
2. ANODE #2
CASE: CATHODE

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:
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