IIS3DWB

Datasheet

Ultrawide bandwidth, low-noise, 3-axis digital vibration sensor

LGA-14L
(2.5 x 3.0 x 0.83 mm) typ.

Product status link
IIS3DWB

Product summary	
Order code	IIS3DWBTR
Temp. range [°C]	-40 to +105
Package	LGA-14L
Packing	Tape and reel

Product resources
TN0018 (design and soldering)

Product labels
SUSTAINABLE TECHNOLOGY; LONGEVITY 10 YEARS COMMITMENT

Features

- 3-axis vibration sensor with digital output
- User-selectable full scale: ±2/±4/±8/±16 *g*
- Ultrawide and flat frequency response range: from dc to 6 kHz (±3 dB point)
- Ultralow noise density: down to 75 µg/√Hz in 3-axis mode / 60 µg/√Hz in single-axis mode
- High stability of the sensitivity over temperature and against mechanical shocks
- Extended temperature range from -40 to +105 °C
- Low power: 1.1 mA with all 3 axes delivering full performance
- SPI serial interface
- Low-pass or high-pass filter with selectable cutoff frequency
- Interrupts for wake-up / activity - inactivity / FIFO thresholds
- Embedded FIFO: 3 KB
- Embedded temperature sensor
- Embedded self-test
- Supply voltage: 2.1 V to 3.6 V
- Compact package: LGA 2.5 x 3 x 0.83 mm 14-lead
- ECOPACK and RoHS compliant

Applications

- Vibration monitoring
- Condition monitoring
- Predictive maintenance
- Test and measurements

Description

The IIS3DWB is a system-in-package featuring a 3-axis digital vibration sensor with low noise over an ultrawide and flat frequency range. The wide bandwidth, low noise, very stable and repeatable sensitivity, together with the capability of operating over an extended temperature range (up to +105 °C), make the device particularly suitable for vibration monitoring in industrial applications.

The high performance delivered at low power consumption together with the digital output and the embedded digital features like the FIFO and the interrupts are enabling features for battery-operated industrial wireless sensor nodes.

The IIS3DWB has a selectable full-scale acceleration range of ±2/±4/±8/±16 *g* and is capable of measuring accelerations with a bandwidth up to 6 kHz with an output data rate of 26.7 kHz. A 3 KB first-in, first-out (FIFO) buffer is integrated in the device to avoid any data loss and to limit intervention from the host processor.

The MEMS sensor module family from ST leverages the robust and mature manufacturing processes already used for the production of micromachined accelerometers and gyroscopes to serve automotive, industrial, and consumer markets. The sensing elements are manufactured using ST's proprietary micromachining process, while the embedded IC interfaces are developed using CMOS technology.

The IIS3DWB has a self-test capability, which allows checking the functioning of the sensor in the final application. The IIS3DWB is available in a 14-lead plastic land grid array (LGA) package and is guaranteed to operate over an extended temperature range from -40 °C to +105 °C.

1 Pin description

Figure 1. Pin connections

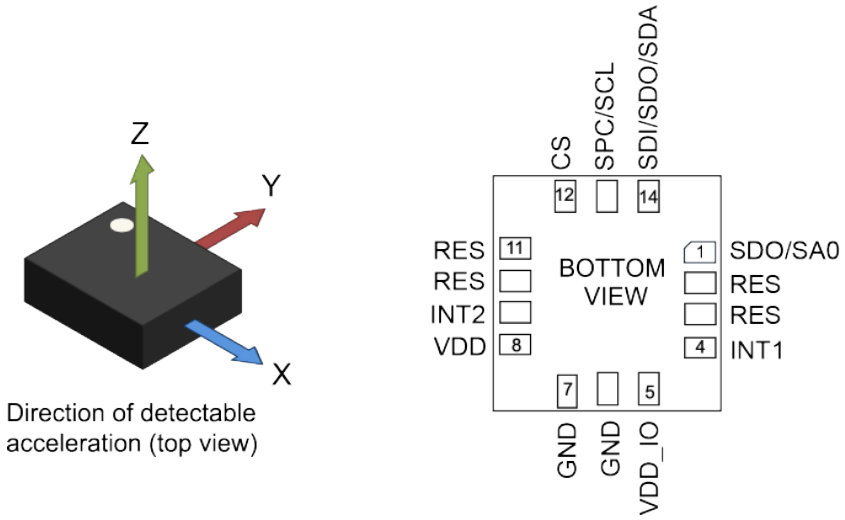


Table 1. Pin desription

Pin #	Name	Function
1	SDO/SA0	SPI 4-wire interface serial data output (SDO) I²C(1) least significant bit of the device address (SA0)
2	RES	Connect to VDD_IO or GND
3	RES	Connect to VDD_IO or GND
4	INT1	Programmable interrupt #1
5	VDD_IO(2)	Power supply for I/O pins
6	GND	Connect to GND
7	GND	Connect to GND
8	VDD(2)	Power supply
9	INT2	Programmable interrupt #2
10	RES	Connect to VDD_IO or leave unconnected(3)
11	RES	Connect to VDD_IO or leave unconnected(3)
12	CS	I²C/SPI(1) mode selection (1: SPI idle mode / I²C(1) communication enabled; 0: SPI communication mode / I²C(1) disabled)
13	SPC/SCL	SPI serial port clock (SPC) I²C serial clock (SCL)
14	SDI/SDO/SDA	SPI serial data input (SDI) 3-wire interface serial data output (SDO) I²C serial data (SDA)

1. *Only the SPI interface supports all the device features and capabilities. Due to limited throughput, the I²C interface can be used only in single-axis mode and it is not recommended.*
2. *Recommended 100 nF filter capacitor.*
3. *Leave pin electrically unconnected and soldered to PCB.*

1.1 Default pin configuration

The IIS3DWB default pin configuration and behavior is given in the table below.

Table 2. Default pin status

Pin#	Name	Function	Default status	Recommended connection
1	SDO/SA0	SPI 4-wire interface serial data output (SDO) I²C least significant bit of the device address (SA0)	Input without pull-up Pull-up is enabled if bit SDO_PU_EN=1 in reg 02h	Application specific
2	RES	Reserved	Input without pull-up	Connect to VDD_IO or GND
3	RES	Reserved	Input without pull-up	Connect to VDD_IO or GND
4	INT1	Programmable interrupt #1	Input with pull-down	Must be set to 0 or left unconnected during device power-up. After device power-up, connection is application specific.
5	VDD_IO	Power supply for I/O pin	-	
6	GND	Ground	-	
7	GND	Ground	-	
8	VDD	Power supply	-	
9	INT2	Programmable interrupt #2	Output forced to GND	Application specific
10	RES	Reserved	Input with pull-up	Connect to VDD_IO or leave pin electrically unconnected and soldered to PCB
11	RES	Reserved	Input with pull-up	Connect to VDD_IO or leave pin electrically unconnected and soldered to PCB
12	CS	I²C/SPI mode selection (1: SPI idle mode / I²C communication enabled; 0: SPI communication mode / I²C disabled)	Input with pull-up Pull-up is disabled if bit I2C_DISABLE=1 in reg 13h	Application specific
13	SPC/SCL	SPI serial port clock (SPC) I²C serial clock (SCL)	Input without pull-up	Application specific
14	SDI/SDO/SDA	SPI serial data input (SDI) 3-wire interface serial data output (SDO) I²C serial data (SDA)	Input without pull-up	Application specific

2 Module specifications

2.1 Mechanical characteristics

@Vdd = 3.0 V, T = +25 °C unless otherwise noted.

The product is factory calibrated at 3.0 V. The operational power supply range is from 2.1 V to 3.6 V.

Table 3. Mechanical characteristics

Symbol	Parameter	Test conditions	Min.(1)	Typ.(2)	Max.(1)	Unit
FS	Linear acceleration measurement range			±2		*g*
				±4		
				±8		
				±16		
So	Linear acceleration sensitivity(3)	@FS = ±2 *g*	-2%	0.061	+2%	mg/LSB
		@FS = ±4 *g*		0.122		
		@FS = ±8 *g*		0.244		
		@FS = ±16 *g*		0.488		
SoDr	Linear acceleration sensitivity change vs. temperature(4)	from -40°C to +105°C delta from T = +25°C		±1	±2	%
TyOff	Linear acceleration zero-*g* level offset accuracy(5)	T = 25 °C	-180	±60	+180	mg
TCOff	Linear acceleration zero-*g* level change vs. temperature(4)			±1		mg/°C
An	Acceleration noise density 3 axes enabled(6)	X-axis		75	110	µg/√Hz
		Y-axis		75	110	
		Z-axis		110	190	
	Acceleration noise density only 1 axis enabled(6)	X-axis		60	90	
		Y-axis		60	90	
		Z-axis		80	130	
BW	Signal bandwidth	±3 dB point	5	6.3		kHz
ODR	Linear acceleration output data rate			26.667		kHz
ODR_ACC	ODR accuracy	Error wrt 26667 Hz @Vdd 3.0 V, T = +25°C		±1	±2	%
ODR_TC	ODR change vs. temperature	Error wrt 26667 Hz @Vdd 3.0 V, from -40°C to +105°C delta from T = +25°C			±0.03	%/°C
F0	Sensor resonant frequency	X-axis		6.9		kHz
		Y-axis		6.9		
		Z-axis		7.0		
Vst	Linear acceleration self-test output change(7)(8)(9)	FS = ±4 *g*	800		3200	mg
Top	Operating temperature range		-40		+105	°C

1. *Min/Max values are based on characterization results at 3σ on a limited number of samples, not tested in production and not guaranteed.*
2. *Typical specifications are not guaranteed.*
3. *Sensitivity values after factory calibration test and trimming.*

4. *Measurements are performed in a uniform temperature setup and they are based on characterization data in a limited number of samples. Not measured in production and not guaranteed.*
5. *Values after factory calibration test and trimming.*
6. *Frequency range 100 Hz - 6.3 kHz. Noise density is independent of the FS selected.*
7. *The sign of the linear acceleration self-test output change is defined by the STx_XL bits in a dedicated register for all axes.*
8. *The linear acceleration self-test output change is defined with the device in stationary condition as the absolute value of: OUTPUT[LSb] (self-test enabled) - OUTPUT[LSb] (self-test disabled). 1LSb =0.122 mg at ±4 g full scale.*
9. *Accelerometer self-test limits are full-scale independent. The self-test should be executed with FS setting ≥4 g.*

2.2 Electrical characteristics

@ Vdd = 3.0 V, T = 25 °C unless otherwise noted.

Table 4. Electrical characteristics

Symbol	Parameter	Test conditions	Min.(1)	Typ. (2)	Max.(1)	Unit
Vdd	Supply voltage		2.1		3.6	V
Vdd_IO	Power supply for I/O		1.62		Vdd + 0.1	V
Idd	Accelerometer current consumption	ODR = 26.667 kHz		1.1	1.3	mA
IddPD	Accelerometer current consumption during power-down			5	16	µA
Ton	Turn-on time(3)			10		ms
V_{IH}(4)	Digital high-level input voltage		0.7 *VDD_IO			V
V_{IL}(4)	Digital low-level input voltage				0.3 *VDD_IO	V
V_{OH}(4)	High-level output voltage	I_{OH} = 4 mA(5)	VDD_IO - 0.2			V
V_{OL}(4)	Low-level output voltage	I_{OL} = 4 mA(5)			0.2	V
Top	Operating temperature range		-40		+105(6)	°C

1. *Min/Max values are based on characterization results at 3σ, not tested in production and not guaranteed.*
2. *Typical specifications are not guaranteed.*
3. *Time to obtain valid data switching from power-down to normal operation.*
4. *Guaranteed by design characterization and not tested in production.*
5. *4 mA is the maximum driving capability, i.e. the maximum DC current that can be sourced/sunk by the digital pad in order to guarantee the correct digital output voltage levels V_{OH} and V_{OL}.*
6. *The IIS3DWB has been qualified with HTOL@125°C for 1000h. In case, in the application, the IIS3DWB has to be operated frequently at high temperature (>50°C), it is recommended, in order to maximize its lifetime, to switch off the sensor, by setting its power supplies to 0 V, when the sensor is not needed to perform measurements. The lower the duty cycle of the IIS3DWB in powered condition, the longer the lifetime of the device which can be extrapolated based on the results of reliability trials.*

2.3 Temperature sensor characteristics

@ Vdd = 3.0 V, T = 25 °C unless otherwise noted.

The product is factory calibrated at 3.0 V.

Symbol	Parameter	Test condition	Min.(1)	Typ.(2)	Max.(1)	Unit
TODR	Temperature refresh rate			104		Hz
Toff	Temperature offset(3)		-15		+15	°C
TSen	Temperature sensitivity			256		LSB/°C
T_delta_Acc	Delta temperature accuracy(4)	from 25°C to 105°C			4	°C
TST	Temperature stabilization time(5)			10		ms
T_ADC_res	Temperature ADC resolution			16		bit
Top	Operating temperature range		-40		+105	°C

1. *Min/Max values are based on characterization results at 3σ on a limited number of samples, not tested in production and not guaranteed.*
2. *Typical specifications are not guaranteed.*
3. *The output of the temperature sensor is 0 LSB (typ.) at 25 °C. Absolute temperature accuracy can be improved (reducing the effect of temperature offset) by performing OPC (one-point calibration) at room temperature (25 °C).*
4. *Applicable if temperature offset is removed with OPC (one-point calibration) at room temperature (25 °C).*
5. *Time from power ON to valid output data.*

2.4 Communication interface characteristics

2.4.1 SPI - serial peripheral interface

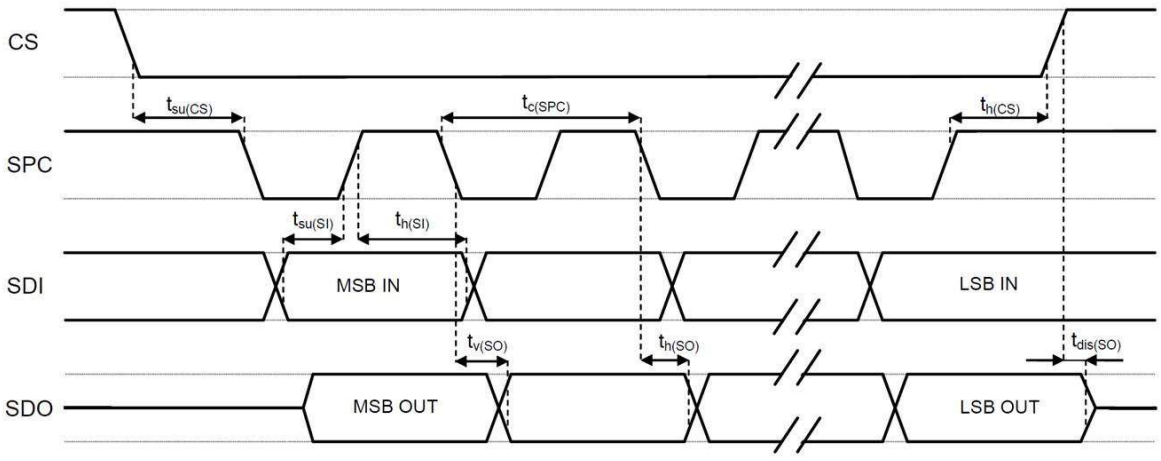
Subject to general operating conditions for Vdd and Top.

Table 5. SPI slave timing values

Symbol	Parameter	Value(1)		Unit
		Min	Max	
$t_{c(SPC)}$	SPI clock cycle	100		ns
$f_{c(SPC)}$	SPI clock frequency		10	MHz
$t_{su(CS)}$	CS setup time	5		ns
$t_{h(CS)}$	CS hold time	20		
$t_{su(SI)}$	SDI input setup time	5		
$t_{h(SI)}$	SDI input hold time	15		
$t_{v(SO)}$	SDO valid output time		50	
$t_{h(SO)}$	SDO output hold time	5		
$t_{dis(SO)}$	SDO output disable time		50	

1. *Values are evaluated at 10 MHz clock frequency for SPI with both 4 and 3 wires, based on characterization results, not tested in production.*

Figure 2. SPI slave timing diagram



Note: Measurement points are done at 0.3·Vdd_IO and 0.7·Vdd_IO for both input and output ports.

2.5 Absolute maximum ratings

Stresses above those listed as “absolute maximum ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device under these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 6. Absolute maximum ratings

Symbol	Ratings	Maximum value	Unit
Vdd	Supply voltage	-0.3 to 4.8	V
T_{STG}	Storage temperature range	-40 to +125	°C
Sg	Acceleration *g* for 0.2 ms	10,000	*g*
ESD	Electrostatic discharge protection (HBM)	2	kV
Vin	Input voltage on any control pin (including CS, SCL/SPC, SDA/SDI/SDO, SDO/SA0)	-0.3 to Vdd_IO +0.3	V

Note: Supply voltage on any pin should never exceed 4.8 V.

This device is sensitive to mechanical shock, improper handling can cause permanent damage to the part.

This device is sensitive to electrostatic discharge (ESD), improper handling can cause permanent damage to the part.

2.6 Terminology

2.6.1 Sensitivity

Linear acceleration sensitivity can be determined, for example, by applying 1 *g* acceleration to the device. Because the sensor can measure DC accelerations, this can be done easily by pointing the selected axis towards the ground, noting the output value, rotating the sensor 180 degrees (pointing towards the sky), and noting the output value again. By doing so, ±1 *g* acceleration is applied to the sensor. Subtracting the larger output value from the smaller one, and dividing the result by 2, leads to the actual sensitivity of the sensor. This value changes very little over temperature and over time. The sensitivity tolerance describes the range of sensitivities of a large number of sensors (see Table 3).

2.6.2 Zero-*g* level

Linear acceleration zero-*g* level offset (TyOff) describes the deviation of an actual output signal from the ideal output signal if no acceleration is present. A sensor in a steady state on a horizontal surface measures 0 *g* on both the X-axis and Y-axis, whereas the Z-axis measures 1 *g*. Ideally, the output is in the middle of the dynamic range of the sensor (content of OUT registers 00h, data expressed as two's complement number). A deviation from the ideal value in this case is called zero-*g* offset.

Offset is to some extent a result of stress to the MEMS sensor and therefore the offset can slightly change after mounting the sensor onto a printed circuit board or exposing it to extensive mechanical stress. Offset changes little over temperature, see "Linear acceleration zero-*g* level change vs. temperature" in Table 3. The zero-*g* level tolerance (TyOff) describes the standard deviation of the range of zero-*g* levels of a group of sensors.

3 Digital interface

3.1 SPI interface

The registers embedded inside the IIS3DWB may be accessed through the SPI serial interface that can be SW configured to operate either in 3-wire or 4-wire interface mode. The device is compatible with SPI modes 0 and 3.

The SPI interface is mapped to the same pins as an I²C interface. However, since it is only with the throughput of the SPI interface that all the device features and capabilities are supported, the I²C interface is not described. To select/exploit the I²C interface, the CS line must be tied high (that is, connected to Vdd_IO).

Table 7. Serial interface pin description

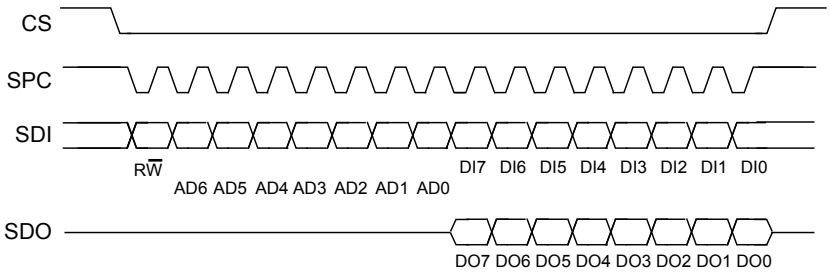
Pin name	Pin description
CS	Enable SPI I²C(1)/SPI mode selection (1: SPI idle mode / I²C(1) communication enabled; 0: SPI communication mode / I²C(1) disabled)
SPC/SCL	SPI serial port clock (SPC) I²C(1) serial clock (SCL)
SDI/SDO/SDA	SPI serial data input (SDI) 3-wire interface serial data output (SDO) I²C(1) serial data (SDA)
SDO/SA0	SPI 4-wire interface serial data output (SDO) I²C(1) least significant bit of the device address (SA0)

1. *Only the SPI interface supports all the device features and capabilities. Due to limited throughput, the I²C interface can be used only in single-axis mode and it is not recommended.*

3.2 SPI bus interface

The IIS3DWB SPI is a bus slave. The SPI allows writing to and reading from the registers of the device.
The serial interface communicates to the application using four wires: **CS**, **SPC**, **SDI**, and **SDO**.

Figure 3. Read and write protocol (in mode 3)



CS enables the serial port and it is controlled by the SPI master. It goes low at the start of the transmission and goes back high at the end. **SPC** is the serial port clock and it is controlled by the SPI master. It is stopped high when **CS** is high (no transmission). **SDI** and **SDO** are, respectively, the serial port data input and output. Those lines are driven at the falling edge of **SPC** and should be captured at the rising edge of **SPC**.

Both the read register and write register commands are completed in 16 clock pulses or in multiples of 8 in case of multiple read/write bytes. Bit duration is the time between two falling edges of **SPC**. The first bit (bit 0) starts at the first falling edge of **SPC** after the falling edge of CS while the last bit (bit 15, bit 23, ...) starts at the last falling edge of **SPC** just before the rising edge of **CS**.

bit 0: $R\overline{W}$ bit. When 0, the data DI(7:0) is written into the device. When 1, the data DO(7:0) from the device is read. In latter case, the chip drives **SDO** at the start of bit 8.

bit 1-7: address AD(6:0). This is the address field of the indexed register.

bit 8-15: data DI(7:0) (write mode). This is the data that is written into the device (MSb first).

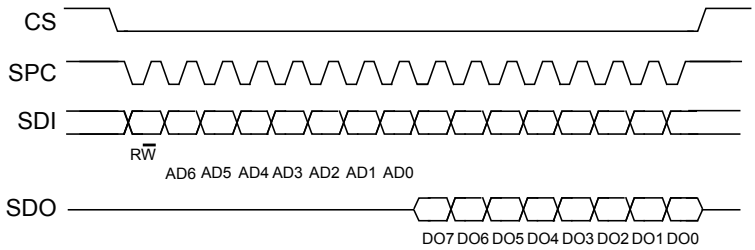
bit 8-15: data DO(7:0) (read mode). This is the data that is read from the device (MSb first).

In multiple read/write commands further blocks of 8 clock periods are added. When the CTRL3_C (12h) (IF_INC) bit is 0, the address used to read/write data remains the same for every block. When the CTRL3_C (12h) (IF_INC) bit is 1, the address used to read/write data is increased at every block.

The function and the behavior of **SDI** and **SDO** remain unchanged.

3.2.1 SPI read

Figure 4. **SPI read protocol (in mode 3)**



The SPI read command is performed with 16 clock pulses. A multiple byte read command is performed by adding blocks of 8 clock pulses to the previous one.

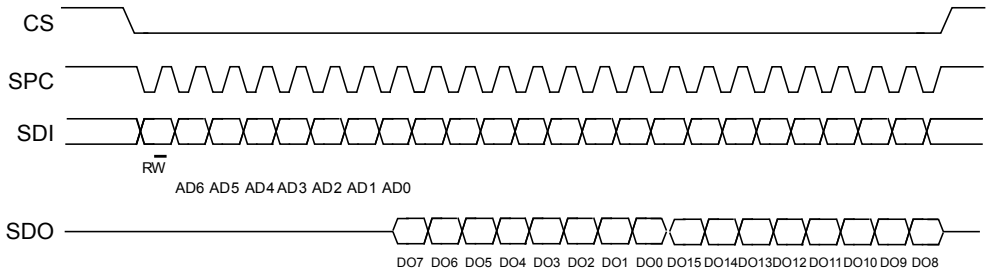
bit 0: READ bit. The value is 1.

bit 1-7: address AD(6:0). This is the address field of the indexed register.

bit 8-15: data DO(7:0) (read mode). This is the data that is read from the device (MSb first).

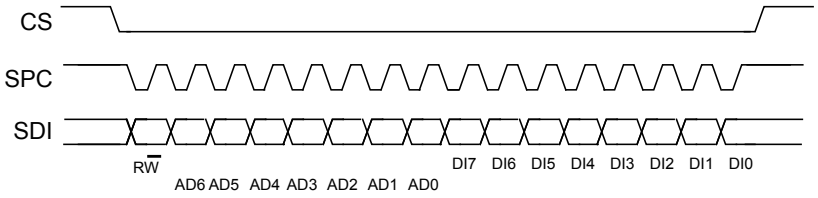
bit 16-...: data DO(...-8). Further data in multiple byte reads.

Figure 5. **Multiple byte SPI read protocol (2-byte example) (in mode 3)**



3.2.2 SPI write

Figure 6. **SPI write protocol (in mode 3)**



The SPI write command is performed with 16 clock pulses. A multiple byte write command is performed by adding blocks of 8 clock pulses to the previous one.

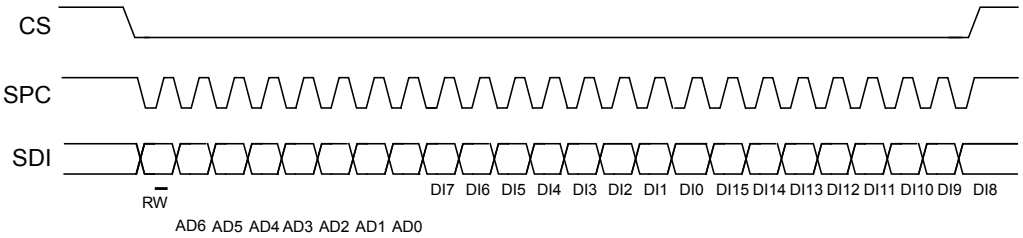
bit 0: WRITE bit. The value is 0.

bit 1-7: address AD(6:0). This is the address field of the indexed register.

bit 8-15: data DI(7:0) (write mode). This is the data that is written inside the device (MSb first).

bit 16-... : data DI(...-8). Further data in multiple byte writes.

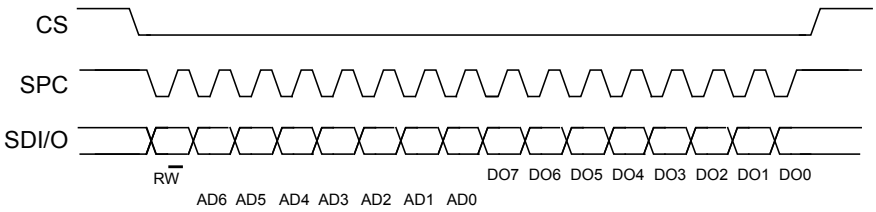
Figure 7. **Multiple byte SPI write protocol (2-byte example) (in mode 3)**



3.2.3 SPI read in 3-wire mode

3-wire mode is entered by setting the CTRL3_C (12h) (SIM) bit equal to 1 (SPI serial interface mode selection).

Figure 8. **SPI read protocol in 3-wire mode (in mode 3)**



The SPI read command is performed with 16 clock pulses:

bit 0: READ bit. The value is 1.

bit 1-7: address AD(6:0). This is the address field of the indexed register.

bit 8-15: data DO(7:0) (read mode). This is the data that is read from the device (MSb first).

A multiple read command is also available in 3-wire mode.

4 Functionality

4.1 Operating modes

The IIS3DWB has two operating modes:

- 3-axis mode: all three axes (X, Y, Z) are simultaneously active and acceleration data can be read from the sensor concurrently for the 3-axis (using registers OUTX_L_A (28h) and OUTX_H_A (29h); OUTY_L_A (2Ah) and OUTY_H_A (2Bh); OUTZ_L_A (2Ch) and OUTZ_H_A (2Dh) or the FIFO registers: FIFO_DATA_OUT (79h – 7Eh).
- Single-axis mode: only one axis is active. The active axis, among X or Y or Z, can be selected when the device is in power-down mode. Acceleration data can be read from the registers associated with the active axis or from the corresponding registers of the FIFO.

In single-axis mode, while the power consumption of IIS3DWB remains the same as 3-axis mode, the resolution (noise density) of the active axis significantly improves.

To change the configuration of the active axis, the device should be in power-down mode. An example of the procedure that can be applied is:

Set the device in power-down mode: CTRL1_XL (10h) XL_EN[2:0] = 000b

Enable the axis: CTRL6_C (15h) XL_AXIS_SEL[1:0] = xxb (00 = 3 axes; 01 = X-axis; 10 = Y-axis; 11 = Z-axis)

Enable the device: CTRL1_XL (10h) XL_EN[2:0] = 101b

4.2 Block diagrams

The IIS3DWB architecture is composed of the following functional blocks:

- MEMS mechanical element
- ADC
- Low-pass digital filter (LPF1)
- Composite filter

Figure 9. Accelerometer architecture

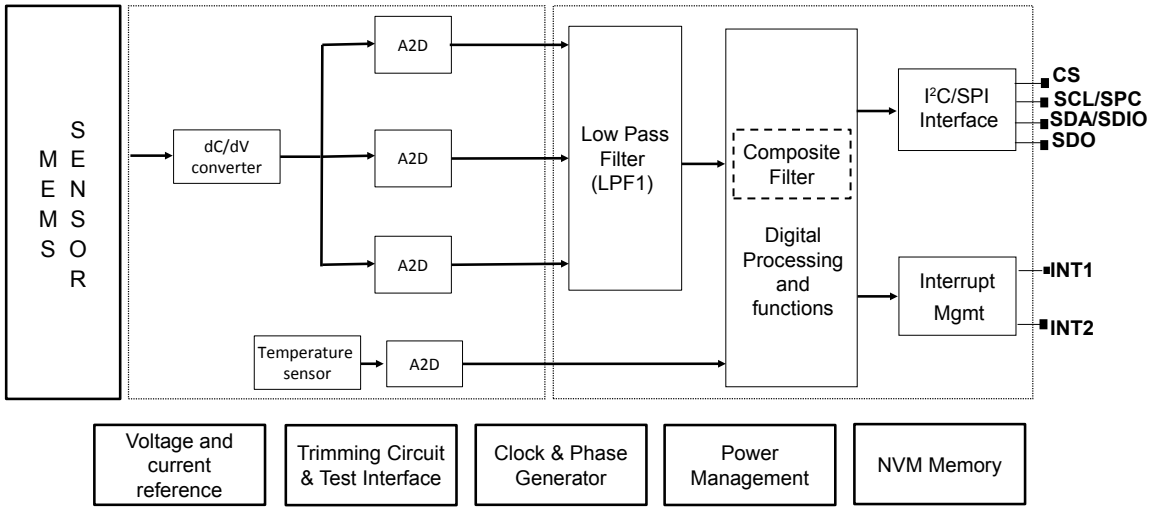
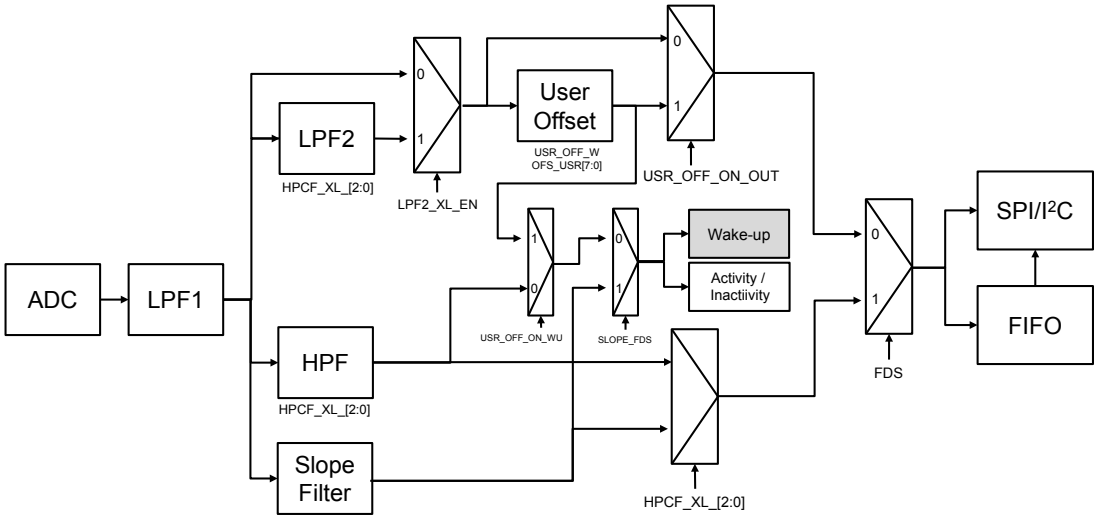


Figure 10. Accelerometer composite filter



4.3 FIFO

The presence of a FIFO allows consistent power saving for the system since the host processor does not need to continuously poll data from the sensor, but it can wake up only when needed and burst the significant data out from the FIFO.

The IIS3DWB embeds 3 KB of data in FIFO to store the following data:

- Accelerometer
- Timestamp
- Temperature

Writing data in the FIFO is triggered by the accelerometer data-ready signal.

It is possible to select decimation for timestamp batching in FIFO with a factor of 1, 8, or 32 compared to the accelerometer BDR (batch data rate).

The reconstruction of a FIFO stream is a simple task thanks to the FIFO_DATA_OUT_TAG byte that allows recognizing the meaning of a word in FIFO.

FIFO allows correct reconstruction of the timestamp information for each sensor stored in FIFO. If a change in the BDR configuration is performed, the application can correctly reconstruct the timestamp and know exactly when the change was applied without disabling FIFO batching. FIFO stores information of the new configuration and timestamp in which the change was applied in the device.

The programmable FIFO watermark threshold can be set in FIFO_CTRL1 (07h) and FIFO_CTRL2 (08h) using the WTM[8:0] bits. To monitor the FIFO status, dedicated registers (FIFO_STATUS1 (3Ah), FIFO_STATUS2 (3Bh)) can be read to detect FIFO overrun events, FIFO full status, FIFO empty status, FIFO watermark status, and the number of unread samples stored in the FIFO. To generate dedicated interrupts on the INT1 and INT2 pins of these status events, the configuration can be set in INT1_CTRL (0Dh) and INT2_CTRL (0Eh).

The FIFO buffer can be configured according to six different modes:

- Bypass mode
- FIFO mode
- Continuous mode
- Continuous-to-FIFO mode
- Bypass-to-continuous mode
- Bypass-to-FIFO mode

Each mode is selected by the FIFO_MODE_[2:0] bits in the FIFO_CTRL4 (0Ah) register.

4.3.1 Bypass mode

In bypass mode (FIFO_CTRL4 (0Ah)(FIFO_MODE_[2:0] = 000), the FIFO is not operational and it remains empty. Bypass mode is also used to reset the FIFO when in FIFO mode.

4.3.2 FIFO mode

In FIFO mode (FIFO_CTRL4 (0Ah)(FIFO_MODE_[2:0] = 001) data from the output channels are stored in the FIFO until it is full.

To reset FIFO content, bypass mode should be selected by writing FIFO_CTRL4 (0Ah)(FIFO_MODE_[2:0]) to 000. After this reset command, it is possible to restart FIFO mode by writing FIFO_CTRL4 (0Ah) (FIFO_MODE_[2:0]) to 001.

The FIFO buffer memorizes up to 3 KB of data but the depth of the FIFO can be resized by setting the WTM[8:0] bits in FIFO_CTRL1 (07h) and FIFO_CTRL2 (08h). If the STOP_ON_WTM bit in FIFO_CTRL2 (08h) is set to 1, FIFO depth is limited up to the WTM[8:0] bits in FIFO_CTRL1 (07h) and FIFO_CTRL2 (08h).

4.3.3 Continuous mode

Continuous mode (FIFO_CTRL4 (0Ah)(FIFO_MODE_[2:0] = 110) provides a continuous FIFO update: as new data arrives, the older data is discarded.

A FIFO threshold flag FIFO_STATUS2 (3Bh)(FIFO_WTM_IA) is asserted when the number of unread samples in FIFO is greater than or equal to FIFO_CTRL1 (07h) and FIFO_CTRL2 (08h)(WTM[8:0]).

It is possible to route the FIFO_WTM_IA flag to the INT1 pin by writing in register INT1_CTRL (0Dh) (INT1_FIFO_TH) = 1 or to the INT2 pin by writing in register INT2_CTRL (0Eh)(INT2_FIFO_TH) = 1.

A full-flag interrupt can be enabled, INT1_CTRL (0Dh)(INT1_FIFO_FULL) = 1 or INT2_CTRL (0Eh) (INT2_FIFO_FULL) = 1, in order to indicate FIFO saturation and eventually read its content all at once.

If an overrun occurs, at least one of the oldest samples in FIFO has been overwritten and the FIFO_OVR_IA flag in FIFO_STATUS2 (3Bh) is asserted.

In order to empty the FIFO before it is full, it is also possible to pull from FIFO the number of unread samples available in FIFO_STATUS1 (3Ah) and FIFO_STATUS2 (3Bh)(DIFF_FIFO_[9:0]).

4.3.4 Continuous-to-FIFO mode

In continuous-to-FIFO mode (FIFO_CTRL4 (0Ah)(FIFO_MODE_[2:0] = 011), FIFO behavior changes according to the trigger event (wake-up) detected.

When the selected trigger bit is equal to 1, FIFO operates in FIFO mode.

When the selected trigger bit is equal to 0, FIFO operates in continuous mode.

4.3.5 Bypass-to-continuous mode

In bypass-to-continuous mode (FIFO_CTRL4 (0Ah)(FIFO_MODE_[2:0] = 100), data measurement storage inside FIFO operates in continuous mode when selected triggers are equal to 1, otherwise FIFO content is reset (bypass mode).

FIFO behavior changes according to the trigger event detected (wake-up).

4.3.6 Bypass-to-FIFO mode

In bypass-to-FIFO mode FIFO_CTRL4 (0Ah)(FIFO_MODE_[2:0] = 111), data measurement storage inside FIFO operates in FIFO mode when selected triggers (wake-up) are equal to 1, otherwise FIFO content is reset (bypass mode)

4.3.7 FIFO reading procedure

The data stored in FIFO are accessible from dedicated registers and each FIFO word is composed of 7 bytes: one tag byte (FIFO_DATA_OUT_TAG (78h), in order to identify the sensor, and 6 bytes of fixed data (FIFO_DATA_OUT registers from (79h) to (7Eh)).

The DIFF_FIFO_[9:0] field in the FIFO_STATUS1 (3Ah) and FIFO_STATUS2 (3Bh) registers contains the number of words (1 byte TAG + 6 bytes DATA) collected in FIFO.

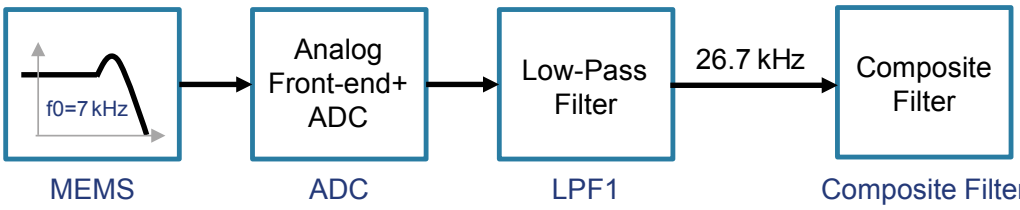
In addition, it is possible to configure a counter of the batch events of the sensor. The flag COUNTER_BDR_IA in FIFO_STATUS2 (3Bh) alerts that the counter has reached a selectable threshold (CNT_BDR_TH_[10:0] field in COUNTER_BDR_REG1 (0Bh) and COUNTER_BDR_REG2 (0Ch)). This allows triggering the reading of FIFO with the desired latency of one single sensor. The sensor is selectable using the TRIG_COUNTER_BDR bit in COUNTER_BDR_REG1 (0Bh). As for the other FIFO status events, the flag COUNTER_BDR_IA can be routed on the INT1 or INT2 pins by asserting the corresponding bits (INT1_CNT_BDR of INT1_CTRL (0Dh) and INT2_CNT_BDR of INT2_CTRL (0Eh)).

5 Frequency response

The IIS3DWB has been specifically designed to provide a wide bandwidth with very flat frequency response in the pass band and a very high attenuation in the stop band so to virtually eliminate any frequency aliasing.

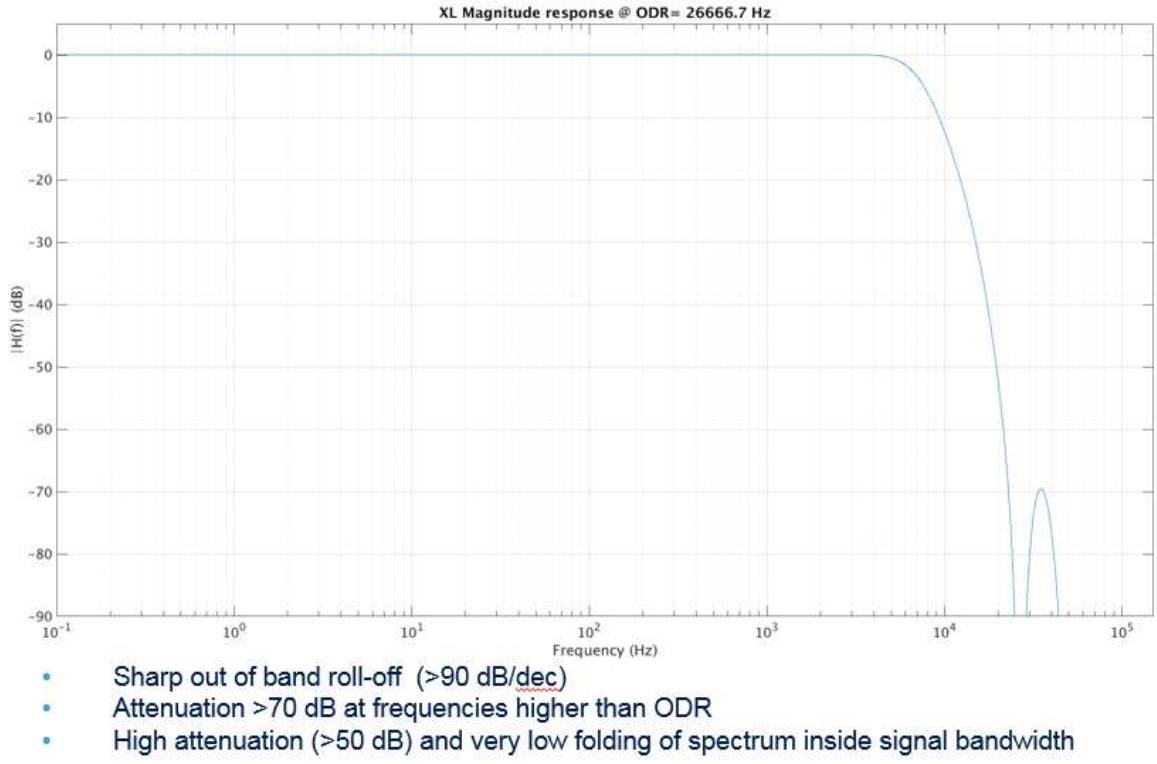
The following figure illustrates the filtering chain and its components.

Figure 11. Filtering chain



The output of the ADC converter is filtered with a digital low-pass filter to ensure the intended sensor's frequency response. The frequency response at the output of the LPF1 filter is indicated in the following figure.

Figure 12. Frequency response at the output of LPF1 filter



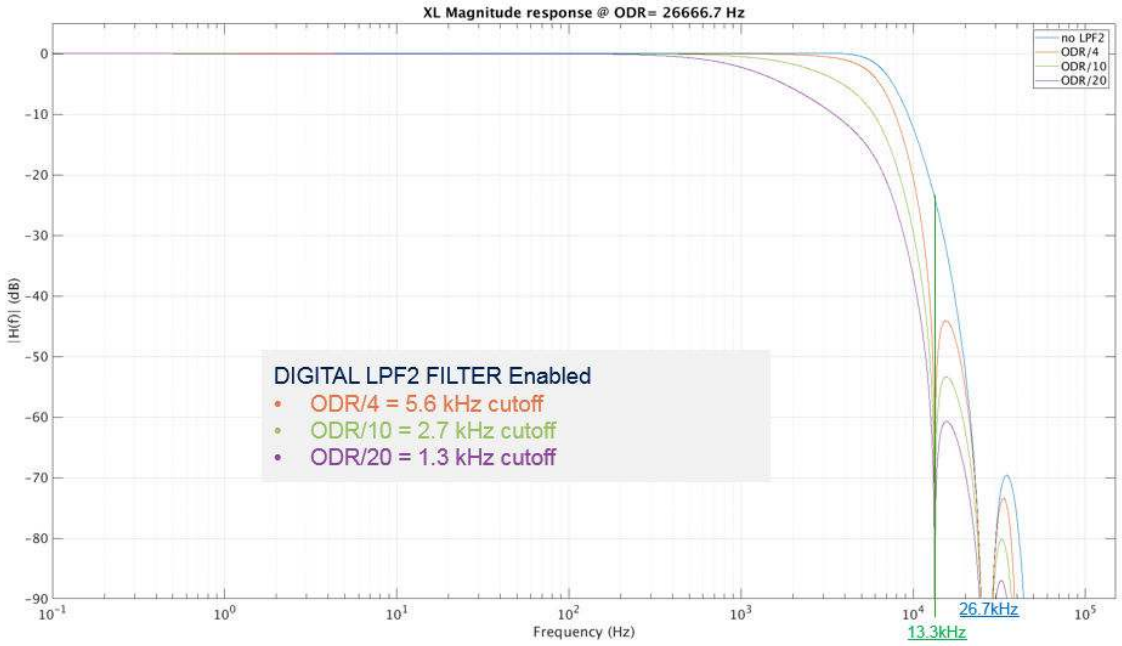
Note: Frequency response determined by CAD simulation – at the output of LPF1.

After the LPF1 filter, it is possible to enable another level of digital filtering through the digital composite filter (refer to Figure 10. Accelerometer composite filter).

The digital composite filter could be:

- High-pass filter
- Low-pass filter

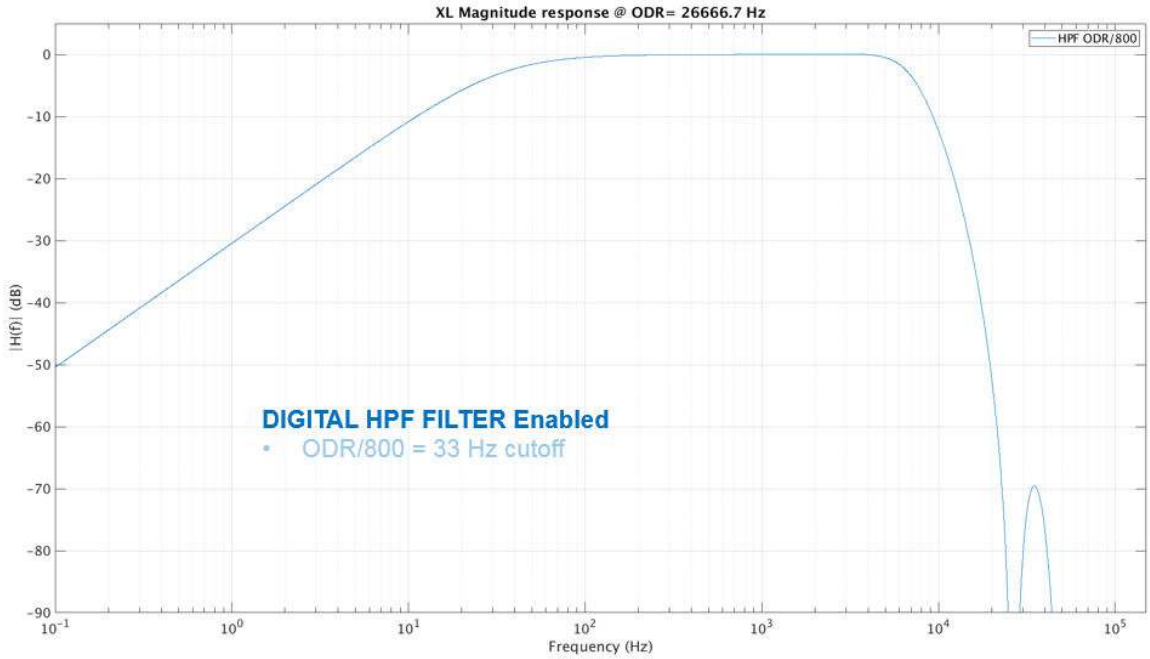
Figure 13. Frequency response with LPF2 enabled



Frequency response at the output of Composite Filter when it is configured as Low-Pass Filter (LPF2)

Note: Frequency response determined by CAD simulation.

Figure 14. Frequency response with HPF enabled



Frequency response at the output of Composite Filter when it is configured as High-Pass Filter (HPF)

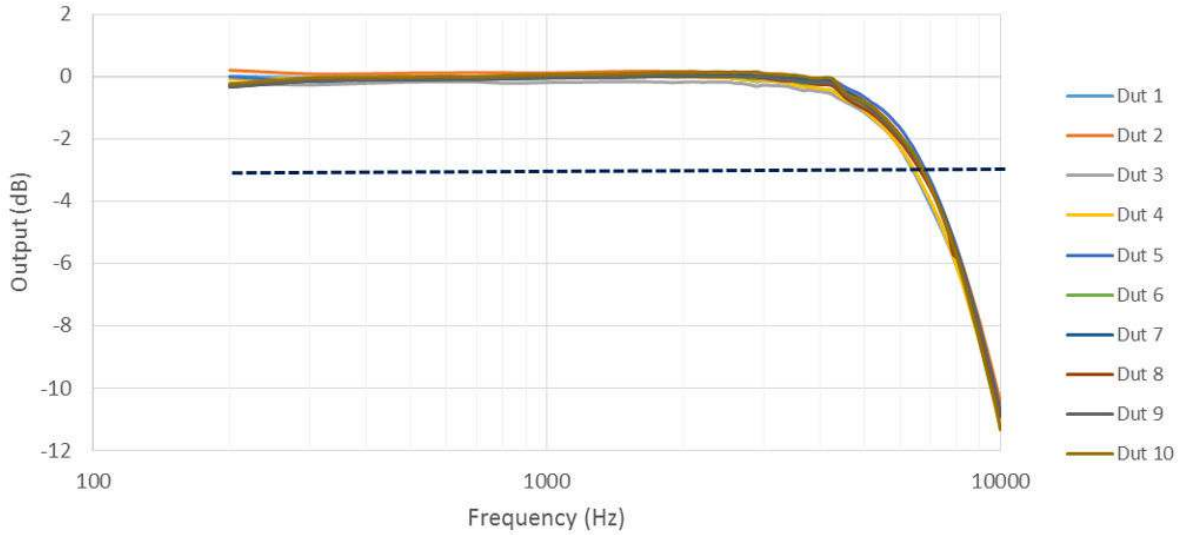
Note: Frequency response determined by CAD simulation.

6 Typical performance characteristics

6.1 Frequency response measurements

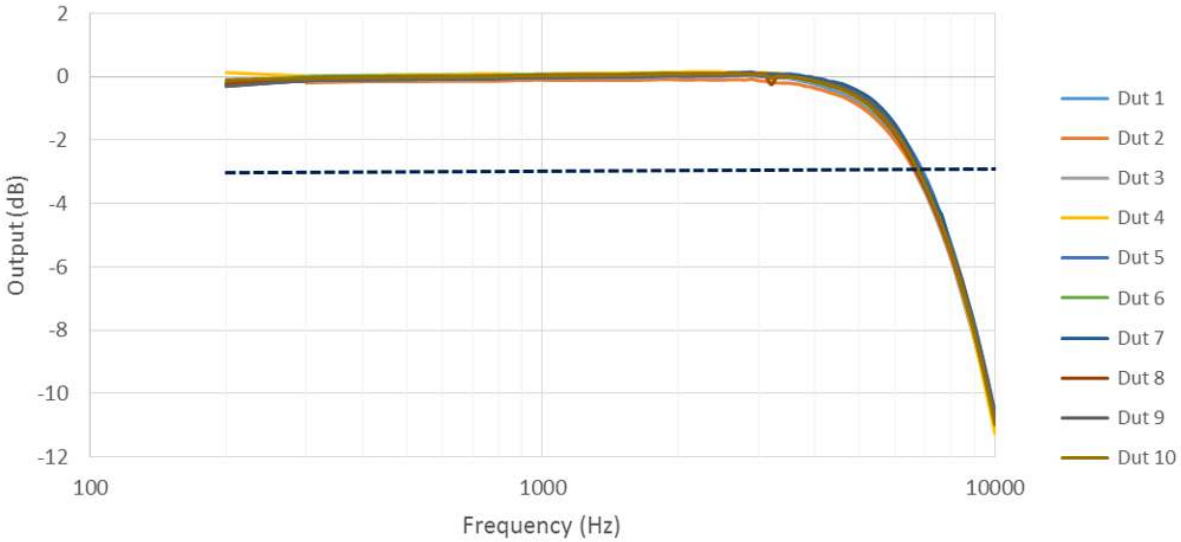
The frequency response of the IIS3DWB, measured on a mechanical shaker, is indicated in the following figures. Measurements have been performed with the IIS3DWB configured with the digital composite filter bypassed.

Figure 15. Frequency response - X-axis



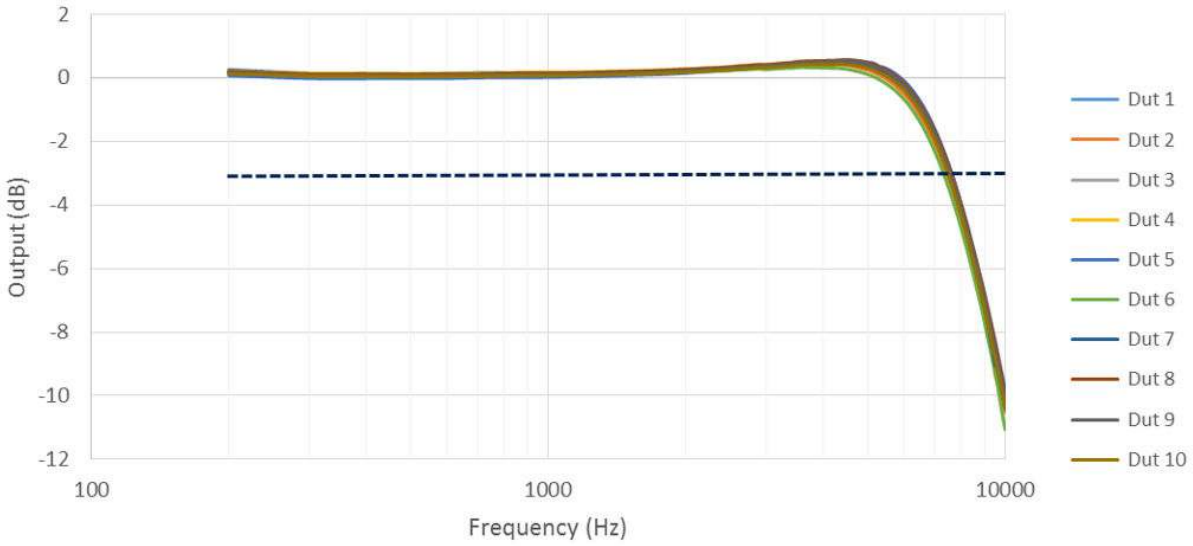
Note: Characterization data on 10 parts. Not measured in production and not guaranteed.

Figure 16. Frequency response - Y-axis



Note: Characterization data on 10 parts. Not measured in production and not guaranteed.

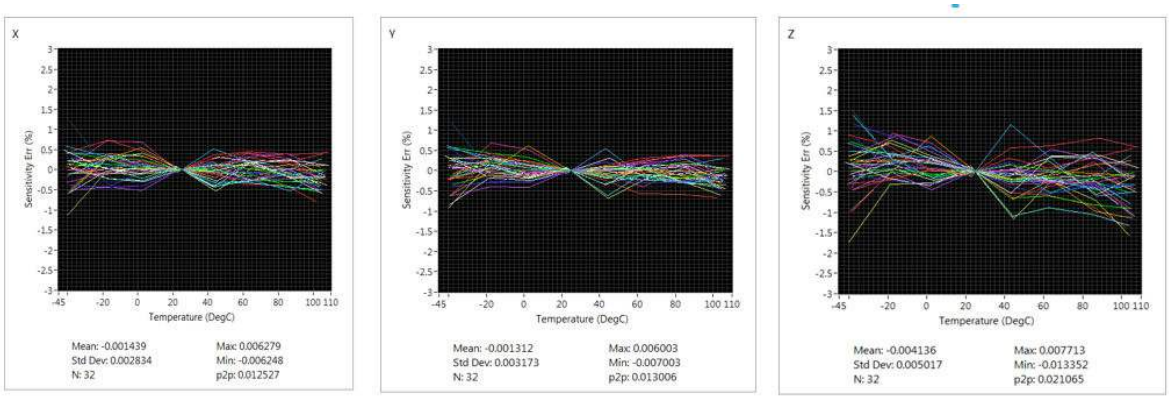
Figure 17. **Frequency response - Z-axis**



Note: Characterization data on 10 parts. Not measured in production and not guaranteed.

6.2 Sensitivity change versus temperature

Figure 18. Sensitivity change versus temperature

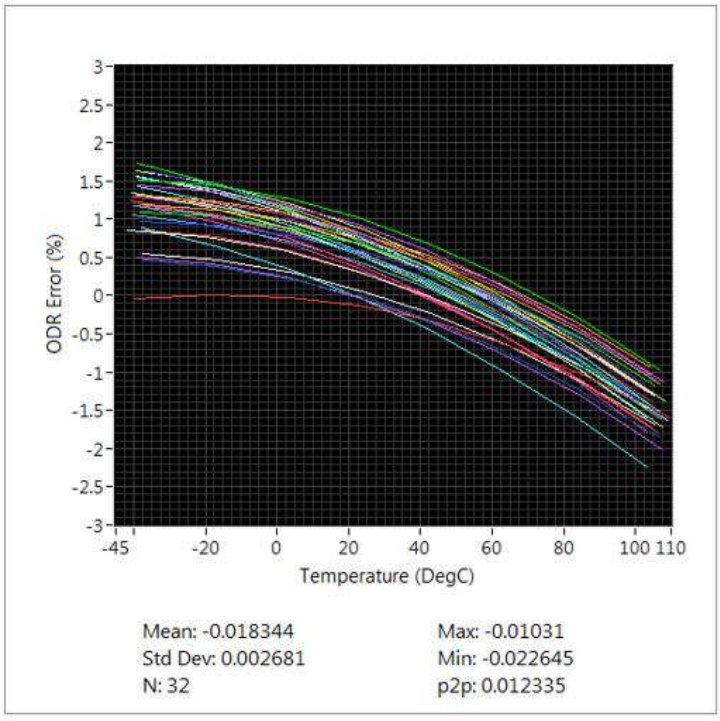


Measured at Vdd 3.0 Volt

Note: Characterization data. Not measured in production and not guaranteed.

6.3 ODR change versus temperature

Figure 19. ODR change versus temperature



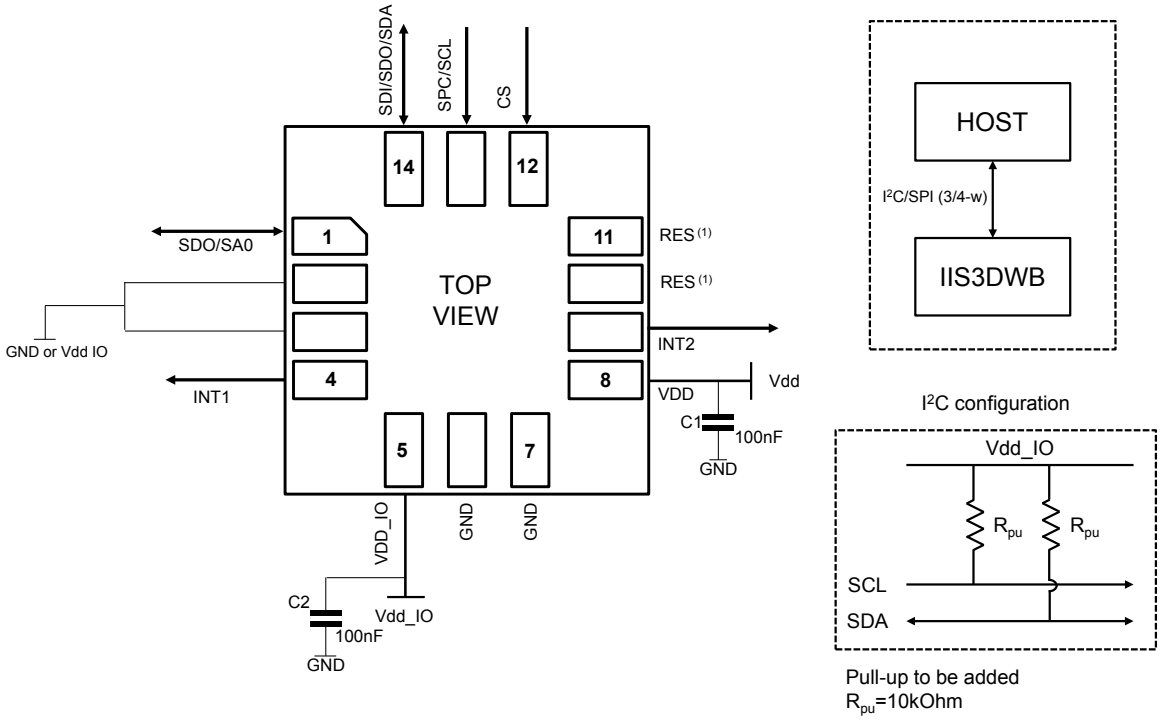
Error evaluted with reference to 26667Hz @ Vdd 3.0 Volt

Note: Characterization data. Not measured in production and not guaranteed.

7 Application hints

7.1 IIS3DWB electrical connections

Figure 20. **IIS3DWB electrical connections**



The device core is supplied through the Vdd line while the I/O pads are supplied through the Vdd_IO line. Power supply decoupling capacitors (C1, C2 = 100 nF ceramic) should be placed as near as possible to the supply pin of the device (common design practice).

The functionality of the device and the measured acceleration data are selectable and accessible through the I²C or SPI interfaces. When using the I²C protocol, CS must be tied high. Every time the CS line is set to low level, the I²C bus is internally reset.

All the functions, the threshold, and the timing of the two interrupt pins can be completely programmed by the user through the I²C/SPI interface.

Note: Only the SPI interface supports all the device features and capabilities. The I²C interface can be used only in single-axis mode and it is not recommended.

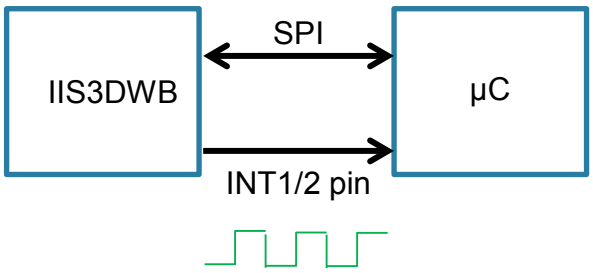
7.2 Measuring the actual ODR

For applications requiring higher ODR accuracy, it is possible to configure the device to generate an interrupt signal on the INT1/2 pin each time new data is generated. By using an accurate timer (that is, with a microcontroller) it is possible to measure the time interval between consecutive interrupt signals obtaining a very accurate value of the actual ODR of the device.

In order to enable the generation of the data_ready interrupt on the INT1 or INT2 pin:

- The dataready_pulsed bit of the COUNTER_BDR_REG1 (0Bh) register should be set to 1 (optional).
- The INTx_ DRDY_XL bit of the INT1_CTRL (0Dh) / INT2_CTRL (0Eh) register has to be set to 1.

Figure 21. Accurately measuring ODR



8 Register mapping

The table given below provides a list of the 8/16-bit registers embedded in the device and the corresponding addresses.

Table 8. Register address map

Name	Type	Register address		Default	Comment
		Hex	Binary		
RESERVED	-	01			
PIN_CTRL	R/W	02	00000010	00111111	
RESERVED	-	03-06			
FIFO_CTRL1	R/W	07	00000111	00000000	
FIFO_CTRL2	R/W	08	00001000	00000000	
FIFO_CTRL3	R/W	09	00001001	00000000	
FIFO_CTRL4	R/W	0A	00001010	00000000	
COUNTER_BDR_REG1	R/W	0B	00001011	00000000	
COUNTER_BDR_REG2	R/W	0C	00001100	00000000	
INT1_CTRL	R/W	0D	00001101	00000000	
INT2_CTRL	R/W	0E	00001110	00000000	
WHO_AM_I	R	0F	00001111	01111011	
CTRL1_XL	R/W	10	00010000	00000000	
RESERVED	-	11			
CTRL3_C	R/W	12	00010010	00000100	
CTRL4_C	R/W	13	00010011	00000000	
CTRL5_C	R/W	14	00010100	00000000	
CTRL6_C	R/W	15	00010101	00000000	
CTRL7_C	R/W	16	00011100	00000000	
CTRL8_XL	R/W	17	00010111	00000000	
RESERVED	-	18			
CTRL10_C	R/W	19	00011001	00000000	
ALL_INT_SRC	R	1A	00011010	output	
WAKE_UP_SRC	R	1B	00011011	output	
RESERVED	-	1C-1D			
STATUS_REG	R	1E	00011110	output	
RESERVED	-	1F	00011111		
OUT_TEMP_L	R	20	00100000	output	
OUT_TEMP_H	R	21	00100001	output	
RESERVED	-	22-27			
OUTX_L_A	R	28	00101000	output	
OUTX_H_A	R	29	00101001	output	
OUTY_L_A	R	2A	00101010	output	
OUTY_H_A	R	2B	00101011	output	
OUTZ_L_A	R	2C	00101100	output	

Name	Type	Register address		Default	Comment
		Hex	Binary		
OUTZ_H_A	R	2D	00101101	output	
RESERVED	-	2E-39			
FIFO_STATUS1	R	3A	00111010	output	
FIFO_STATUS2	R	3B	00111011	output	
RESERVED	-	3C-3F			
TIMESTAMP0	R	40	01000000	output	
TIMESTAMP1	R	41	01000001	output	
TIMESTAMP2	R	42	01000010	output	
TIMESTAMP3	R	43	01000011	output	
RESERVED	-	44-55			
SLOPE_EN	R/W	56	01010111	00000000	
RESERVED	-	57			
INTERRUPTS_EN	R/W	58	01011000	00000000	
RESERVED	-	59-5A			
WAKE_UP_THS	R/W	5B	01011011	00000000	
WAKE_UP_DUR	R/W	5C	01011100	00000000	
RESERVED	-	5D			
MD1_CFG	R/W	5E	01011110	00000000	
MD2_CFG	R/W	5F	01011111	00000000	
RESERVED	-	60-62			
INTERNAL_FREQ_FINE	R	63	01100011	output	
RESERVED	-	64-72			
X_OFS_USR	R/W	73	01110011	00000000	
Y_OFS_USR	R/W	74	01110100	00000000	
Z_OFS_USR	R/W	75	01110101	00000000	
RESERVED	-	76-77			
FIFO_DATA_OUT_TAG	R	78	01111000	output	
FIFO_DATA_OUT_X_L	R	79	01111001	output	
FIFO_DATA_OUT_X_H	R	7A	01111010	output	
FIFO_DATA_OUT_Y_L	R	7B	01111011	output	
FIFO_DATA_OUT_Y_H	R	7C	01111100	output	
FIFO_DATA_OUT_Z_L	R	7D	01111101	output	
FIFO_DATA_OUT_Z_H	R	7E	01111110	output	

Reserved registers must not be changed. Writing to those registers may cause permanent damage to the device.

The content of the registers that are loaded at boot should not be changed. They contain the factory calibration values. Their content is automatically restored when the device is powered up.

9 Register description

9.1 PIN_CTRL (02h)

Enable/disable SDO pin pull-up register (R/W)

Table 9. PIN_CTRL register

0	SDO_PU_EN	1	1	1	1	1	1

Table 10. PIN_CTRL register description

SDO_PU_EN	Enables pull-up on SDO pin (0: SDO pin pull-up disconnected (default); 1: SDO pin with pull-up)

9.2 FIFO_CTRL1 (07h)

FIFO control register 1 (R/W)

Table 11. FIFO_CTRL1 register

WTM7	WTM6	WTM5	WTM4	WTM3	WTM2	WTM1	WTM0

Table 12. FIFO_CTRL1 register description

WTM[7:0]	FIFO watermark threshold, in conjunction with WTM8 in FIFO_CTRL2 (08h). 1 LSB = 1 sensor (6 bytes) + TAG (1 byte) written in FIFO Watermark flag rises when the number of bytes written in the FIFO is greater than or equal to the threshold level.

9.3 FIFO_CTRL2 (08h)

FIFO control register 2 (R/W)

Table 13. FIFO_CTRL2 register

STOP_ON_WTM	0(1)	0(1)	0(1)	0(1)	0(1)	0(1)	WTM8

1. *This bit must be set to 0 for the correct operation of the device.*

Table 14. FIFO_CTRL2 register description

STOP_ON_WTM	Sensing chain FIFO stop values memorization at threshold level (0: FIFO depth is not limited (default); 1: FIFO depth is limited to threshold level, defined in FIFO_CTRL1 (07h) and FIFO_CTRL2 (08h))
WTM8	FIFO watermark threshold, in conjunction with WTM_FIFO[7:0] in FIFO_CTRL1 (07h) 1 LSB = 1 sensor (6 bytes) + TAG (1 byte) written in FIFO Watermark flag rises when the number of bytes written in the FIFO is greater than or equal to the threshold level.

9.4 FIFO_CTRL3 (09h)

FIFO control register 3 (R/W)

Table 15. FIFO_CTRL3 register

0(1)	0(1)	0(1)	0(1)	BDR_XL_3	BDR_XL_2	BDR_XL_1	BDR_XL_0

1. *This bit must be set to 0 for the correct operation of the device.*

Table 16. FIFO_CTRL3 register description

BDR_XL_[3:0]	Selects batch data rate (write frequency in FIFO) for accelerometer data. (0000: accelerometer not batched in FIFO (default); 1010: 26667 Hz; 1011 - 1111: not allowed)

9.5 FIFO_CTRL4 (0Ah)

FIFO control register 4 (R/W)

Table 17. FIFO_CTRL4 register

DEC_TS_ BATCH_1	DEC_TS_ BATCH_0	ODR_T_ BATCH_1	ODR_T_ BATCH_0	0(1)	FIFO_ MODE_2	FIFO_ MODE_1	FIFO_ MODE_0

1. *This bit must be set to 0 for the correct operation of the device.*

Table 18. FIFO_CTRL4 register description

DEC_TS_ BATCH[1:0]	Selects decimation for timestamp batching in FIFO. The write rate is the rate between the accelerometer BDR divided by the decimation decoder. (00: timestamp not batched in FIFO (default); 01: decimation 1: BDR_XL[Hz]; 10: decimation 8: BDR_XL[Hz]/8; 11: decimation 32: BDR_XL[Hz]/32)
ODR_T_ BATCH[1:0]	Selects batch data rate (write frequency in FIFO) for temperature data (00: temperature not batched in FIFO (default); 11: 104 Hz)
FIFO_ MODE[2:0]	FIFO mode selection (000: bypass mode: FIFO disabled; 001: FIFO mode: stops collecting data when FIFO is full; 010: reserved; 011: continuous-to-FIFO mode: continuous mode until the trigger is deasserted, then FIFO mode; 100: bypass-to-continuous mode: bypass mode until the trigger is deasserted, then continuous mode; 101: reserved; 110: continuous mode: if the FIFO is full, the new sample overwrites the older one; 111: bypass-to-FIFO mode: bypass mode until the trigger is deasserted, then FIFO mode.)

9.6 COUNTER_BDR_REG1 (0Bh)

Counter batch data rate register 1 (R/W)

Table 19. COUNTER_BDR_REG1 register

dataready _pulsed	RST_ COUNTER _BDR	0(1)	0(1)	0(1)	CNT_BDR _TH_10	CNT_BDR _TH_9	CNT_BDR _TH_8

1. *This bit must be set to 0 for the correct operation of the device.*

Table 20. COUNTER_BDR_REG1 register description

dataready_pulsed	Enables pulsed data-ready mode (0: data-ready latched mode (returns to 0 only after an interface reading) (default); 1: data-ready pulsed mode (the data ready pulses are 18.75 µs long)
RST_ COUNTER_BDR	Resets the internal counter of batch events. This bit is automatically reset to zero if it was set to 1.
CNT_BDR_TH_ [10:8]	In conjunction with CNT_BDR_TH[7:0] in COUNTER_BDR_REG2 (0Ch), sets the threshold for the internal counter of batch events. When this counter reaches the threshold, the counter is reset and the COUNTER_BDR_IA flag in FIFO_STATUS2 (3Bh) is set to 1.

9.7 COUNTER_BDR_REG2 (0Ch)

Counter batch data rate register 2 (R/W)

Table 21. COUNTER_BDR_REG2 register

CNT_BDR _TH_7	CNT_BDR _TH_6	CNT_BDR _TH_5	CNT_BDR _TH_4	CNT_BDR _TH_3	CNT_BDR _TH_2	CNT_BDR _TH_1	CNT_BDR _TH_0

Table 22. COUNTER_BDR_REG2 register description

CNT_BDR_TH_ [7:0]	In conjunction with CNT_BDR_TH[10:8] in COUNTER_BDR_REG1 (0Bh), sets the threshold for the internal counter of batch events. When this counter reaches the threshold, the counter is reset and the COUNTER_BDR_IA flag in FIFO_STATUS2 (3Bh) is set to 1.

9.8 INT1_CTRL (0Dh)

INT1 pin control register (R/W)

Each bit in this register enables a signal to be carried over INT1.

Table 23. INT1_CTRL register

0(1)	INT1_ CNT_BDR	INT1_ FIFO _FULL	INT1_ FIFO_ OVR	INT1_ FIFO_TH	INT1_ BOOT	0(1)	INT1_ DRDY_XL

1. *This bit must be set to 0 for the correct operation of the device.*

Table 24. INT1_CTRL register description

INT1_CNT_BDR	Enables COUNTER_BDR_IA interrupt on INT1.
INT1_ FIFO _FULL	Enables FIFO full flag interrupt on INT1 pin.
INT1_ FIFO_ OVR	Enables FIFO overrun interrupt on INT1 pin.
INT1_FIFO_TH	Enables FIFO threshold interrupt on INT1 pin.
INT1_BOOT	Enables boot status on INT1 pin
INT1_ DRDY_XL	Enables accelerometer data-ready interrupt on INT1 pin.

9.9 INT2_CTRL (0Eh)

INT2 pin control register (R/W)

Each bit in this register enables a signal to be carried over INT2.

Table 25. INT2_CTRL register

0(1)	INT2_ CNT_BDR	INT2_ FIFO _FULL	INT2_ FIFO_ OVR	INT2_ FIFO_TH	INT2_ DRDY_TEMP	0(1)	INT2_ DRDY_XL

1. *This bit must be set to 0 for the correct operation of the device.*

Table 26. INT2_CTRL register description

INT2_CNT_BDR	Enables COUNTER_BDR_IA interrupt on INT2.
INT2_ FIFO _FULL	Enables FIFO full flag interrupt on INT2 pin.
INT2_ FIFO_ OVR	Enables FIFO overrun interrupt on INT2 pin.
INT2_FIFO_TH	Enables FIFO threshold interrupt on INT2 pin.
INT2_DRDY_TEMP	Enables temperature sensor data-ready interrupt on INT2 pin.
INT2_ DRDY_XL	Enables accelerometer data-ready interrupt on INT2 pin.

9.10 WHO_AM_I (0Fh)

Device identification register

Table 27. WHO_AM_I register

0	1	1	1	1	0	1	1

9.11 CTRL1_XL (10h)

Accelerometer control register 1 (R/W)

Table 28. CTRL1_XL register

XL_EN_2	XL_EN_1	XL_EN_0	0(1)	FS1_XL	FS0_XL	LPF2_XL_EN	0(1)

1. *This bit must be set to 0 for the correct operation of the device.*

Table 29. CTRL1_XL register description

XL_EN[2:0]	Enables accelerometer: (000: power-down (default); 101: accelerometer enabled;) All other configurations are not allowed.
FS[1:0]_XL	Selects accelerometer full-scale (see Table 30).
LPF2_XL_EN	Selects accelerometer high-resolution. (0: output from first stage digital filtering selected (default); 1: output from LPF2 second filtering stage selected)

Table 30. Accelerometer full-scale selection

FS[1:0]_XL	Full scale
00 (default)	±2 *g*
01	±16 *g*
10	±4 *g*
11	±8 *g*

9.12 CTRL3_C (12h)

Control register 3 (R/W)

Table 31. CTRL3_C register

BOOT	BDU	H_LACTIVE	PP_OD	SIM	IF_INC	0(1)	SW_RESET

1. *This bit must be set to 0 for the correct operation of the device.*

Table 32. CTRL3_C register description

BOOT	Reboots memory content. Default value: 0 (0: normal mode; 1: reboot memory content) *Note: The accelerometer must be ON. This bit is automatically cleared.*
BDU	Block data update. Default value: 0 (0: continuous update; 1: output registers are not updated until MSB and LSB have been read)
H_LACTIVE	Interrupt activation level. Default value: 0 (0: interrupt output pins active high; 1: interrupt output pins active low)
PP_OD	Push-pull/open-drain selection on INT1 and INT2 pins. Default value: 0 (0: push-pull mode; 1: open-drain mode)
SIM	SPI serial interface mode selection. Default value: 0 (0: 4-wire interface; 1: 3-wire interface)
IF_INC	Register address automatically incremented during a multiple byte access with a serial interface (I²C or SPI). Default value: 1 (0: disabled; 1: enabled)
SW_RESET	Software reset. Default value: 0 (0: normal mode; 1: reset device) This bit is automatically cleared.

9.13 CTRL4_C (13h)

Control register 4 (R/W)

Table 33. CTRL4_C register

0(1)	0(1)	INT2_ on_INT1	0(1)	DRDY_ MASK	I2C_disable	0(1)	1AX_TO_ 3REGOUT

1. *This bit must be set to 0 for the correct operation of the device.*

Table 34. CTRL4_C register description

INT2_on_INT1	Enables bit to route all interrupt signals available on INT1 pin. Default value: 0 (0: interrupt signals divided between INT1 and INT2 pins; 1: all interrupt signals in logic OR on INT1 pin)
DRDY_MASK	Enables data available (0: disabled; 1: mask DRDY on pin until filter settling ends.
I2C_disable	Disables I²C interface. Default value: 0 (0: SPI and I²C interfaces enabled (default); 1: I²C interface disabled)
1AX_TO_3REGOUT	In single-axis mode, uses the output of the XYZ registers to give 3 consecutive samples of the selected single axis.

9.14 CTRL5_C (14h)

Control register 5 (R/W)

Table 35. CTRL5_C register

0(1)	ROUNDING1	ROUNDING0	0(1)	0(1)	0(1)	ST1_XL	ST0_XL

1. *This bit must be set to 0 for the correct operation of the device.*

Table 36. CTRL5_C register description

ROUNDING[1:0]	Circular burst mode (wraparound) read from the output registers. Default value: 00 (00: no wraparound; 01: wraparound enabled)
ST[1:0]_XL	Enables linear acceleration sensor self-test. Default value: 00 (00: self-test disabled; other: refer to Table 37)

Table 37. Linear acceleration sensor self-test mode selection

ST1_XL	ST0_XL	Self-test mode
0	0	Normal mode
0	1	Positive sign self-test
1	0	Negative sign self-test
1	1	Not allowed

9.15 CTRL6_C (15h)

Control register 6 (R/W)

Table 38. CTRL6_C register

0(1)	0(1)	0(1)	0(1)	USR_ OFF_W	0(1)	XL_AXIS_ SEL_1	XL_AXIS_ SEL_0

1. *This bit must be set to 0 for the correct operation of the device.*

Table 39. CTRL6_C register description

USR_OFF_W	Weight of accelerometer user offset bits of registers X_OFS_USR (73h), Y_OFS_USR (74h), Z_OFS_USR (75h) (0 = 2^{-10} *g*/LSB; 1 = 2^{-6} *g*/LSB)
XL_AXIS_SEL[1:0]	Selects the active axis of the accelerometer in single-axis mode. Refer to Table 40 The selection or the switching of the active axis (3 axes or 1 axis among X, Y, Z) should be performed when the device is in power-down condition

Table 40. Accelerometer active axis

XL_AXIS_ SEL[1:0]	Active axis
00 (default)	3 axes (XYZ)
01	X-axis
10	Y-axis
11	Z-axis

9.16 CTRL7_C (16h)

Control register 7 (R/W)

Table 41. CTRL7_C register

0(1)	0(1)	0(1)	0(1)	0(1)	0(1)	USR_OFF_ ON_OUT	0(1)

1. *This bit must be set to 0 for the correct operation of the device.*

Table 42. CTRL7_C register description

USR_OFF_ON_OUT	Enables the accelerometer user offset correction block; it is valid for the low-pass path - see Figure 10. Accelerometer composite filter. Default value: 0 (0: accelerometer user offset correction block bypassed; (1: accelerometer user offset correction block enabled)

9.17 CTRL8_XL (17h)

Control register 8 (R/W)

Table 43. CTRL8_XL register

HPCF_XL_2	HPCF_XL_1	HPCF_XL_0	HP_REF_ MODE_XL	FASTSETTL_ MODE_XL	FDS	0(1)	0(1)

1. *This bit must be set to 0 for the correct operation of the device.*

Table 44. CTRL8_XL register description

HPCF_XL_[2:0]	Accelerometer LPF2 and HP filter configuration and cutoff setting. Refer to Table 45.
HP_REF_MODE_XL	Enables accelerometer high-pass filter reference mode (valid for high-pass path - FDS bit must be 1 and HPCF_XL_[2:0] must be set to 111). Default value: 0(1) (0: disabled, 1: enabled)
FASTSETTL_MODE_XL	Enables accelerometer LPF2 and HPF fast-settling mode. The filter sets the second samples after writing this bit. Default value: 0 (0: disabled, 1: enabled)
FDS	Accelerometer low-pass / high-pass filter selection. Refer to Figure 10.

1. *When enabled, the first output data have to be discarded.*

Table 45. Accelerometer bandwidth configurations

Filter type	FDS	LPF2_XL_EN	HPCF_XL_[2:0]	Bandwidth
Low pass	0	0	-	6.3 kHz
		1	000	ODR/4
			001	ODR/10
			010	ODR/20
			011	ODR/45
			100	ODR/100
			101	ODR/200
			110	ODR/400
			111	ODR/800
High pass	1	--	000	SLOPE (ODR/4)
			001	ODR/10
			010	ODR/20
			011	ODR/45
			100	ODR/100
			101	ODR/200
			110	ODR/400
			111	ODR/800

9.18 CTRL10_C (19h)

Control register 10 (R/W)

Table 46. CTRL10_C register

0(1)	0(1)	TIMESTAMP_EN	0(1)	0(1)	0(1)	0(1)	0(1)

1. *This bit must be set to 0 for the correct operation of the device.*

Table 47. CTRL10_C register description

TIMESTAMP_EN	Enables timestamp counter. Default value: 0 (0: disabled; 1: enabled) The counter is readable in TIMESTAMP0 (40h), TIMESTAMP1 (41h), TIMESTAMP2 (42h), and TIMESTAMP3 (43h).

9.19 ALL_INT_SRC (1Ah)

Source register for all interrupts (R)

Table 48. ALL_INT_SRC register

TIMESTAMP_ENDCOUNT	0	SLEEP_CHANGE_IA	0	0	0	WU_IA	0

Table 49. ALL_INT_SRC register description

TIMESTAMP_ENDCOUNT	Alerts timestamp overflow within 6.4 ms
SLEEP_CHANGE_IA	Detects change event in activity/inactivity status. Default value: 0 (0: change status not detected; 1: change status detected)
WU_IA	Wake-up event status. Default value: 0 (0: event not detected, 1: event detected)

9.20 WAKE_UP_SRC (1Bh)

Wake-up interrupt source register (R)

Table 50. WAKE_UP_SRC register

0	SLEEP_ CHANGE_IA	0	SLEEP_ STATE_IA	WU_IA	X_WU	Y_WU	Z_WU

Table 51. WAKE_UP_SRC register description

SLEEP_CHANGE_IA	Detects change event in activity/inactivity status. Default value: 0 (0: change status not detected; 1: change status detected)
SLEEP_STATE_IA	Sleep event status. Default value: 0 (0: sleep event not detected; 1: sleep event detected)
WU_IA	Wake-up event detection status. Default value: 0 (0: wake-up event not detected; 1: wake-up event detected.)
X_WU	Wake-up event detection status on X-axis. Default value: 0 (0: wake-up event on X-axis not detected; 1: wake-up event on X-axis detected)
Y_WU	Wake-up event detection status on Y-axis. Default value: 0 (0: wake-up event on Y-axis not detected; 1: wake-up event on Y-axis detected)
Z_WU	Wake-up event detection status on Z-axis. Default value: 0 (0: wake-up event on Z-axis not detected; 1: wake-up event on Z-axis detected)

9.21 STATUS_REG (1Eh)

Status register (R)

Table 52. STATUS_REG register

0	0	0	0	0	TDA	0	XLDA

Table 53. STATUS_REG register description

TDA	Temperature new data available. Default: 0 (0: no set of data is available at temperature sensor output; 1: a new set of data is available at temperature sensor output)
XLDA	Accelerometer new data available. Default value: 0 (0: no set of data available at accelerometer output; 1: a new set of data is available at accelerometer output)

9.22 OUT_TEMP_L (20h), OUT_TEMP_H (21h)

Temperature data output register (R). L and H registers together express a 16-bit word in two's complement.

Table 54. OUT_TEMP_L register

Temp7	Temp6	Temp5	Temp4	Temp3	Temp2	Temp1	Temp0

Table 55. OUT_TEMP_H register

Temp15	Temp14	Temp13	Temp12	Temp11	Temp10	Temp9	Temp8

Table 56. OUT_TEMP register description

Temp[15:0]	Temperature sensor output data The value is expressed as two's complement sign extended on the MSB.

9.23 OUTX_L_A (28h) and OUTX_H_A (29h)

Linear acceleration sensor X-axis output register (R). The value is expressed as a 16-bit word in two's complement.

Table 57. OUTX_L_A register

D7	D6	D5	D4	D3	D2	D1	D0

Table 58. OUTX_H_A register

D15	D14	D13	D12	D11	D10	D9	D8

Table 59. OUTX_H_A register description

D[15:0]	X-axis linear acceleration value D[15:0] expressed in two's complement

9.24 OUTY_L_A (2Ah) and OUTY_H_A (2Bh)

Linear acceleration sensor Y-axis output register (R). The value is expressed as a 16-bit word in two's complement.

Table 60. OUTY_L_A register

D7	D6	D5	D4	D3	D2	D1	D0

Table 61. OUTY_H_A register

D15	D14	D13	D12	D11	D10	D9	D8

Table 62. OUTY_H_A register description

D[15:0]	Y-axis linear acceleration value D[15:0] expressed in two's complement

9.25 OUTZ_L_A (2Ch) and OUTZ_H_A (2Dh)

Linear acceleration sensor Z-axis output register (R). The value is expressed as a 16-bit word in two's complement.

Table 63. OUTZ_L_A register

D7	D6	D5	D4	D3	D2	D1	D0

Table 64. OUTZ_H_A register

D15	D14	D13	D12	D11	D10	D9	D8

Table 65. OUTZ_H_A register description

D[15:0]	Z-axis linear acceleration value D[15:0] expressed in two's complement

9.26 FIFO_STATUS1 (3Ah)

FIFO status register 1 (R)

Table 66. FIFO_STATUS1 register

DIFF_ FIFO_7	DIFF_ FIFO_6	DIFF_ FIFO_5	DIFF_ FIFO_4	DIFF_ FIFO_3	DIFF_ FIFO_2	DIFF_ FIFO_1	DIFF_ FIFO_0

Table 67. FIFO_STATUS1 register description

DIFF_FIFO_[7:0]	Number of unread sensor data (TAG + 6 bytes) stored in FIFO In conjunction with DIFF_FIFO[9:8] in FIFO_STATUS2 (3Bh).

9.27 FIFO_STATUS2 (3Bh)

FIFO status register 2 (R)

Table 68. FIFO_STATUS2 register

FIFO_ WTM_IA	FIFO_ OVR_IA	FIFO_ FULL_IA	COUNTER_ BDR_IA	FIFO_OVR_ LATCHED	0	DIFF_ FIFO_9	DIFF_ FIFO_8

Table 69. FIFO_STATUS2 register description

FIFO_WTM_IA	FIFO watermark status. Default value: 0 (0: FIFO filling is lower than WTM; 1: FIFO filling is equal to or greater than WTM) Watermark is set through bits WTM[8:0] in FIFO_CTRL2 (08h) and FIFO_CTRL1 (07h).
FIFO_OVR_IA	FIFO overrun status. Default value: 0 (0: FIFO is not completely filled; 1: FIFO is completely filled)
FIFO_FULL_IA	Smart FIFO full status. Default value: 0 (0: FIFO is not full; 1: FIFO is full at the next ODR)
COUNTER_BDR_IA	Counter BDR reaches the CNT_BDR_TH_[10:0] threshold set in COUNTER_BDR_REG1 (0Bh) and COUNTER_BDR_REG2 (0Ch). Default value: 0 This bit is reset when these registers are read.
FIFO_OVR_LATCHED	Latched FIFO overrun status. Default value: 0 This bit is reset when this register is read.
DIFF_FIFO_[9:8]	Number of unread sensor data (TAG + 6 bytes) stored in FIFO. Default value: 00 In conjunction with DIFF_FIFO[7:0] in FIFO_STATUS1 (3Ah)

9.28 TIMESTAMP0 (40h), TIMESTAMP1 (41h), TIMESTAMP2 (42h), and TIMESTAMP3 (43h)

Timestamp first data output register (R). The value is expressed as a 32-bit word and the bit resolution is 12.5 µs.

Table 70. TIMESTAMP output registers

D31	D30	D29	D28	D27	D26	D25	D24
D23	D22	D21	D20	D19	D18	D17	D16
D15	D14	D13	D12	D11	D10	D9	D8
D7	D6	D5	D4	D3	D2	D1	D0

Table 71. TIMESTAMP output register description

D[31:0]	Timestamp output registers: 1LSB = 12.5 µs

The formula below can be used to calculate a better estimation of the actual timestamp resolution:
TS_Res = 1 / (80000 + (0.0015 * INTERNAL_FREQ_FINE * 80000))
where INTERNAL_FREQ_FINE is the content of INTERNAL_FREQ_FINE (63h).

9.29 SLOPE_EN (56h)

Slope enable (R/W)

Table 72. SLOPE_EN register

0(1)	0(1)	SLEEP_STATUS_ON_INT	SLOPE_FDS	0(1)	0(1)	0(1)	LIR

1. *This bit must be set to 0 for the correct operation of the device.*

Table 73. SLOPE_EN register description

SLEEP_STATUS_ON_INT	Activity/inactivity interrupt mode configuration. If the INT1_SLEEP_CHANGE or INT2_SLEEP_CHANGE bits are enabled, drives the sleep status or sleep change on the INT pins. Default value: 0 (0: sleep change notification on INT pins; 1: sleep status reported on INT pins)
SLOPE_FDS	HPF or slope filter selection on wake-up and activity/inactivity functions. Default value: 0 (0: slope filter applied; 1: HPF applied)
LIR	Latched interrupt. Default value: 0 (0: interrupt request not latched; 1: interrupt request latched)

9.30 INTERRUPTS_EN (58h)

Enables interrupt functions (R/W)

Table 74. INTERRUPTS_EN register

INTERRUPTS_ENABLE	0(1)	0(1)	0(1)	0(1)	0(1)	0(1)	0(1)

1. *This bit must be set to 0 for the correct operation of the device.*

Table 75. INTERRUPTS_EN register description

INTERRUPTS_ENABLE	Enables wake-up and activity/inactivity interrupt logic. Default value: 0 (0: interrupt disabled; 1: interrupt enabled)

9.31 WAKE_UP_THS (5Bh)

Wake-up configuration (R/W)

Table 76. WAKE_UP_THS register

0(1)	USR_OFF_ON_WU	WK_THS5	WK_THS4	WK_THS3	WK_THS2	WK_THS1	WK_THS0

1. *This bit must be set to 0 for the correct operation of the device.*

Table 77. WAKE_UP_THS register description

USR_OFF_ON_WU	Drives the low-pass filtered data with user offset correction (instead of high-pass filtered data) to the wake-up function.
WK_THS[5:0]	Threshold for wake-up: 1 LSB weight depends on WAKE_THS_W in WAKE_UP_DUR (5Ch). Default value: 000000

9.32 WAKE_UP_DUR (5Ch)

Wake-up and sleep mode functions duration setting register (R/W)

Table 78. WAKE_UP_DUR register

0(1)	WAKE_DUR1	WAKE_DUR0	WAKE_THS_W	SLEEP_DUR3	SLEEP_DUR2	SLEEP_DUR1	SLEEP_DUR0

1. *This bit must be set to 0 for the correct operation of the device.*

Table 79. WAKE_UP_DUR register description

WAKE_DUR[1:0]	Wake-up duration event. Default: 00 1LSB = 1 ODR_time
WAKE_THS_W	Weight of 1 LSB of wake-up threshold. Default: 0 (0: 1 LSB = FS_XL / (2^6); 1: 1 LSB = FS_XL / (2^8))
SLEEP_DUR[3:0]	Duration to go in sleep mode. Default value: 0000 (this corresponds to 16 ODR) 1 LSB = 512 ODR

9.33 MD1_CFG (5Eh)

Functions routing to INT1 register (R/W)

Table 80. MD1_CFG register

INT1_SLEEP_CHANGE	0(1)	INT1_WU	0(1)	0(1)	0(1)	0(1)	0(1)

1. *This bit must be set to 0 for the correct operation of the device.*

Table 81. MD1_CFG register description

INT1_SLEEP_CHANGE(1)	Routing activity/inactivity recognition event to INT1. Default: 0 (0: routing activity/inactivity event to INT1 disabled; 1: routing activity/inactivity event to INT1 enabled)
INT1_WU	Routing wake-up event to INT1. Default value: 0 (0: routing wake-up event to INT1 disabled; 1: routing wake-up event to INT1 enabled)

1. *Activity/inactivity interrupt mode (sleep change or sleep status) depends on the SLEEP_STATUS_ON_INT bit in the SLOPE_EN (56h) register.*

9.34 MD2_CFG (5Fh)

Functions routing to INT2 register (R/W)

Table 82. MD2_CFG register

INT2_SLEEP_CHANGE	0(1)	INT2_WU	0(1)	0(1)	0(1)	0(1)	INT2_TIMESTAMP

1. *This bit must be set to 0 for the correct operation of the device.*

INT2_SLEEP_CHANGE(1)	Routing activity/inactivity recognition event to INT2. Default: 0 (0: routing activity/inactivity event to INT2 disabled; 1: routing activity/inactivity event to INT2 enabled)
INT2_WU	Routing wake-up event to INT2. Default value: 0 (0: routing wake-up event to INT2 disabled; 1: routing wake-up event to INT2 enabled)
INT2_TIMESTAMP	Enables routing the alert for timestamp overflow within 6.4 ms to the INT2 pin

1. *Activity/inactivity interrupt mode (sleep change or sleep status) depends on the SLEEP_STATUS_ON_INT bit in the SLOPE_EN (56h) register.*

9.35 INTERNAL_FREQ_FINE (63h)

Internal frequency register (R)

Table 83. INTERNAL_FREQ_FINE register

FREQ_ FINE7	FREQ_ FINE6	FREQ_ FINE5	FREQ_ FINE4	FREQ_ FINE3	FREQ_ FINE2	FREQ_ FINE1	FREQ_ FINE0

Table 84. INTERNAL_FREQ_FINE register description

FREQ_FINE[7:0]	Difference in percentage of the effective ODR (and timestamp rate) with respect to the typical. Step: 0.15%. 8-bit format, two's complement.

The formula below can be used to calculate a better estimation of the actual ODR:
ODR_Actual = (26667 + ((0.0015 * INTERNAL_FREQ_FINE) * 26667))

9.36 X_OFS_USR (73h)

Accelerometer X-axis user offset correction (R/W). The offset value set in the X_OFS_USR offset register is internally subtracted from the acceleration value measured on the X-axis.

Table 85. X_OFS_USR register

X_OFS_ USR_7	X_OFS_ USR_6	X_OFS_ USR_5	X_OFS_ USR_4	X_OFS_ USR_3	X_OFS_ USR_2	X_OFS_ USR_1	X_OFS_ USR_0

Table 86. X_OFS_USR register description

X_OFS_USR_[7:0]	Accelerometer X-axis user offset correction expressed in two's complement, weight depends on USR_OFF_W in CTRL6_C (15h). The value must be in the range [-127 127].

9.37 Y_OFS_USR (74h)

Accelerometer Y-axis user offset correction (R/W). The offset value set in the Y_OFS_USR offset register is internally subtracted from the acceleration value measured on the Y-axis.

Table 87. Y_OFS_USR register

Y_OFS_ USR_7	Y_OFS_ USR_6	Y_OFS_ USR_5	Y_OFS_ USR_4	Y_OFS_ USR_3	Y_OFS_ USR_2	Y_OFS_ USR_1	Y_OFS_ USR_0

Table 88. Y_OFS_USR register description

Y_OFS_USR_[7:0]	Accelerometer Y-axis user offset calibration expressed in two's complement, weight depends on USR_OFF_W in CTRL6_C (15h). The value must be in the range [-127, +127].

9.38 Z_OFS_USR (75h)

Accelerometer Z-axis user offset correction (R/W). The offset value set in the Z_OFS_USR offset register is internally subtracted from the acceleration value measured on the Z-axis.

Table 89. Z_OFS_USR register

Z_OFS_USR_7	Z_OFS_USR_6	Z_OFS_USR_5	Z_OFS_USR_4	Z_OFS_USR_3	Z_OFS_USR_2	Z_OFS_USR_1	Z_OFS_USR_0

Table 90. Z_OFS_USR register description

Z_OFS_USR_[7:0]	Accelerometer Z-axis user offset calibration expressed in two's complement, weight depends on USR_OFF_W in CTRL6_C (15h). The value must be in the range [-127, +127].

9.39 FIFO_DATA_OUT_TAG (78h)

FIFO tag register (R)

Table 91. FIFO_DATA_OUT_TAG register

TAG_SENSOR_4	TAG_SENSOR_3	TAG_SENSOR_2	TAG_SENSOR_1	TAG_SENSOR_0	TAG_CNT_1	TAG_CNT_0	TAG_PARITY

Table 92. FIFO_DATA_OUT_TAG register description

TAG_SENSOR_[4:0]	FIFO tag: identifies the sensor in: FIFO_DATA_OUT_X_L (79h) and FIFO_DATA_OUT_X_H (7Ah), FIFO_DATA_OUT_Y_L (7Bh) and FIFO_DATA_OUT_Y_H (7Ch), and FIFO_DATA_OUT_Z_L (7Dh) and FIFO_DATA_OUT_Z_H (7Eh) For details, refer to Table 93.
TAG_CNT_[1:0]	2-bit counter that identifies sensor time slot
TAG_PARITY	Parity check of TAG content

Table 93. FIFO tag

TAG_SENSOR_[4:0]	Sensor name
0x02	Accelerometer
0x03	Temperature
0x04	Timestamp

9.40 FIFO_DATA_OUT_X_L (79h) and FIFO_DATA_OUT_X_H (7Ah)

FIFO data output X (R)

Table 94. FIFO_DATA_OUT_X_H and FIFO_DATA_OUT_X_L registers

D15	D14	D13	D12	D11	D10	D9	D8
D7	D6	D5	D4	D3	D2	D1	D0

Table 95. FIFO_DATA_OUT_X_H and FIFO_DATA_OUT_X_L register description

D[15:0]	FIFO X-axis output

9.41 FIFO_DATA_OUT_Y_L (7Bh) and FIFO_DATA_OUT_Y_H (7Ch)

FIFO data output Y (R)

Table 96. FIFO_DATA_OUT_Y_H and FIFO_DATA_OUT_Y_L registers

D15	D14	D13	D12	D11	D10	D9	D8
D7	D6	D5	D4	D3	D2	D1	D0

Table 97. FIFO_DATA_OUT_Y_H and FIFO_DATA_OUT_Y_L register description

D[15:0]	FIFO Y-axis output

9.42 FIFO_DATA_OUT_Z_L (7Dh) and FIFO_DATA_OUT_Z_H (7Eh)

FIFO data output Z (R)

Table 98. FIFO_DATA_OUT_Z_H and FIFO_DATA_OUT_Z_L registers

D15	D14	D13	D12	D11	D10	D9	D8
D7	D6	D5	D4	D3	D2	D1	D0

Table 99. FIFO_DATA_OUT_Z_H and FIFO_DATA_OUT_Z_L register description

D[15:0]	FIFO Z-axis output

10 Soldering information

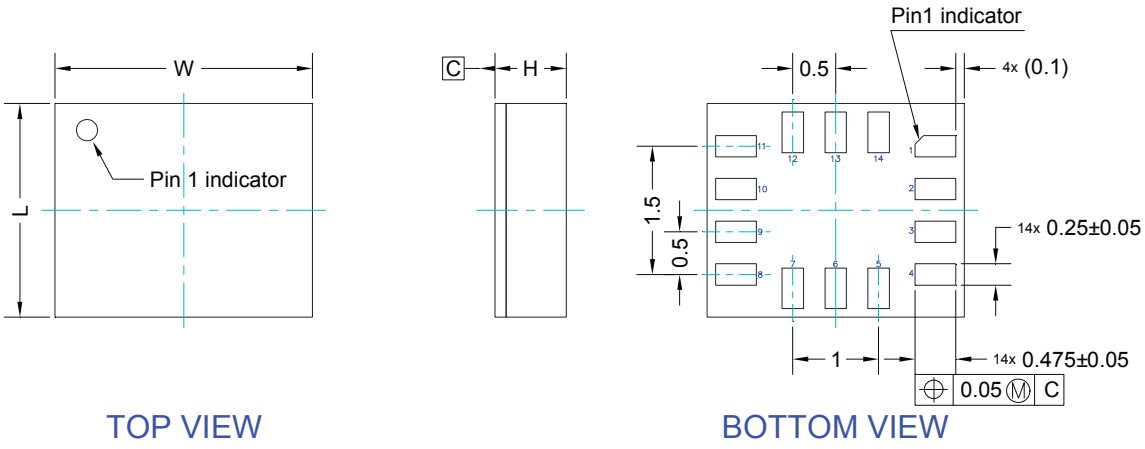
The LGA package is compliant with the ECOPACK and RoHS standard.
It is qualified for soldering heat resistance according to JEDEC J-STD-020.
For land pattern and soldering recommendations, consult technical note TN0018 available on www.st.com.

11 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

11.1 LGA-14L package information

Figure 22. LGA-14L 2.5 x 3.0 x 0.86 mm package outline and mechanical data



Dimensions are in millimeter unless otherwise specified
General tolerance is +/-0.1mm unless otherwise specified

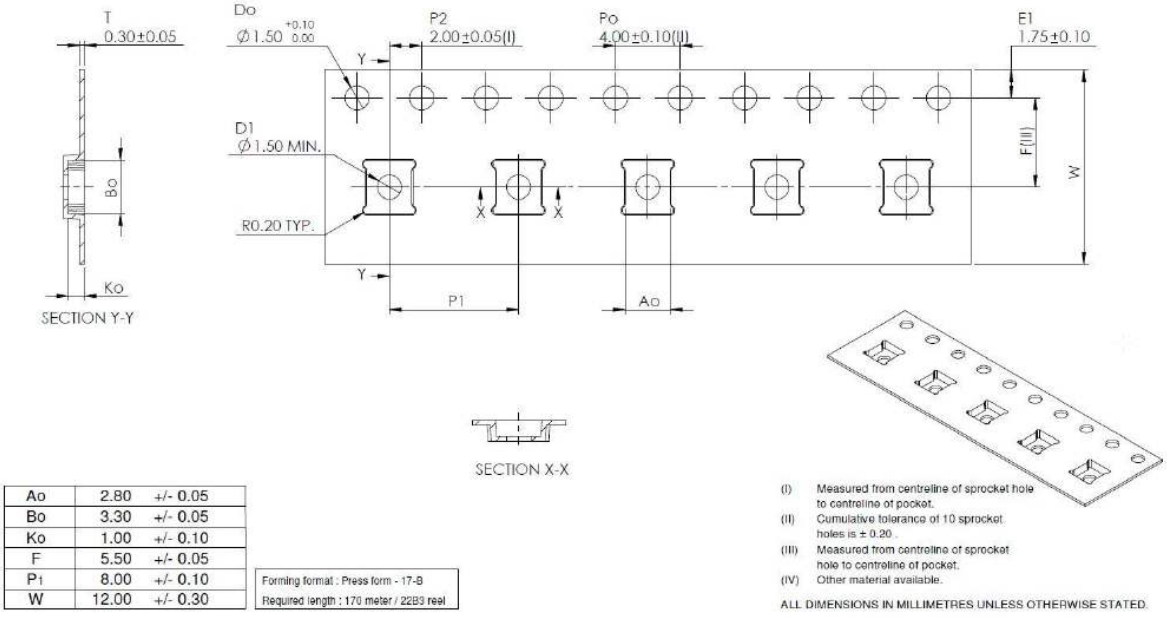
OUTER DIMENSIONS

ITEM	DIMENSION [mm]	TOLERANCE [mm]
Length [L]	2.50	±0.1
Width [W]	3.00	±0.1
Height [H]	0.86	MAX

DM00249496_5

11.2 LGA-14 packing information

Figure 23. **Carrier tape information for LGA-14 package**



Ao	2.80	+/- 0.05
Bo	3.30	+/- 0.05
Ko	1.00	+/- 0.10
F	5.50	+/- 0.05
P_1	8.00	+/- 0.10
W	12.00	+/- 0.30

Forming format : Press form - 17-B
Required length : 170 meter / 2283 reel

Figure 24. **LGA-14 package orientation in carrier tape**

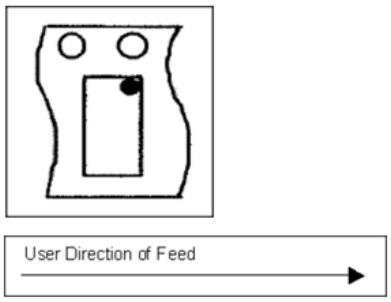


Figure 25. **Reel information for carrier tape of LGA-14 package**

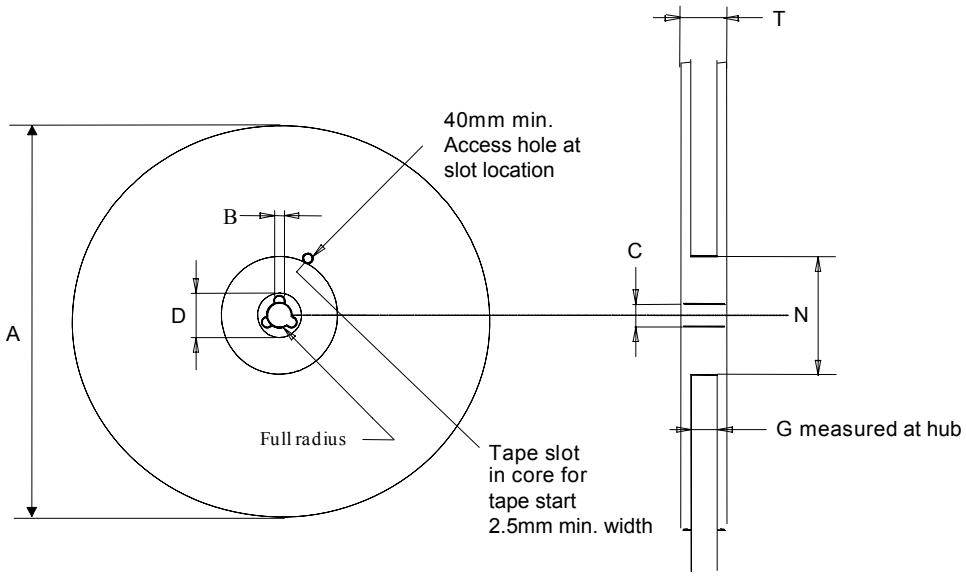


Table 100. **Reel dimensions for carrier tape of LGA-14 package**

Reel dimensions (mm)	
A (max)	330
B (min)	1.5
C	13 ±0.25
D (min)	20.2
N (min)	60
G	12.4 +2/-0
T (max)	18.4

Revision history

Table 101. **Document revision history**

Date	Version	Changes
29-Jan-2020	3	First public release
20-Feb-2020	4	Updated CTRL8_XL (17h) Updated SLOPE_EN (56h) Added INTERRUPTS_EN (58h) Updated Table 92. FIFO tag Minor textual changes
21-Jul-2020	5	Updated Section 3.3.7 FIFO reading procedure Updated description of dataready_pulsed bit in COUNTER_BDR_REG1 (0Bh) Updated TIMESTAMP0 (40h), TIMESTAMP1 (41h), TIMESTAMP2 (42h), and TIMESTAMP3 (43h)
13-Aug-2020	6	Added Section 3 Digital interface
13-Mar-2023	7	Updated product summary and added product resources (page 1) Updated Note below Figure 2. SPI slave timing diagram Minor textual updates

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