HARRIS

IRFF9230, IRFF9231 IRFF9232, IRFF9233

Avalanche Energy Rated P-Channel Power MOSFETs

August 1991

Features

- -3.5A and -4.0A, -150V and -200V
- $r_{DS(ON)}$ = 0.8Ω and 1.20Ω
- Single Pulse Avalanche Energy Rated
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance

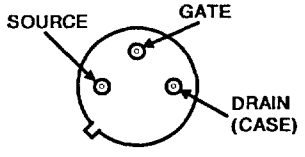
Description

The IRFF9230, IRFF9231, IRFF9232 and IRFF9233 are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. These are p-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRFF types are supplied in the JEDEC TO-205AF (Low Profile TO-39) metal package.

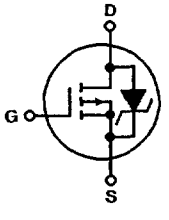
Package

TO-205AF
BOTTOM VIEW



Terminal Diagram

P-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = 25°C) Unless Otherwise Specified

		IRFF9230	IRFF9231	IRFF9232	IRFF9233	UNITS
Drain-Source Voltage (1)	V_{DS}	-200	-150	-200	-150	V
Drain-Gate Voltage (R_{GS} = 20kΩ) (1)	V_{DGR}	-200	-150	-200	-150	V
Continuous Drain Current T_C = 25°C	I_D	-4.0	-4.0	-3.5	-3.5	A
Pulsed Drain Current (3)	I_{DM}	-16	-16	-14	-14	A
Gate-Source Voltage	V_{GS}	±20	±20	±20	±20	V
Maximum Power Dissipation (See Figure 14)	P_D	25	25	25	25	W
Linear Derating Factor (See Figure 14)		0.2	0.2	0.2	0.2	W/°C
Single Pulse Avalanche Energy Rating (4)	E_{as}	500	500	500	500	mJ
Operating and Storage Junction Temperature Range	T_J, T_{STG}	-55 to +150	-55 to +150	-55 to +150	-55 to +150	°C
Maximum Lead Temperature for Soldering (0.063" (1.6mm) from case for 10s)	T_L	300	300	300	300	°C

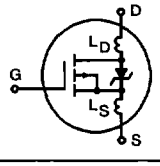
NOTES:

1. T_J = +25°C to +150°C
2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%
3. Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Figure 5)
4. V_{DD} = 50V, Start T_J = +25°C, L = 46.9mH, R_G = 25Ω, Peak I_L = 4.0A (See Figures 15 and 16)

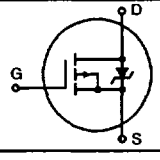
5 P-CHANNEL POWER MOSFETs

File Number 2225

Electrical Characteristics T_C = +25°C, Unless Otherwise Specified

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Drain-Source Breakdown Voltage IRFF9230, IRFF9232	BV_{DSS}	V_{GS} = 0V, I_D = -250μA	-200	-	-	V
IRFF9231, IRFF9233			-150	-	-	V
Gate Threshold Voltage	$V_{GS(TH)}$	V_{DS} = V_{GS}, I_D = -250μA	-2.0	-	-4.0	V
Gate-Source Leakage Forward	I_{GSS}	V_{GS} = -20V	-	-	-100	nA
Gate-Source Leakage Reverse	I_{GSS}	V_{GS} = 20V	-	-	100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = Max Rating, V_{GS} = 0V	-	-	-250	μA
		V_{DS} = Max Rating x 0.8, V_{GS} = 0V, T_C = +125°C	-	-	-1000	μA
On-State Drain Current (Note 2) IRFF9230, IRFF9231	$I_{D(ON)}$	V_{DS} > $I_{D(ON)}$ x $r_{DS(ON)}$ Max, V_{GS} = -10V	-4.0	-	-	A
IRFF9232, IRFF9233			-3.5	-	-	A
Static Drain-Source On-State Resistance (Note 2) IRFF9230, IRFF9231	$r_{DS(ON)}$	V_{GS} = -10V, I_D = -2.0A	-	0.5	0.8	Ω
IRFF9232, IRFF9233			-	0.8	1.2	Ω
Forward Transconductance (Note 2)	g_{fs}	V_{DS} > $I_{D(ON)}$ x $r_{DS(ON)}$ Max, I_D = -2.0A	2.2	3.5	-	S(℧)
Input Capacitance	C_{ISS}	V_{GS} = 0V, V_{DS} = -25V, f = 1.0MHz See Figure 10	-	550	-	pF
Output Capacitance	C_{OSS}		-	170	-	pF
Reverse Transfer Capacitance	C_{RSS}		-	50	-	pF
Turn-On Delay Time	$t_{d(ON)}$	V_{DD} =0.5 BV_{DSS}, I_D = -4.0A, R_G = 9.1Ω See Figure 17. (MOSFET switching times are essentially independent of operating temperature.)	-	30	50	ns
Rise Time	t_r		-	50	100	ns
Turn-Off Delay Time	$t_{d(OFF)}$		-	50	100	ns
Fall Time	t_f		-	40	80	ns
Total Gate Charge (Gate-Source + Gate-Drain)	Q_g	V_{GS} = -10V, I_D = -4.0V$_{DS}$ = 0.8 Max Rating. See Figure 18 for test circuit. (Gate charge is essentially independent of operating temperature.)	-	31	45	nC
Gate-Source Charge	Q_{gs}		-	18	-	nC
Gate-Drain ("Miller") Charge	Q_{gd}		-	13	-	nC
Internal Drain Inductance	L_D	Measured from the drain lead, 5mm (0.2") from header to center of die. Modified MOSFET symbol showing the internal device inductances.	-	5.0	-	nH
Internal Source Inductance	L_S	Measured from the source lead, 5mm (0.2") from header to source bonding pad. 	-	15	-	nH
Junction-to-Case	$R_{\theta JC}$		-	-	5.0	°C/W
Junction-to-Ambient	$R_{\theta JA}$	Typical socket mount	-	-	175	°C/W

Source Drain Diode Ratings and Characteristics

Continuous Source Current (Body Diode)	I_S	Modified MOSFET symbol showing the integral reverse P-N junc. rectifier. 	-	-	-4.0	A
Pulse Source Current (Body Diode) (Note 3)	I_{SM}		-	-	-16	A
Diode Forward Voltage (Note 2)	V_{SD}	T_C = +25°C, I_S = -4.0A, V_{GS} = 0V	-	-	-1.5	V
Reverse Recovery Time	t_{rr}	T_J = +150°C, I_F = -4.0A, dI_F/dt = 100A/μs	-	400	-	ns
Reverse Recovered Charge	Q_{RR}	T_J = +150°C, I_F = -4.0A, dI_F/dt = 100A/μs	-	2.6	-	μC
Forward Turn-on Time	t_{ON}	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.	-	-	-	-

NOTES: 1. T_J = +25°C to +150°C
2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%
3. Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Figure 5)
4. V_{DD} = 50V, Start T_J = +25°C, L = 46.9mH, R_G = 25Ω, Peak I_L = 4.0A (See Figures 15 and 16)

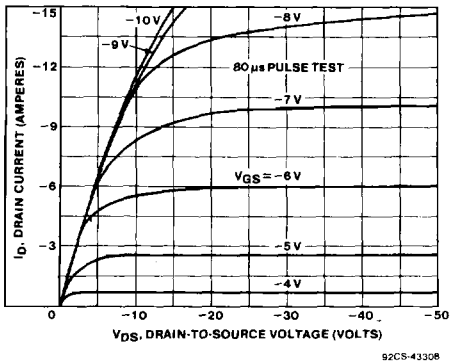


Fig. 1 - Typical output characteristics.

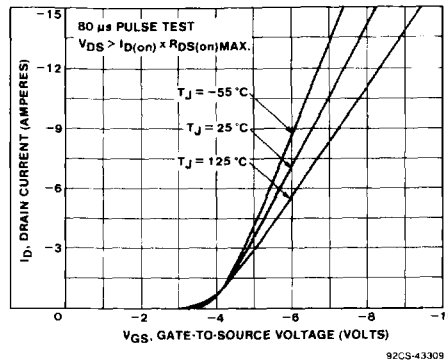


Fig. 2 - Typical transfer characteristics.

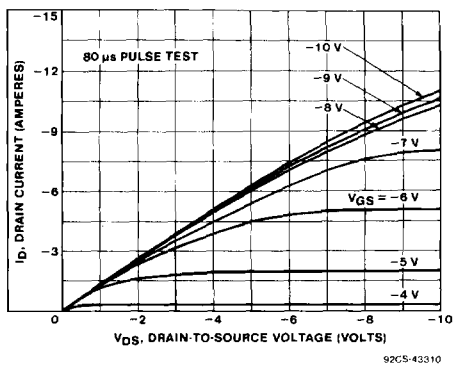


Fig. 3 - Typical saturation characteristics.

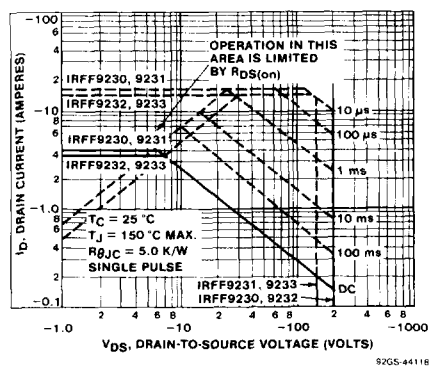


Fig. 4 - Maximum safe operating area.

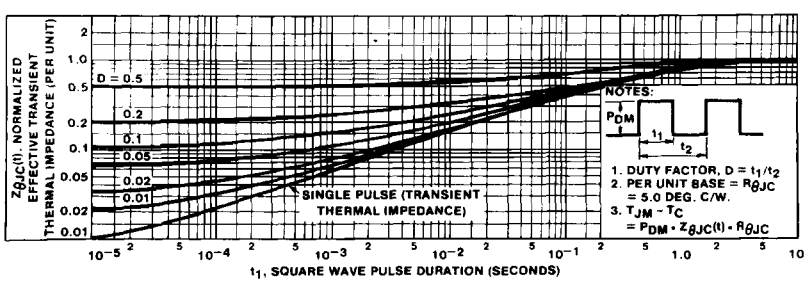


Fig. 5 - Maximum effective transient thermal impedance, junction-

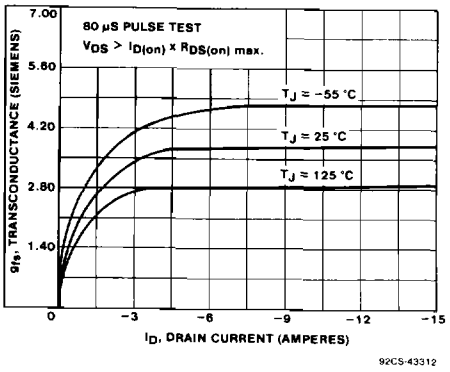


Fig. 6 - Typical transconductance vs. drain current.

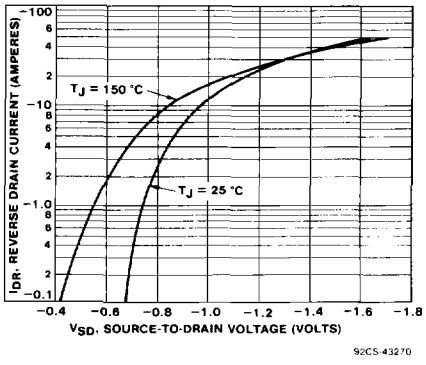


Fig. 7 - Typical source-drain diode forward voltage.

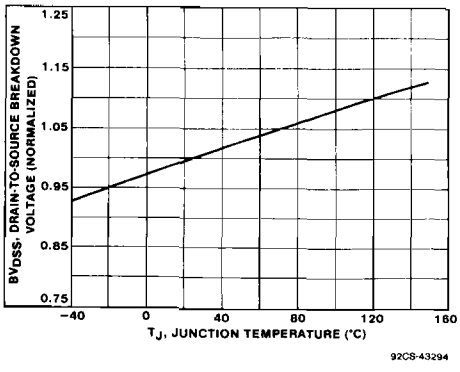


Fig. 8 - Breakdown voltage vs. temperature.

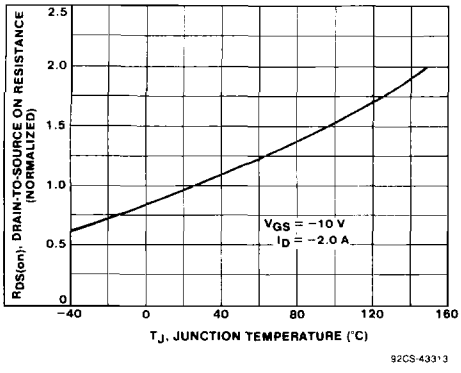


Fig. 9 - Normalized on-resistance vs. temperature.

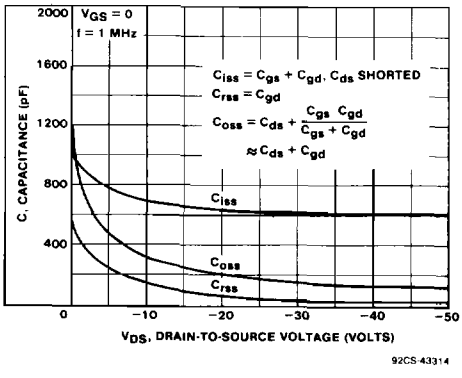


Fig. 10 - Typical capacitance vs. drain-to-source voltage.

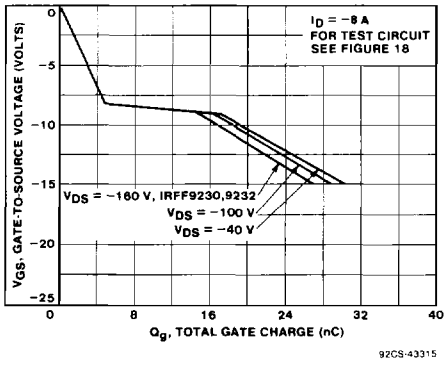


Fig. 11 - Typical gate charge vs. gate-to-source voltage.

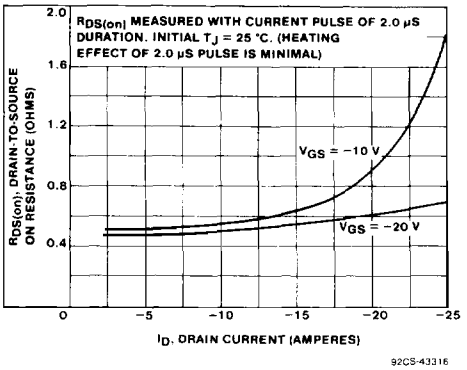


Fig. 12 - Typical on-resistance vs. drain current.

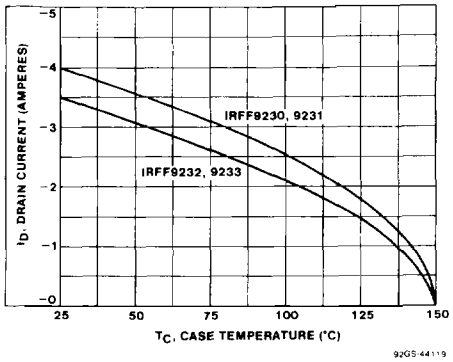


Fig. 13 - Maximum drain current vs. case temperature.

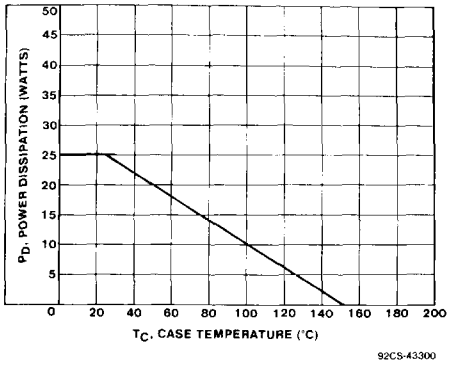


Fig. 14 - Power vs. temperature derating curve.

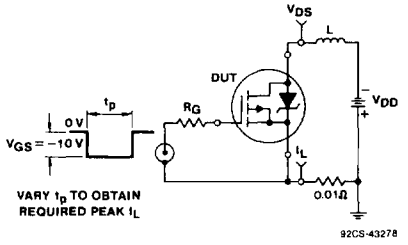


Fig. 15 - Unclamped inductive test circuit.

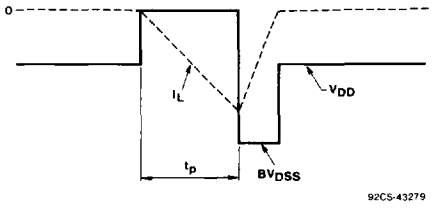


Fig. 16 - Unclamped inductive waveforms.

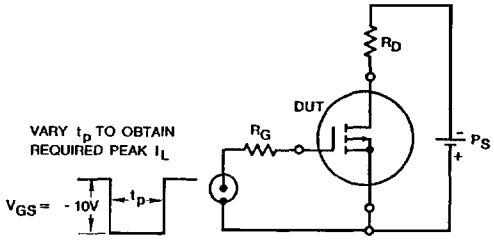


Fig. 17 - Switching time test circuit.

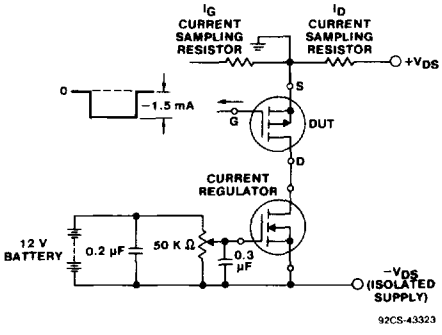


Fig. 18 - Gate charge test circuit.