DC-DC Converters + LDO PMIC for Industrial/Automotive Application

General Description

The RTQ2077S is a highly-integrated, low-power high performance PMIC (Power Management IC) for Industrial/Automotive applications. The device includes one 400mA high voltage synchronous step-down DC-DC converter and one 200mA low dropout LDO. All MOSFETs are integrated, and compensation networks are built-in.

The RTQ2077S is an Automotive-Grade Product that is AEC-Q100 Grade 1 Qualified and provides fault condition protections, including over-current protection, under-voltage lockout, over-voltage protection and over-temperature protection. The RTQ2077S is available in WQFN-16L 3x3 package.

Applications

- Automotive Systems
- Car Camera Module and Car Cockpit Systems
- Connected Car Systems
- Point of Load Regulator in Distributed Power Systems
- Digital Set Top Boxes
- Broadband Communications

Ordering Information

RTQ2077S □□-QT

- Grade
  QT : AEC-Q100 Qualified
- Package Type
  QW : WQFN-16L 3x3 (W-Type)
- Lead Plating System
  G : Green (Halogen Free and Pb Free)

Note :

Richtek products are :

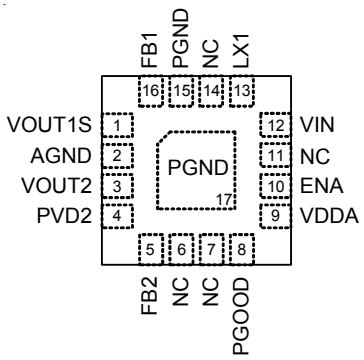
- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

Features

- **AEC-Q100 Grade 1 Qualified**
- **–40°C to 125°C Operating Ambient Temperature Range**
- **2.7V to 5.5V Input Voltage Range for LDO**
- **4.5V to 15V Input Voltage Range for HV-Step-Down Regulator**
- **2MHz Switching Frequency**
- **Adjustable Output Voltage from 2.7V to 5V for HV-Step-Down Regulator**
- **Adjustable Output Voltage from 1V to 3.6V for LDO**
- **Peak Current Mode Control**
- **Integrated 330mΩ /150mΩ MOSFETs**
- **Enable Control**
- **Power Good Indicator**
- **Cycle-by-Cycle Over-Current Limit Protection**
- **Input Under-Voltage Lockout**
- **Output Under-Voltage Protection**
- **Over-Temperature Protection**

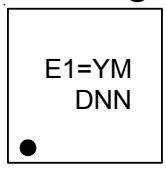
Pin Configuration

(TOP VIEW)



WQFN-16L 3X3

Marking Information



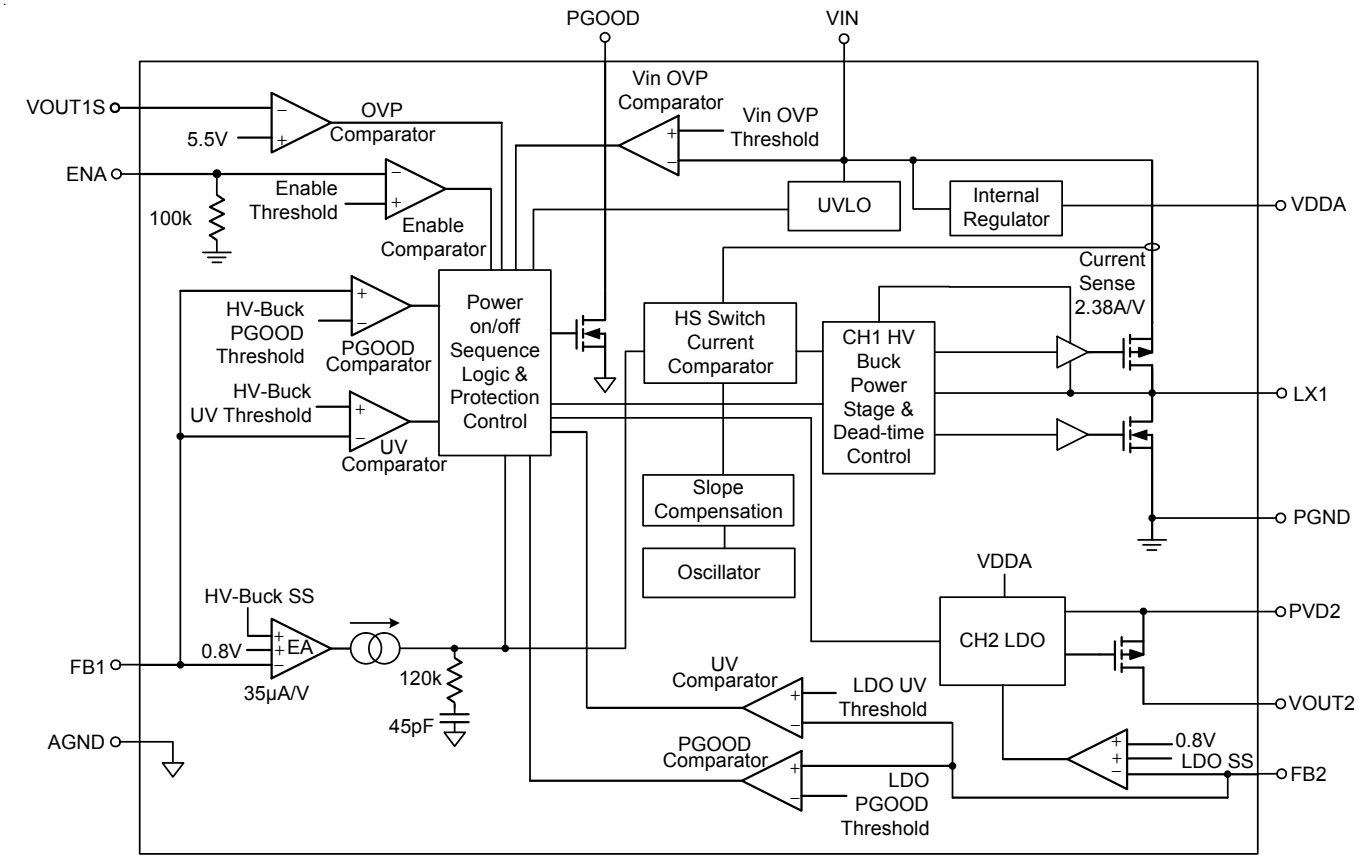
E1= : Product Code

YMDNN : Date Code

Functional Pin Description

Pin No.	Pin Name	Pin Function
1	VOUT1S	HV-Buck output voltage sense input. Connect this pin to the HV-buck output voltage for OVP detection.
2	AGND	Analog ground.
3	VOUT2	LDO output pin. AGND and PGND are connected with a short trace and at only one point to reduce circulating currents. A 2.2μF, X7R or larger ceramic capacitor is required for stability. Place the output capacitor as close to the device as possible and minimize the impedance between VOUT2 pin to load.
4	PVD2	Power input for LDO. The input voltage range is from 2.7V to 5.5V after soft-start is finished. Connect input capacitors between this pin and PGND. It is recommended to use a 10μF, X7R capacitors.
5	FB2	Feedback voltage input for LDO. Connect this pin to the midpoint of the external feedback resistive divider to set the output voltage of the converter to the desired regulation level. The device regulates the FB voltage at a feedback reference voltage, typically 0.8V.
6, 7, 11, 14	NC	No internal connection.
8	PGOOD	Open-drain power-good indication output. Once soft-start is finished, PGOOD will be pulled low to ground if any internal protection is triggered.
9	VDDA	Internal LDO output pin. VDDA is the output of the internal 4.45V linear regulator powered by VIN. Decouple with a 1μF, X7R ceramic capacitor from VDDA to ground for normal operation.
10	ENA	Enable control input. A logic-high enables the PMIC; a logic-low forces the device into shutdown mode.
12	VIN	Power input for HV-Buck. The input voltage range is from 3V to 36V after soft-start is finished. Connect input capacitors between this pin and PGND. It is recommended to use a 4.7μF, X7R and a 0.1μF, X7R capacitors.
13	LX1	Switch node for HV-Buck. LX1 is the switching node that supplies power to the output and connect the output LC filter from LX1 to the output load.
15	PGND	Power ground. Connect this pin to the negative terminals of the input capacitor and output capacitor.
16	FB1	Feedback voltage input for HV-Buck. Connect this pin to the midpoint of the external feedback resistive divider to set the output voltage of the converter to the desired regulation level. The device regulates the FB voltage at a feedback reference voltage, typically 0.8V.
17 (Exposed Pad)	PAD	Exposed pad. The exposed pad is internally unconnected and must be soldered to a large PGND plane. Connect this PGND plane to other layers with thermal vias to help dissipate heat from the device.

Functional Block Diagram



Operation

The RTQ2077S is a highly-integrated PMIC for automotive systems, including a HV step-down DC-DC converter and LDO. The RTQ2077S application mechanism will be introduced in later sections.

When the ENA pin is at high level, the PMIC follows the power-on sequence to turn on channels. The IC turns on base and calibrates. Time is less than 500µs.

Main Control Loop

The HV step-down converter of the RTQ2077S utilizes the peak current mode control. An internal oscillator initiates turn-on of the high-side MOSFET switch.

At the beginning of each clock cycle, the internal high-side MOSFET switch turns on, allowing current to ramp-up in the inductor. The inductor current is internally monitored during each switching cycle. The output voltage is sensed on the FB1 pin via the resistor divider, R_{FB11} and R_{FB12}, and compared with the internal reference voltage for constant voltage control.

When the inductor current reaches its threshold, the high-side MOSFET switch is turned off and inductor current ramps-down. While the high-side switch is off, inductor current is supplied through the low-side MOSFET switch. This cycle repeats at the next clock cycle. In this way, duty-cycle and output voltage are controlled by regulating inductor current.

Enable Control

The RTQ2077S provides an ENA pin, as an external chip enable control, to enable or disable the device. If V_{ENA} is held below a logic-low threshold voltage (V_{ENA_L}), switching is inhibited even if the VIN voltage is above VIN under-voltage lockout threshold (V_{UVLO}). If V_{ENA} is held below 0.5V, the converter will enter into shutdown mode, that is, the converter is disabled. During shutdown mode, the supply current can be reduced to I_{SHDN} (15µA or below). If the ENA voltage rises above the logic-high threshold voltage (V_{ENA_H}) while the VIN voltage is higher than V_{UVLO}, the device will be turned on, that is, switching being enabled and soft-start sequence being initiated. In addition, the ENA pin features an internal typically 100kΩ pull-low resistor.

Pre-Regulator

This HV regulator is designed to handle input operation range of 4.5V to 15V. The regulator provides low voltage power to supply the internal control circuits and avoid connecting any load from VDDA pin. In noisy environments, a 1µF decoupling capacitor must be connected between VDDA and AGND.

Over-Temperature Protection

An Over-Temperature Protection (OTP) is featured in the device. The protection is triggered to force device shutdown when the junction temperature exceeds 160°C typically. If OTP is set to Hiccup once the junction temperature drops below the hysteresis 20°C typically, the device is re-enabled and automatically reinstated the power-on sequence.

Input Over-Voltage Protection

The device provides an input Over-Voltage Protection (OVP) once the input voltage exceeds 15.5V typically; the OVP function is started and all channels will be turned off after 5ms. The OVP is designed to be auto-recovery, once the input voltage drops below the hysteresis 2V typically, the device is re-enabled and automatically reinstates the power-on sequence. This OVP feature can easily minimize the input overshoot.

Power Good (PGOOD) Control

The power good output is an open-drain output and needs to be connected to a voltage source with a pull-up 4.7kΩ resistor to avoid PGOOD floating. Each channel turns on according to power-on sequence. When the VOUT2 reaches 90% of its target voltage, PMU (Power Management Unit) starts counting t_{PGOOD} = 20ms (Power Good Delay time) then pulls PGOOD Hi until ENA is pulled low or any other protection happens.

Absolute Maximum Ratings (Note 1)

- Analog Base Input Voltage, VIN ---------- –0.3V to 20V
- Control Output Voltage, PGOOD ---------- –0.3V to 6V
- Control Input Voltage, ENA ---------- –0.3V to 15V
- HV-Buck Power Switch (DC), LX1 ---------- –0.3V to 20.5V
  <50ns ---------- –5V to 20.5V
- Other Pins ---------- –0.3V to 6V
- Power Dissipation, P_D @ T_A = 25°C
  WQFN-16L 3x3 ---------- 4.167W
- Package Thermal Resistance (Note 2)
  WQFN-16L 3x3, θ_{JA} ---------- 30°C/W
  WQFN-16L 3x3, θ_{JC} ---------- 7.5°C/W
- Junction Temperature ---------- 150°C
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 4)
  HBM (Human Body Model) ---------- 2kV

Recommended Operating Conditions (Note 4)

- Supply Voltage ---------- 4.5V to 15V
- Supply Voltage (HV-Buck) ---------- 4.5V to 15V
- Supply Voltage (LDO) ---------- 2.7V to 5.5V
- Junction Temperature Range ---------- –40°C to 150°C
- Ambient Temperature Range ---------- –40°C to 125°C

Electrical Characteristics

(Note 5)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
VIN Operation Voltage Range			4.5	--	15	V
Quiescent Current	I_Q	V_{IN} = 5V, HV-Buck and LDO are not switching	500	650	800	μA
Shutdown Current	I_{SHDN}	V_{IN} = 5V, V_{ENA} = 0V, HV-Buck and LDO are both off.	2	7	15	μA
VIN OVP (Hysteresis High)	V_{OVP}		15	15.5	16	V
VIN OVP Hysteresis (Gap)	V_{OVP_HYS}		1.5	2	2.5	V
VIN UVLO	V_{UVLO}		3.8	3.9	4	V
UVLO Hysteresis (Gap)	V_{UVLO_HYS}		0.2	0.3	0.4	V
VDDA Voltage			4.25	4.45	4.65	V
Switching Frequency	f_{SW}		1.8	2	2.2	MHz

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
CH1 HV-Buck						
Output Voltage Range	V_{OUT1}		1.6	--	5	V
Reference Voltage for HV-Buck	V_{REF1}		0.788	0.8	0.812	V
V_{REF1} Under-Voltage Protection Trip Threshold	V_{REF1_UVP}		0.3	0.4	0.5	V
Current Limit	I_{LIM1}	T_A = 25°C	510	600	690	mA
	I_{LIM1_T}	–40°C ≤ T_A ≤ 125°C	450	600	750	
LX1 Low-Side Switch Leakage Current	I_{LK_LX1L}		--	--	5	μA
Load Regulation (Note 6)	ΔV_{LINE}	T_A = 25°C, V_{IN} = 6V, V_{OUT1} = 3.3V, I_{OUT1} = 0mA to 200mA	–1	--	1	%
Line Regulation (Note 6)	ΔV_{LOAD}	T_A = 25°C, V_{IN} = 5V to 15V, V_{OUT1} = 3.3V, I_{OUT1} = 200mA	–1	--	1	%
P-MOSFET On-Resistance	$R_{DS(ON)\_P}$	V_{IN} = 5V, I_{LX1} = 200mA	220	330	470	mΩ
N-MOSFET On-Resistance	$R_{DS(ON)\_N}$	V_{IN} = 5V, I_{LX1} = 200mA	100	150	250	mΩ
Soft-Start Time	t_{SS1}	$V_{OUT1} \geq 0.9 \times V_{Target}$, I_{OUT1} = 0mA	0.7	1	1.3	ms
Discharge Resistance	$R_{DISCHG1}$	V_{IN} = 5V, V_{OUT1} = 3.3V	--	220	--	Ω
CH2 LDO						
Input Voltage for LDO2	PVD2		2.7	--	5.5	V
Output Voltage Range	V_{OUT2}		1	--	3.6	V
Reference Voltage for LDO	V_{REF2}		0.788	0.8	0.812	V
Current Limit	I_{LIM2}	T_A = 25°C	255	300	345	mA
	I_{LIM2_T}	–40°C ≤ T_A ≤ 125°C	210	300	390	
Dropout Voltage (PVD2 – V_{OUT2})	V_{DROP}	I_{OUT2} = 150mA, PVD2 = V_{OUT2} – 0.1V	0.03	--	0.15	V
Line Regulation	ΔV_{LINE}	PVD2 = 3V to 5V, V_{OUT2} = 2.7V, I_{OUT2} = 100mA	0	1	5	mV
Load Regulation	ΔV_{LOAD}	PVD2 = 3.3V, I_{OUT2} = 10mA to 200mA	0	0.1	1	%
V_{REF2} Under-Voltage Protection Trip Threshold	V_{REF2_UVP}		0.2	0.3	0.4	V
Soft-Start Time	t_{SS2}	$V_{OUT2} \geq 0.9 \times V_{Target}$, I_{OUT2} = 0mA	0.7	1	1.3	ms
Discharge Resistance	$R_{DISCHG2}$	PVD2 = 3.3V, V_{OUT2} = 2.7V	--	50	--	Ω
Power Good						
Power Good Pull-Down Voltage	PGOOD	PGOOD current equal to 5mA	--	40	--	mV
Power Good Delay Time	t_{PGOOD}		18	20	22	ms
Control						
ENA Input Voltage	Logic-High	V_{ENA_H}	2	--	--	V
	Logic-Low	V_{ENA_L}	--	--	0.5	

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
ENA Pull Down Resistor	R_{LOW}	V_{IN} = 5V, temperature = –40°C to 125°C.	70	--	140	kΩ

Note 1. Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 2. θ_{JA} is measured under natural convection (still air) at T_A = 25°C with the component mounted on a high effective-thermal-conductivity four-layer test board on a JEDEC 51-7 thermal measurement standard. The first layer is filled with copper. θ_{JC} is measured at the exposed pad of the package.

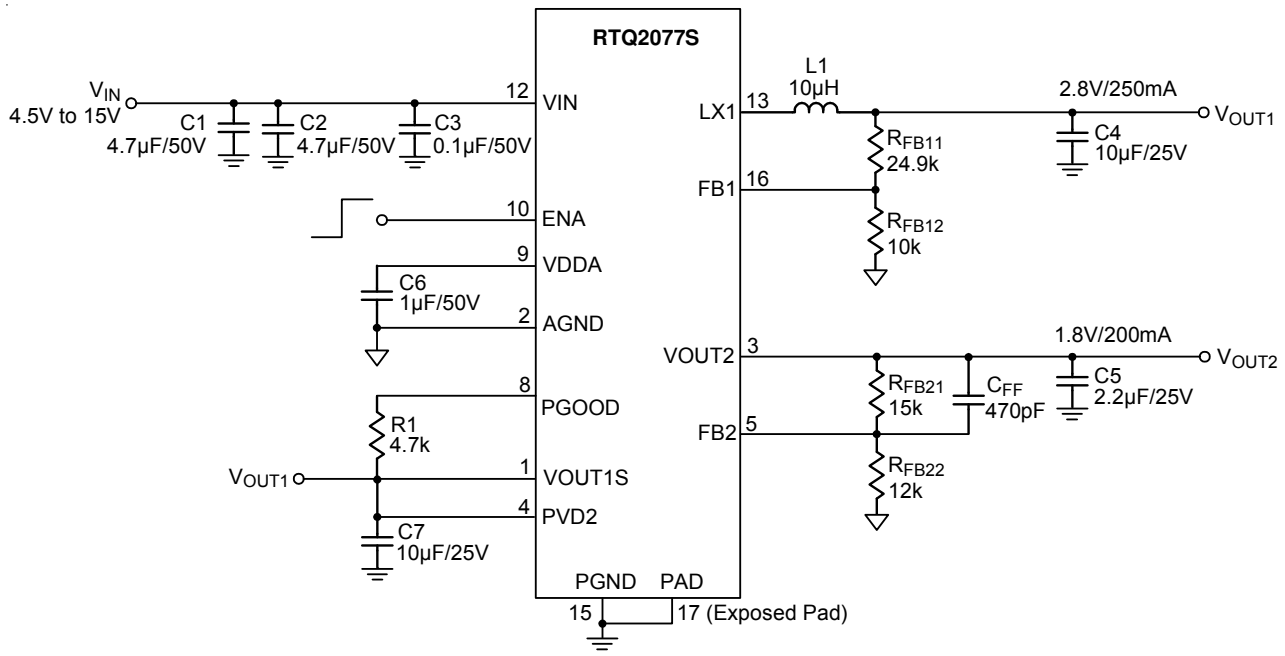
Note 3. Devices are ESD sensitive. Handling precaution is recommended.

Note 4. The device is not guaranteed to function outside its operating conditions.

Note 5. Limits apply to the recommended V_{IN} = 4.5V to 15V, T_A = –40°C to 125°C, unless otherwise noted. Minimum and maximum limits are verified through test, design, or statistical correlation. Typical values represent the most likely parametric norm at T_A = 25°C, and are provided for reference purposes only.

Note 6. Guaranteed by design.

Typical Application Circuit

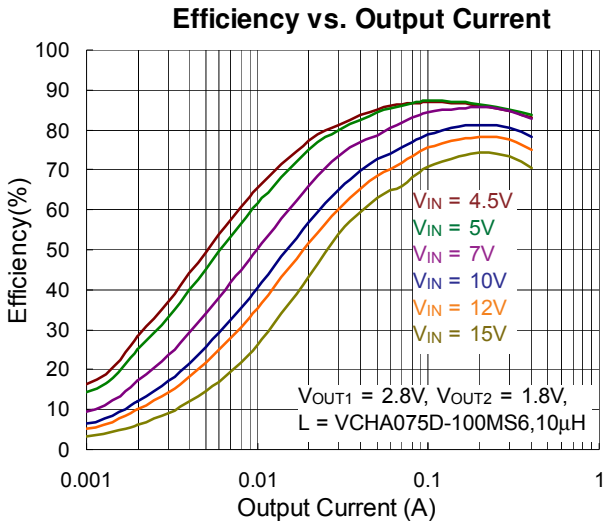


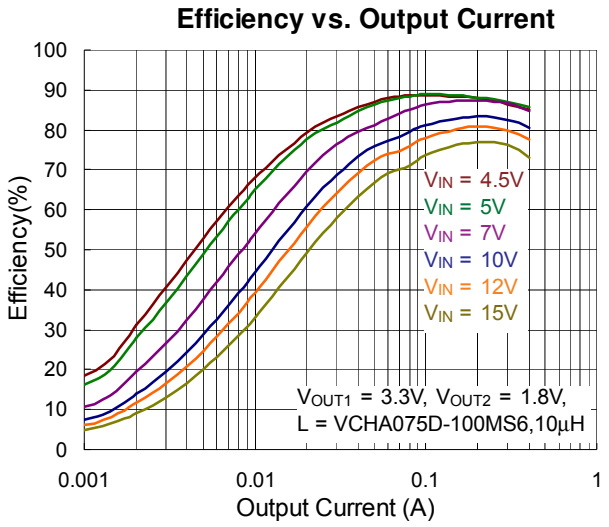
Note : All the input and output capacitors are the suggested values, referring to the effective capacitances, subject to any de-rating effect, like a DC bias.

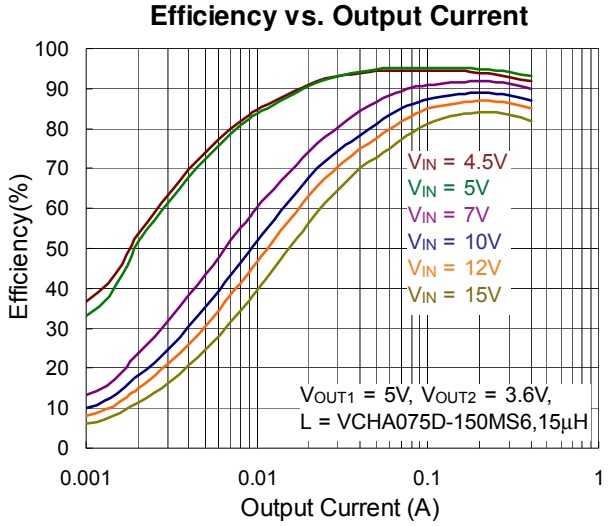
Table 1. Suggested Components for Typical Application Circuit

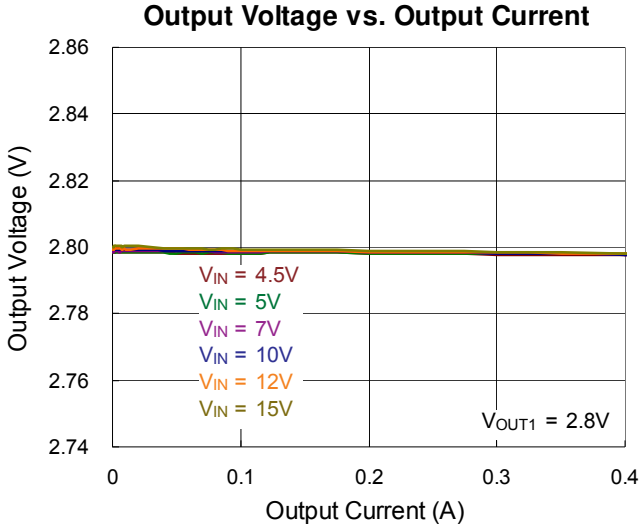
Reference	Q'ty	P/N	Description	Manufacturer
C1, C2	2	GRM31CR71E475KA40	4.7µF/50V/1206/X7R	Murata
C3	1	C1608X7R1H104KT000N	0.1µF/50V/0603/X7R	TDK
C4, C7	1	GRM31CR71E106KA12L	10µF/25V/1206/X7R	Murata
C5	1	C3216X7R1E225KT000N	2.2µF/25V/1206/X7R	TDK
C6	1	UMK107AB7105KA-T	1µF/50V/0603/X7R	Taiyo Yuden
CFF	1	GCM1885C1H470JA16D	470pF/50V/C0G	Murata
R1	1	WR06X4701FTL	4.7k/0603	WALSIN
R_{FB11}	1	WR06X2492FTL	24.9k/0603	WALSIN
R_{FB12}	1	WR06X1002FTL	10k/0603	WALSIN
R_{FB21}	1	WR06X1502FTL	15k/0603	WALSIN
R_{FB22}	1	WR06X1202FTL	12k/0603	WALSIN
L1	1	VCMT063T-100MN5	10µH, DCR = 70.5 mΩ	Cyntec
		VCHA075D-100MS6	10µH, DCR = 38 mΩ	Cyntec
		VCMT063T-150MN5	15µH, DCR = 110 mΩ	Cyntec
		VCHA075D-150MS6	15µH, DCR = 66 mΩ	Cyntec

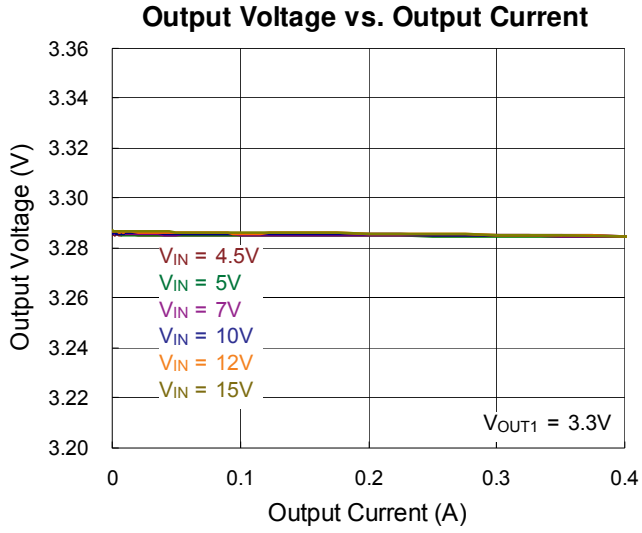
Typical Operating Characteristics

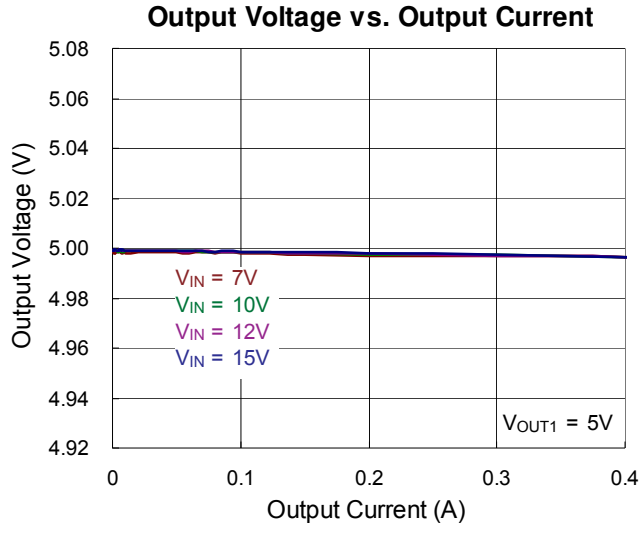




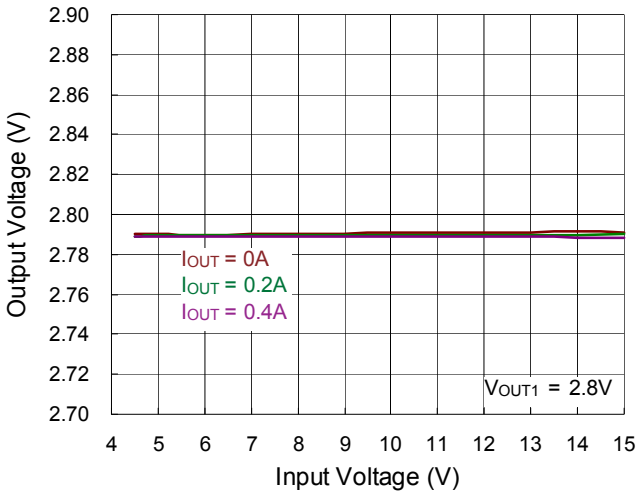




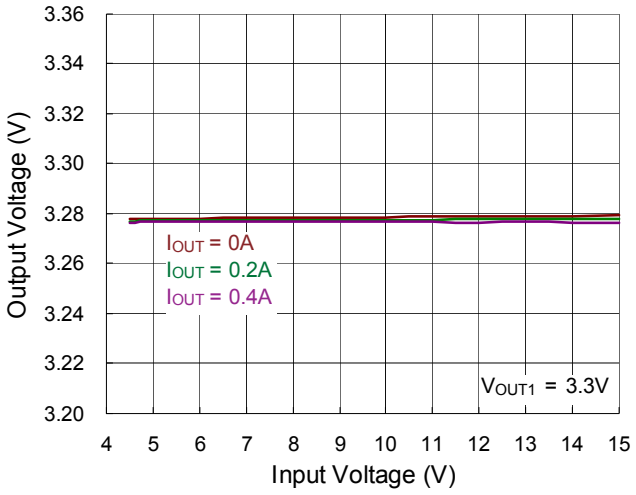




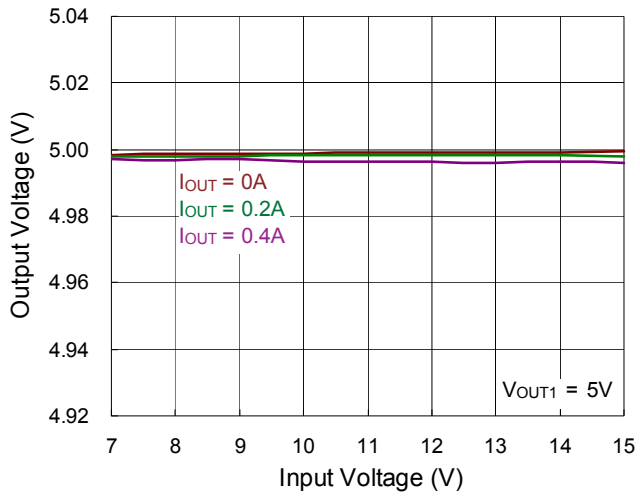
Input Voltage vs. Output Current



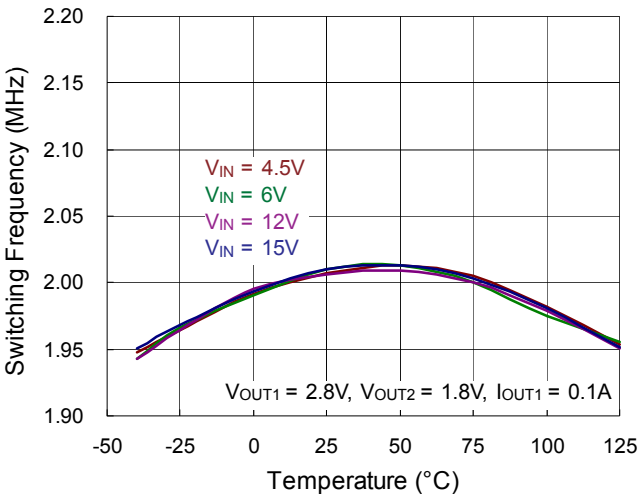
Input Voltage vs. Output Current



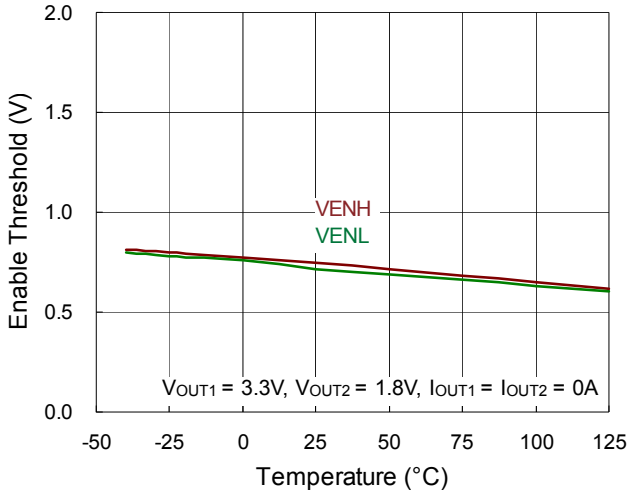
Input Voltage vs. Output Current



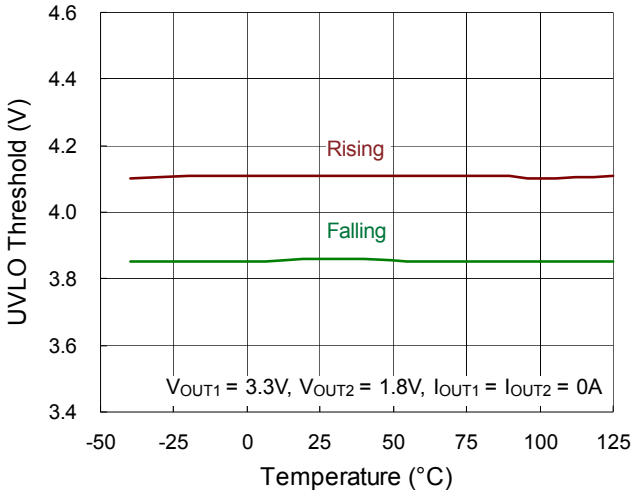
Switching Frequency vs. Temperature



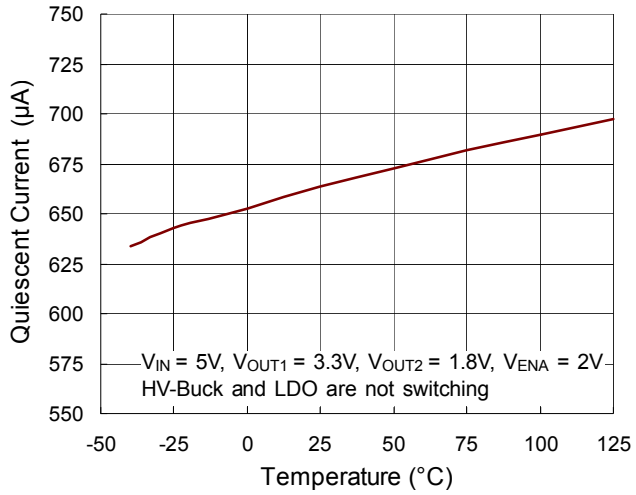
Enable Threshold vs. Temperature



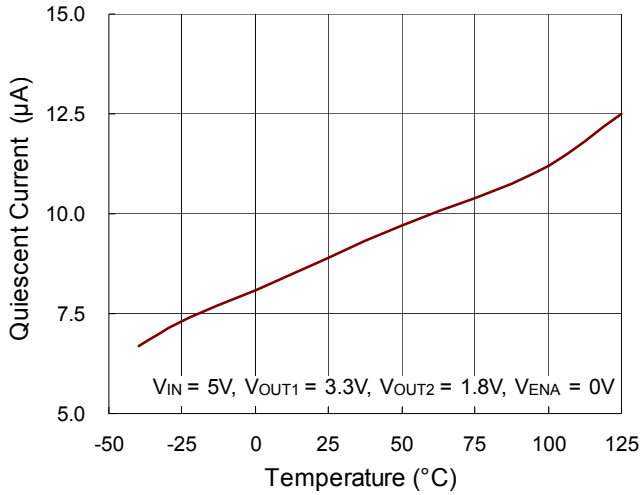
UVLO Threshold vs. Temperature



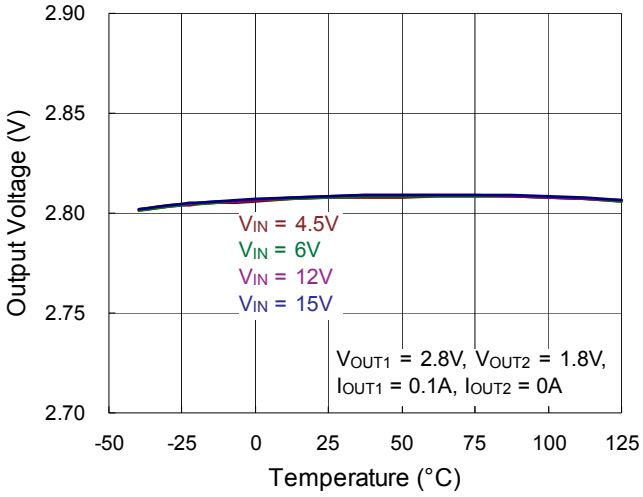
Quiescent Current vs. Temperature



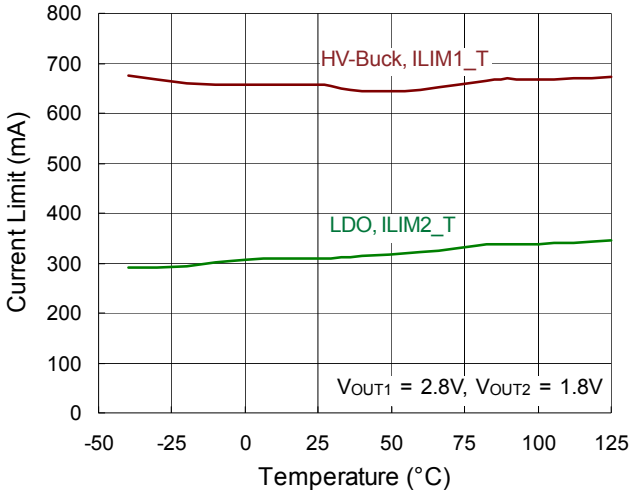
Shutdown Current vs. Temperature



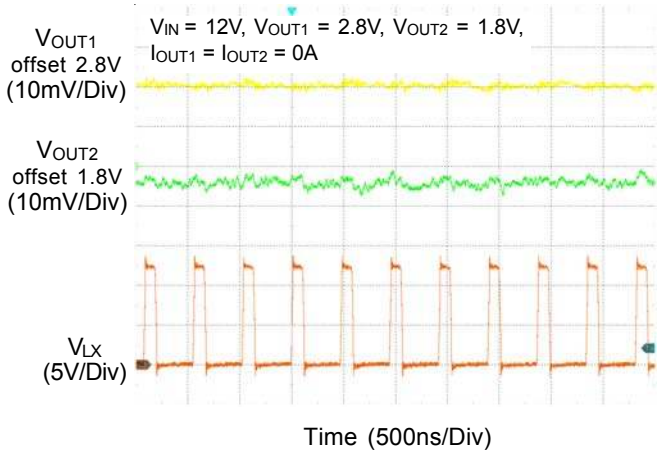
Output Voltage vs. Temperature



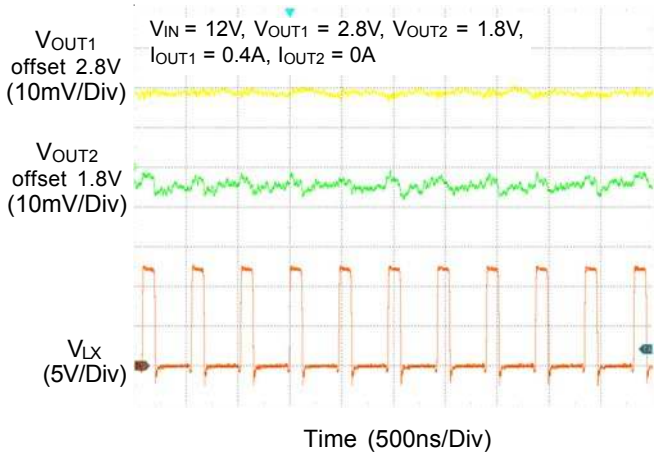
Current Limit vs. Temperature



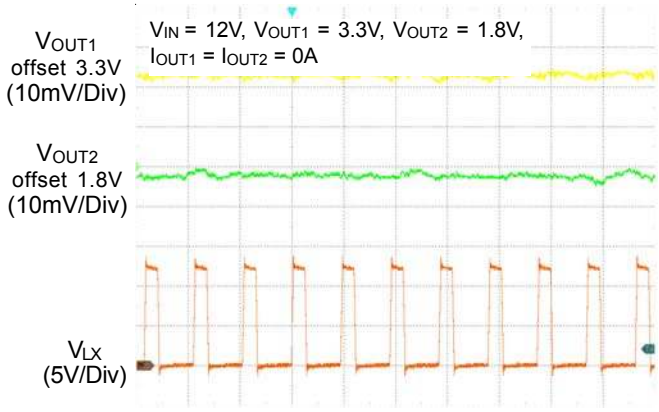
Output Ripple Voltage



Output Ripple Voltage



Output Ripple Voltage



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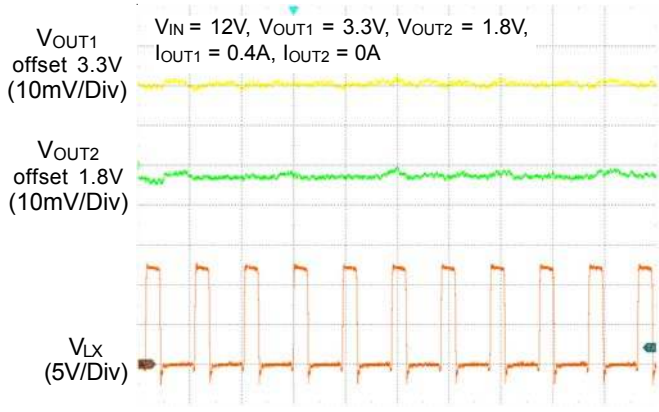
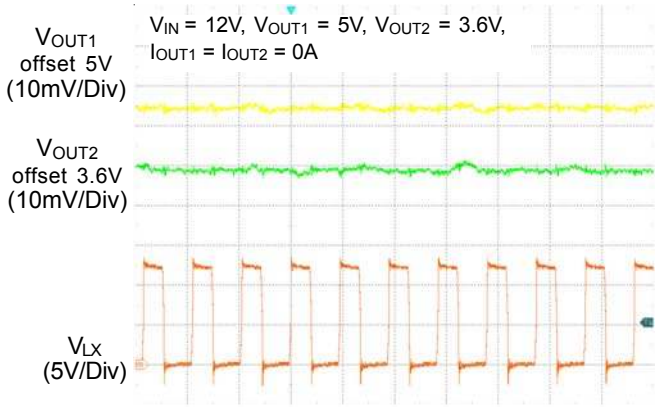
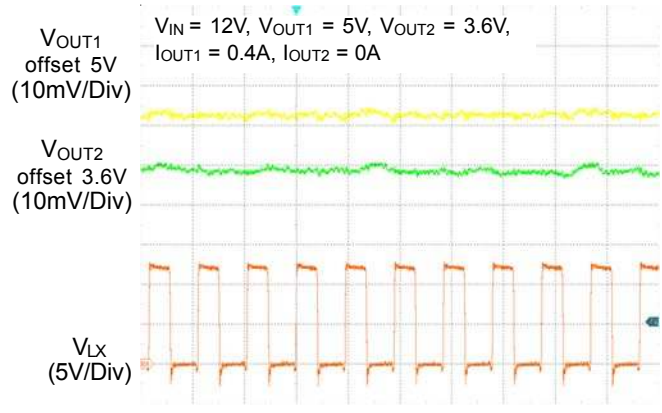


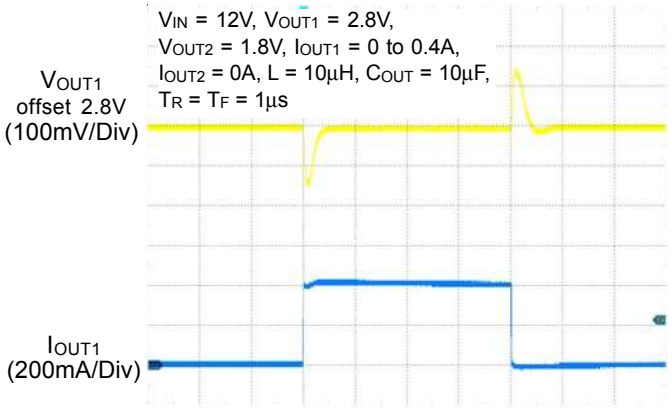
Output Ripple Voltage



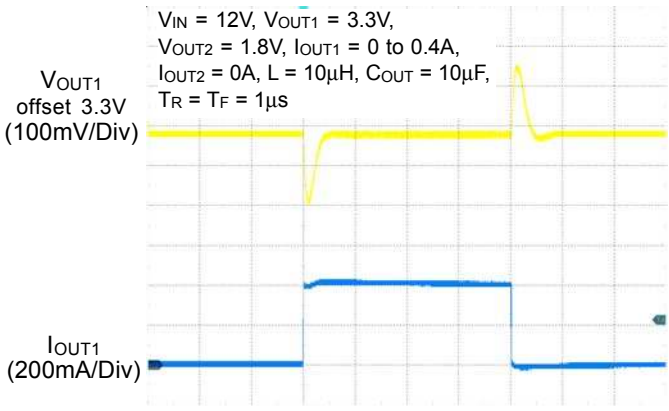
Output Ripple Voltage



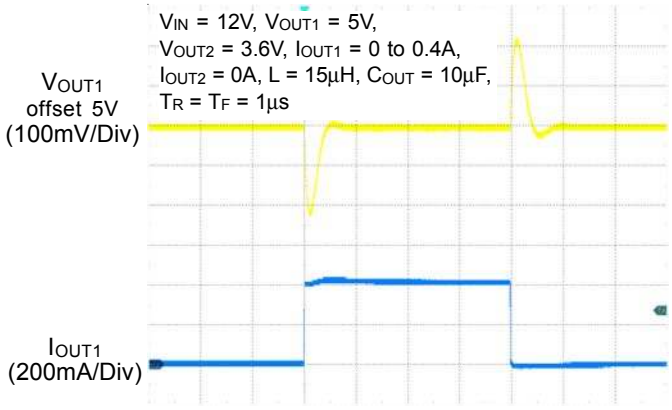
Load Transient Response



Load Transient Response

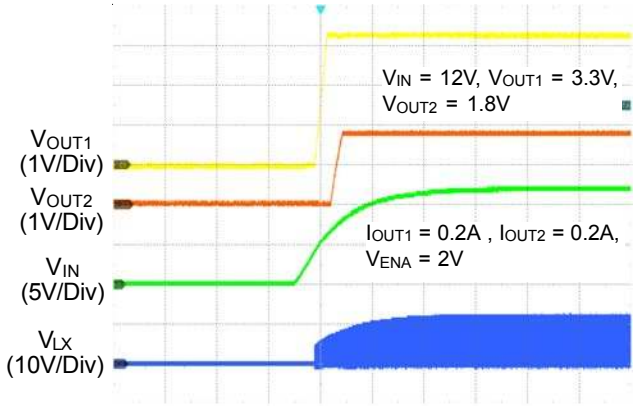


Load Transient Response



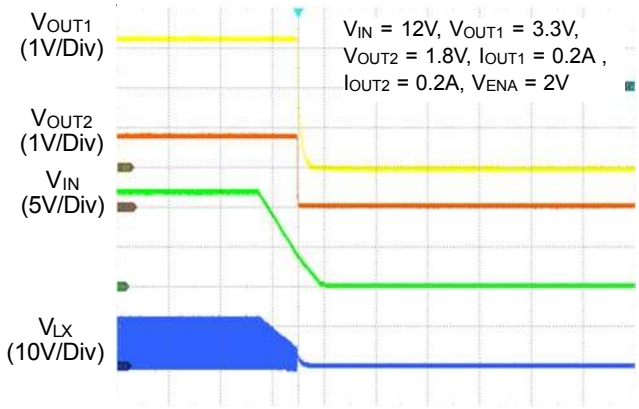
Time (100µs/Div)

Power On from VIN



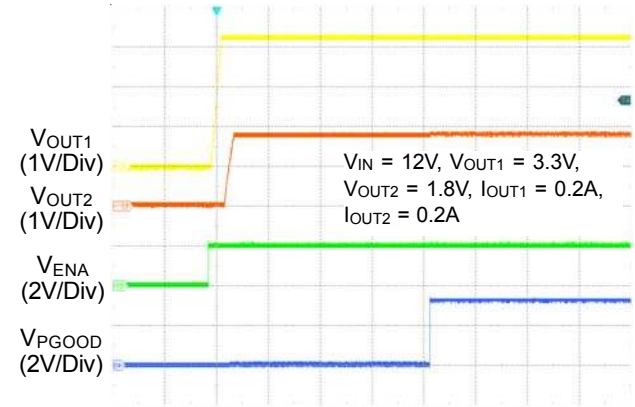
Time (4ms/Div)

Power Off from VIN



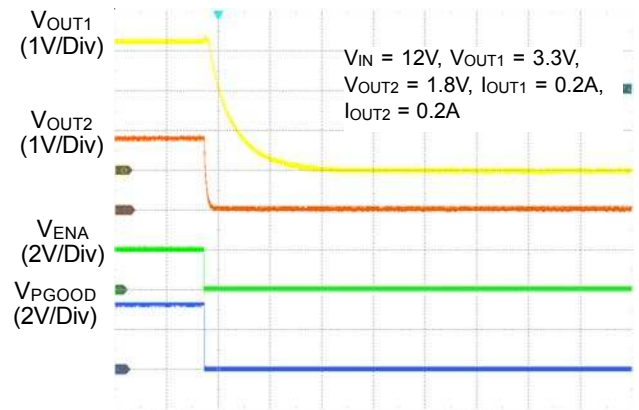
Time (4ms/Div)

Power On from ENA



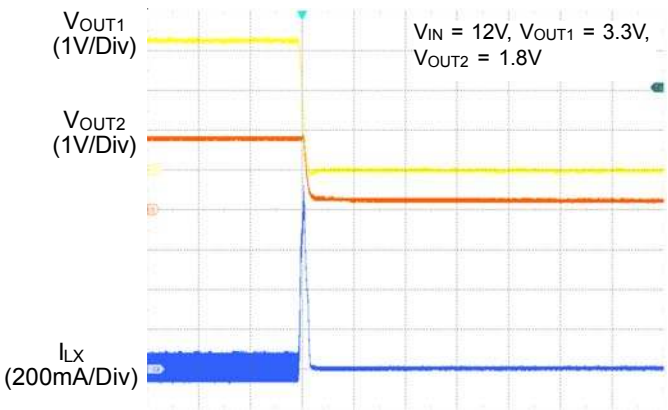
Time (20ms/Div)

Power Off from ENA



Time (500µs/Div)

Latch-Up Behavior



Time (100µs/Div)

Applications Information

A general RTQ2077S application circuit is shown in typical application circuit section. External component selection is largely driven by the load requirement and begins with the selection of application conditions. Next, the inductor L, the input capacitor C_{IN}, and the output capacitor C_{OUT} are chosen. Finally, the remaining external components can be selected for functions such as the enable, PGOOD, inductor peak current limit.

Output Voltage Setting

CH1 : HV Step-Down DC-DC Converter

CH1 is a HV step-down converter for LV DC-DC converter power. The resistive divider allows the FB1 pin to sense a fraction of the output voltage as shown in Figure 1.

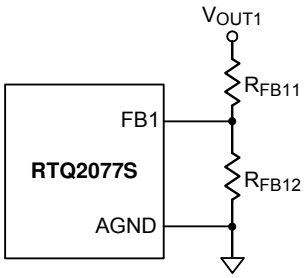


Figure 1. Output Voltage Setting for CH1

The current-mode PWM converter with integrated internal MOSFETs and compensation network operates at fixed frequency. The output voltage of CH1 is set by external feedback resistors, as expressed in the following equation :

$$V_{OUT1} = V_{FB1} \times \left(1 + \frac{R_{FB11}}{R_{FB12}}\right)$$

Where V_{FB1} is 0.8V typically and suggested value for R_{FB11} is 10k to 500k.

CH2 : LDO

CH2 is a low-dropout (LDO) voltage regulator which offers benefits of high input voltage and low-dropout voltage for sensor power. The resistive divider allows the FB2 pin to sense a fraction of the output voltage as shown in Figure 2.

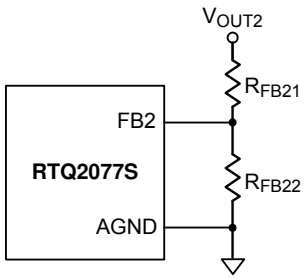


Figure 2. Output Voltage Setting for CH2

The output voltage of CH2 is set by external feedback resistors, as expressed in the following equation :

$$V_{OUT2} = V_{FB2} \times \left(1 + \frac{R_{FB21}}{R_{FB22}}\right)$$

Where V_{FB2} is 0.8V typically and suggested value for R_{FB21} is 5k to 500k.

Inductor Selection

The inductor selection trade-offs among size, cost, efficiency, and transient response requirements. Generally, three key inductor parameters are specified for operation with the device: inductance value (L), inductor saturation current (I_{SAT}), and DC resistance (DCR).

A good compromise between size and loss is a 30% peak-to-peak ripple current to the IC rated current. The switching frequency, input voltage, output voltage, and selected inductor ripple current determines the inductor value as follows :

$$L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times f_{SW} \times \Delta I_L}$$

Larger inductance values result in lower output ripple voltage and higher efficiency, but a slightly degraded transient response. This result in additional phase lag in the loop and reduce the crossover frequency. As the ratio of the slope-compensation ramp to the sensed-current ramp increases, the current-mode system tilts towards voltage-mode control. Lower inductance values allow for smaller case size, but the increased ripple lowers the effective current limit threshold, increases the AC losses in the inductor and may trigger low-side switch sinking current limit. It also causes insufficient slope compensation and ultimately loop instability as duty cycle approaches or exceeds 50%. When duty cycle exceeds

50%, below condition needs to be satisfied :

$$2.1\times f_{SW} > \frac{V_{OUT}}{L}$$

A good compromise among size, efficiency, and transient response can be achieved by setting an inductor current ripple (ΔI_L) with about 10% to 50% of the maximum rated output current (400mA).

To enhance the efficiency, choose a low-loss inductor having the lowest possible DC resistance that fits in the allotted dimensions. The inductor value determines not only the ripple current but also the load-current value at which DCM/CCM switchover occurs. The inductor selected should have a saturation current rating greater than the peak current limit of the device. The core must be large enough not to saturate at the peak inductor current (I_{L_PEAK}) :

$$\Delta I_L = \frac{V_{OUT}\times(V_{IN}-V_{OUT})}{V_{IN}\times f_{SW}\times L}$$

$$I_{L\_PEAK} = I_{OUT\_MAX} + \frac{1}{2}\Delta I_L$$

The current flowing through the inductor is the inductor ripple current plus the output current. During power up, faults or transient load conditions, the inductor current can increase above the calculated peak inductor current level calculated above. In transient conditions, the inductor current can increase up to the switch current limit of the device. For this reason, the most conservative approach is to specify an inductor with a saturation current rating equal to or greater than the switch current limit rather than the peak inductor current. It is recommended to use shielded inductors for good EMI performance.

Input Capacitor Selection

Input capacitance, C_{IN}, is needed to filter the pulsating current at the drain of the high-side power MOSFET. C_{IN} should be sized to do this without causing a large variation in input voltage. The peak-to-peak voltage ripple on input capacitor can be estimated as equation below :

$$\Delta V_{CIN} = D\times I_{OUT}\times\frac{1-D}{C_{IN}\times f_{SW}} + ESR\times I_{OUT}$$

where

$$D = \frac{V_{OUT}}{V_{IN}\times\eta}$$

Figure 3 shows the C_{IN} ripple current flowing through the input capacitors and the resulting voltage ripple across the capacitors. For ceramic capacitors, the equivalent series resistance (ESR) is very low, the ripple which is caused by ESR can be ignored, and the minimum value of effective input capacitance can be estimated as equation below :

$$C_{IN\_MIN} = I_{OUT\_MAX}\times\frac{D(1-D)}{\Delta V_{CIN\_MAX}\times f_{SW}}$$

Where $\Delta V_{CIN\_MAX} \le 200mV$

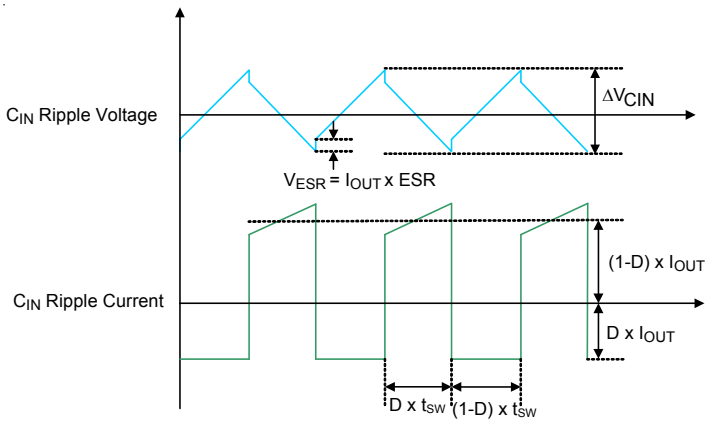


Figure 3. C_{IN} Ripple Voltage and Ripple Current

In addition, the input capacitor needs to have a very low ESR and must be rated to handle the worst-case RMS input current. The RMS ripple current (I_{RMS}) of the regulator can be determined by the input voltage (V_{IN}), output voltage (V_{OUT}), and rated output current (I_{OUT}) as the following equation :

$$I_{RMS} \cong I_{OUT\_MAX}\times\frac{V_{OUT}}{V_{IN}}\times\sqrt{\frac{V_{IN}}{V_{OUT}}-1}$$

From the above, the maximum RMS input ripple current occurs at maximum output load, which will be used as the requirements to consider the current capabilities of the input capacitors. The maximum ripple voltage usually occurs at 50% duty cycle, that is, V_{IN} = 2 x V_{OUT}. It is commonly to use the worse $I_{RMS} \cong 0.5 \times I_{OUT\_MAX}$ at V_{IN} = 2 x V_{OUT} for design. Note that ripple current ratings from capacitor manufacturers are often based on only 2000 hours of life which makes it advisable to further de-rate the capacitor, or choose a capacitor rated at a higher temperature than required.

Several capacitors may also be paralleled to meet size, height and thermal requirements in the design. For low

input voltage applications, sufficient bulk input capacitance is needed to minimize transient effects during output load changes.

Ceramic capacitors are ideal for switching regulator applications due to its small, robust and very low ESR. However, care must be taken when these capacitors are used at the input. A ceramic input capacitor combined with trace or cable inductance forms a high quality (under damped) tank circuit. If the RTQ2077S circuit is plugged into a live supply, the input voltage can ring to twice its nominal value, possibly exceeding the device's rating. This situation is easily avoided by placing the low ESR ceramic input capacitor in parallel with a bulk capacitor with higher ESR to damp the voltage ringing.

The input capacitor should be placed as close as possible to the VIN pin, with a low inductance connection to the PGND of the IC. It is recommended to connect a 4.7μF, X7R capacitors between VIN pin to PGND pin for 2MHz switching frequency. The larger input capacitance is required when a lower switching frequency is used. For filtering high frequency noise, additional small capacitor 0.1μF should be placed close to the part and the capacitor should be 0402 or 0603 in size. X7R capacitors are recommended for best performance across temperature and input voltage variations.

Output Capacitor Selection

The selection of C_{OUT} is determined by considering to satisfy the voltage ripple and the transient loads. The peak-to-peak output ripple, ΔV_{OUT}, is determined by :

$$\Delta V_{OUT} \leq \Delta I_L \left(ESR + \frac{1}{8 \times f_{SW} \times C_{OUT}} \right)$$

Where the ΔI_L is the peak-to-peak inductor ripple current. The output ripple is highest at maximum input voltage since ΔI_L increases with input voltage. Multiple capacitors placed in parallel may be needed to meet the ESR and RMS current handling requirements.

Regarding to the transient loads, the V_{SAG} and V_{SOAR} requirement should be taken into consideration for choosing the effective output capacitance value. The amount of output sag/soar is a function of the crossover frequency factor at PWM, which can be calculated from below.

$$V_{SAG} = V_{SOAR} = \frac{\Delta I_{OUT}}{2 \times \pi \times C_{OUT} \times f_C}$$

Ceramic capacitors have very low equivalent series resistance (ESR) and provide the best ripple performance. The recommended dielectric type of the capacitor is X7R best performance across temperature and input voltage variations. The variation of the capacitance value with temperature, DC bias voltage and switching frequency needs to be taken into consideration. For example, the capacitance value of a capacitor decreases as the DC bias across the capacitor increases. Be careful to consider the voltage coefficient of ceramic capacitors when choosing the value and case size. Most ceramic capacitors lose 50% or more of their rated value when used near their rated voltage.

Transient performance can be improved with a higher value output capacitor. Increasing the output capacitance will also decrease the output voltage ripple.

EN Pin for Start-Up and Shutdown Operation

For automatic start-up, the ENA pin, with high-voltage rating, can be connected to the input supply V_{IN} directly. The large built-in hysteresis band makes the ENA pin useful for simple delay and timing circuits. The ENA pin can be externally connected to V_{IN} by adding a resistor R_{ENA} and a capacitor C_{ENA}, as shown in Figure 4, to have an additional delay. The time delay can be calculated with the ENA's internal threshold, at which switching operation begins (Minimum V_{ENA_H} is 2V).

An external MOSFET can be added for the ENA pin to be logic-controlled, as shown in Figure 5. In this case, a pull-up resistor, R_{ENA}, is connected between VIN and the ENA pin. The MOSFET Q1 will be under logic control to pull down the ENA pin. To prevent the device being enabled when V_{IN} is smaller than the V_{OUT} target level or some other desired voltage level, a resistive divider (R_{ENA1} and R_{ENA2}) can be used to externally set the input under-voltage lockout threshold, as shown in Figure 6.

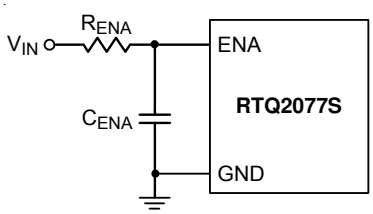


Figure 4. Enable Timing Control

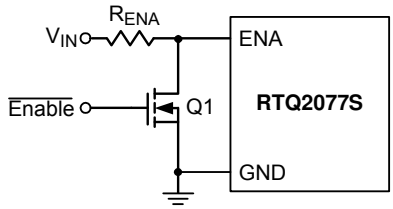


Figure 5. Logic Control for the ENA Pin

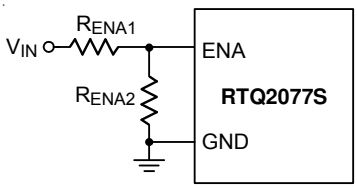


Figure 6. Resistive Divider for Under-Voltage Lockout Threshold Setting

Power-Good Output

The PGOOD pin is an open-drain power-good indication output and is to be connected to an external voltage source through a pull-up resistor.

The external voltage source can be an external voltage supply below 5.5V, VDDA or the output of the RTQ2077S if the output voltage is regulated under 5.5V. It is recommended to connect a 4.7kΩ between external voltage source to PGOOD pin.

Under-Voltage Protection

The RTQ2077S provides under-voltage protection (UVP) with hiccup mode. When the FB voltage drops below 50% of the reference voltage V_{REF}, the UVP function will be triggered to shut down switching operation. If the UVP condition remains for a period, the RTQ2077S will automatically attempt to restart. When the UVP condition is removed, the converter will resume normal operation. The UVP is disabled during soft-start.

Over-Temperature Protection

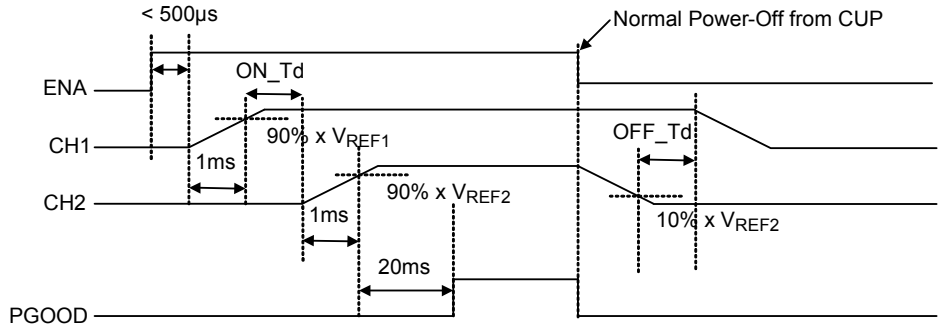
The RTQ2077S features over-temperature protection (OTP) to prevent the device from being overheated due to excessive power dissipation. The OTP will shut down switching operation when the junction temperature exceeds 160°C. Once the junction temperature cools down by approximately 20°C, the converter will resume normal operation. To maintain continuous operation, the junction temperature should never exceed 150°C.

Soft-Start

The RTQ2077S provides internal soft-start function. The soft-start function is used to prevent large inrush current while the converter is being powered-up. For the RTQ2077S, the fixed soft-start time is 1ms. The FB voltage will track the internal ramp voltage during soft-start.

Power-On/Off Sequence

In the RTQ2077S, the HV-Buck (CH1) always firstly turns on and then turns on the LDO (CH2). The off sequence will follow first-on-last-off rule to turn off channels.



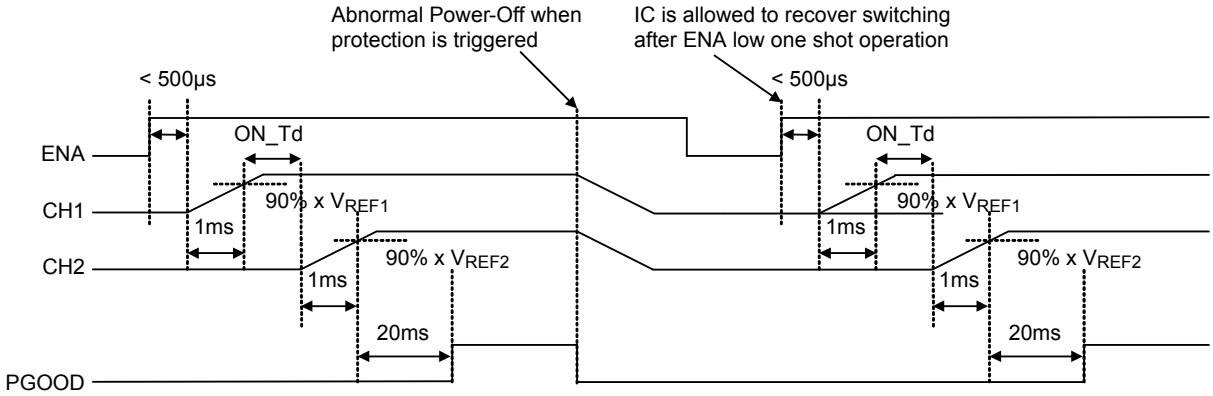
Note : ON_Td is 400µs and OFF_Td is 0s.

Figure 7. Normally Power-On/Off Sequence

Abnormal Off

When the abnormal event occurs, all channels turns off immediately.

If users want to turn on again, users must pull ENA low to reset state then pull high to turn on again.



Note : ON_Td is 400µs and OFF_Td is 0s.

Figure 8. Protection for Abnormal Off : Each Channel Shutdown at the Same Time

When output channel take time to discharge over 64ms and ENA keep low level, all channels turn off at 64ms after starting Power-Off Sequence.

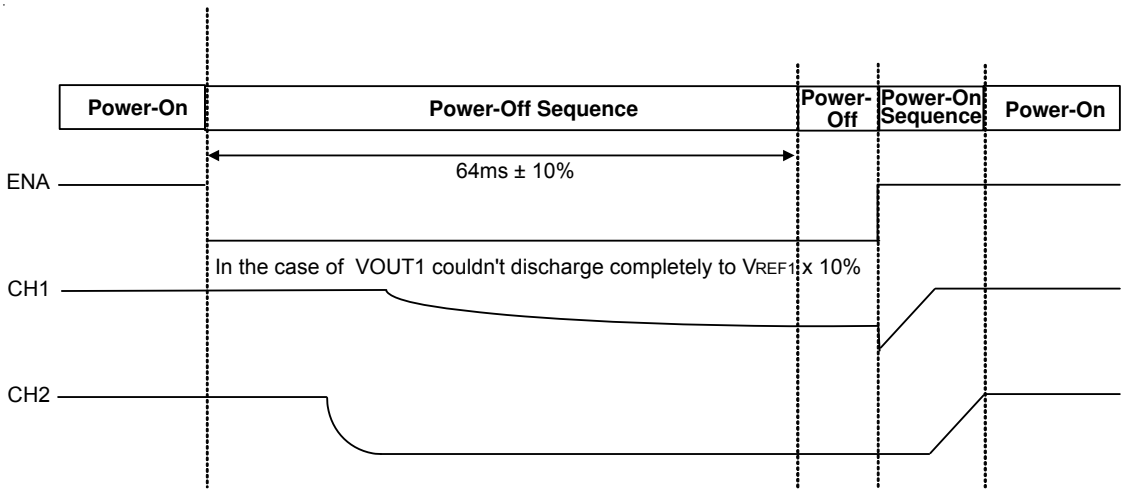


Figure 9. Protection for Abnormal Off : CH1 Take Time to Discharge Over 64ms and ENA Keep Low Level

When output channel take time to discharge over 64ms and ENA goes high level at 64ms after starting Power-Off Sequence, the RTQ2077S re-start immediately.

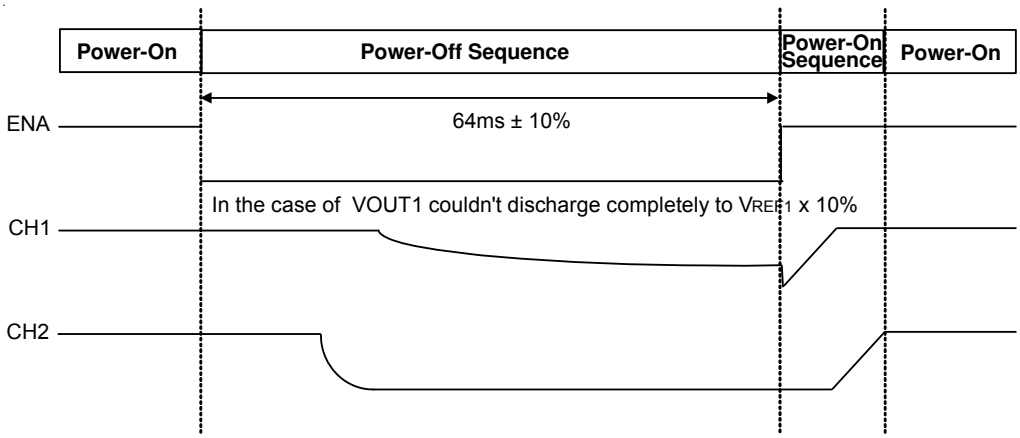


Figure 10. Protection for Abnormal Off : CH1 Take Time to Discharge Over 64ms and ENA goes High Level at 64ms after Starting Power-Off Sequence

When output channel take time to discharge over 64ms and ENA keep high level at Power-Off Sequence, the RTQ2077S re-start immediately.

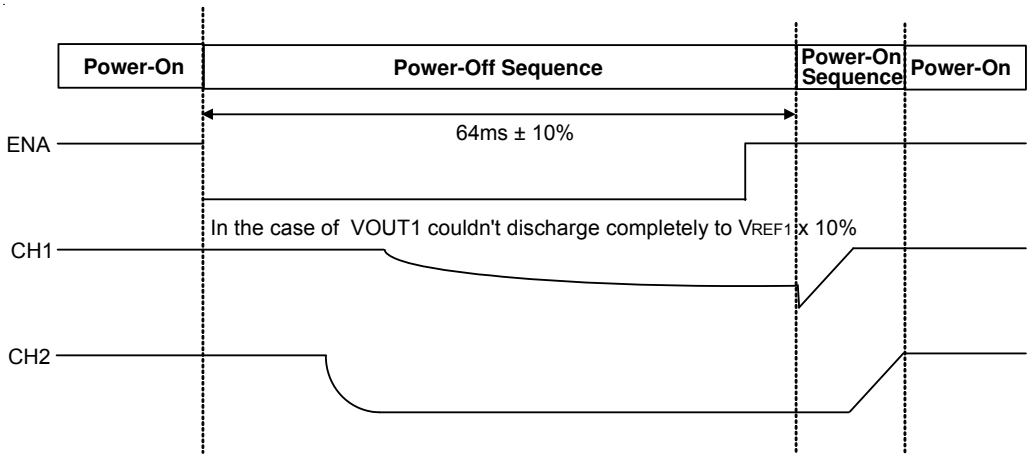


Figure 11. Protection for Abnormal Off : CH1 Take Time to Discharge Over 64ms and ENA goes High Level at Power-Off Sequence

Protections List

	Protection Type	Threshold (Typical Value)	Mask Time	Protection Method	Reset Method
VIN	UVLO	V_{IN} < 3.9V	32µs	Disable all channels	Latch-off protection, restart if V_{IN} > 4.4V and ENA = Hi
	OVP	V_{IN} > 15.5V	5ms	Disable all channels	Latch-off protection, restart if V_{IN} < 13.5V, VDDA < 1.6V or ENA = low
CH1 HV-Buck	OCP	Inductor current peak value > 0.6A	4ms	Cycle-by-cycle detection then disable all channels	Latch-off protection, VDDA < 1.6V or ENA = low
	UVP	CH1 UVP : VOUT1 < VOUT1 x 0.5 (50%)	N/A	Disable all channels	Latch-off protection, restart if VDDA < 1.6V or ENA = low
	VOUT1 OVP	V_{OUT1} > 5.5V	N/A	Disable all channels	Hiccup Until fail event to be dissolved
CH2 LDO	OCP	P-MOSFET current > 0.3A	4ms	Disable all channels	Latch-off protection, VDDA < 1.6V or ENA = low
	UVP	CH2 UVP : VOUT2 < VOUT2 x 0.4 (40%)	N/A	Disable all channels	Latch-off protection, VDDA < 1.6V or ENA = low
Thermal	Thermal shutdown	Temperature > 160°C	N/A	Disable all channels	Latch-off protection, ENA = high and temperature < 140°C

Thermal Consideration

In many applications, the RTQ2077S does not generate much heat due to its high efficiency and low thermal resistance of its WQFN- 16L 3x3 package.

However, in applications in which the RTQ2077S is running at a high ambient temperature and high input voltage or high switching frequency, the generated heat may exceed the maximum junction temperature of the part.

The junction temperature should never exceed the absolute maximum junction temperature $T_{J(MAX)}$, listed under Absolute Maximum Ratings, to avoid permanent damage to the device. If the junction temperature reaches approximately 160°C, the RTQ2077S a stop switching the power MOSFETs until the temperature drops about 20°C cooler.

The maximum power dissipation can be calculated by the following formula :

$$P_{D(MAX)} = \left(T_{J(MAX)} - T_A\right) / \theta_{JA(EFFECTIVE)}$$

where $T_{J(MAX)}$ is the maximum allowed junction temperature of the die. For recommended operating condition specifications, the maximum junction temperature is 150°C. T_A is the ambient operating temperature, $\theta_{JA(EFFECTIVE)}$ is the system-level junction to ambient thermal resistance. It can be estimated from thermal modeling or measurements in the system.

The device thermal resistance depends strongly on the surrounding PCB layout and can be improved by providing a heat sink of surrounding copper ground. The addition of backside copper with thermal vias, stiffeners, and other enhancements can also help reduce thermal resistance.

Experiments in the Richtek thermal lab show that simply set $\theta_{JA(EFFECTIVE)}$ as 110% to 120% of the θ_{JA} is reasonable to obtain the allowed $P_{D(MAX)}$.

As an example, consider the case when the RTQ2077S is used in applications where V_{IN} = 12V, I_{OUT} = 0.4A, f_{SW} = 2000kHz, V_{OUT} = 5V. The efficiency at 5V, 0.4A is 84.9% by using Cyntec- VCHA075D-150MS6 (15µH,66mΩ DCR) as the inductor and measured at room temperature. The core loss can be obtained from its website of 20.5mW in this case. In this case, the power dissipation of the RTQ2077S is

$$P_{D,\,RT} = \frac{1-\eta}{\eta} \times P_{OUT} - \left(I_O^2 \times DCR + P_{CORE}\right) = 0.333W$$

Considering the $\theta_{JA(EFFECTIVE)}$ is 30°C/W by using the RTQ2077S evaluation board with 4 layers PCB, 1 OZ. Cu, the junction temperature of the regulator operating in a 25°C ambient temperature is approximately :

T_J = 0.333W x 30°C/W + 25C = 35°C

Figure 12 shows the RTQ2077S $R_{DS(ON)}$ versus different junction temperature. If the application calls for a higher ambient temperature, we might recalculate the device power dissipation and the junction temperature based on a higher $R_{DS(ON)}$ since it increases with temperature.

Using 105°C ambient temperature as an example, the change of the equivalent $R_{DS(ON)}$ can be obtained from Figure 12 and yields a new power dissipation of 0.343W.

Therefore, the estimated new junction temperature is

T_J' = 0.343W x 30°C/W + 105°C = 115.3°C

If the application calls for a higher ambient temperature and may exceed the recommended maximum junction temperature of 150°C, care should be taken to reduce the temperature rise of the part by using a heat sink or air flow. Note that the over temperature protection is intended to protect the device during momentary overload conditions. The protection is activated outside of the absolute maximum range of operation as a secondary failsafe and therefore should not be relied upon operationally.

Continuous operation above the specified absolute maximum operating junction temperature may impair device reliability or permanently damage the device.

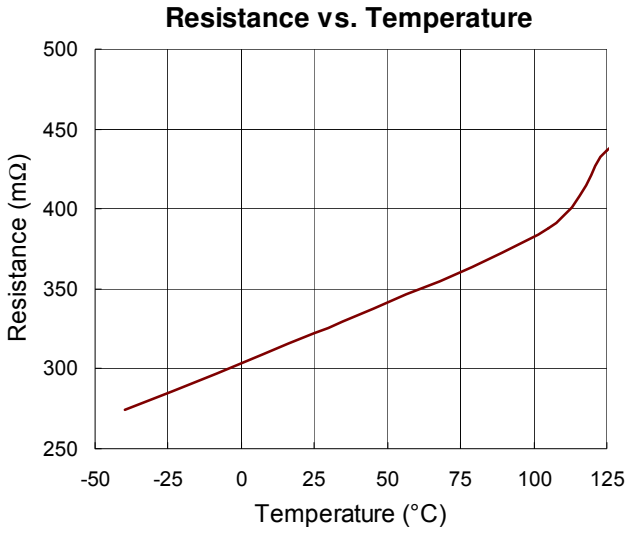


Figure 12. RTQ2077S $R_{DS(ON)}$ vs. Temperature

Layout Considerations

When laying out the printed circuit board, the following checklist should be used to ensure proper operation of the RTQ2077S :

- Four-layer or six-layer PCB with maximum ground plane is strongly recommended for good thermal performance.
- Keep the traces of the main current paths wide and short.
- Place high frequency decoupling capacitor C3 as close as possible to the IC to reduce the loop impedance and minimize switch node ringing.
- Place the VDDA decoupling capacitor, C6, as close to VDDA pin as possible.
- Routing the trace with width of 20mil or wider.
- Place multiple vias under the device near VIN and PGND and near input capacitors to reduce parasitic inductance and improve thermal performance. To keep thermal resistance low, extend the ground plane as much as possible, and add thermal vias under and near the
- The RTQ2077S to additional ground planes within the circuit board and on the bottom side.
- Reducing the area size of the LX1 exposed copper to reduce the electrically coupling from this voltage.
- Connect the feedback sense network behind via of output capacitor.
- Place the feedback components R_{FB11} / R_{FB12} / R_{FB21}/ R_{FB22} / C_{FF} near the IC.
- Connect all analog grounds to common node and then connect the common node to the power ground with a single point.

Figure 13 is the layout example which uses 70mm x 50mm, four-layer PCB with 1 OZ. Cu.

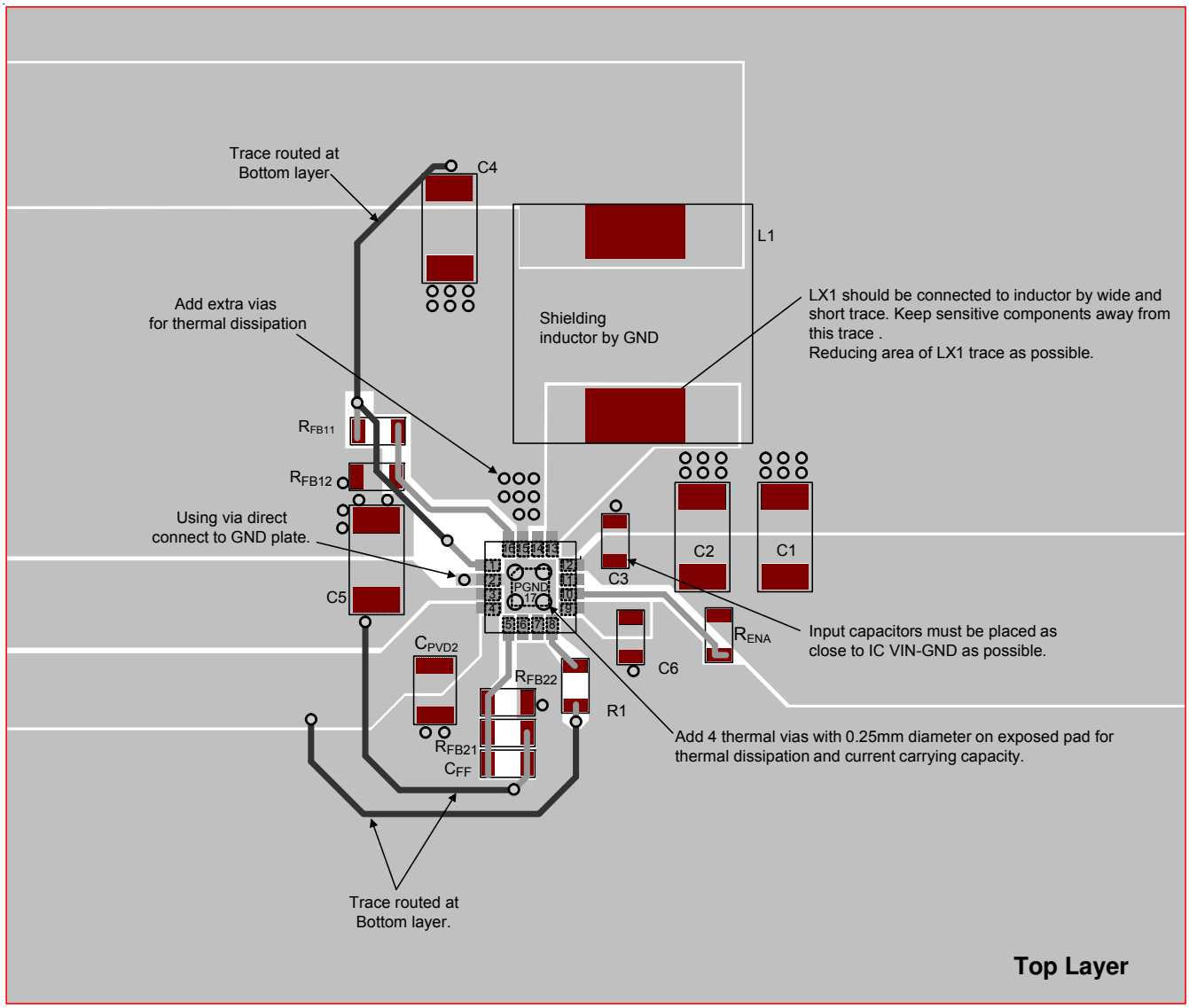
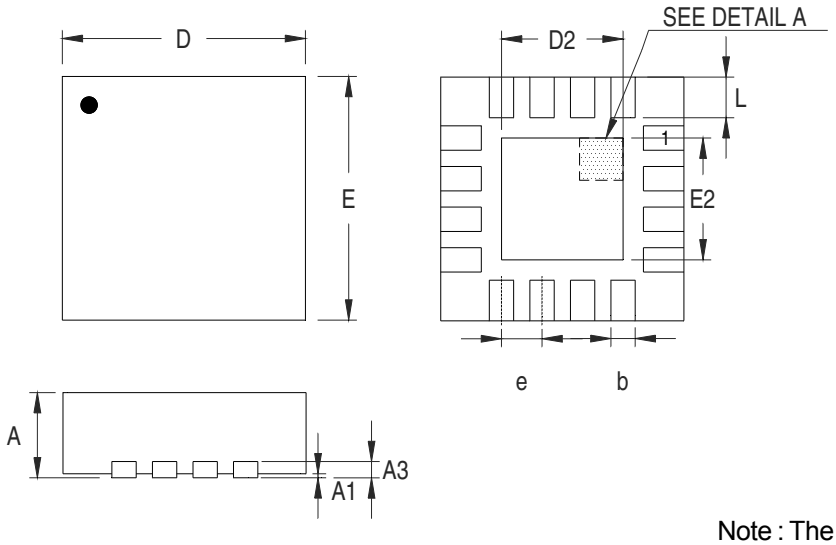
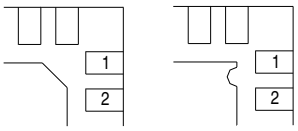


Figure 13. PCB Layout Guide

Outline Dimension





DETAIL A

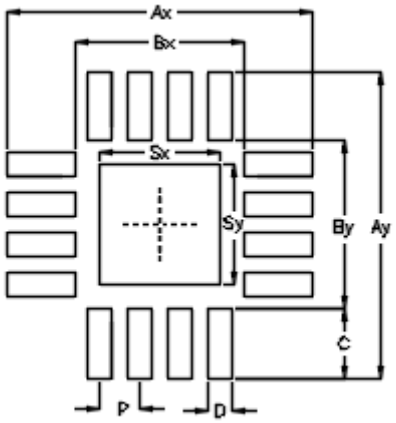
Pin #1 ID and Tie Bar Mark Options

Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010
b	0.180	0.300	0.007	0.012
D	2.950	3.050	0.116	0.120
D2	1.300	1.750	0.051	0.069
E	2.950	3.050	0.116	0.120
E2	1.300	1.750	0.051	0.069
e	0.500		0.020	
L	0.350	0.450	0.014	0.018

W-Type 16L QFN 3x3 Package

Footprint Information



Package	Number of Pin	Footprint Dimension (mm)									Tolerance
		P	Ax	Ay	Bx	By	C	D	Sx	Sy	
V/W/U/XQFN3*3-16	16	0.50	3.80	3.80	2.10	2.10	0.85	0.30	1.50	1.50	±0.05

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