Rochester Electronics®

Datasheet

AM29C821A/BLA

High-Performance CMOS Bus Interface Registers

The Am29C821A and Am29C82311 CMOS Bus Interface Registers are designed to eliminate the extra devices required to buffer stand alone registers and to provide extra data width for wider address/data paths or buses carrying parity.

Rochester Electronics Manufactured Components

Rochester branded components are manufactured using either die/wafers purchased from the original suppliers or Rochester wafers recreated from the original IP. All re-creations are done with the approval of the Original Component Manufacturer (OCM).

Parts are tested using original factory test programs or Rochester developed test solutions to guarantee product meets or exceeds the OCM data sheet.

Quality Overview

- ISO-9001
- AS9120 certification
- Qualified Manufacturers List (QML) MIL-PRF-35835
    - Class Q Military
    - Class V Space Level
- Qualified Suppliers List of Distributors (QSLD)
    - Rochester is a critical supplier to DLA and meets all industry and DLA standards.

Rochester Electronics, LLC is committed to supplying products that satisfy customer expectations for quality and are equal to those originally supplied by industry manufacturers.

The original manufacturer's datasheet accompanying this document reflects the performance and specifications of the Rochester manufactured version of this device. Rochester Electronics guarantees the performance of its semiconductor products to the original OCM specifications. 'Typical' values are for reference purposes only. Certain minimum or maximum ratings may be based on product characterization, design, simulation, or sample testing.

FOR REFERENCE ONLY

Am29C821A/Am29C823A

High-Performance CMOS Bus Interface Registers

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- **Proprietary edge-rate controlled outputs dramatically reduce undershoots, overshoots and ground bounce**
- **High-speed parallel positive edge-triggered registers with D-type flip-flops**
  - CP-Y propagation delay = 5 ns typical
- **Low standby power**
- **Very high output drive**
  - I_{OL} = 48 mA Commercial, 32 mA Military
- **Extra-wide (9- and 10-bit) data paths**
- **Power-up/down disable circuit provides for glitch-free power supply sequencing**
- **Can be powered off while in 3-state, ideal for card edge interface applications**
- **Minimal speed degradation with multiple outputs switching**
- **JEDEC FCT-compatible specs**

GENERAL DESCRIPTION

The Am29C821A and Am29C823A CMOS Bus Interface Registers are designed to eliminate the extra devices required to buffer stand alone registers and to provide extra data width for wider address/data paths or buses carrying parity. The Am29C800A registers are produced with AMD's exclusive CS11SA CMOS process, and feature typical propagation delays of 5 ns, as well as an output current drive of 48 mA.

The Am29C821A is a buffered, 10-bit version of the popular '374/'534 function. The Am29C823A is a 9-bit buffered register with Clock Enable ($\overline{EN}$) and Clear ($\overline{CLR}$)—ideal for parity bus interfacing in high-performance microprogrammed systems.

The Am29C821A and Am29C823A incorporate AMD's proprietary edge-controlled outputs in order to minimize simultaneous switching noise (ground bounce), undershoots and overshoots. By controlling the output transient currents, ground bounce and output ringing have been greatly reduced. A modified AMD output provides a stable, usable voltage level in less time than a non-controlled output.

Additionally, speed degradation due to increasing number of outputs switching is reduced. Together, these benefits of edge-rate control result in significant increase in system performance despite a minor increase in device propagation delay.*

A unique I/O circuitry, which utilizes n-channel pull-up transistors (eliminating the parasitic diode to V_{CC}), provides for high-impedance outputs during power-off and power-up/down sequencing, thus providing glitch-free operation for card-edge and other active bus applications.

The Am29C821A and Am29C823A are available in the standard package options: DIPs, PLCCs, and SOICs.

*For more details refer to a Minimization of Ground Bounce Through Output Edge-Rate Control Application Note (See Chapter 3).

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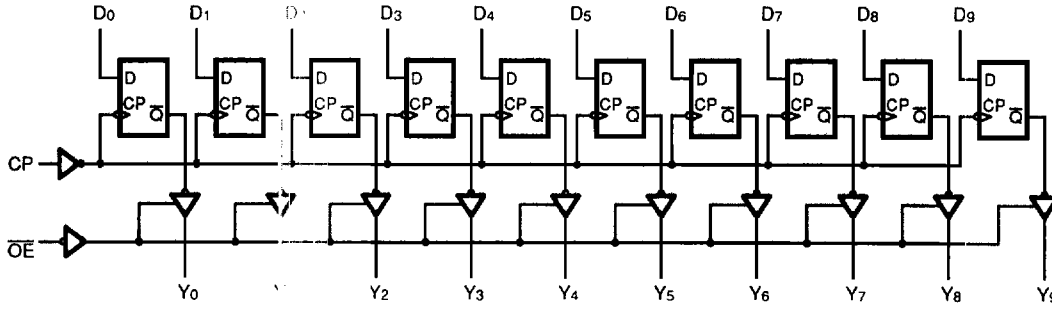
BLOCK DIAGRAMS
Am29C821A



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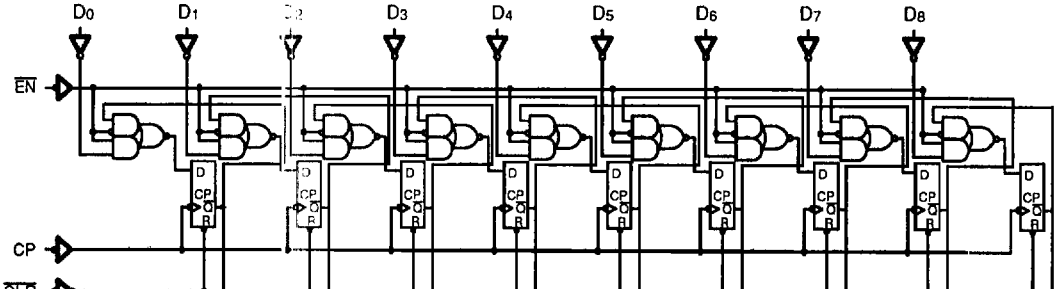
Am29C823A



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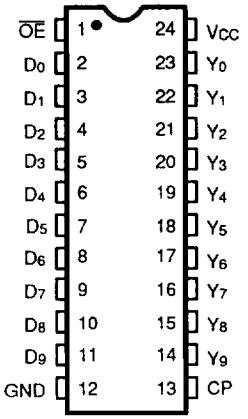
CONNECTION DIAGRAMS (Top View)

Am29C821A

DIP*



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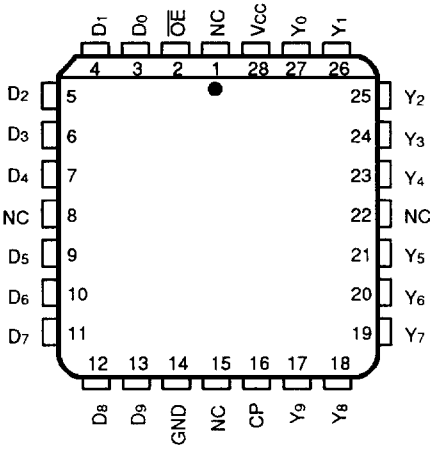
PLCC



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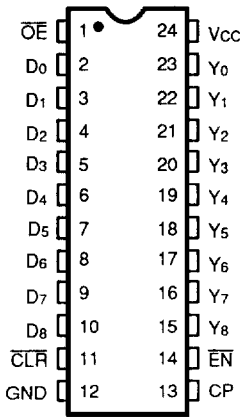
Am29C823A

DIP*



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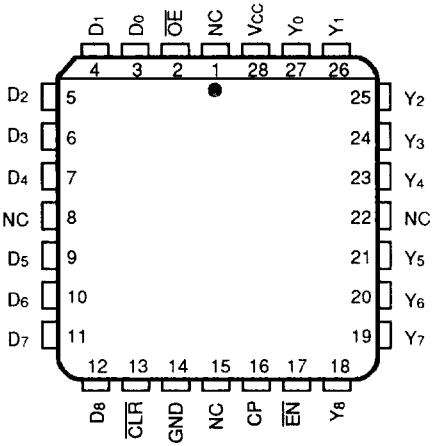
PLCC



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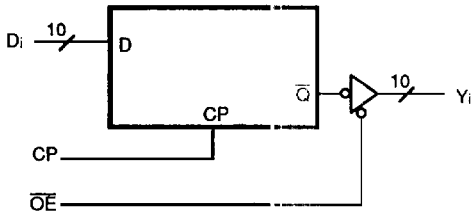
*Also available in 24-Pin Small Outline package; pinout identical to DIPs.

LOGIC SYMBOLS

Am29C821A



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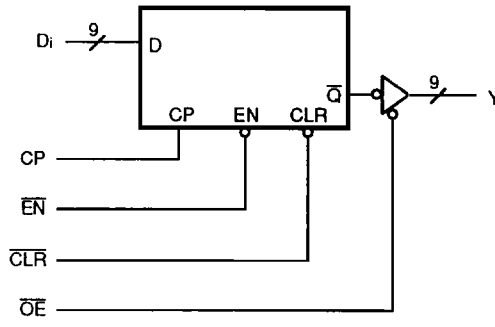
Am29C823A



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FUNCTION TABLES

Am29C821A

Inputs			Internal	Outputs	
$\overline{OE}$	D	CP	$\overline{Q}_i$	Y_i	Function
H	L	↑	H	Z	Hi-Z
H	H	↑	L	Z	
L	L	↑	H	L	Load
L	H	↑	L	H	

Am29C823A

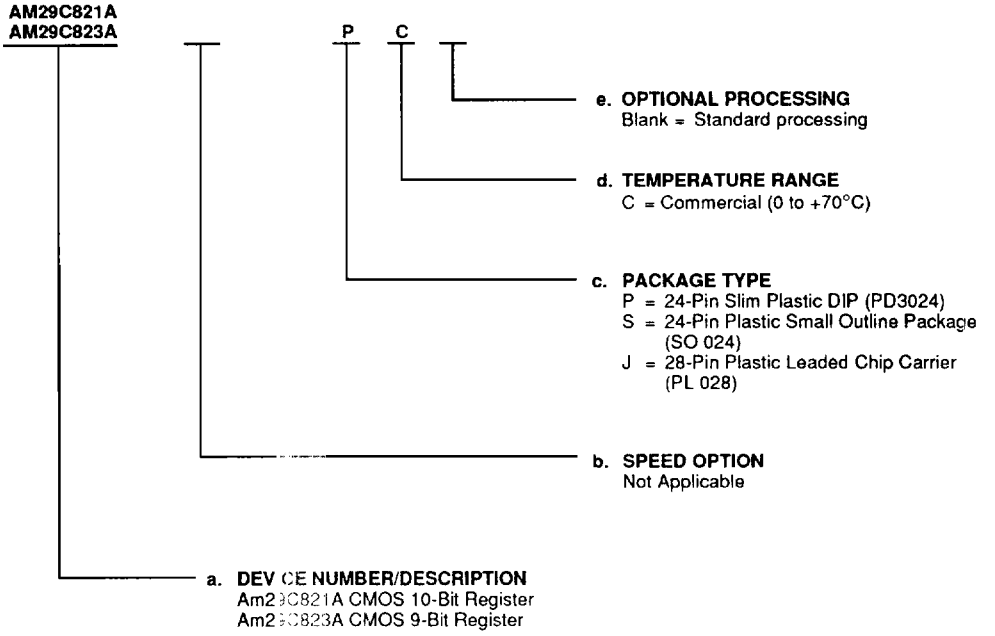
Inputs					Internal	Outputs	
$\overline{OE}$	$\overline{CLR}$	$\overline{EN}$	D_i	CP	$\overline{Q}_i$	Y_i	Function
H	H	L	L	↑	H	Z	Hi-Z
H	H	L	H	↑	L	Z	
H	L	X	X	X	H	Z	Clear
L	L	X	X	X	H	L	
H	H	H	X	X	NC	Z	Hold
L	H	H	X	X	NC	NC	
H	H	L	L	↑	H	Z	Load
H	H	L	H	↑	L	Z	
L	H	L	L	↑	H	L	
L	H	L	H	↑	L	H	

H = HIGH
L = LOW
X = Don't Care
NC = No Change
↑ = LOW-to-HIGH Transition
Z = High Impedance

ORDERING INFORMATION
Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

a. Device Number
b. Speed Option (if applicable)
c. Package Type
d. Temperature Range
e. Optional Processing



Valid Combinations	
AM29C821A	PC, SC, JC
AM29C823A	

Valid Combinations

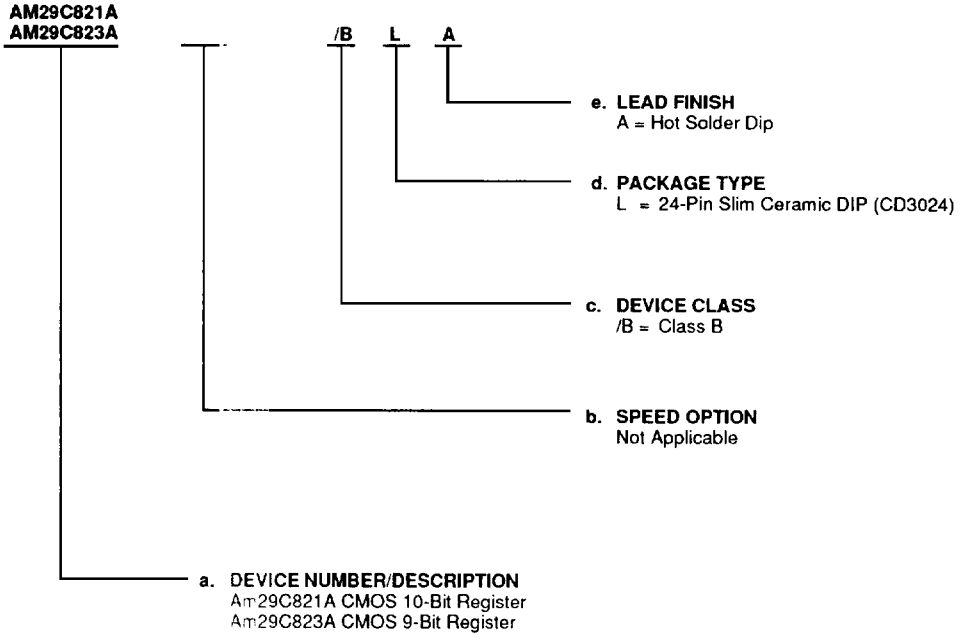
Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

MILITARY ORDERING INFORMATION

APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. The order number (Valid Combination) is formed by a combination of:

a. **Device Number**
b. **Speed Option (if applicable)**
c. **Device Class**
d. **Package Type**
e. **Lead Finish**



Valid Combinations	
AM29C821A	/BLA
AM29C823A	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, or to check on newly released combinations.

Group A Tests

Group A tests consist of Subgroups 1, 2, 3, 7, 8, 9, 10, 11.

PIN DESCRIPTION

Am29C821A/Am29C823A

D_i

Data Input (Input)

D_i are the register data inputs.

CP

Clock Pulse (Input, LOW-to-HIGH Transition)

Clock Pulse is the clock input for the registers. Data is entered into the registers on the LOW-to-HIGH transitions.

Y_i

Data Outputs (Output)

Y_i are the three-state outputs.

$\overline{OE}$

$\overline{\text{Output Enable}}$ (Input, Active LOW)

When the $\overline{OE}$ input is HIGH, the Y_i outputs are in the high-impedance state. When $\overline{OE}$ is LOW, the register data is present at the Y_i outputs.

Am29C823A only

$\overline{EN}$

$\overline{\text{Clock Enable}}$ (Input, Active LOW)

When $\overline{EN}$ is LOW, data on the Di inputs are transferred to the $\overline{Q}_i$ outputs on the LOW-to-HIGH clock transition. When $\overline{EN}$ is HIGH, the $\overline{Q}_i$ outputs do not change state, regardless of the data or clock input transitions.

$\overline{CLR}$

$\overline{\text{Clear}}$ (Input, Active LOW)

When $\overline{CLR}$ is LOW, the internal register is cleared. When $\overline{CLR}$ is LOW and $\overline{OE}$ is LOW, the $\overline{Q}_i$ outputs are HIGH. When $\overline{CLR}$ is HIGH, data can be entered into the register.

ABSOLUTE MAXIMUM RATINGS

StorageTemperature	–65 to +150°C
Supply Voltage to Ground Potential Continous	–0.5 V to +7.0 V
DC Output Voltage	–0.5 V to +6.0 V
DC Input Voltage	–0.5 V to +6.0 V
DC Output Diode Current:	
Into Output	+50 mA
Out of Output	–50 mA
DC Input Diode Current:	
Into Input	+20 mA
Out of Input	–20 mA
DC Output Current:	
Into Output	+100 mA
Out of Output	–100 mA
Total DC Ground Current	
($n \times I_{OL} + m \times I_{CCT}$) mA (Note 1)	
Total DC Vcc Current	
($n \times I_{OH} + m \times I_{CCT}$) mA (Note 1)	

Note:

1. n = number of outputs, m = number of inputs.

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices

Ambient Temperature (T_A)	0 to +70°C
Supply Voltage (Vcc)	+4.5 to +5.5 V

Military (M) Devices

Ambient Temperature (T_A)	–55 to +125°C
Supply Voltage (Vcc)	+4.5 to +5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating ranges unless otherwise specified (for APL Products, Group A, Subgroups 1, 2, 3 are tested unless otherwise noted)

Parameter Symbol	Parameter Description	Test Conditions			Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = 4.5 V, V_{IN} = V_{IH} or V_{IL}	I_{OH} = −15 mA		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = 4.5 V, V_{IN} = V_{IH} or V_{IL}	MIL I_{OL} = 32 mA			0.5	V
			COM'L I_{OL} = 48 mA			0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for All Inputs (Note 1)			2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for All Inputs (Note 1)				0.8	V
V_I	Input Clamp Voltage	V_{CC} = 4.5 V, I_{IN} = −18 mA				−1.2	V
I_{IL}	Input LOW Current	V_{CC} = 5.5 V, V_{IN} = GND				−5	µA
I_{IH}	Input HIGH Current	V_{CC} = 5.5 V, V_{IN} = 5.5 V				5	µA
I_{OZH}	Output Off-State Current (High Impedance)	V_{CC} = 5.5 V, V_O = 5.5 V				+10	µA
I_{OZL}		V_{CC} = 5.5 V, V_O = GND				−10	µA
I_{SC}	Output Short-Circuit Current	V_{CC} = 5.5 V, V_O = 0 V (Note 2)			−60		mA
I_{CCQ}	Static Supply Current	V_{CC} = 5.5 V, Outputs Open	V_{IN} = V_{CC} or GND	MIL		1.5	mA
				COM'L		1.2	
I_{CCT}			V_{IN} = 3.4 V	Data Input		1.5	mA/ Bit
				$\overline{OE}$, $\overline{CLR}$, CP, $\overline{EN}$		3.0	
I_{CCD}†	Dynamic Supply Current	V_{CC} = 5.5 V (Note 3)		Outputs Open		275	µA/ MHz/ Bit
				Outputs Loaded		400	

Notes:

1. Input thresholds are tested in combination with other DC parameters or by correlation.
2. Not more than one output shorted at a time. Duration should not exceed 100 milliseconds.
3. Measured at a frequency ≤ 10 MHz with 50% duty cycle.

† Not included in Group A tests.

SWITCHING CHARACTERISTICS for light capacitive loading over operating ranges unless otherwise specified (for APL Products, Group A, Subgroups 9, 10, 11 are tested unless otherwise noted)

Symbol	Parameter Description		Test Conditions*	Commercial		Military		Unit
				Min.	Max.	Min.	Max.	
t_{PLH}	Propagation Delay Clock to Y_i		C_L = 50 pF R_1 = 500 Ω R_2 = 500 Ω	2	8.5	2	9.5	ns
t_{PHL}	($\overline{OE}$ = LOW) (Note 1)			3	8.5	3	9.5	ns
t_S	Data to CP Setup Time			3		3		ns
t_H	Data to CP Hold Time			2		2		ns
t_S	Enable ($\overline{EN}$ ↑) to CP Setup Time			4		4		ns
t_S	Enable ($\overline{EN}$ ↓) to CP Setup Time			4		4		ns
t_H	Enable ($\overline{EN}$) Hold Time			0		0		ns
t_{PHL}	Propagation Delay, Clear to Y_i			3	10	3	10.5	ns
t_{REC}	Clear ($\overline{CLR}$ ↓) to CP Setup Time			6		6		ns
t_{PWH}	Clock Pulse Width	HIGH		6		6		ns
t_{PWL}		LOW		6		6		ns
t_{PWL}	Clear Pulse Width	LOW		6		6		ns
t_{ZH}	Output Enable Time $\overline{OE}$ ↑ to Y_i			1	8.5	1	9	ns
t_{ZL}				3	12	3	13	ns
t_{HZ}	Output Disable Time $\overline{OE}$ ↓ to Y_i			2	8	2	8.5	ns
t_{LZ}				2	8	2	8.5	ns

SWITCHING CHARACTERISTICS for heavy capacitive loading over operating ranges unless otherwise specified (Note 2)

Symbol	Parameter Description	Test Conditions*	Commercial		Military		Unit
			Min.	Max.	Min.	Max.	
t_{PLH}	Propagation Delay Clock to Y_i	C_L = 300 pF R_1 = 500 Ω R_2 = 500 Ω	2	15.5	2	17.5	ns
t_{PHL}	($\overline{OE}$ = LOW) (Note 1)		3	15.5	3	17.5	ns
t_{ZH}	Output Enable Time $\overline{OE}$ ↑ to Y_i		2	15	2	15.5	ns
t_{ZL}			3	18.5	3	19.5	ns
t_{HZ}	Output Disable Time $\overline{OE}$ ↓ to Y_i	C_L = 5 pF R_1 = 500 Ω R_2 = 500 Ω	2	6.5	2	7	ns
t_{LZ}			2	6.5	2	7	ns

*See Test Circuit and Waveforms listed in Chapter 2.

Notes:

1. For more details refer to a Minimization of Ground Bounce Through Output Edge-Rate Control Application Note (See Chapter 3).
2. These parameters are guaranteed by characterization but not production tested.