



Dual N-Channel 30 V (D-S) MOSFETs

PRODUCT SUMMARY							
	V _{DS} (V)	$R_{DS(on)}\left(\Omega\right)$ (Max.)	I_D (A) ^g	Q _g (Typ.)			
Channel-1	30	$0.00640 \text{ at V}_{GS} = 10 \text{ V}$	16 ^a	7.2 nC			
Channel-1		$0.01000 \text{ at V}_{GS} = 4.5 \text{ V}$	16 ^a	7.2110			
Channel-2	nnel-2 30	$0.00137 \text{ at V}_{GS} = 10 \text{ V}$	40 ^a	30.1 nC			
		$0.00194 \text{ at V}_{GS} = 4.5 \text{ V}$	40 ^a	30.1110			

PowerPAIR® 6 x 5 5 mm 6 mm **Ordering Information:**

SiZ914DT-T1-GE3 (Lead (Pb)-free and Halogen-free)

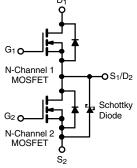
FEATURES

- TrenchFET® Gen IV Power MOSFETs
- 100 % R_{α} and UIS Tested
- Material categorization: For definitions of compliance please see www.vishay.com/doc?99912



APPLICATIONS

- **CPU Core Power**
- Computer/Server Peripherals
- Synchronous Buck Converter
- POL
- Telecom DC/DC



Parameter		Symbol	Channel-1	Channel-2	Unit
Drain-Source Voltage		V_{DS}	30		V
Gate-Source Voltage	V_{GS}	+ 20			
	T _C = 25 °C		16 ^a	40 ^a	۸
Continuous Drain Current /T 150 °C)	T _C = 70 °C		16 ^a	40 ^a	
Continuous Drain Current (T _J = 150 °C)	T _A = 25 °C	ID	16 ^{a, b, c}	40 ^{a, b, c}	
	T _A = 70 °C		15.5 ^{b, c}	38.8 ^{b, c}	
Pulsed Drain Current (t = 100 μs)	I _{DM}	80	100	Α	
0 " 0 5 " 0 0	T _C = 25 °C	1	19	28	
Continuous Source Drain Diode Current	T _A = 25 °C	- I _S	3.25 ^{b, c}	4.3 ^{b, c}	
Single Pulse Avalanche Current L = 0.1 mH		I _{AS}	10	20	
Single Pulse Avalanche Energy		E _{AS}	5	20	mJ
	T _C = 25 °C		22.7	100	
Maximum Dawar Dissination	T _C = 70 °C		14.5	64	w
Maximum Power Dissipation	T _A = 25 °C	P_{D}	3.9 ^{b, c}	5.2 ^{b, c}	
	T _A = 70 °C		2.5 ^{b, c}	3.3 ^{b, c}	
Operating Junction and Storage Temperature Ra	T _J , T _{stg}	- 55 to 150		°C	
Soldering Recommendations (Peak Temperatur		2			

THERMAL RESISTANCE RATINGS									
			Char	nnel-1	Channel-2				
Parameter		Symbol	Тур.	Max.	Тур.	Max.	Unit		
Maximum Junction-to-Ambient ^{b, f}	t ≤ 10 s	R _{thJA}	25	32	19	24	°C/W		
Maximum Junction-to-Case (Drain)	Steady State	R_{thJC}	4.4	5.5	1	1.25	C/VV		

Notes:

- a. Package limited
- b. Surface mounted on 1" x 1" FR4 board.
- d. See solder profile (www.vishay.com/doc?73257). The PowerPAIR is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
- e. Rework conditions: manual soldering with a soldering iron is not recommended for leadless components.
- f. Maximum under steady state conditions is 62 °C/W for channel-1 and 55 °C/W for channel-2.
- g. $T_C = 25$ °C.

SiZ914DT

Vishay Siliconix



SPECIFICATIONS ($T_J = 25$ °C	C, unless otl	herwise noted)						
Parameter	Symbol	Test Conditions		Min.	Тур.	Max.	Unit	
Static								
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0 \text{ V, } I_D = 250 \mu\text{A}$		30			V	
Diain-Source Breakdown voltage	VDS	$V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}$	Ch-2	30				
Cata Threshold Valtage	V	$V_{DS} = V_{GS}, I_D = 250 \mu A$	Ch-1	1.2		2.4	V	
Gate Threshold Voltage	V _{GS(th)}	$V_{DS} = V_{GS}$, $I_D = 250 \mu A$	Ch-2	1		2.4		
Gate Source Leakage	I _{GSS}	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 20 \text{ V}, -16 \text{ V}$	Ch-1			± 100	nA	
	433		Ch-2			± 100		
		V _{DS} = 30 V, V _{GS} = 0 V	Ch-1			1		
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 30 V, V _{GS} = 0 V	Ch-2		60	240	μΑ	
	566	$V_{DS} = 30 \text{ V}, V_{GS} = 0 \text{ V}, T_{J} = 55 ^{\circ}\text{C}$	Ch-1			5		
		$V_{DS} = 30 \text{ V}, V_{GS} = 0 \text{ V}, T_{J} = 55 ^{\circ}\text{C}$	Ch-2		0.5	5	mA	
On-State Drain Current ^b	I _{D(on)}	$V_{DS} \ge 5 \text{ V}, V_{GS} = 10 \text{ V}$	Ch-1	20			Α	
On State Brain Surrent	D(OII)	$V_{DS} \ge 5 \text{ V}, V_{GS} = 10 \text{ V}$	Ch-2	25				
Drain-Source On-State Resistance ^b		$V_{GS} = 10 \text{ V}, I_D = 19 \text{ A}$	Ch-1		0.00530	0.00640	 I	
	R _{DS(on)}	V _{GS} = 10 V, I _D = 20 A	Ch-2		0.00114	0.00137	Ω	
	' 'DS(on)	$V_{GS} = 4.5 \text{ V}, I_D = 15 \text{ A}$	Ch-1		0.00800	0.01000	22	
		$V_{GS} = 4.5 \text{ V}, I_D = 20 \text{ A}$	Ch-2		0.00155	0.00194		
h	Q.	$V_{DS} = 10 \text{ V}, I_{D} = 19 \text{ A}$	Ch-1		55		s	
Forward Transconductance ^b	9 _{fs}	V _{DS} = 10 V, I _D = 20 A	Ch-2		68			
Dynamic ^a								
Input Capacitance	C _{iss}		Ch-1		1208		pF	
mput Supusitanios	Olss	Channal 1	Ch-2		5603			
Output Capacitance	C _{oss}	Channel-1 $V_{DS} = 15 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}$	Ch-1		375			
	- 035	VDS = 10 1, 1GS = 0 1, 1 = 1 1011 12	Ch-2		2202			
Reverse Transfer Capacitance	C_{rss}	Channel-2	Ch-1		30		-	
·		$V_{DS} = 15 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}$	Ch-2		168			
C _{rss} /C _{iss} Ratio			Ch-1		0.025	0.050		
		V 45 V V 40 V L 00 A	Ch-2		0.032	0.064		
		$V_{DS} = 15 \text{ V}, V_{GS} = 10 \text{ V}, I_{D} = 20 \text{ A}$	Ch-1		17	26		
Total Gate Charge	Q_g	$V_{DS} = 15 \text{ V}, V_{GS} = 10 \text{ V}, I_{D} = 20 \text{ A}$	Ch-2		66	99	nC	
	3	Channel-1	Ch-1		7.2	11		
		$V_{DS} = 15 \text{ V}, V_{GS} = 4.5 \text{ V}, I_D = 20 \text{ A}$	Ch-2		30.1	45.2		
Gate-Source Charge	Q_{gs}	20 / do / b	Ch-1		3.6			
	Q _{gd}	Channel-2	Ch-2		10.9			
Gate-Drain Charge		$V_{DS} = 15 \text{ V}, V_{GS} = 4.5 \text{ V}, I_D = 20 \text{ A}$	Ch-1		0.94			
	3-	1	Ch-2 Ch-1		3.8			
Output Charge	Q _{oss}	$V_{DS} = 15 \text{ V}, V_{GS} = 0 \text{ V}$			10			
		+	Ch-2 Ch-1	0.5	60 2.5	5		
Gate Resistance	R_{g}	f = 1 MHz	Ch-2	0.5	1	2	Ω	

a. Guaranteed by design, not subject to production testing.

b. Pulse test; pulse width \leq 300 μ s, duty cycle \leq 2 %.



Parameter	Symbol	Symbol Test Conditions			Тур.	Max.	Unit
Dynamic ^a				l	•	ı	l
Turn-On Delay Time	t _{d(on)}	Channel-1	Ch-1		16	24	
	=(/	$V_{DD} = 15 \text{ V}, R_1 = 1.5 \Omega$	Ch-2		40	60	
Rise Time	t _r	$I_D \cong 10 \text{ A}, V_{GEN} = 4.5 \text{ V}, R_g = 1 \Omega$	Ch-1 Ch-2		11 127	20 190	
		Ohannal O	Ch-1		15	23	
Turn-Off Delay Time	t _{d(off)}	Channel-2 $V_{DD} = 15 \text{ V}, R_{I} = 1.5 \Omega$	Ch-2		40	60	
Fall Time	t _f	$I_D \cong 10 \text{ A}, V_{GEN} = 4.5 \text{ V}, R_q = 1 \Omega$	Ch-1		5	10	
Fall Time	l lf	S GEN 9	Ch-2		19	29	no
Turn-On Delay Time	t., ,		Ch-1		10	20	ns
Turn-On Delay Time	t _{d(on)}	Channel-1	Ch-2		12	20	
Rise Time	t _r	V_{DD} = 15 V, R_L = 1.5 Ω $I_D \cong$ 10 A, V_{GEN} = 10 V, R_q = 1 Ω	Ch-1		10	20	
Tuse Time	4	D = 10 A, VGEN - 10 V, Hg - 122	Ch-2		30	45	
Turn-Off Delay Time	t _{d(off)}	Channel-2	Ch-1		20	30	
Tan on Boldy Time		$V_{DD} = 15 \text{ V}, R_{L} = 1.5 \Omega$	Ch-2		35	53	
Fall Time	t _f	$I_D \cong 10 \text{ A}, V_{GEN} = 10 \text{ V}, R_g = 1 \Omega$	Ch-1		5	10	
B : 0			Ch-2		7	14	
Drain-Source Body Diode Characteristic	S	T		1	T	1 40	1
Continuous Source-Drain Diode Current	I _S	T _C = 25 °C	Ch-1 Ch-2			40 40	
			Ch-1			80	Α
Pulse Diode Forward Current (t = 100 μ s)	I _{SM}		Ch-2			100	1
	.,	I _S = 10 A, V _{GS} = 0 V	Ch-1		0.8	1.2	
Body Diode Voltage	V_{SD}	I _S = 2 A, V _{GS} = 0 V	Ch-2		0.33	0.42	V
Dady Diada Dayaraa Daasyary Tima			Ch-1		15	23	
Body Diode Reverse Recovery Time	t _{rr}		Ch-2		62	93	ns
Body Diode Reverse Recovery Charge	Q _{rr}	Channel-1	Ch-1		4	8	nC
body blode neverse necovery Charge		$I_F = 10 \text{ A}, \text{ dI/dt} = 100 \text{ A/}\mu\text{s}, T_J = 25 ^{\circ}\text{C}$	Ch-2		96	144	IIC
Reverse Recovery Fall Time	t _a	Channel-2	Ch-1		9		
Tierenee Hoodvery Fall Tillio	*a	$I_F = 10 \text{ A}, \text{ dI/dt} = 100 \text{ A/}\mu\text{s}, T_J = 25 ^{\circ}\text{C}$	Ch-2		30.5		ns
Reverse Recovery Rise Time	t _b		Ch-1		6		'''
	15		Ch-2		31.5		

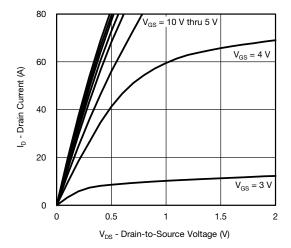
Notes:

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

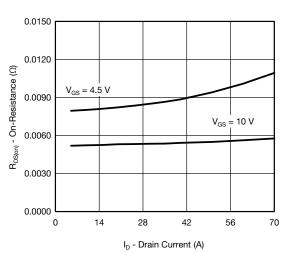
a. Guaranteed by design, not subject to production testing.

b. Pulse test; pulse width \leq 300 μ s, duty cycle \leq 2 %.

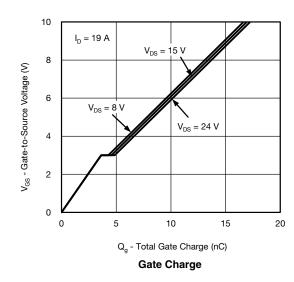
CHANNEL-1 TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

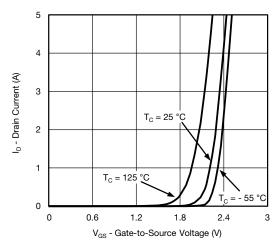


Output Characteristics

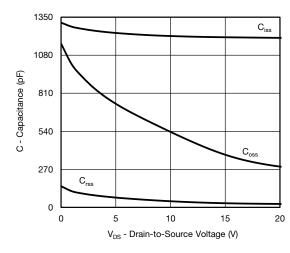


On-Resistance vs. Drain Current

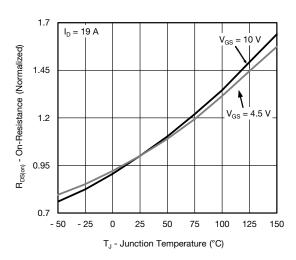




Transfer Characteristics



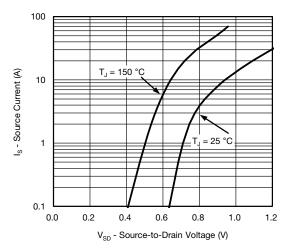
Capacitance



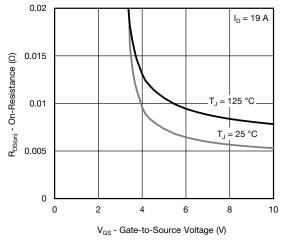
On-Resistance vs. Junction Temperature



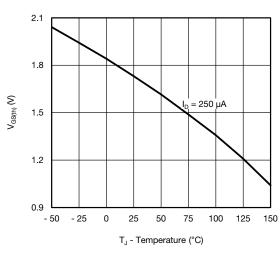
CHANNEL-1 TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



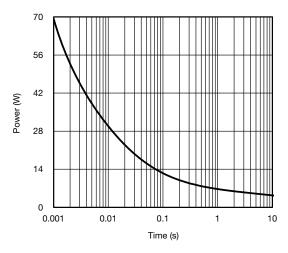
Source-Drain Diode Forward Voltage



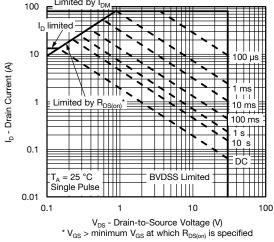
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage

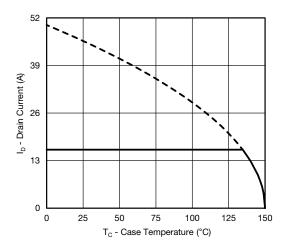


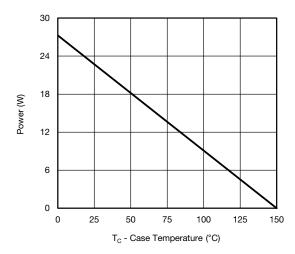
Single Pulse Power, Junction-to-Ambient



Safe Operating Area, Junction-to-Ambient

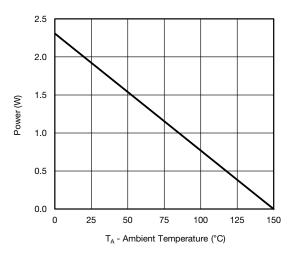
CHANNEL-1 TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)





Current Derating*

Power, Junction-to-Case

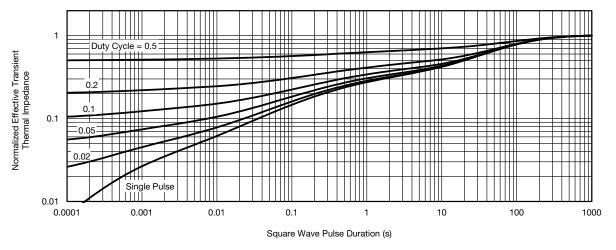


Power, Junction-to-Ambient

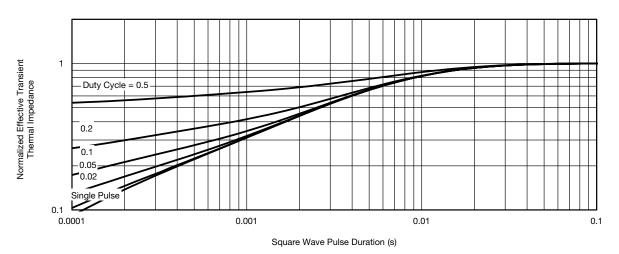
^{*} The power dissipation P_D is based on $T_{J(max.)}$ = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.



CHANNEL-1 TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

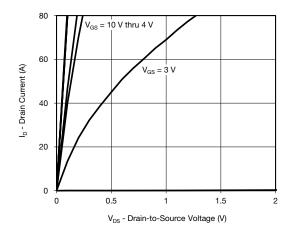


Normalized Thermal Transient Impedance, Junction-to-Ambient

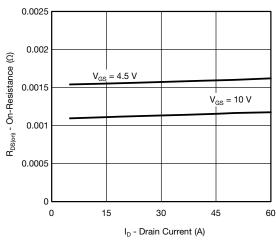


Normalized Thermal Transient Impedance, Junction-to-Case

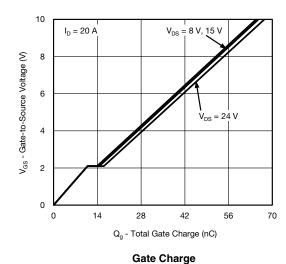
CHANNEL-2 TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

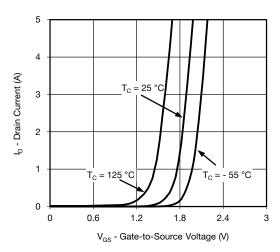


Output Characteristics

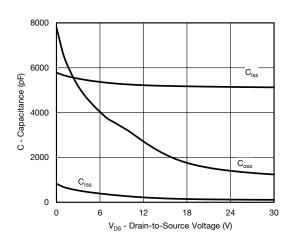


On-Resistance vs. Drain Current

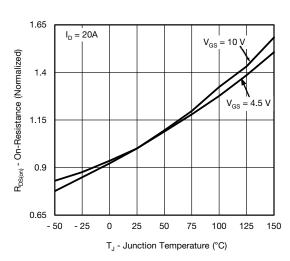




Transfer Characteristics



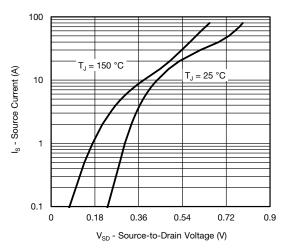
Capacitance



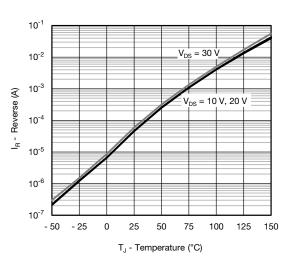
On-Resistance vs. Junction Temperature



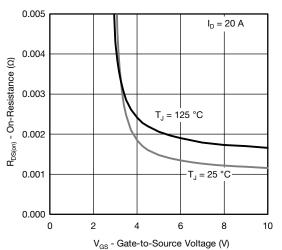
CHANNEL-2 TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



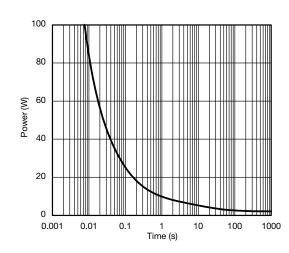
Source-Drain Diode Forward Voltage



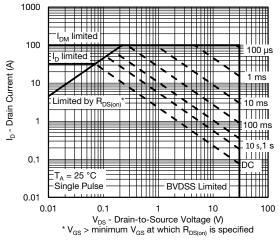
Reverse Current (Schottky)



On-Resistance vs. Gate-to-Source Voltage



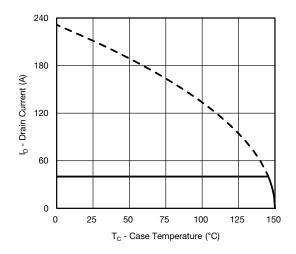
Single Pulse Power, Junction-to-Ambient

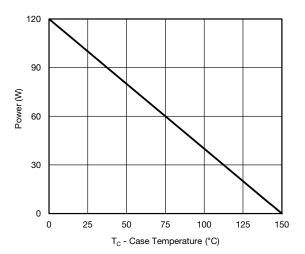


Safe Operating Area, Junction-to-Ambient



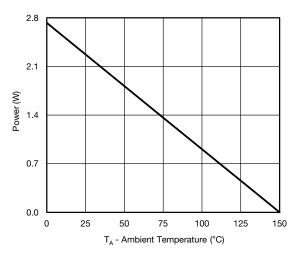
CHANNEL-2 TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)





Current Derating*

Power, Junction-to-Case

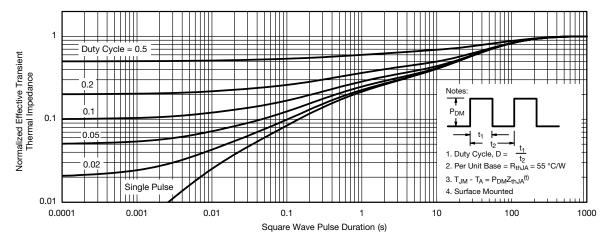


Power, Junction-to-Ambient

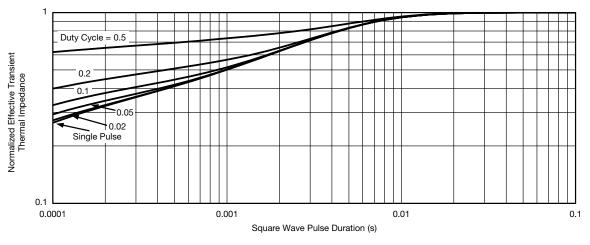
^{*} The power dissipation P_D is based on $T_{J(max.)}$ = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.



CHANNEL-2 TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Ambient



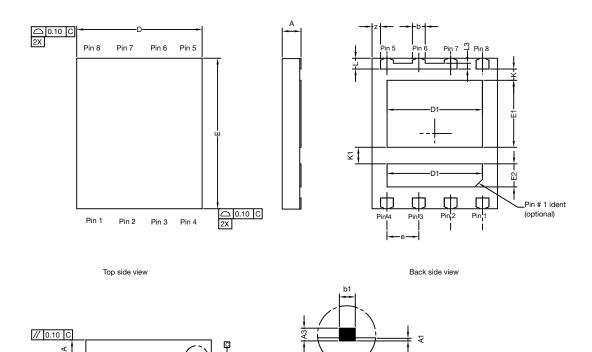
Normalized Thermal Transient Impedance, Junction-to-Case

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?62905.



△ 0.08 C

PowerPAIR® 6 x 5 Case Outline

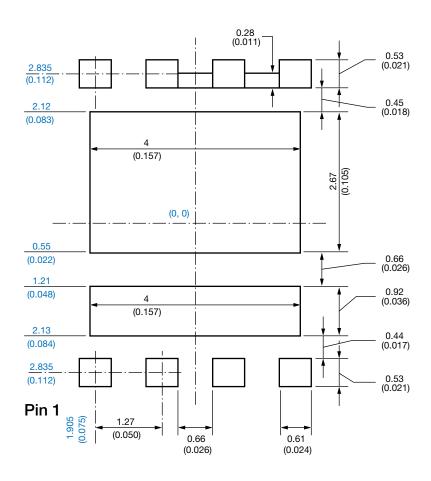


		MILLIMETERS		INCHES				
DIM.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.		
А	0.70	0.75	0.80	0.028	0.030	0.032		
A1	0.00	-	0.10	0.000	-	0.004		
A3	0.15	0.20	0.25	0.006	0.007	0.009		
b	0.43	0.51	0.61	0.017	0.020	0.024		
b1		0.25 BSC			0.010 BSC			
D	4.90	5.00	5.10	0.192	0.196	0.200		
D1	3.75	3.80	3.85	0.148	0.150	0.152		
E	5.90	6.00	6.10	0.232	0.236	0.240		
E1 Option AA (for W/B)	2.62	2.67	2.72	0.103	0.105	0.107		
E1 Option AB (for BWL)	2.42	2.47	2.52	0.095	0.097	0.099		
E2	0.87	0.92	0.97	0.034	0.036	0.038		
е		1.27 BSC		0.050 BSC				
K Option AA (for W/B)		0.45 typ.			0.018 typ.			
K Option AB (for BWL)		0.65 typ.			0.025 typ.			
K1	0.66 typ.			0.025 typ.				
L	0.33	0.43	0.53	0.013	0.017	0.020		
L3		0.23 BSC	.23 BSC 0.009 BSC					
z	0.34 BSC 0.013 BSC							
ECN: T14-0782-Rev. C, 22-Dec- DWG: 6005	-14							

Revision: 22-Dec-14 1 Document Number: 63656



Recommended Minimum PAD for PowerPAIR® 6 x 5



Dimensions in millimeters (inch)

Note

• Linear dimensions are in black, the same information is provided in ordinate dimensions which are in blue.



Legal Disclaimer Notice

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