120V 175°C N-CHANNEL ENHANCEMENT MODE MOSFET
PowerDI5060-8

Product Summary

BV_{DSS}	$R_{DS(ON)}$ Max	I_D T_C = +25°C (Note 10)
120V	8.9mΩ @ V_{GS} = 10V	84A
	16mΩ @ V_{GS} = 6V	70A

Features

- Rated to +175°C – Ideal for High Ambient Temperature Environments
- 100% Unclamped Inductive Switching (UIS) Test in Production – Ensures More Reliable and Robust End Application
- Thermally Efficient Package – Cooler Running Applications
- High Conversion Efficiency
- Low $R_{DS(ON)}$ – Minimizes On-State Losses
- <1.1mm Package Profile – Ideal for Thin Applications
- **Lead-Free Finish; RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**
- **For automotive applications requiring specific change control (i.e. parts qualified to AEC-Q100/101/200, PPAP capable, and manufactured in IATF 16949 certified facilities), please contact us or your local Diodes representative.**
  https://www.diodes.com/quality/product-definitions/

Description and Applications

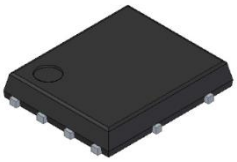
This MOSFET is designed to minimize the on-state resistance ($R_{DS(ON)}$) yet maintain superior switching performance, making it ideal for high efficiency power management applications.

- Switchings
- DC-DC Converters

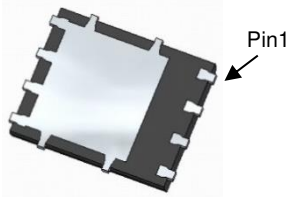
Mechanical Data

- Package: PowerDI®5060-8
- Package Material: Molded Plastic, "Green" Molding Compound. UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminal Finish – Matte Tin Annealed over Copper Leadframe. Solderable per MIL-STD-202, Method 208 e3
- Weight: 0.097 grams (Approximate)

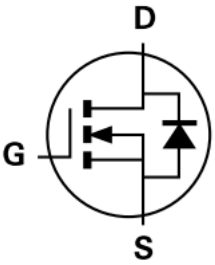
PowerDI5060-8



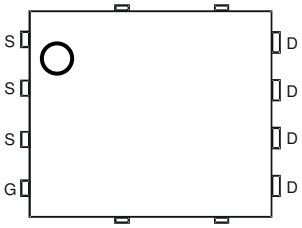
Top View



Bottom View



Internal Schematic



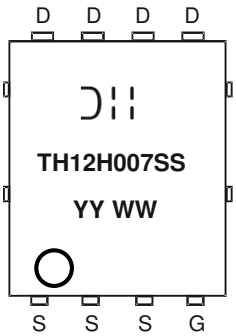
Top View
Pin Configuration

Ordering Information (Note 4)

Part Number	Package	Packing	
		Qty.	Carrier
DMTH12H007SPS-13	PowerDI5060-8	2,500	Tape & Reel

Notes:
1. EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant. All applicable RoHS exemptions applied.
2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
4. For packaging details, go to our website at https://www.diodes.com/design/support/packaging/diodes-packaging/.

Marking Information



= Manufacturer's Marking
TH12H007SS = Product Type Marking Code
YYWW = Date Code Marking
YY = Last Two Digits of Year (ex: 22 = 2022)
WW = Week Code (01 to 53)

PowerDI is a registered trademark of Diodes Incorporated.

Maximum Ratings (@T_A = +25°C, unless otherwise specified.)

Characteristic		Symbol	Value	Unit
Drain-Source Voltage		V_{DSS}	120	V
Gate-Source Voltage		V_{GSS}	±20	V
Continuous Drain Current, V_{GS} = 10V (Note 6)	T_C = +25°C (Note 10) T_C = +100°C	I_D	84 60	A
Pulsed Drain Current (10µs Pulse, T_C = +25°C, Package Limited)		I_{DM}	336	A
Continuous Body Diode Forward Current (Note 6)	T_C = +25°C	I_S	84	A
Pulsed Body Diode Current (10µs Pulse, T_C = +25°C, Package Limited)	T_C = +25°C	I_{SM}	336	A
Avalanche Current, L = 3mH (Note 9)		I_{AS}	15.5	A
Avalanche Energy, L = 3mH (Note 9)		E_{AS}	360.4	mJ

Thermal Characteristics

Characteristic	Symbol	Value (Typ.)	Unit
Total Power Dissipation (Note 5)	P_D	3.5	W
Thermal Resistance, Junction to Ambient (Note 5)	$R_{\theta JA}$	43	°C/W
Total Power Dissipation (Note 6)	P_D	125	W
Thermal Resistance, Junction to Case (Note 6)	$R_{\theta JC}$	1.2	°C/W
Operating and Storage Temperature Range	T_J, T_{STG}	-55 to +175	°C

Electrical Characteristics (@T_A = +25°C, unless otherwise specified.)

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
OFF CHARACTERISTICS (Note 7)						
Drain-Source Breakdown Voltage	BV_{DSS}	120	—	—	V	V_{GS} = 0V, I_D = 10mA
Zero Gate Voltage Drain Current	I_{DSS}	—	—	1	µA	V_{DS} = 96V, V_{GS} = 0V
Gate-Source Leakage	I_{GSS}	—	—	±100	nA	V_{GS} = ±20V, V_{DS} = 0V
ON CHARACTERISTICS (Note 7)						
Gate Threshold Voltage	$V_{GS(TH)}$	2	—	4	V	V_{DS} = V_{GS}, I_D = 250µA
Static Drain-Source On-Resistance	$R_{DS(ON)}$	—	7.5	8.9	mΩ	V_{GS} = 10V, I_D = 30A
		—	12	16		V_{GS} = 6V, I_D = 10A
Diode Forward Voltage	V_{SD}	—	0.8	1.2	V	V_{GS} = 0V, I_S = 30A
DYNAMIC CHARACTERISTICS (Note 8)						
Input Capacitance	C_{iss}	—	3142	—	pF	V_{DS} = 60V, V_{GS} = 0V, f = 1MHz
Output Capacitance	C_{oss}	—	665	—		
Reverse Transfer Capacitance	C_{rss}	—	29	—		
Gate Resistance	R_G	—	1.9	—	Ω	V_{DS} = 0V, V_{GS} = 0V, f = 1MHz
Total Gate Charge (V_{GS} = 10V)	Q_g	—	44	—	nC	V_{DS} = 60V, I_D = 25A
Gate-Source Charge	Q_{gs}	—	15	—		
Gate-Drain Charge	Q_{gd}	—	9	—		
Turn-On Delay Time	$t_{D(ON)}$	—	12.5	—	ns	V_{DD} = 60V, V_{GS} = 10V, I_D = 25A, R_G = 2.7Ω
Turn-On Rise Time	t_R	—	13.7	—		
Turn-Off Delay Time	$t_{D(OFF)}$	—	24.4	—		
Turn-Off Fall Time	t_F	—	10.9	—		
Reverse Recovery Time	t_{RR}	—	55	—	ns	I_F = 25A, di/dt = 100A/µs
Reverse Recovery Charge	Q_{RR}	—	105	—	nC	

Notes:
5. Device mounted on FR-4 substrate PC board, 2oz copper, with thermal bias to bottom layer 1inch square copper plate.
6. Thermal resistance from junction to soldering point (on the exposed drain pad).
7. Short duration pulse test used to minimize self-heating effect.
8. Guaranteed by design. Not subject to product testing.
9. I_{AS} and E_{AS} ratings are based on low frequency and duty cycles to keep T_J = +25°C.
10. Package limited.

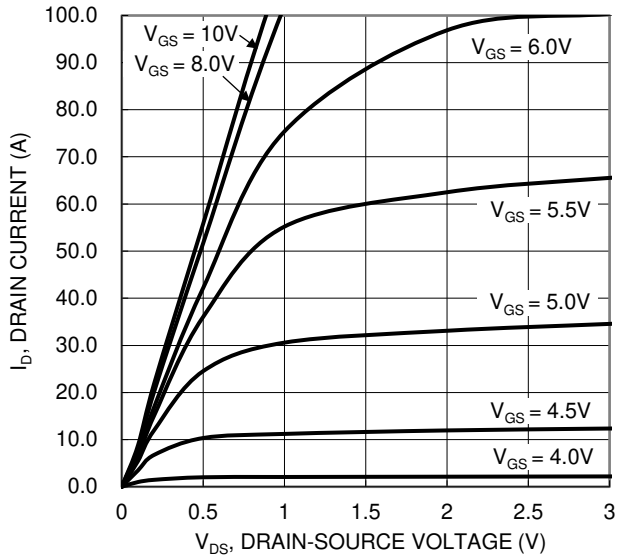


Figure 1. Typical Output Characteristic

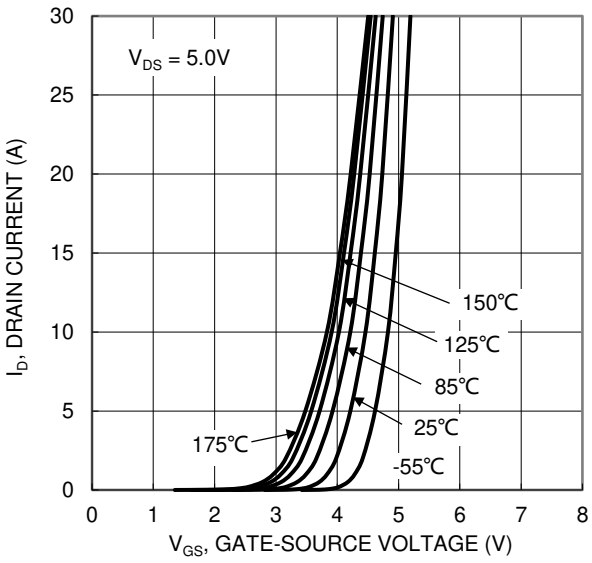


Figure 2. Typical Transfer Characteristic

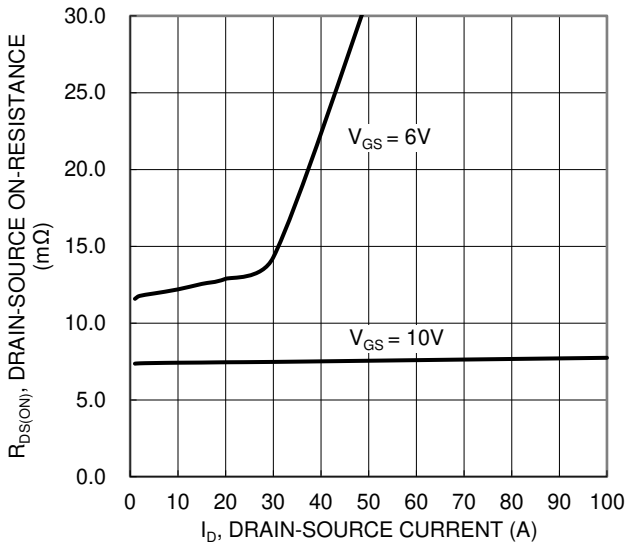


Figure 3. Typical On-Resistance vs. Drain Current and Gate Voltage

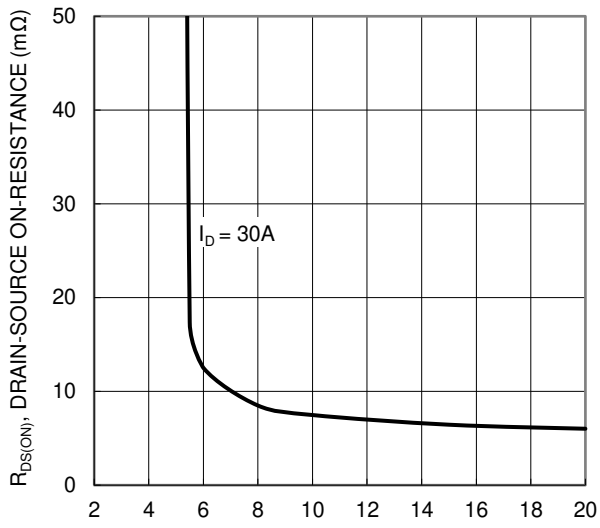


Figure 4. Typical Transfer Characteristic

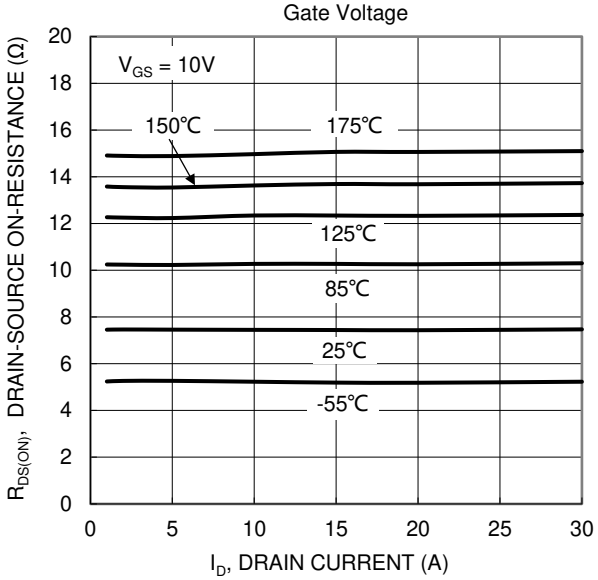


Figure 5. Typical On-Resistance vs. Drain Current and Temperature

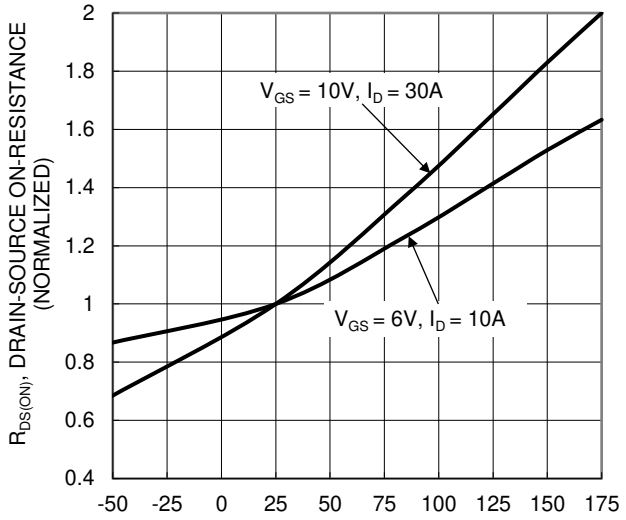


Figure 6. On-Resistance Variation with Temperature

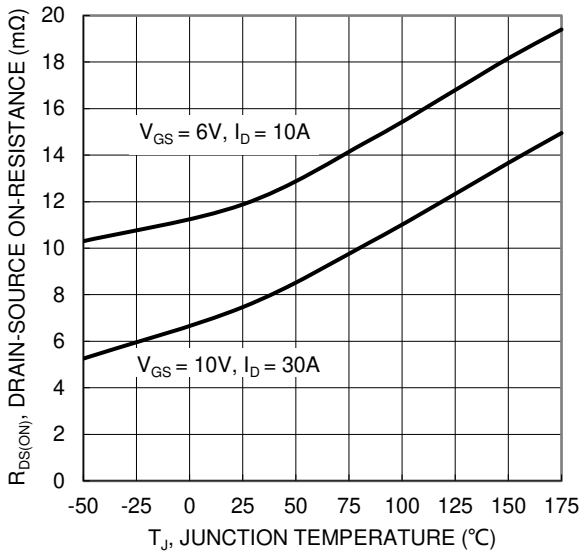


Figure 7. On-Resistance Variation with Temperature

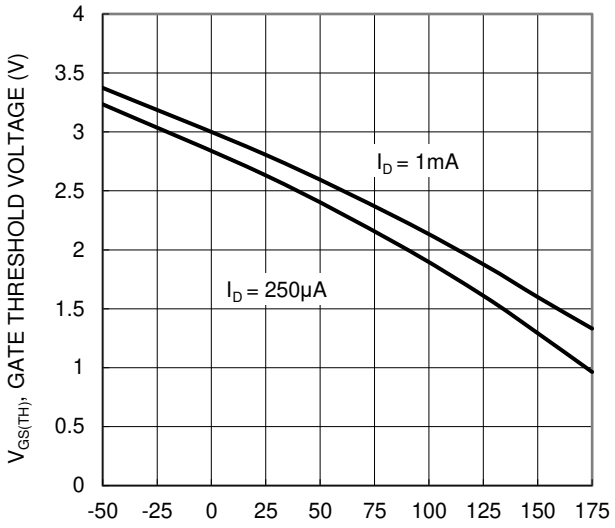


Figure 8. Gate Threshold Variation vs. Junction Temperature

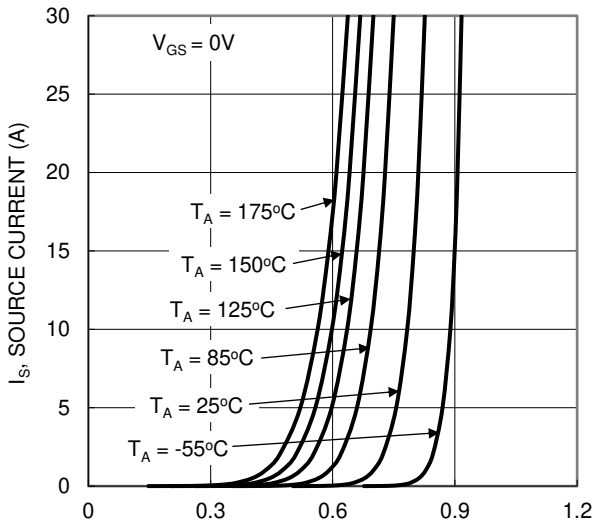


Figure 9. Diode Forward Voltage vs. Current

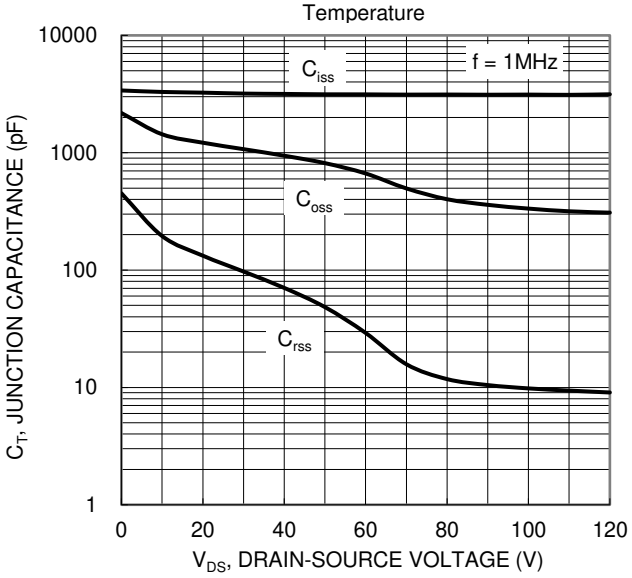


Figure 10. Typical Junction Capacitance

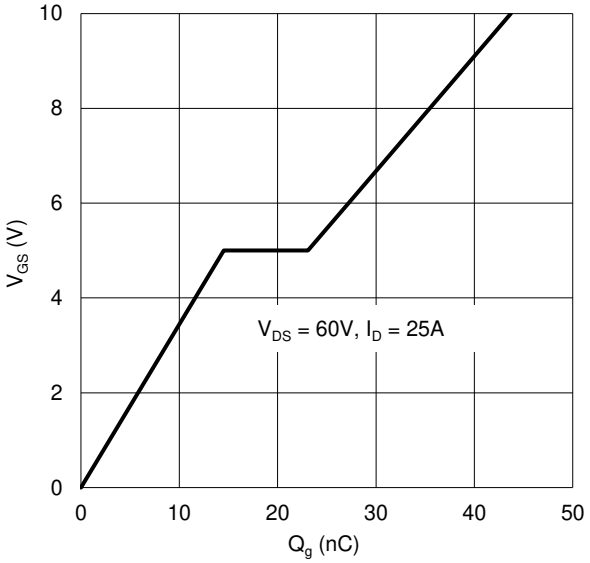


Figure 11. Gate Charge

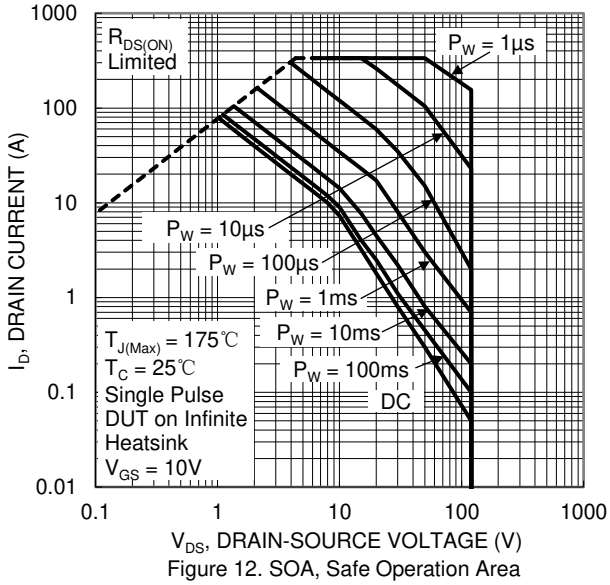


Figure 12. SOA, Safe Operation Area

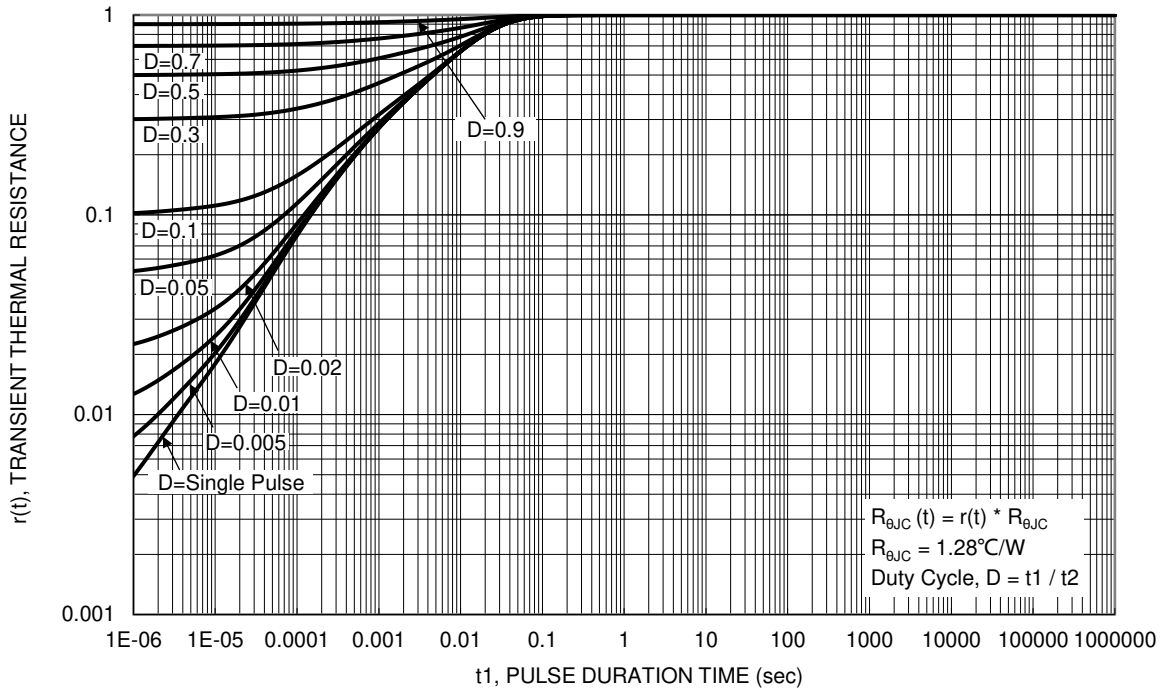
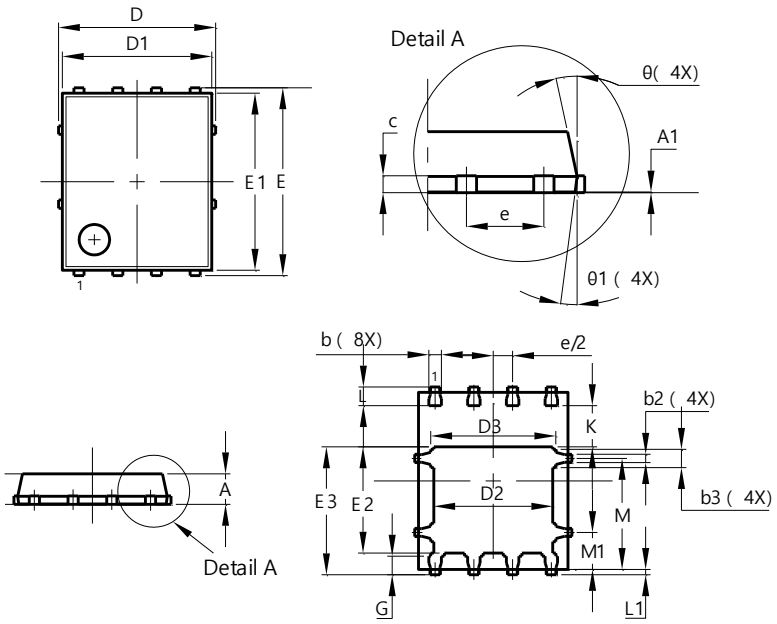


Figure 13. Transient Thermal Resistance

Package Outline Dimensions

Please see http://www.diodes.com/package-outlines.html for the latest version.

PowerDI5060-8

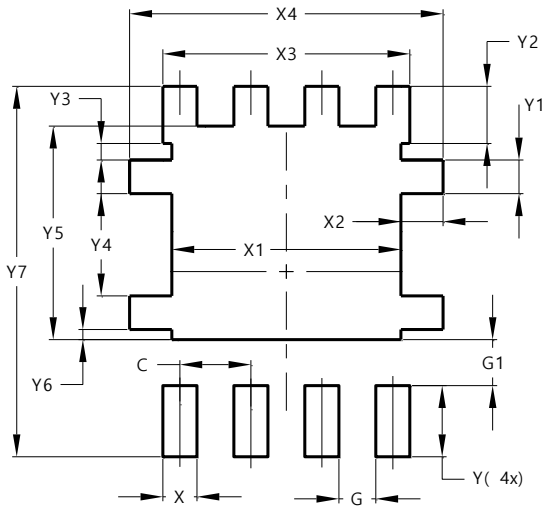


PowerDI5060-8			
Dim	**Min**	**Max**	**Typ**
A	0.90	1.10	1.00
A1	0.00	0.05	–
b	0.33	0.51	0.41
b2	0.200	0.350	0.273
b3	0.40	0.80	0.60
c	0.230	0.330	0.277
D	5.15 BSC		
D1	4.70	5.10	4.90
D2	3.70	4.10	3.90
D3	3.90	4.30	4.10
E	6.15 BSC		
E1	5.60	6.00	5.80
E2	3.28	3.68	3.48
E3	3.99	4.39	4.19
e	1.27 BSC		
G	0.51	0.71	0.61
K	0.51	–	–
L	0.51	0.71	0.61
L1	0.100	0.200	0.175
M	3.235	4.035	3.635
M1	1.00	1.40	1.21
Θ	10°	12°	11°
Θ1	6°	8°	7°
All Dimensions in mm			

Suggested Pad Layout

Please see http://www.diodes.com/package-outlines.html for the latest version.

PowerDI5060-8



Dimensions	Value (in mm)
C	1.270
G	0.660
G1	0.820
X	0.610
X1	4.100
X2	0.755
X3	4.420
X4	5.610
Y	1.270
Y1	0.600
Y2	1.020
Y3	0.295
Y4	1.825
Y5	3.810
Y6	0.180
Y7	6.610

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