19-4240; Rev 0; 8/08

High-Voltage Liquid Lens Driver

General Description

The MAX14515 high-voltage liquid lens driver features a high-voltage differential output controlled through an I²C interface. The MAX14515 uses a charge-pump-based boost converter and integrated H-bridge to provide a compact lens driver solution with minimal external components to achieve a small overall footprint suitable for small space constraints inside camera modules.

The MAX14515 features an 8-bit monotonic DAC with a single differential high-voltage output controlled by a 2-wire I²C interface to set the amplitude. The high-voltage outputs are capable of delivering up to $42V_{RMS}$ (min) into a 220pF liquid lens load at 1.0kHz (min).

The MAX14515 also features two power-saving modes (shutdown mode and sleep mode) to minimize power consumption when the device is inactive. Shutdown mode places the device in a low-power state that resets all registers and disables the I²C interface to reduce current below 500nA (max). In sleep mode, the power-on reset circuit remains active. If no activity is detected on the I²C interface, current consumption is less than 3µA.

The MAX14515 operates over the +2.7V to +5.5V supply voltage range, ideal for portable applications using lithium ion battery sources. The MAX14515 is specified over the -40°C to +85°C extended temperature range and is available in a small (1mm x 2mm) 8-bump WLP package.

Applications

Autofocus Camera Modules

Barcode Readers

Webcams

Features

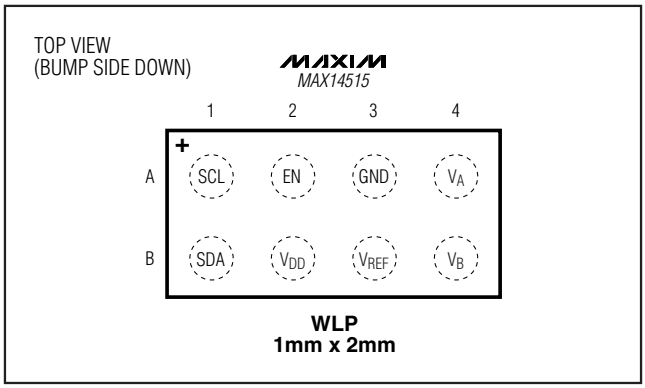
- **Small Footprint for Placement Inside Camera Modules**
- **47V_{RMS} Maximum Output (C_{LENS} = 220pF)**
- **I²C-Compatible Interface for Setting Output Voltage**
- **8-Bit Output Voltage Resolution**
- **Guaranteed Monotonic Output**
- **±15kV Human Body Model ESD Protection on Outputs**
- **Low 500nA (max) Shutdown Current**
- **+2.7V to +5.5V Input Voltage Range**
- **Space-Saving, 8-Bump WLP (1mm x 2mm) Package**

Ordering Information

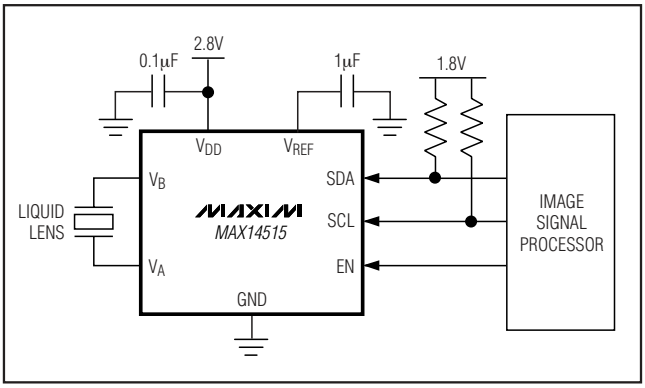
PART	TEMP RANGE	PIN-PACKAGE	TOP MARK
MAX14515EWA+	-40°C to +85°C	8 WLP	+AAA

+Denotes a lead-free/RoHS-compliant package.

Pin Configuration



Typical Application Circuit



High-Voltage Liquid Lens Driver

ABSOLUTE MAXIMUM RATINGS

(All voltages referenced to GND.)
V_{DD} .....-0.3V to +6.0V
V_A, V_B .....-0.3V to +52V
V_{REF}.....MAX (-0.3V, V_{DD} - 0.3V) to +6.0V
SDA, SCL, EN.....-0.3V to +6.0V
Continuous Power Dissipation (T_A = +70°C):
8-Bump WLP (derate 5.2mW/°C above +70°C).....416mW

Junction-to-Ambient Thermal Resistance (q_{JA}) (Note 1)
8-Bump WLP .....192°C/W
Operating Temperature Range .....-40°C to +85°C
Junction Temperature.....+150°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maxim-ic.com/thermal-tutorial**.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DD} = +2.7V to +5.5V, C_{VDD} = 0.1µF, C_{REF} = 1µF, C_{LENS} = 220pF, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{DD} = +2.8V and T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Input Voltage	V_{DD}			2.7		5.5	V
Input Supply Current	I_{DD}	Peak output voltage register (VP) = 0xFF			9		mA
Reference Output Voltage	V_{REF}					5.5	V
Shutdown Supply Current	I_{SHDN}	EN = GND			1	500	nA
Sleep Supply Current	I_{SLEEP}	$\overline{SM}$ = 0, SDA = SCL	V_{EN} = 1.8V, V_{DD} = 4.2V		8		µA
			V_{EN} = V_{DD}, V_{DD} = 2.8V		1.2	3	
POR Threshold	V_{TH_POR}					2.6	V
HIGH-VOLTAGE OUTPUTS (V_A, V_B)							
Peak Output Voltage (Note 3)	V_{PEAK}	VP = 0x01				10	V
		VP = 0xFF				52	
Output RMS Voltage	V_{RMS}	VP = 0x01				10	V
		VP = 0xFF		42		47	
Output Voltage Ripple	V_{RPL}	C_{LENS} = 120pF			±250		mV
Pulldown Strength	RL_{PD}	$\overline{SM}$ = 0				2	kΩ
Output Switching Frequency	f_{LENS}			1	1.1	1.2	kHz
CONTROL INPUTS (SDA, SCL, EN)							
Input Logic-High Voltage	V_{IH}			1.5			V
Input Logic-Low Voltage	V_{IL}					0.5	V
Output Logic-Low Voltage	V_{OL}	I_{SINK} = 3mA				0.4	V
Input Low Leakage Current	I_{IL}	EN = V_{CC}			0.01	6	µA
		EN = GND			0.01	0.5	
Input High Leakage Current	I_{IH}				0.01	2.5	µA
Input Capacitance	C_{IN}				10		pF

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = +2.7V to +5.5V, C_{VDD} = 0.1µF, C_{REF} = 1µF, C_{LENS} = 220pF, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{DD} = +2.8V and T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
OUTPUT-VOLTAGE STATIC PERFORMANCE (V_A, V_B)						
Resolution	N			8		Bits
Least Significant Bit	LSB	(Note 4)		157.5		mV
Integral Nonlinearity	INL		-4		+4	LSB
Differential Nonlinearity	DNL	(Note 5)	-1		+1	LSB
OUTPUT VOLTAGE DYNAMIC PERFORMANCE (V_A, V_B)						
Peak-Output Voltage Settling Time	t_{SV}	VP = any value to any other value transition; time to settle within 7 LSBs of final value, Figure 1			1	ms
Output Slew Rate	SR_V	Peak output voltage register = FFh			5	V/µs
Wake-Up Time	t_{WAKE}	Time to settle within 7 LSBs of peak value, Figure 1			2	ms
Shutdown Time	t_{SHDN}	Figure 2		100		µs
I^2C INTERFACE						
Serial-Clock Frequency	f_{SCL}				400	kHz
Bus Free Time Between START and STOP Condition	t_{BUF}		1.3			µs
Hold Time for Repeated START Condition	$t_{HD:STA}$		0.6			µs
Low Period for SCL Clock	t_{LOW}		1.3			µs
High Period for SCL Clock	t_{HIGH}		0.6			µs
Setup Time for Repeated START Condition	$t_{SU:STA}$		0.6			µs
Data Hold Time	$t_{HD:DAT}$		0		0.9	µs
Data Setup Time	$t_{SU:DAT}$		100			ns
Rise Time of Both SDA and SCL Signals	t_r				300	ns
Fall Time of Both SDA and SCL Signals	t_f				300	ns
Setup Time for STOP Condition	$t_{SU:STO}$		0.6			µs
Capacitive Load for Each Bus Line	C_b				400	pF
ESD PROTECTION						
V_A, V_B		Human Body Model		±15		kV
		IEC 61000-4-2		±4		
All Other Pins		Human Body Model		±2		kV

Note 2: All devices are tested at T_A = +25°C. All temperature limits are guaranteed by design.
Note 3: V_{PEAK} is the average peak output voltage of V_A or V_B.
Note 4: V_{PEAK} = 9.5V + (N-1) x 0.1575, (accuracy ±3%).
Note 5: Guaranteed monotonic.

Timing Diagrams

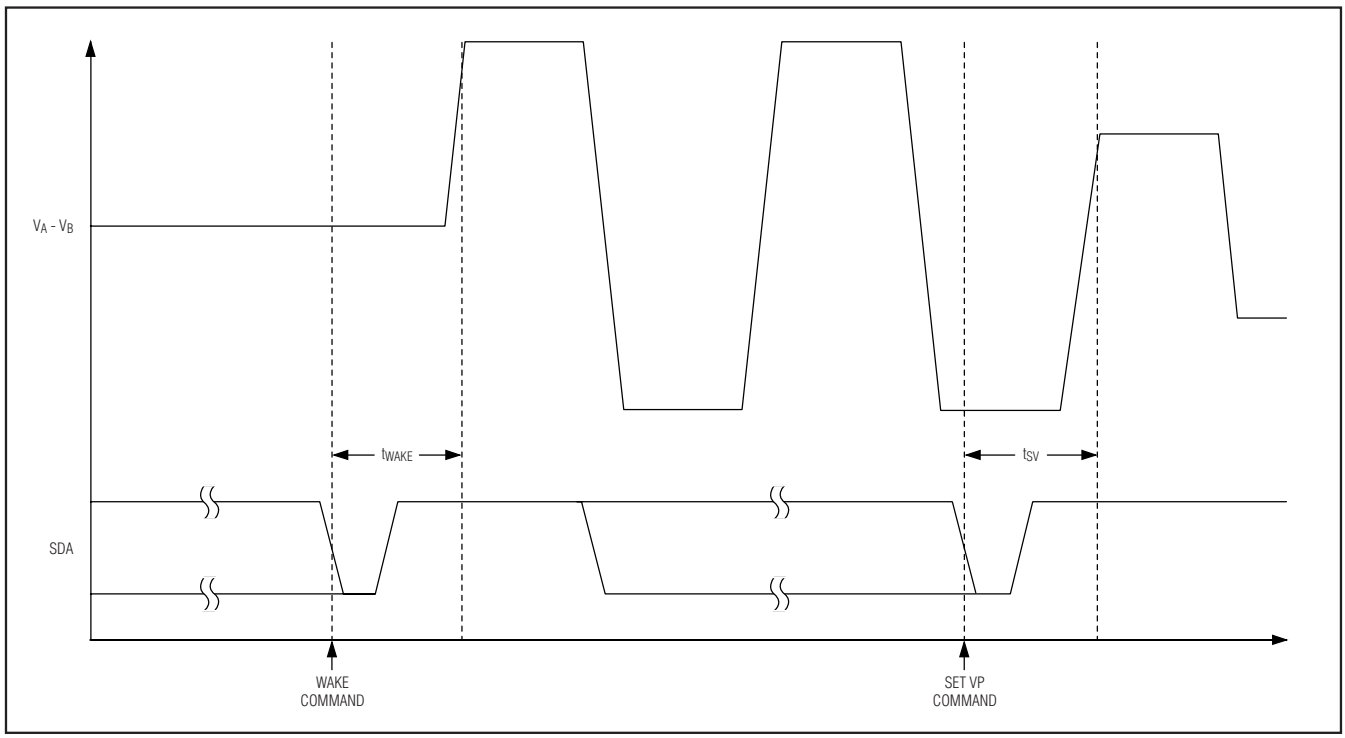


Figure 1. Wake-Up and Peak Output Voltage Settling Timing Diagram

Timing Diagrams (continued)

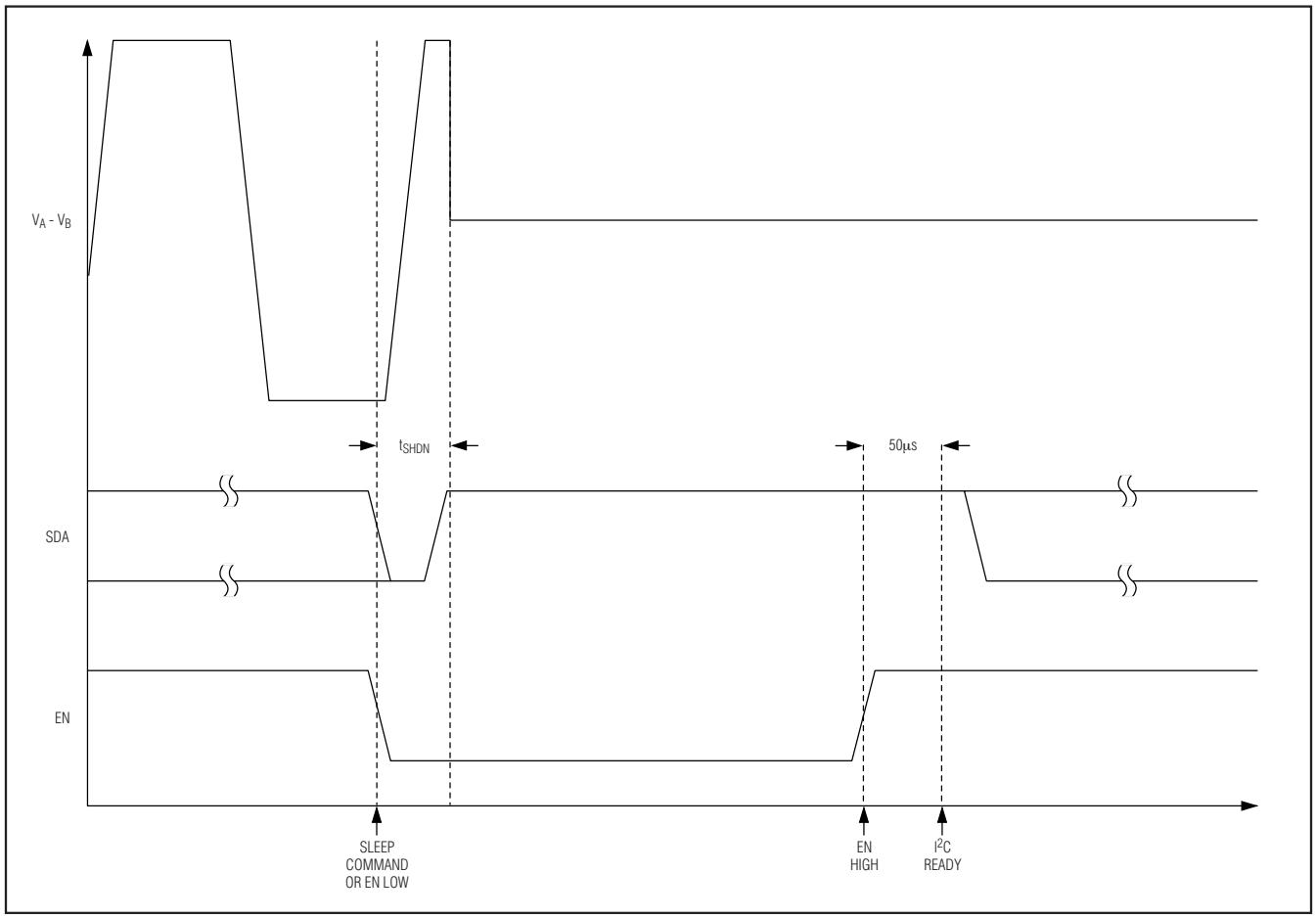


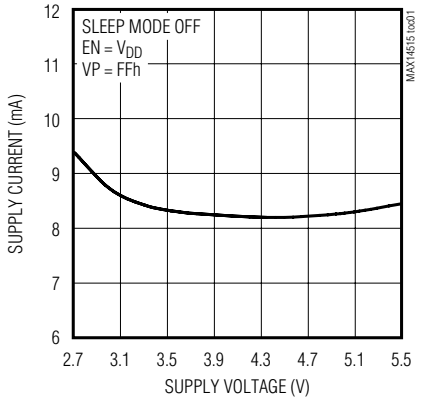
Figure 2. Shutdown/Sleep Mode Timing Diagram

High-Voltage Liquid Lens Driver

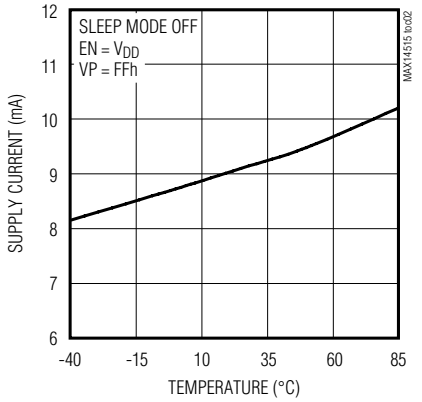
Typical Operating Characteristics

(V_{DD} = +2.8V, T_A = +25°C, C_{LENS} = 220pF, unless otherwise noted.)

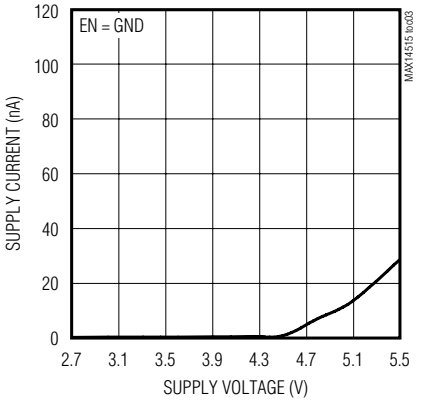
SUPPLY CURRENT vs. SUPPLY VOLTAGE



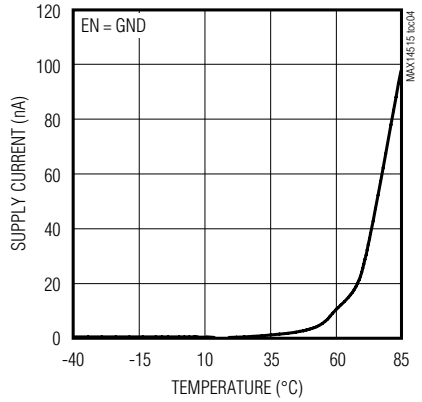
SUPPLY CURRENT vs. TEMPERATURE



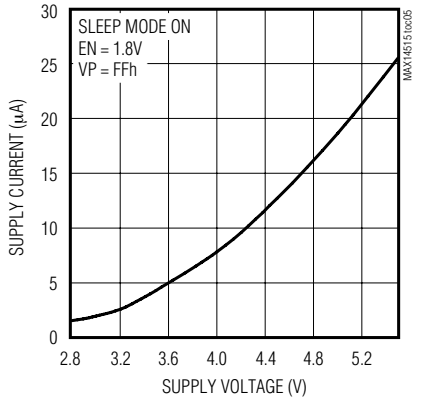
SHUTDOWN SUPPLY CURRENT vs. SUPPLY VOLTAGE



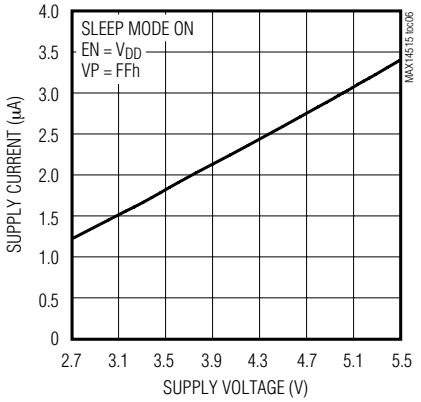
SHUTDOWN SUPPLY CURRENT vs. TEMPERATURE



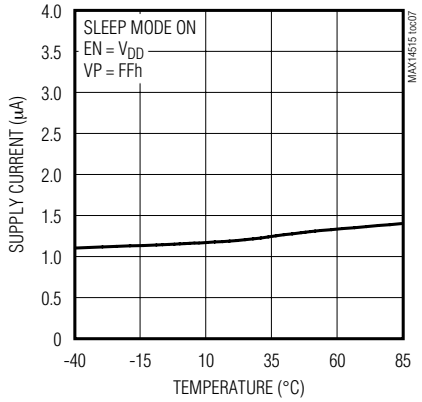
SLEEP MODE SUPPLY CURRENT vs. SUPPLY VOLTAGE



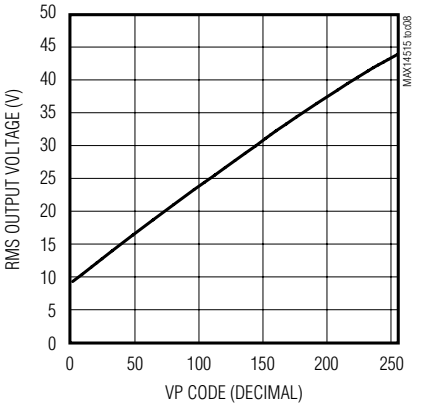
SLEEP MODE SUPPLY CURRENT vs. SUPPLY VOLTAGE



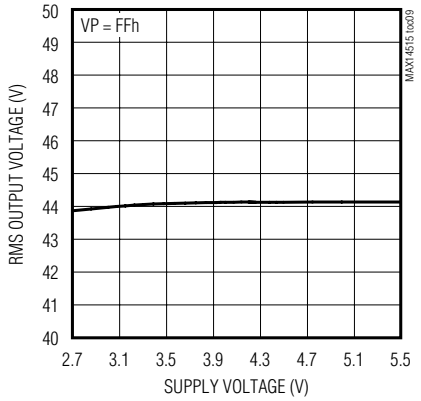
SLEEP MODE SUPPLY CURRENT vs. TEMPERATURE



RMS OUTPUT VOLTAGE vs. VP CODE



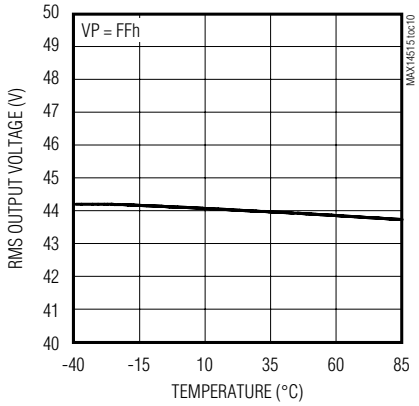
RMS OUTPUT VOLTAGE vs. SUPPLY VOLTAGE



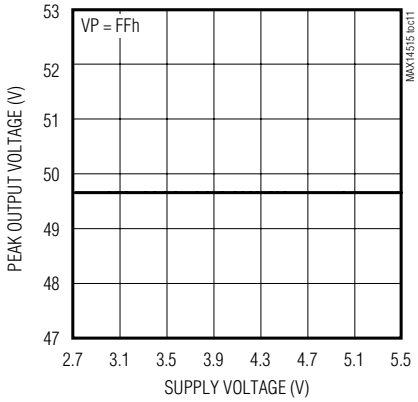
Typical Operating Characteristics (continued)

(V_{DD} = +2.8V, T_A = +25°C, C_{LENS} = 220pF, unless otherwise noted.)

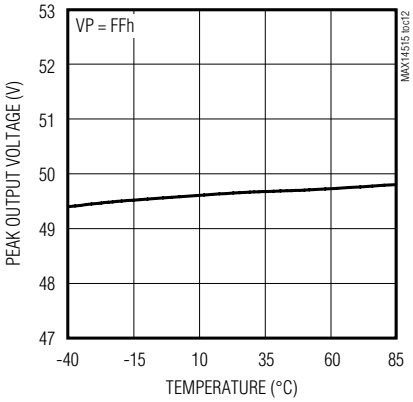
RMS OUTPUT VOLTAGE vs. TEMPERATURE



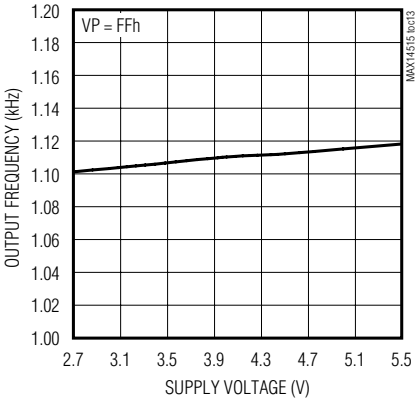
PEAK OUTPUT VOLTAGE vs. SUPPLY VOLTAGE



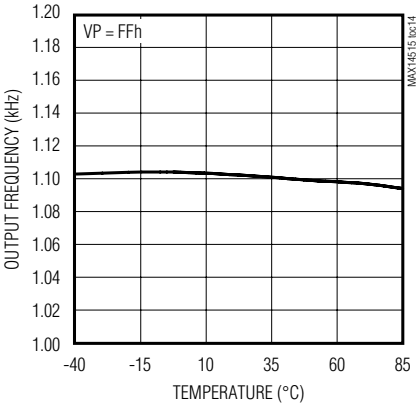
PEAK OUTPUT VOLTAGE vs. TEMPERATURE



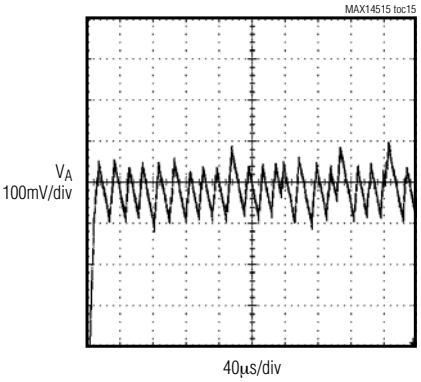
OUTPUT FREQUENCY vs. SUPPLY VOLTAGE



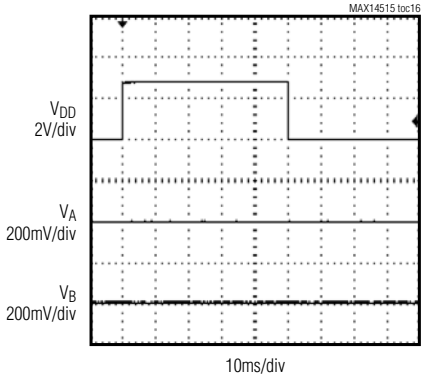
OUTPUT FREQUENCY vs. TEMPERATURE



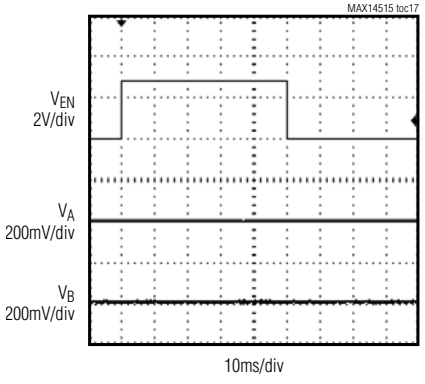
OUTPUT VOLTAGE RIPPLE



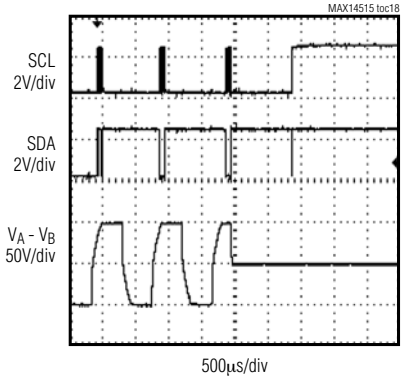
POWER-UP/-DOWN



POWER-UP/-DOWN



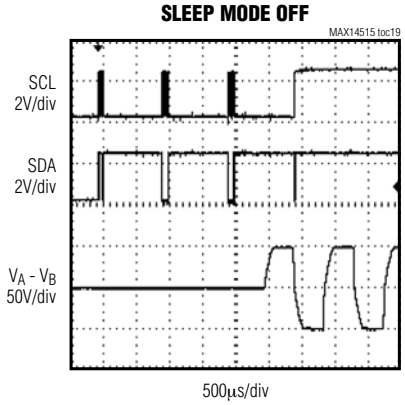
SLEEP MODE ON



High-Voltage Liquid Lens Driver

Typical Operating Characteristics (continued)

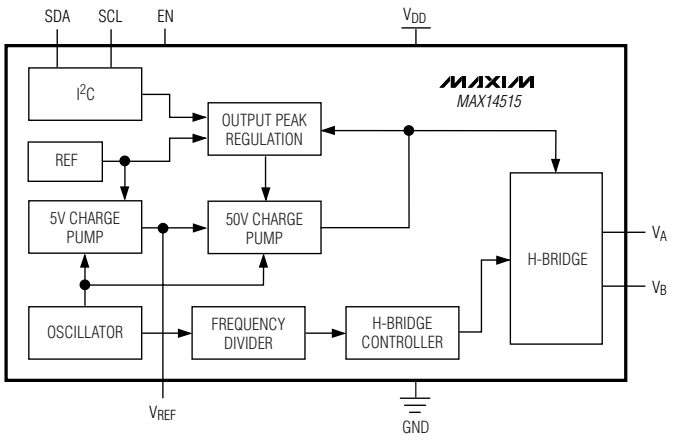
(V_{DD} = +2.8V, T_A = +25°C, C_{LENS} = 220pF, unless otherwise noted.)



Pin Description

PIN	NAME	FUNCTION
A1	SCL	I²C Open-Drain Serial Clock Input
B1	SDA	I²C Open-Drain Serial Data Input/Output
A2	EN	Enable Input. Drive EN high for normal operation. Drive EN low to enter shutdown mode.
B2	V_{DD}	Input Supply Voltage. Bypass V_{DD} to GND with a 0.1µF capacitor as close to the device as possible.
A3	GND	Ground
B3	V_{REF}	Reference Voltage. Connect a 1µF ceramic capacitor from V_{REF} to GND as close to the device as possible. V_{REF} is nominally +5V. Do not use V_{REF} to drive external circuitry.
A4	V_A	High-Voltage Output. Connect to terminal 1 of liquid lens.
B4	V_B	High-Voltage Output. Connect to terminal 2 of liquid lens.

Functional Diagram



Detailed Description

The MAX14515 high-voltage liquid lens driver utilizes a charge-pump-based boost converter and integrated H-bridge to provide a compact lens driver solution with minimal external components. This device features an 8-bit monotonic DAC controlled by a simple 2-wire I²C interface to set the peak amplitude of the high-voltage output.

Power-On Reset

When the MAX14515 initially powers up, all the registers are cleared and the device is in sleep mode.

High-Voltage Outputs (V_A, V_B)

Connect a liquid lens in between the high-voltage outputs (V_A, V_B) of the MAX14515. The peak output voltage of V_A and V_B is controlled by the value set in the high-voltage output register (VP). (See *Register Definition*). The internal H-bridge that drives V_A and V_B switches at 1.1kHz (typ).

Reference Output (V_{REF})

V_{REF} is the internal 5V charge-pump reference voltage of the MAX14515. Connect a 1µF ceramic capacitor from V_{REF} to GND. V_{REF} is not intended to drive external circuitry.

Shutdown Mode (EN)

The MAX14515 features a shutdown mode that reduces supply current to less than 500nA (max). In shutdown, all registers are in a reset state, and the I²C interface is disabled. Drive EN low to place the device in shutdown mode. Drive EN high for normal operation. Driving EN rail-to-rail minimizes power consumption.

Sleep Mode

When EN is high and the sleep mode bit ($\overline{SM}$) in the power mode register (see *Register Definition*) is reset, the device is in sleep mode. During sleep mode, only the power-on reset circuit remains active. If no activity is detected on the I²C interface, current consumption is less than 3µA.

I²C Serial Interface

Serial Addressing

The MAX14515 operates as a slave device that sends and receives data through an I²C-compatible 2-wire interface. The interface uses a serial-data line (SDA) and a serial-clock line (SCL) to achieve bidirectional communication between master(s) and slave(s). A master (typically a microcontroller) initiates all data transfers to and from the MAX14515, and generates the SCL clock that synchronizes the data transfer. The SDA line operates as both an input and an open-drain output. A pullup resistor is required on SDA. The SCL line

Register Definition

DEVICE ADDRESS				WRITE	0xEC
				READ	0xED
FIELD NAME	**READ WRITE**	**BITS**	**POWER-ON RESET**	**DESCRIPTION**	
POWER MODE (I²C ADDRESS = 0x00)					
RSVD	Read/Write	[7:1]	0000 000	Reserved. All bits must be set to 0.	
$\overline{SM}$	Read/Write	0	0	Sleep Mode Bit 0 = Sleep Mode 1 = Normal Operation All the registers keep the same values as before sleep unless a POR occurs.	
HIGH-VOLTAGE OUTPUT LEVEL (I²C ADDRESS = 0x01)					
VP(7:0)	Read/Write	[7:0]	0000 0000	Code 0x00 = $0V_{PEAK}$ Code 0x01 = $10V_{PEAK}$ Code 0xFF = $49.5V_{PEAK}$, linear scale. $V_{OUT(PEAK)} = 9.5V_{PEAK} + 0.1575V_{PEAK} \times (N - 1)$ where N = Code 0x01 to 0xFF in decimal. Accuracy (±3%).	

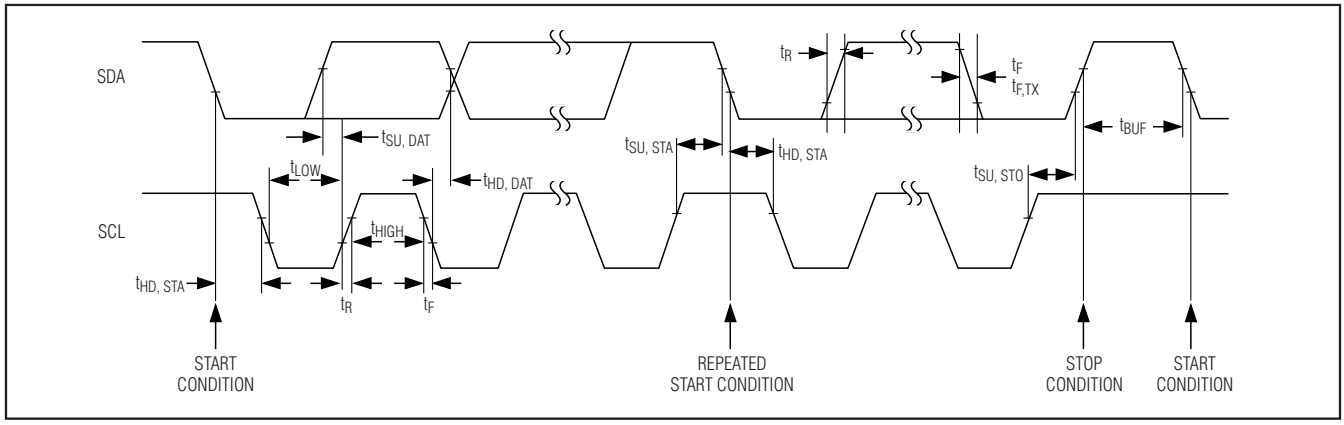


Figure 3. I²C Interface Timing Details

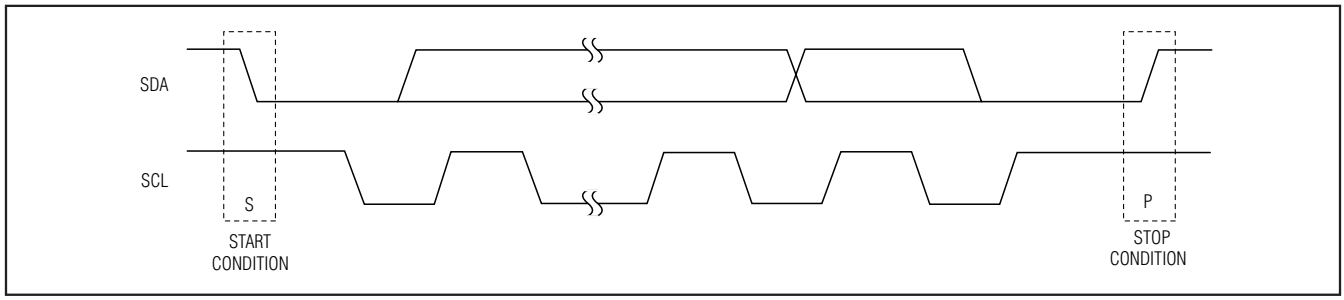


Figure 4. START and STOP Conditions

operates only as an input. A pullup resistor is required on SCL if there are multiple masters on the 2-wire interface, or if the master in a single-master system has an open-drain SCL output. Each transmission consists of a START condition sent by a master, followed by the MAX14515's 7-bit slave address plus R/W bit, a register address byte, 1 or more data bytes, and finally a STOP condition.

START and STOP Conditions

Both SCL and SDA remain high when the interface is not busy. A master signals the beginning of a transmission with a START (S) condition by transitioning SDA from high to low while SCL is high (Figure 4). When the master has finished communicating with the slave, it issues a STOP (P) condition by transitioning SDA from low to high while SCL is high. The bus is then free for another transmission.

Bit Transfer

One data bit is transferred during each clock pulse (Figure 5). The data on SDA must remain stable while SCL is high.

Acknowledge

The acknowledge bit is a clocked 9th bit (Figure 6), which the recipient uses to handshake receipt of each byte of data. Thus, each byte transferred effectively requires 9 bits. The master generates the 9th clock pulse, and the recipient pulls down SDA during the acknowledge clock pulse. The SDA line is stable low during the high period of the clock pulse. When the master is transmitting to the MAX14515, it generates the acknowledge bit because the MAX14515 is the recipient. When the MAX14515 is transmitting to the master, the master generates the acknowledge bit because the master is the recipient.

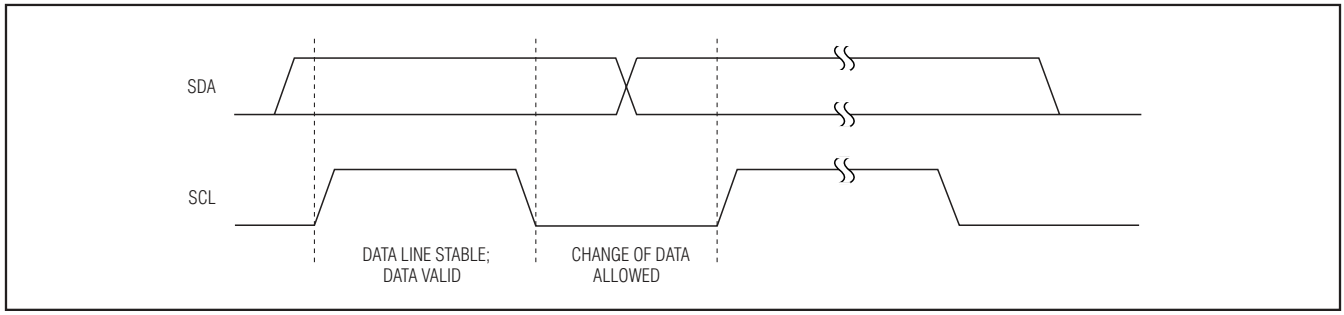


Figure 5. Bit Transfer

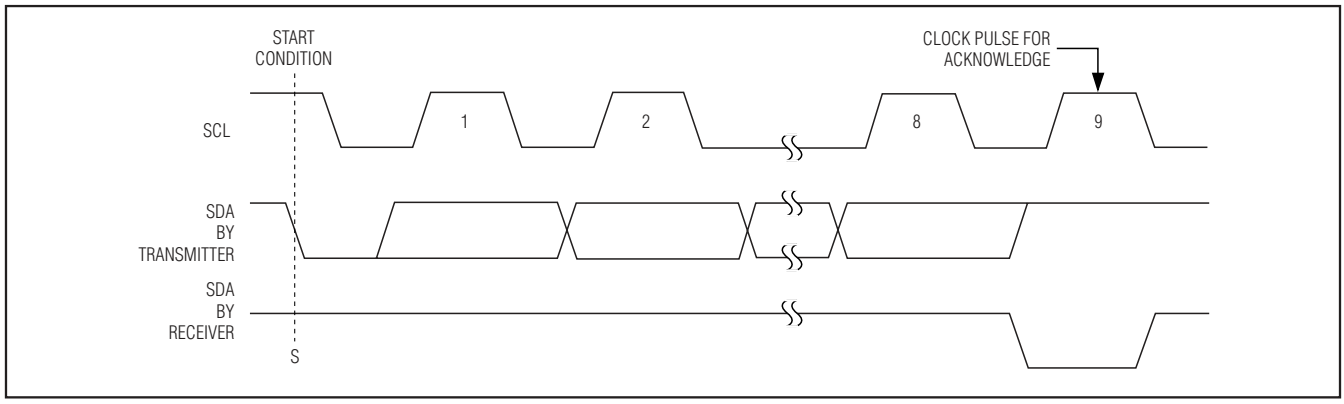


Figure 6. Acknowledge

Slave Address

The MAX14515 has a 7-bit long slave address. The bit following a 7-bit slave address is the R/$\overline{W}$ bit, which is low for a write command and high for a read command. The slave address is 0xEC for write commands and 0xED for read commands (Figure 7).

Format for Writing

A write to the MAX14515 comprises the transmission of the slave address with the R/W bit set to zero, followed by at least 1 byte of information. The first byte of information is the register address or command byte. The register address determines which register of the MAX14515 is to be written by the next byte, if received. If a STOP condition is detected after the register address is received, then the MAX14515 takes no further action beyond storing the register address (Figure 8). Any bytes received after the register address are data bytes. The first data byte goes into the register selected by the register address and subsequent data bytes go into subsequent registers (Figure 9). If multiple data bytes are transmitted before a STOP condition, these bytes are stored in subsequent registers because the register address autoincrements.

Format for Reading

The MAX14515 is read using the internally stored register address as an address pointer, the same way the stored register address is used as an address pointer for a write. The pointer autoincrements after each data byte is read using the same rules as for a write. Thus, a read is initiated by first configuring the register address by performing a write (Figure 10). The master can now read consecutive bytes from the MAX14515, with the first data byte being read from the register address pointed by the previously written register address. Once the master sounds a NACK, the MAX14515 stops sending valid data.

High-Voltage Liquid Lens Driver

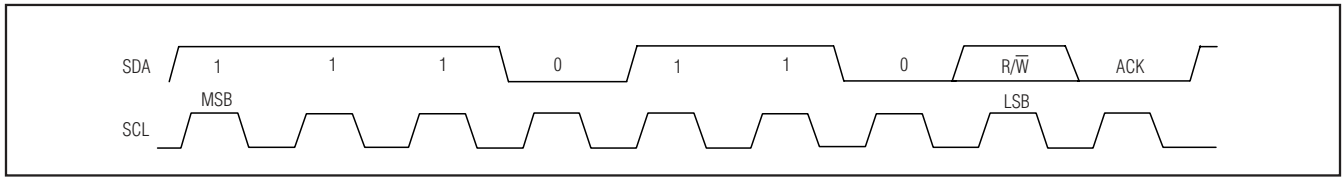


Figure 7. Slave Address

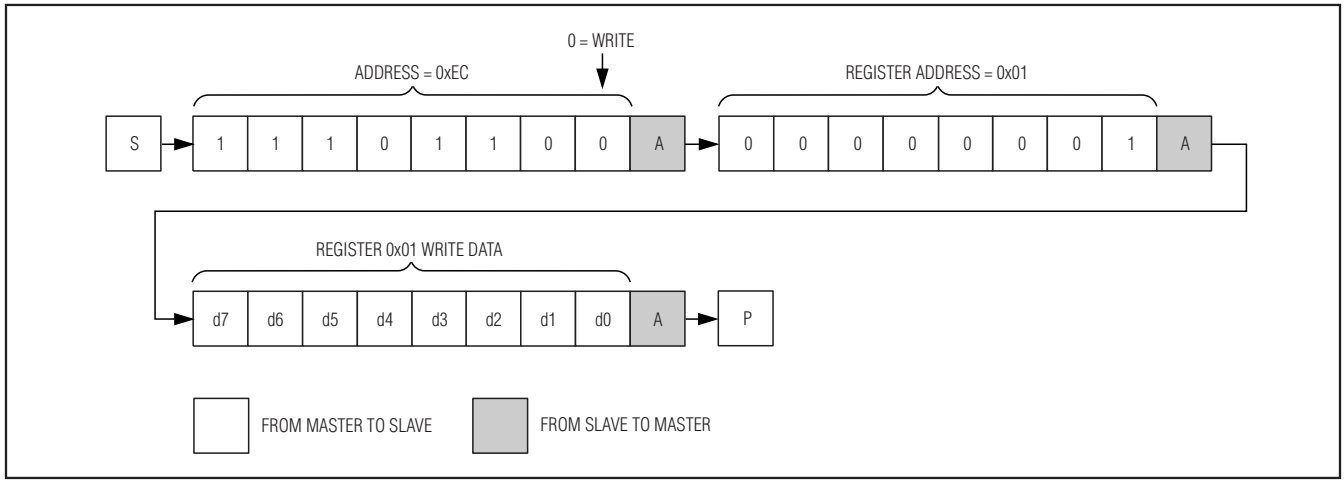


Figure 8. Format for I²C Write

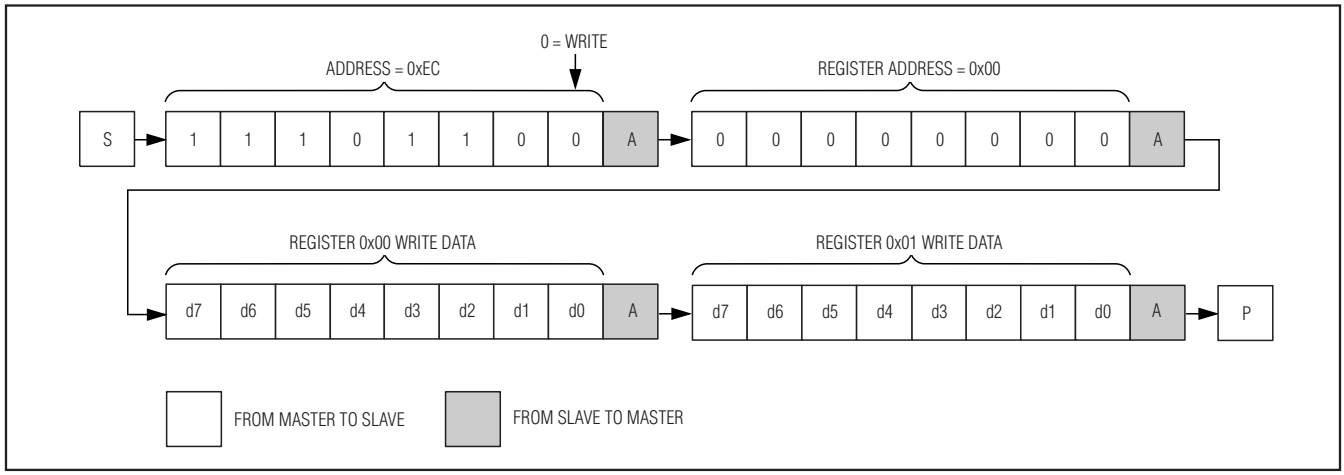


Figure 9. Format for Writing to Multiple Registers

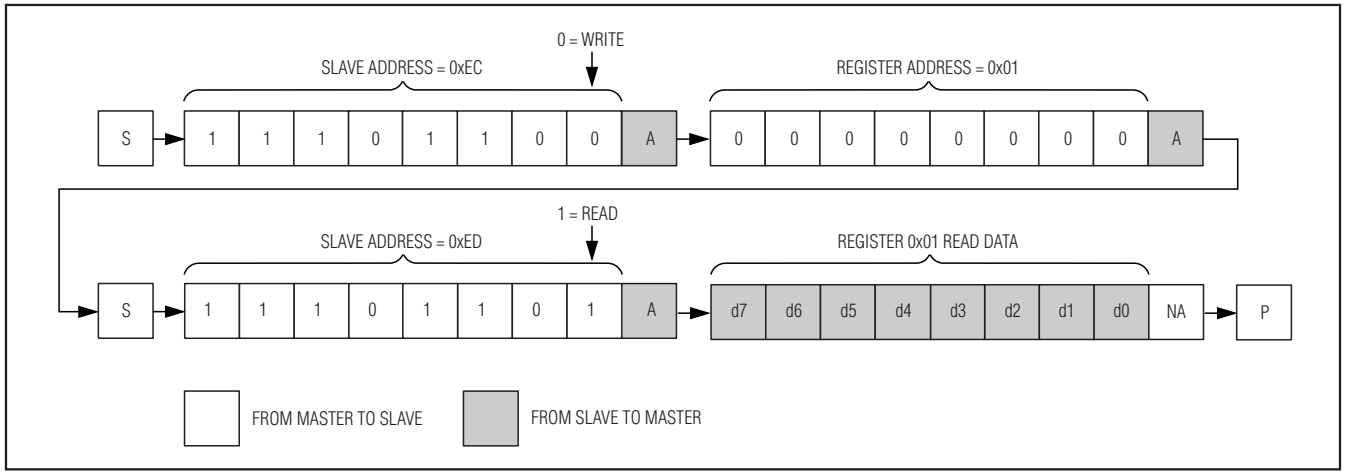


Figure 10. Format for Reading

Applications Information

Layout

Circuit board layout can significantly affect the performance of the MAX14515. Ensure that bypass capacitors are as close to the device as possible. Keep PCB traces as short as possible and minimize trace inductances to V_{DD}. Use large ground planes where possible.

ESD Protection

ESD performance depends on a number of conditions. The MAX14515 is rated for ±15kV (Human Body Model) and ±4kV (IEC 61000-4-2 Contact) typical ESD resistance on V_A and V_B. All other pins are rated for ±2kV (HBM) typical ESD resistance.

Human Body Model

Figure 11 shows the Human Body Model, and Figure 12 shows the current waveform it generates when discharged into a low impedance. This model consists of a 100pF capacitor charged to the ESD voltage of interest that is then discharged into the device through a 1.5kΩ resistor.

IEC 61000-4-2

The main difference between tests done using the Human Body Model and IEC 61000-4-2 is higher peak current in IEC 61000-4-2. Because series resistance is lower in the IEC 61000-4-2 ESD test model (Figure 13), the ESD-withstand voltage measured to this standard is generally lower than that measured using the Human Body Model. Figure 14 shows the current waveform for the IEC 61000-4-2 Level 4 ESD Contact Discharge test.

Chip Information

PROCESS: CMOS

High-Voltage Liquid Lens Driver

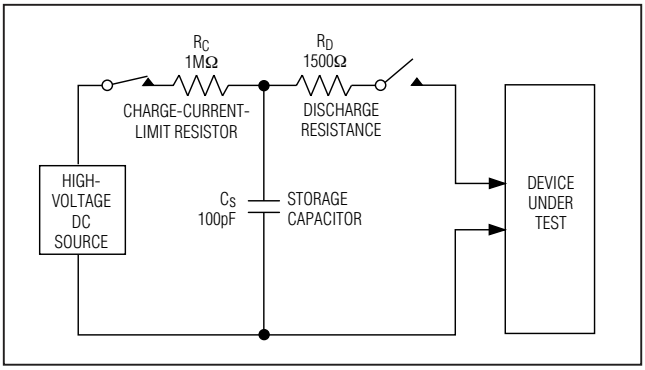


Figure 11. Human Body ESD Test Model

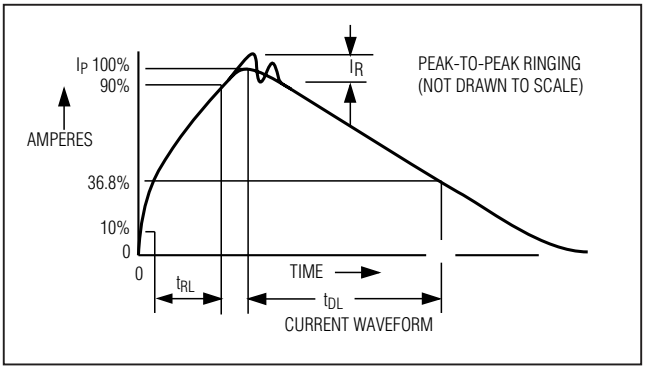


Figure 12. Human Body Current Waveform

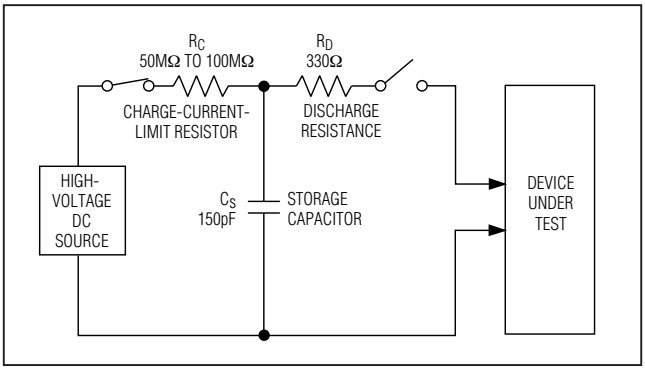


Figure 13. IEC 61000-4-2 ESD Test Model

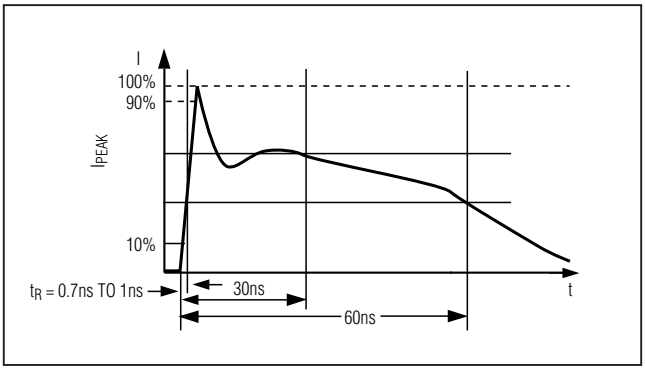


Figure 14. IEC 61000-4-2 ESD Generator Current Waveform

Package Information

For the latest package outline information and land patterns, go to **www.maxim-ic.com/packages**.

PACKAGE TYPE	PACKAGE CODE	DOCUMENT NO.
8 WLP	W81A2-1	**21-0210**