PE42553

Document Category: Product Specification

UltraCMOS® SPDT RF Switch, 9 kHz–8 GHz

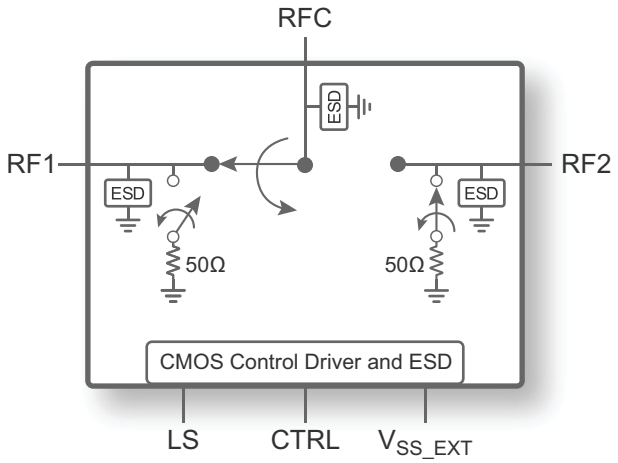
Features

- Excellent power handling: 36 dBm CW and 38 dBm pulsed power in 50Ω @ 8 GHz
- High linearity: IIP3 of 66 dBm
- High isolation
  - 45 dB @ 3 GHz
  - 41 dB @ 8 GHz
- HaRP™ technology enhanced
  - Fast settling time
  - No gate and phase lag
  - No drift in insertion loss and phase
- High ESD performance
  - 2.5 kV HBM on all pins, 4 kV HBM on RF pins to GND
  - 1 kV CDM on all pins
- Packaging – 16-lead 3 × 3 mm QFN

Applications

- Test and measurement
  - Signal sources
  - Communication testers
  - Spectrum analyzers
  - Network analyzers
- Automated test equipment
- General purpose TX/RX switch

Figure 1 • *PE42553 Functional Diagram*



Product Description

The PE42553 is a HaRP™ technology-enhanced absorptive SPDT RF switch that supports a broad frequency range from 9 kHz to 8 GHz. This general purpose switch maintains excellent linearity, high RF performance and fast settling time making this device ideal for test and measurement (T&M), automated test equipment (ATE) and other high performance wireless applications.

The PE42553 is a pin-compatible version of the PE42552 with improved power handling capability of 36 dBm continuous wave (CW) and 38 dBm pulsed power in 50Ω at 8 GHz. No blocking capacitors are required if DC voltage is not present on the RF ports. The PE42553 is manufactured on pSemi's UltraCMOS® process, a patented variation of silicon-on-insulator (SOI) technology on a sapphire substrate.

pSemi's HaRP technology enhancements deliver high linearity and excellent harmonics performance. It is an innovative feature of the UltraCMOS process, offering the performance of GaAs with the economy and integration of conventional CMOS.

Optional External V_{SS}

For proper operation, the V_{SS_EXT} pin must be grounded or tied to the V_{SS} voltage specified in **Table 2**. When the V_{SS_EXT} pin is grounded, FETs in the switch are biased with an internal negative voltage generator. For applications that require the lowest possible spur performance, V_{SS_EXT} can be applied externally to bypass the internal negative voltage generator.

Absolute Maximum Ratings

Exceeding absolute maximum ratings listed in **Table 1** may cause permanent damage. Operation should be restricted to the limits in **Table 2**. Operation between operating range maximum and absolute maximum for extended periods may reduce reliability.

ESD Precautions

When handling this UltraCMOS device, observe the same precautions as with any other ESD-sensitive devices. Although this device contains circuitry to protect it from damage due to ESD, precautions should be taken to avoid exceeding the rating specified in **Table 1**.

Latch-up Immunity

Unlike conventional CMOS devices, UltraCMOS devices are immune to latch-up.

Table 1 • *Absolute Maximum Ratings for PE42553*

Parameter/Condition	Min	Max	Unit
Supply voltage, V_{DD}	–0.3	5.5	V
Digital input voltage, CTRL	–0.3	3.6	V
LS input voltage	–0.3	3.6	V
RF input power, CW (RFC–RFX)[1] 9 kHz–10 MHz >10 MHz–8 GHz		 **Fig. 2, Fig. 3** 37	 dBm dBm
RF input power, pulsed (RFC–RFX)[2] 9 kHz–10 MHz >10 MHz–8 GHz		 **Fig. 2, Fig. 3** **Fig. 4, Fig. 5**	 dBm dBm
RF input power into terminated ports, CW (RFX)[1] 9–800 kHz >800 kHz–8 GHz		 **Fig. 2, Fig. 3** 28	 dBm dBm
Maximum junction temperature		+150	°C
Storage temperature range	–65	+150	°C

Table 1 • *Absolute Maximum Ratings for PE42553*

Parameter/Condition	Min	Max	Unit
ESD voltage HBM[3] RF pins to GND All pins		 4000 2500	 V V
ESD voltage MM, all pins[4]		200	V
ESD voltage CDM, all pins[5]		1000	V

Notes:
1) 100% duty cycle, all bands, 50Ω.
2) Pulsed, 5% duty cycle of 4620 µs period, 50Ω.
3) Human body model (MIL-STD 883 Method 3015).
4) Machine model (JEDEC JESD22-A115).
5) Charged device model (JEDEC JESD22-C101).

Recommended Operating Conditions

Table 2 list the recommending operating condition for PE42553. Devices should not be operated outside the recommended operating conditions listed below.

Table 2 • *Recommended Operating Condition for PE42553*

Parameter	Min	Typ	Max	Unit
Normal mode (V_{SS_EXT} = 0V)[1]				
Supply voltage, V_{DD}	2.3		5.5	V
Supply current, I_{DD}		120	200	µA
Bypass mode (V_{SS_EXT} = –3.4V, V_{DD} ≥ 3.4V for full spec. compliance)[2]				
Supply voltage, V_{DD}	2.6	3.4	5.5	V
Supply current, I_{DD}		50	80	µA
Negative supply voltage, V_{SS_EXT}	–3.6		–2.6	V
Negative supply current, I_{SS}	–40	–16		µA
Normal or Bypass mode				
Digital input high, CTRL	1.17		3.6	V
Digital input low, CTRL	–0.3		0.6	V
Digital input current, I_{CTRL}			10	µA
RF input power, CW (RFC–RFX)[3] 9 kHz–10 MHz >10 MHz–8 GHz			 Fig. 2, Fig. 3 36	 dBm dBm
RF input power, pulsed (RFC–RFX)[4] 9 kHz–10 MHz >10 MHz–8 GHz			 Fig. 2, Fig. 3 Fig. 4, Fig. 5	 dBm dBm
RF input power, hot switch, CW[3] 9–300 kHz >300 kHz–8 GHz			 Fig. 2, Fig. 3 20	 dBm dBm
RF input power into terminated ports, CW (RFX)[3] 9–600 kHz >600 kHz–8 GHz			 Fig. 2, Fig. 3 26	 dBm dBm
Operating temperature range	–40	+25	+85	°C

Notes:

1) Normal mode: connect V_{SS_EXT} (pin 13) to GND (V_{SS_EXT} = 0V) to enable internal negative voltage generator.
2) Bypass mode: use V_{SS_EXT} (pin 13) to bypass and disable internal negative voltage generator.
3) 100% duty cycle, all bands, 50Ω.
4) Pulsed, 5% duty cycle of 4620 µs period, 50Ω.

Electrical Specifications

Table 3 provides the PE42553 key electrical specifications at 25 °C (Z_S = Z_L = 50Ω), unless otherwise specified. Normal mode[1] is at V_{DD} = 3.3V and V_{SS_EXT} = 0V. Bypass mode[2] is at V_{DD} = 3.4V and V_{SS_EXT} = –3.4V.

Table 3 • *PE42553 Electrical Specifications*

Parameter	Path	Condition	Min	Typ	Max	Unit
Operating frequency			9 kHz		8 GHz	As shown
Insertion loss	RFC–RFX	9 kHz–10 MHz 10 MHz–3 GHz 3–8 GHz		0.60 0.80 0.85	0.80 1.00 1.05	dB dB dB
Isolation	RFX–RFX	9 kHz–10 MHz 10 MHz–3 GHz 3–8 GHz	70 46 33	90 54 36		dB dB dB
	RFC–RFX	9 kHz–10 MHz 10 MHz–3 GHz 3–8 GHz	80 42 38	90 45 41		dB dB dB
Return loss (active port)	RFC–RFX	9 kHz–10 MHz 10 MHz–3 GHz 3–8 GHz		23 17 15		dB dB dB
Return loss (RFC port)	RFC–RFX	9 kHz–10 MHz 10 MHz–3 GHz 3–8 GHz		23 17 15		dB dB dB
Return loss (terminated port)	RFX	9 kHz–10 MHz 10 MHz–3 GHz 3–8 GHz		32 24 19		dB dB dB
Input 0.1dB compression point[3]	RFC–RFX	10 MHz–8 GHz		**Fig. 4** **Fig. 5**		dBm dBm
Input IP2	RFC–RFX	834 MHz, 1950 MHz		120		dBm
Input IP3	RFC–RFX	834 MHz, 1950 MHz and 2700 MHz		66		dBm
Settling time		50% CTRL to 0.05 dB final value		15	20	µs
Switching time		50% CTRL to 90% or 10% of RF		5.5	9.5	µs

Notes:

1) Normal mode: connect V_{SS_EXT} (pin 29) to GND (V_{SS_EXT} = 0V) to enable internal negative voltage generator.
2) Bypass mode: use V_{SS_EXT} (pin 29) to bypass and disable internal negative voltage generator.
3) The input 0.1dB compression point is a linearity figure of merit. Refer to **Table 2** for the RF input power (50Ω).

Switching Frequency

The PE42553 has a maximum 25 kHz switching rate in normal mode (pin 13 tied to ground). A faster switching rate is available in bypass mode (pin 13 tied to V_{SS_EXT}). The rate at which the PE42553 can be switched is then limited to the switching time as specified in **Table 3**.

Switching frequency describes the time duration between switching events. Switching time is the time duration between the point the control signal reached 50% of the final value and the point the output signal reaches within 10% or 90% of its target value.

Spur-Free Performance

The typical spurious performance of the PE42553 in normal mode is –152 dBm (pin 13 tied to ground). If spur-free performance is desired, the internal negative voltage generator can be disabled by applying a negative voltage to V_{SS_EXT} (pin 13).

Thermal Data

Psi-JT (Ψ_{JT}), junction top-of-package, is a thermal metric to estimate junction temperature of a device on the customer application PCB (JEDEC JESD51-2).

$$\Psi_{JT} = (T_J - T_T)/P$$

where

Ψ_{JT} = junction-to-top of package characterization parameter, °C/W

T_J = die junction temperature, °C

T_T = package temperature (top surface, in the center), °C

P = power dissipated by device, Watts

Table 4 • *Thermal Data for PE42553*

Parameter	Typ	Unit
Ψ_{JT}	41	°C/W
Θ_{JA}, junction-to-ambient thermal resistance	93	°C/W

Control Logic

Table 5 provides the control logic truth table for the PE42553.

Table 5 • *Truth Table for PE42553*

LS	CTRL	RFC–RF1	RFC–RF2
0	0	OFF	ON
0	1	ON	OFF
1	0	ON	OFF
1	1	OFF	ON

Logic Select

The Logic Select feature is used to determine the definition for the CTRL pin.

Figure 2 • *Power De-rating Curve for 9 kHz–10 MHz @ 25 °C Ambient (50Ω)*(*)

Note: * $V_{SS\_EXT} = -V_{DD}$.

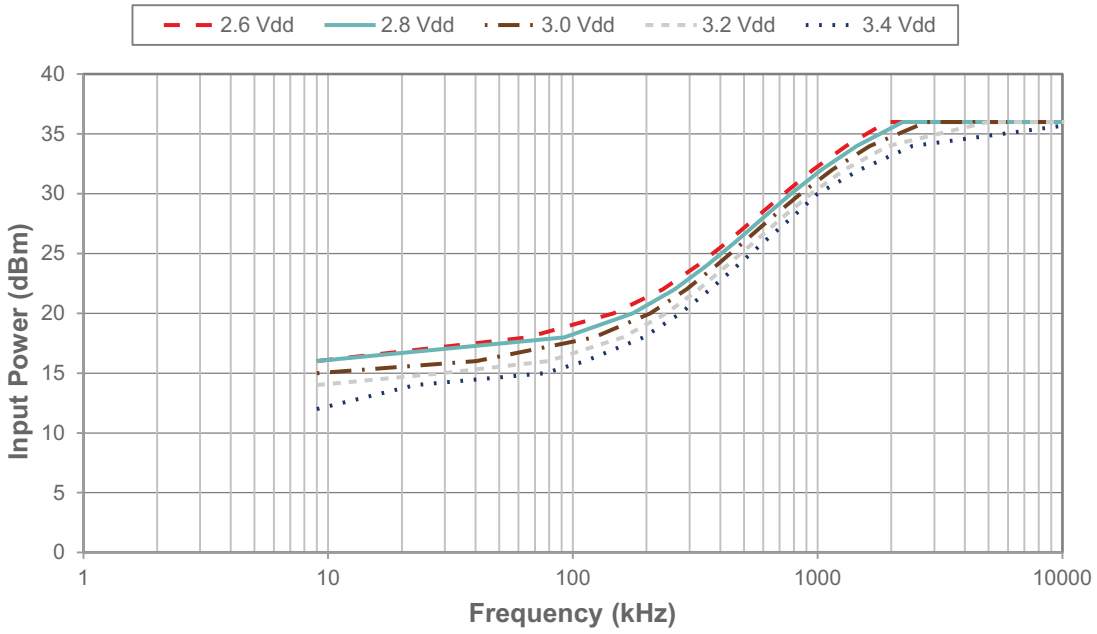


Figure 3 • *Power De-rating Curve for 9 kHz–10 MHz @ 85 °C Ambient (50Ω)*(*)

Note: * $V_{SS\_EXT} = -V_{DD}$.

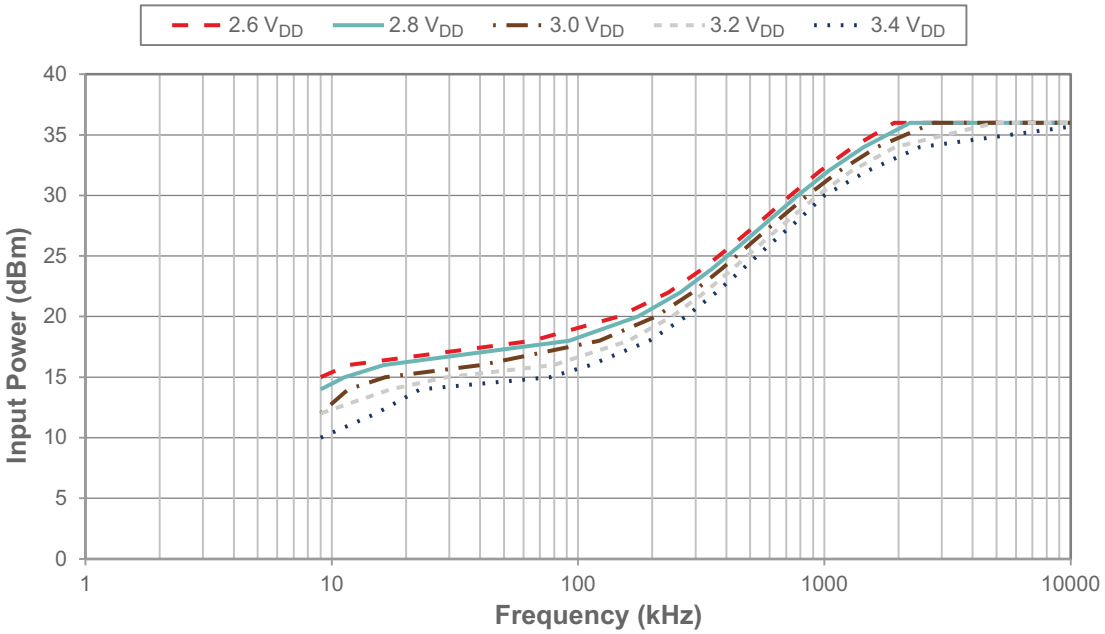


Figure 4 • *Power De-rating Curve for 10 MHz–8 GHz @ 25 °C Ambient (50Ω)*(*)

Note: * Normal mode at 2.3V ≥ V_{DD} ≥ 5.5V and V_{SS_EXT} = 0V, Bypass mode at V_{DD} = 3.4V and V_{SS_EXT} = –3.4V.

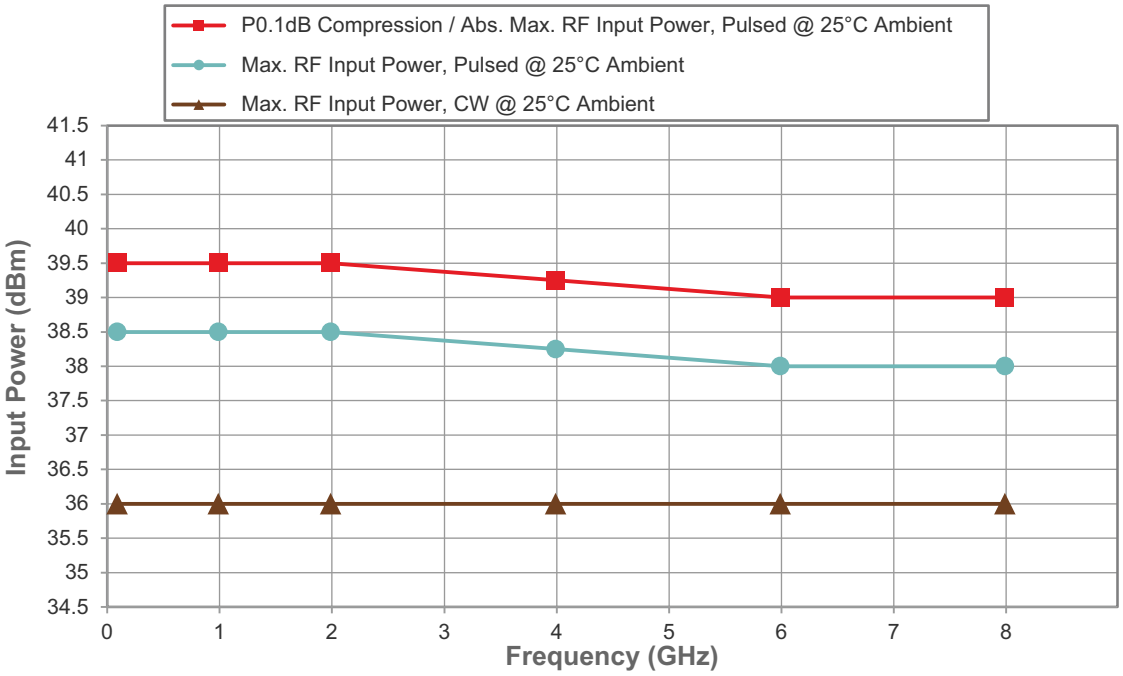
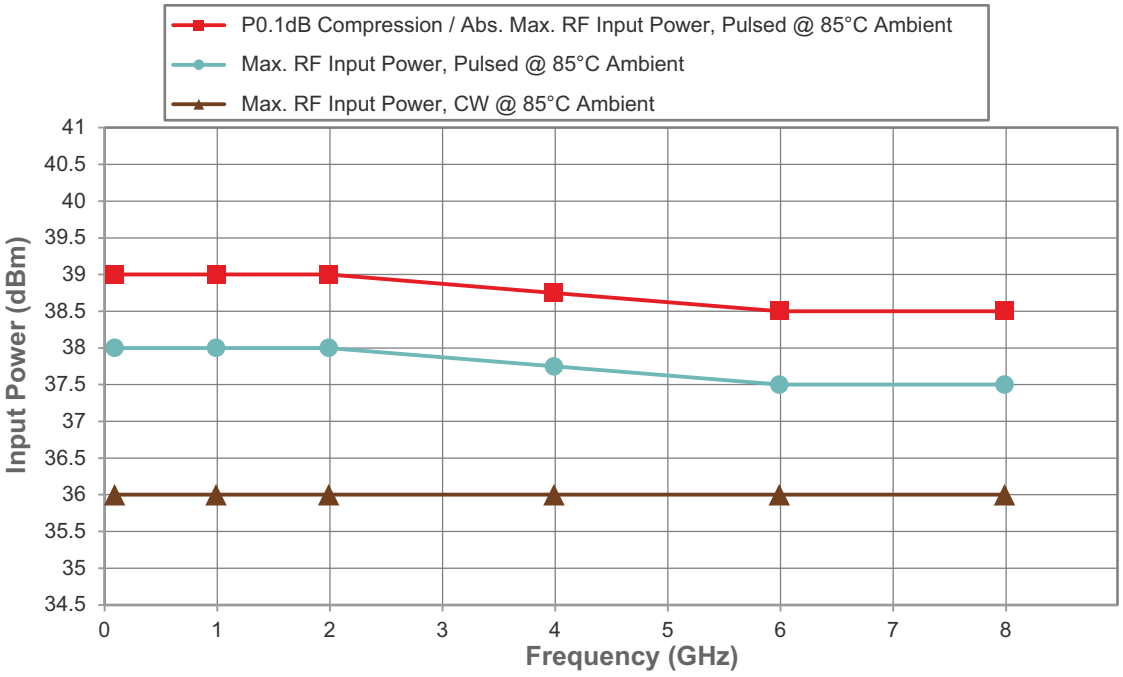


Figure 5 • *Power De-rating Curve for 10 MHz–8 GHz @ 85 °C Ambient (50Ω)*(*)

Note: * Normal mode at 2.3V ≥ V_{DD} ≥ 5.5V and V_{SS_EXT} = 0V, Bypass mode at V_{DD} = 3.4V and V_{SS_EXT} = –3.4V.



Typical Performance Data

Figure 6–Figure 17 show the typical performance data @ 25 °C and V_{DD} = 3.4V (Z_S = Z_L = 50Ω), unless otherwise specified.

Figure 6 • ***Insertion Loss vs Temperature (RFC–RFX)***

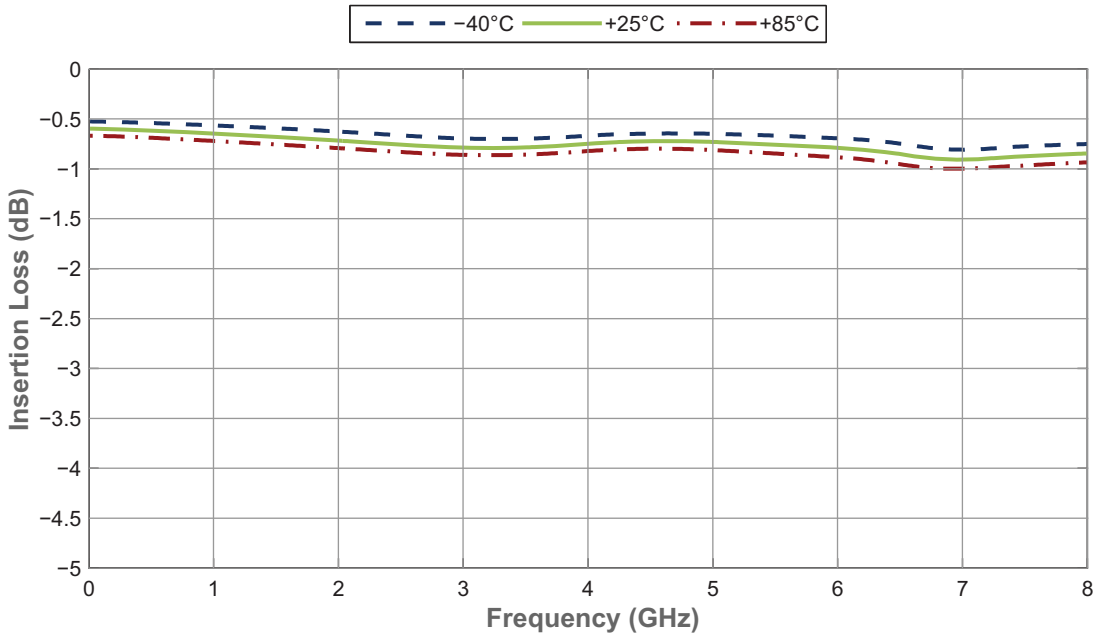


Figure 7 • *Insertion Loss vs V_{DD} (RFC–RFX)*

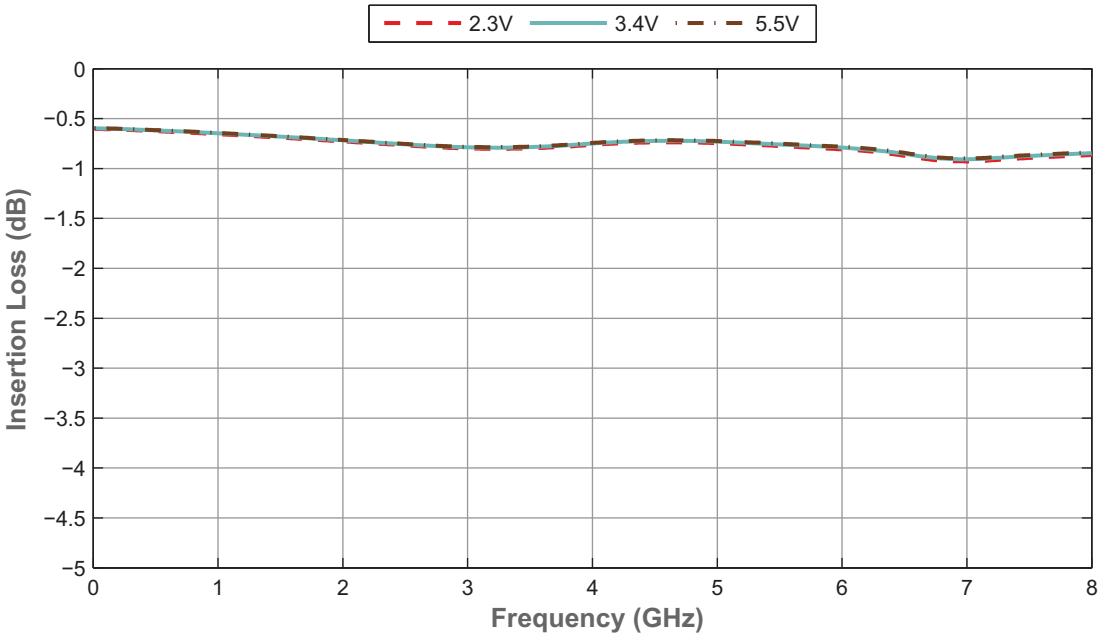


Figure 8 • *RFC Port Return Loss vs Temperature*

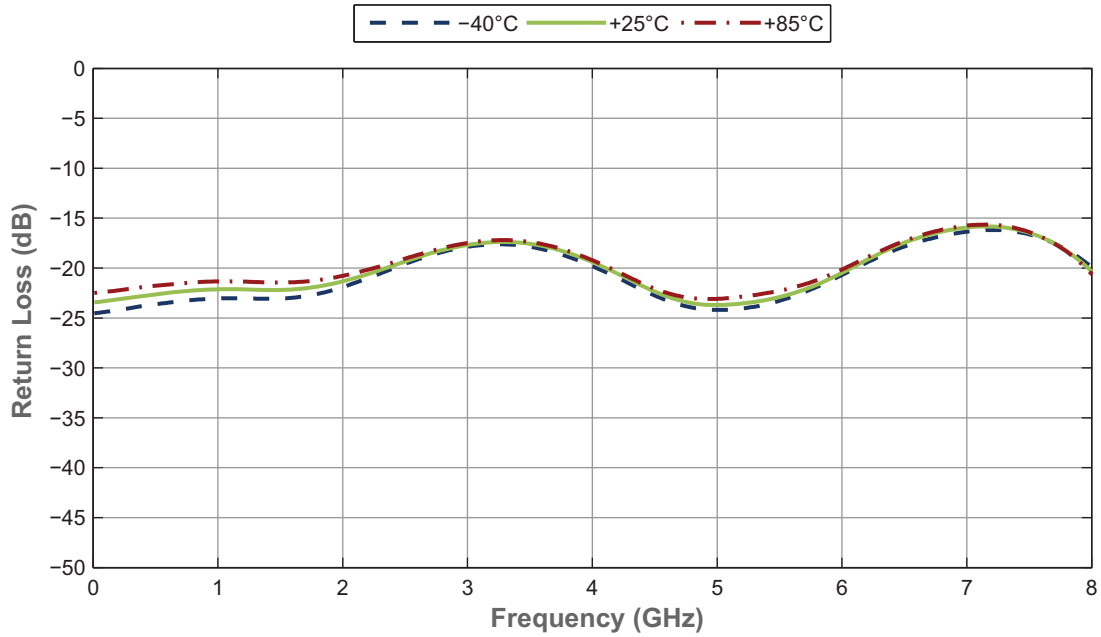


Figure 9 • *RFC Port Return Loss vs V_{DD}*

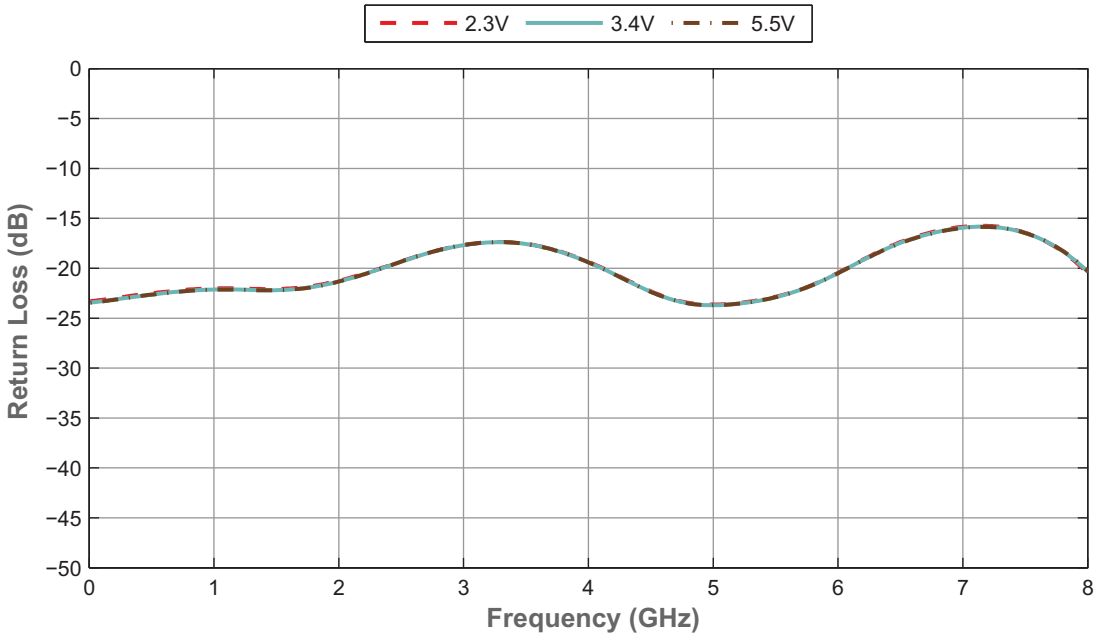


Figure 10 • *Active Port Return Loss vs Temperature*

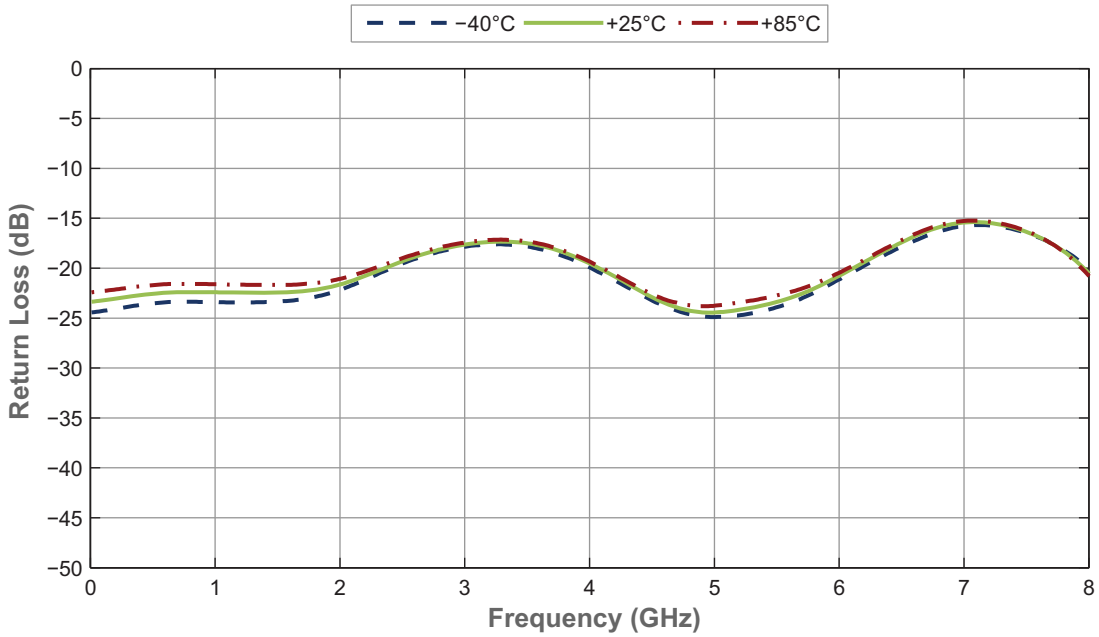


Figure 11 • *Active Port Return Loss vs V_{DD}*

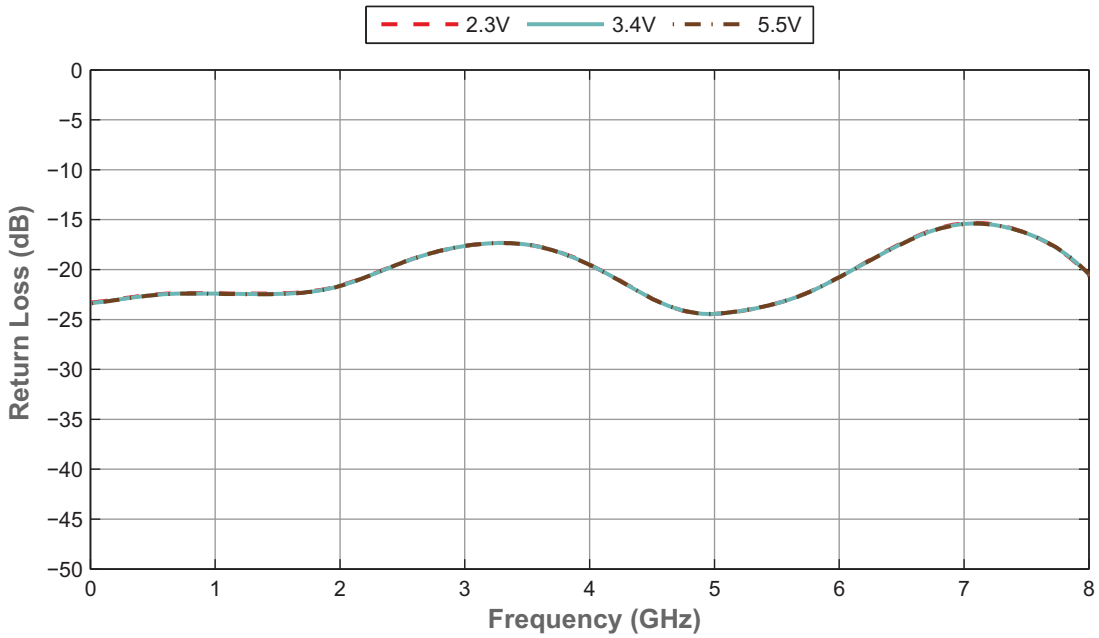


Figure 12 • *Terminated Port Return Loss vs Temperature*

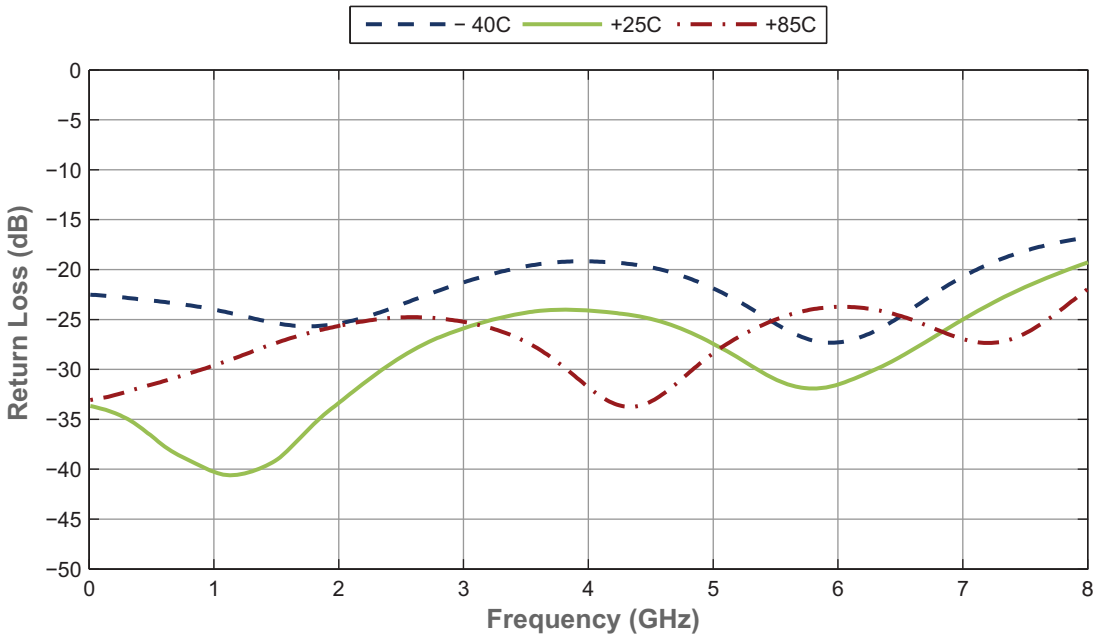


Figure 13 • *Terminated Port Return Loss vs V_{DD}*

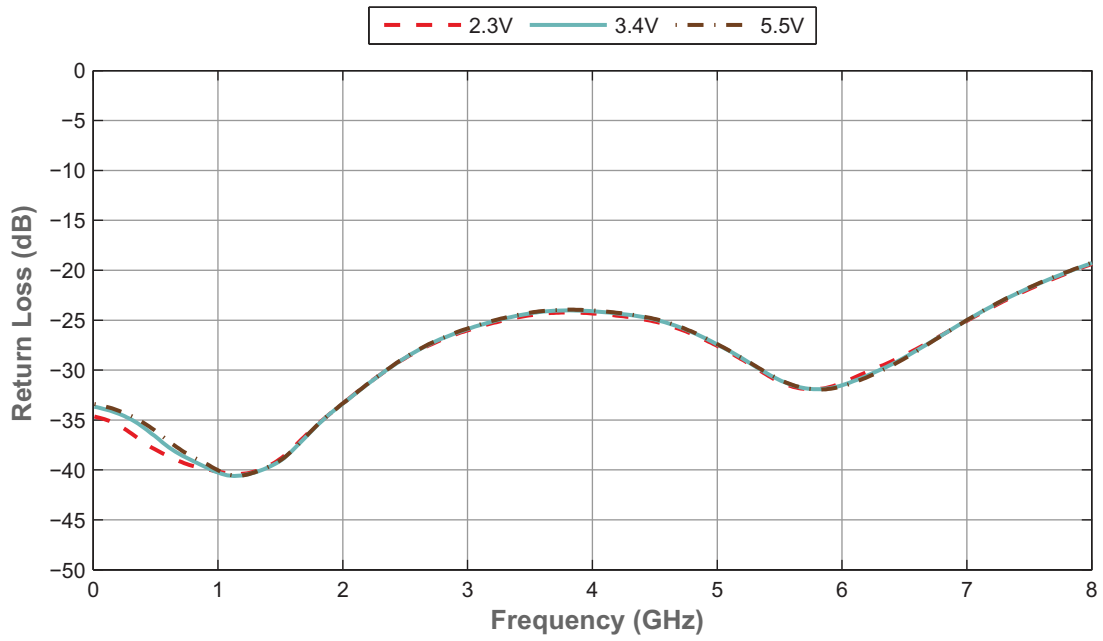


Figure 14 • *Isolation vs Temperature (RFX–RFX)*

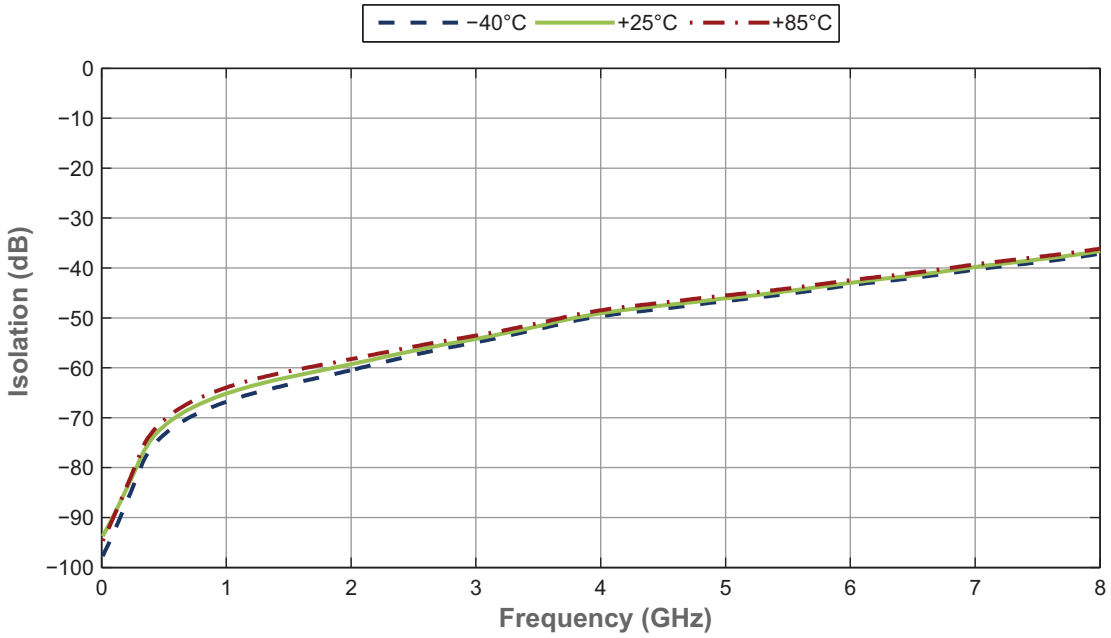


Figure 15 • *Isolation vs V_{DD} (RFX–RFX)*

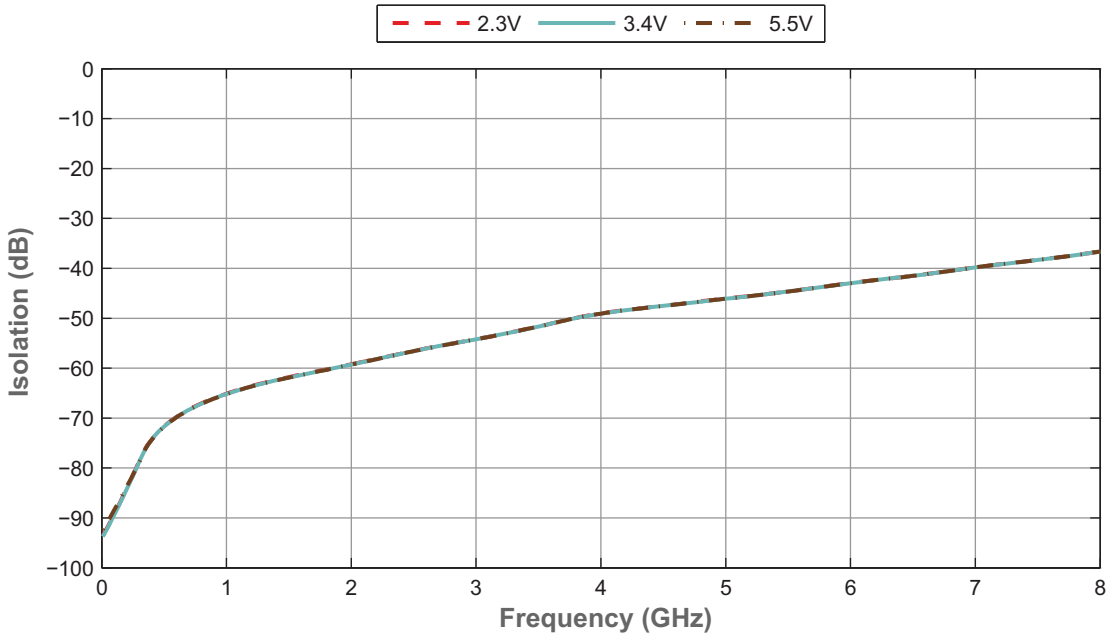


Figure 16 • *Isolation vs Temperature (RFC–RFX)*

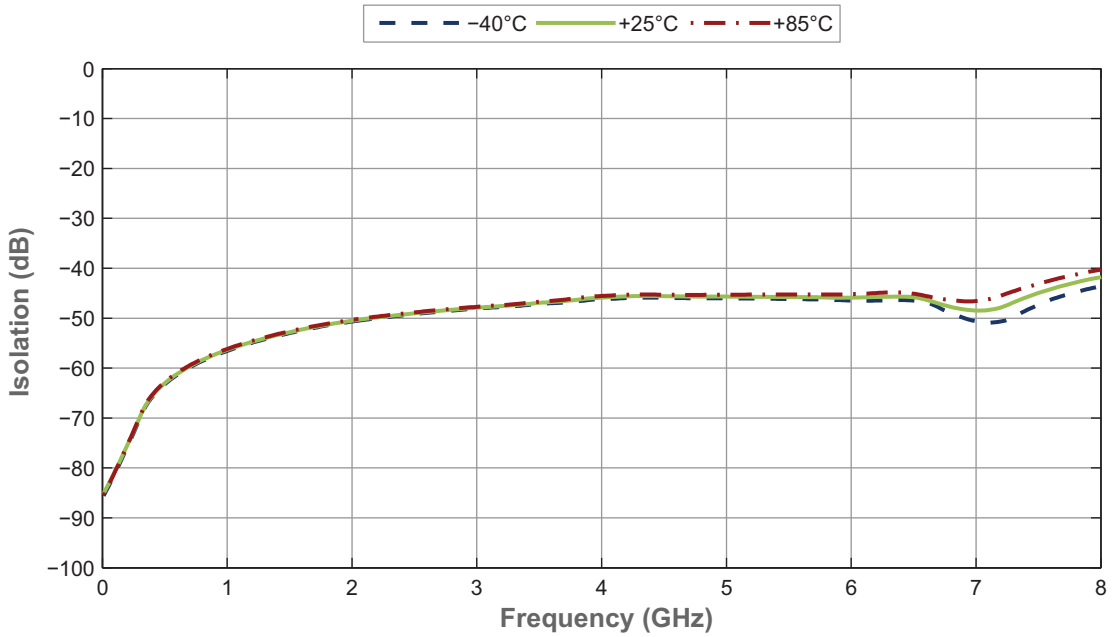
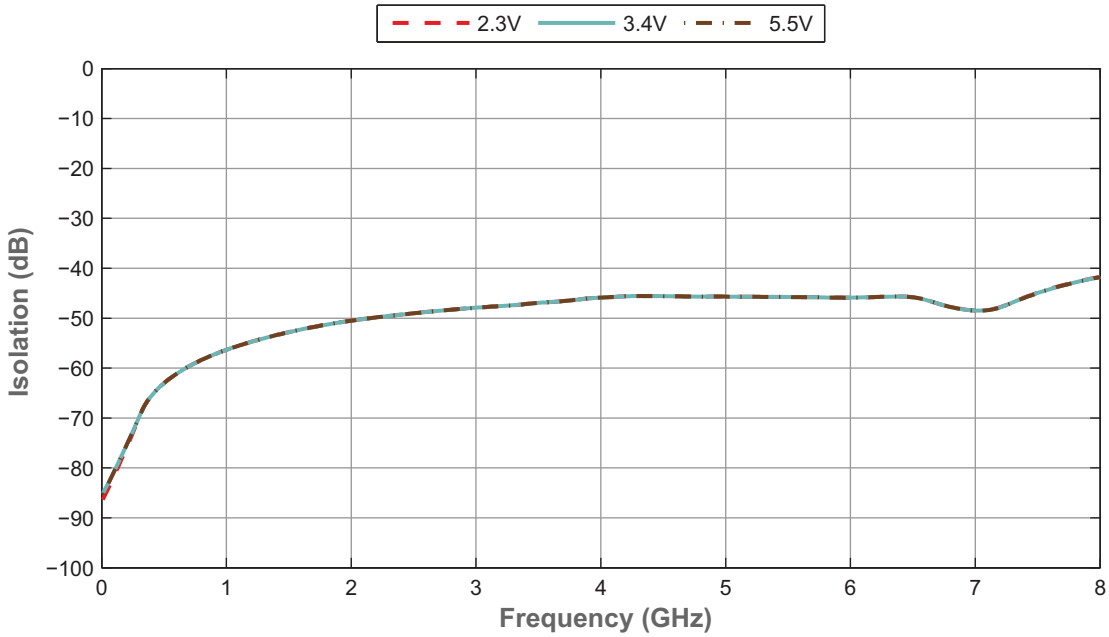


Figure 17 • *Isolation vs V_{DD} (RFC–RFX)*

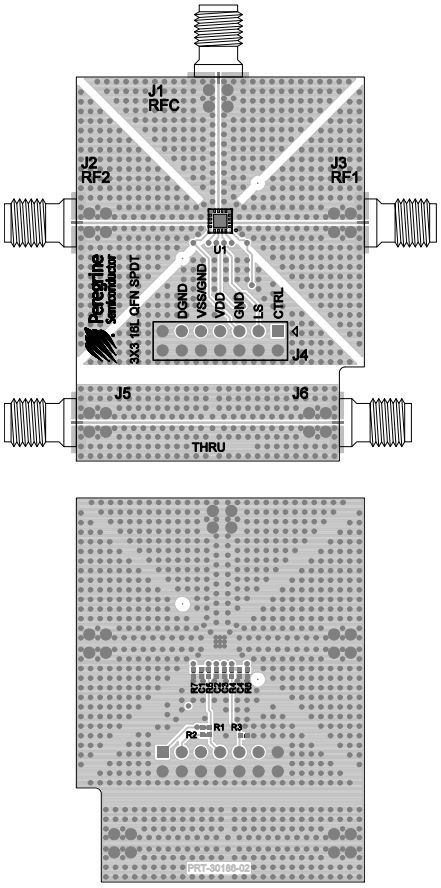


Evaluation Kit

The SPDT switch evaluation board was designed to ease customer evaluation of pSemi's PE42553. The RF common port is connected through a 50Ω transmission line via the SMA connector, J1. RF1 and RF2 ports are connected through 50Ω transmission lines via SMA connectors J2 and J3, respectively. A 50Ω through transmission line is available via SMA connectors J5 and J6, which can be used to de-embed the loss of the PCB. J4 provides DC and digital inputs to the device.

For the true performance of the PE42553 to be realized, the PCB must be designed in such a way that RF transmission lines and sensitive DC I/O traces are well isolated from one another.

Figure 18 • *Evaluation Kit Layout for PE42553*



Pin Information

This section provides pinout information for the PE42553. **Figure 19** shows the pin map of this device for the available package. **Table 6** provides a description for each pin.

Figure 19 • *Pin Configuration (Top View)*

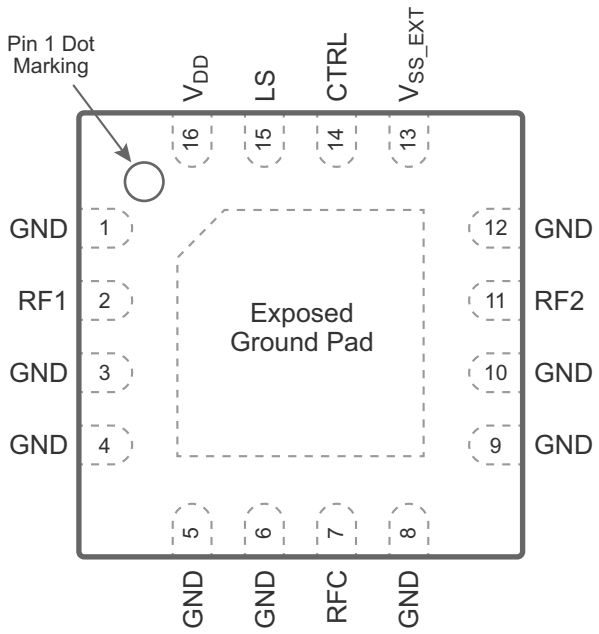


Table 6 • *Pin Descriptions for PE42553*

Pin No.	Pin Name	Description
1, 3–6, 8–10, 12	GND	Ground
2	RF1[1]	RF port 1
7	RFC[1]	RF common
11	RF2[1]	RF port 2
13	V_{SS_EXT}[2]	External V_{SS} negative voltage control
14	CTRL	Digital control logic input
15	LS	Logic Select: used to determine the definition for the CTRL pin (see **Table 5**)
16	V_{DD}	Supply voltage
Pad	GND	Exposed pad: ground for proper operation

Notes:

1) RF pins 2, 7 and 11 must be at 0 VDC. The RF pins do not require DC blocking capacitors for proper operation if the 0 VDC requirement is met.
2) Use V_{SS_EXT} (pin 13) to bypass and disable internal negative voltage generator. Connect V_{SS_EXT} (pin 13) to GND (V_{SS_EXT} = 0V) to enable internal negative voltage generator.

Packaging Information

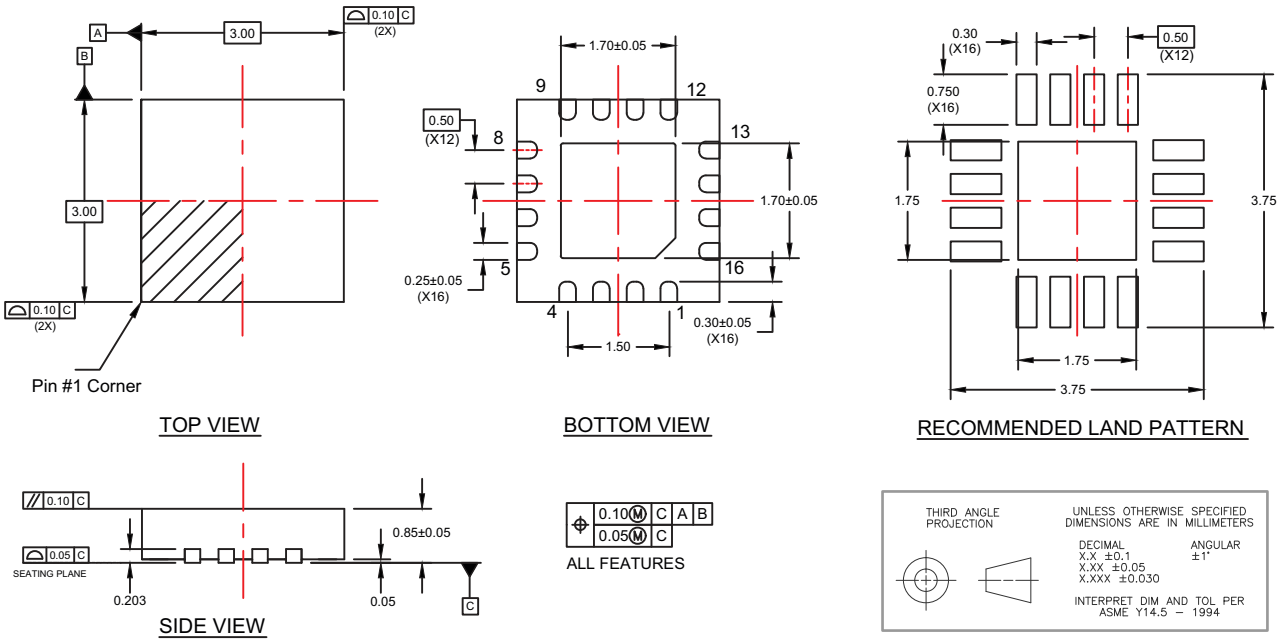
This section provides packaging data including the moisture sensitivity level, package drawing, package marking and tape-and-reel information.

Moisture Sensitivity Level

The moisture sensitivity level rating for the PE42553 in the 16-lead 3 × 3 mm QFN package is MSL3.

Package Drawing

Figure 20 • ***Package Mechanical Drawing for 16-lead 3 × 3 × 0.85 mm QFN***



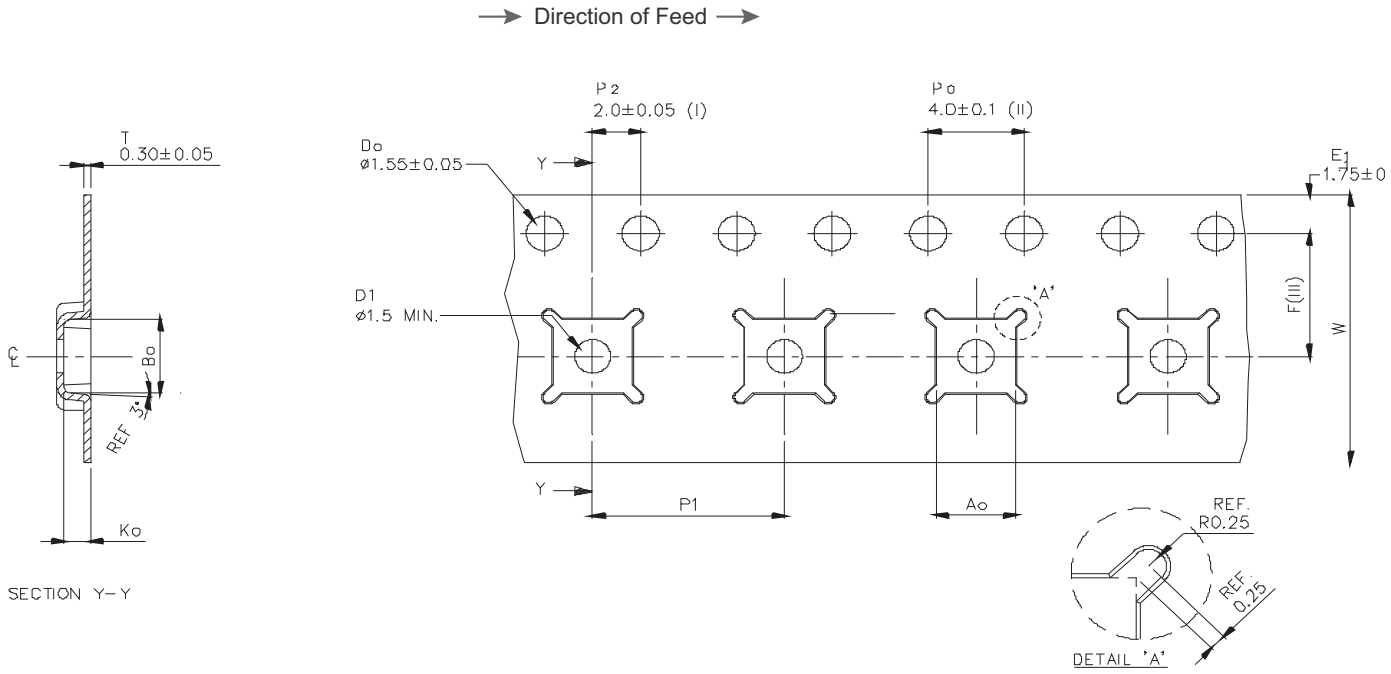
Top-Marking Specification

Figure 21 • ***Package Marking Specifications for PE42553***

● = Pin 1 indicator
YY = Last two digits of assembly year
WW = Assembly work week
ZZZZZZ = Assembly lot code (maximum six characters)

Tape and Reel Specification

Figure 22 • *Tape and Reel Specifications for 16-lead 3 × 3 × 0.85 mm QFN*

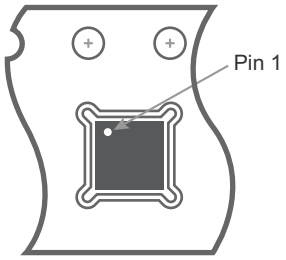


Ao	3.30 ± 0.1
Bo	3.30 ± 0.1
Ko	1.10 ± 0.1
F	5.50 ± 0.05
P1	8.00 ± 0.1
W	12.00 ± 0.3

Notes:

1. Measured from centerline of sprocket hole to centerline of pocket.
2. Cumulative tolerance of 10 sprocket holes ± 0.20.
3. Measured from centerline of sprocket hole to centerline of sprocket.

Dimensions are in millimeters unless otherwise specified.



Device Orientation in Tape

Ordering Information

Table 7 lists the available ordering codes for the PE42553 as well as available shipping methods.

Table 7 • *Order Codes for PE42553*

Order Codes	Description	Packaging	Shipping Method
PE42553B-Z	PE42553 SPDT RF switch	Green 16-lead 3 × 3 mm QFN	3000 units / T&R
EK42553-02	PE42553 Evaluation kit	Evaluation kit	1 / Box

Document Categories

Advance Information

The product is in a formative or design stage. The datasheet contains design target specifications for product development. Specifications and features may change in any manner without notice.

Preliminary Specification

The datasheet contains preliminary data. Additional data may be added at a later date. pSemi reserves the right to change specifications at any time without notice in order to supply the best possible product.

Product Specification

The datasheet contains final data. In the event pSemi decides to change the specifications, pSemi will notify customers of the intended changes by issuing a CNF (Customer Notification Form).

Sales Contact

For additional information, contact Sales at sales@psemi.com.

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