San Technology, Inc.

SPECIFICATION
FOR
LCD Module

Customer P/N:

Santek P/N: ST0350I3W-RSLW-F

DOC. Revision: RS02

Customer Approval:

	SIGNATURE	DATE
PREPARED BY	Zhiyi Liao	2017-10-09
CHECKED BY	Tom Liao	2017-10-11
APPROVED BY	Natty Lee	2017-Nov-7

Document Revision History

Version	Revise Date	Description	Changed by
RS01	2012-08-06	First issue	Chris
RS02	2017-10-09	Modify to San Technology	Zhiyi Liao

Table of Contents

1. General Specifications

No.	Item	Specification	Remark
1	LCD size	3.5” inch	
2	Driver element	a-Si TFT active matrix	
3	Resolution	320 × 3(RGB) × 240	
4	Display mode	Normally White, Transmissive	
5	Dot pitch	0.073(W) × 0.219(H) mm	
6	Active area	70.08(W) × 52.56(H) mm	
7	Module size	76.9(W) × 64.4(H) × 3.23(D) mm	Note 1
8	Surface treatment	Hard-coating	
9	Color arrangement	RGB-stripe	
10	Interface	Digital	
11	Backlight power consumption	0.396W(typ.)	
12	Panel power consumption	0.040W(typ.)	
13	Weight	0.034kg (typ.)	

Note 1: Refer to Mechanical Drawing.

2. Pin Assignment

2.1 TFT LCD Panel Driving Section

FPC connector is used for the module electronics interface.

Pin No.	Symbol	I/O	Function	Remark
1	V_{LED-}	P	Power for LED backlight cathode	
2	V_{LED+}	P	Power for LED backlight anode	
3	GND	P	Power Ground	
4	NC	-	No connection	
5	NC	-	No connection	
6	NC	-	No connection	
7	NC	-	No connection	
8	C4M	I	Boost capacitor	
9	C4P	I		
10	VGH	I	Stabilizing capacitor	
11	C3M	I	Boost capacitor	
12	C3P	I		
13	C2P	I	Boost capacitor	
14	C2M	I		
15	C1AP	I	Boost capacitor	
16	C1AM	I		
17	C1M	I	Boost capacitor	
18	C1P	I		
19	GND	P	Power Ground	
20	V_{DD}	P	Power voltage	
21	VGL	I	Stabilizing capacitor	
22	Vint2	I	Stabilizing capacitor	
23	V_{DD}	P	Power voltage	
24	VCOMOUT	I	Coupled capacitor	
25	VCOMDC	I		
26	GND	P	Power Ground	
27	Vint1	I	Stabilizing capacitor	
28	VCOMAC	I	Stabilizing capacitor	

29	VDDA	C	Stabilizing capacitor	
30	RESET	I	Global reset pin	
31	SPDA	I/O	SPI interface input pin	
32	SPCK	I	SPI clock signal	
33	SPENB	I	SPI chip select signal	
34	DE	I	Data enable pin	
35	Hsync	I	Horizontal synchronizing input signal	
36	Vsync	I	Vertical synchronizing input signal	
37	GND	P	Power Ground	
38	DCLK	I	DCLK	
39	GND	P	Power Ground	
40	B5	I	Blue data	
41	B4	I	Blue data	
42	B3	I	Blue data	
43	B2	I	Blue data	
44	B1	I	Blue data	
45	B0	I	Blue data	
46	G5	I	Green data	
47	G4	I	Green data	
48	G3	I	Green data	
49	G2	I	Green data	
50	G1	I	Green data	
51	G0	I	Green data	
52	R5	I	Red data	
53	R4	I	Red data	
54	R3	I	Red data	
55	R2	I	Red data	
56	R1	I	Red data	
57	R0	I	Red data	
58	NC	-	No connection	
59	GND	P	Power Ground	
60	GND	P	Power Ground	

3. Operation Specifications

3.1. Absolute Maximum Ratings

(GND =0V, Note 1)

Item	Symbol	Values		Unit	Remark
		Min.	Max.		
Power Voltage	V_{DD}	-0.3	5	V	
OperationTemperature	T_{OP}	-20	70	℃	
Storage Temperature	T_{ST}	-30	80	℃	
LED Reverse Voltage	Vr	-	1.2	V	Each LED Note 2
LED Forward Current	I_f	-	25	mA	Each LED

Note 1: Device is subject to be damaged permanently if stresses beyond those absolute maximum ratings listed above.
Note 2: Vr conditions: Zener Diode 20mA.

3.2. Typical Operation Conditions

(GND =0V)

Item	Symbol	Values			Unit	Remark
		Min.	Typ.	Max.		
Power voltage	V_{DD}	3.2	3.3	3.4	V	
Current for driver	IV_{DD}	-	12	18	mA	V_{DD} =3.3V
Input logic high voltage	V_{IH}	$0.8V_{DD}$	-	V_{DD}	V	
Input logic low voltage	V_{IL}	0	-	$0.2V_{DD}$	V	

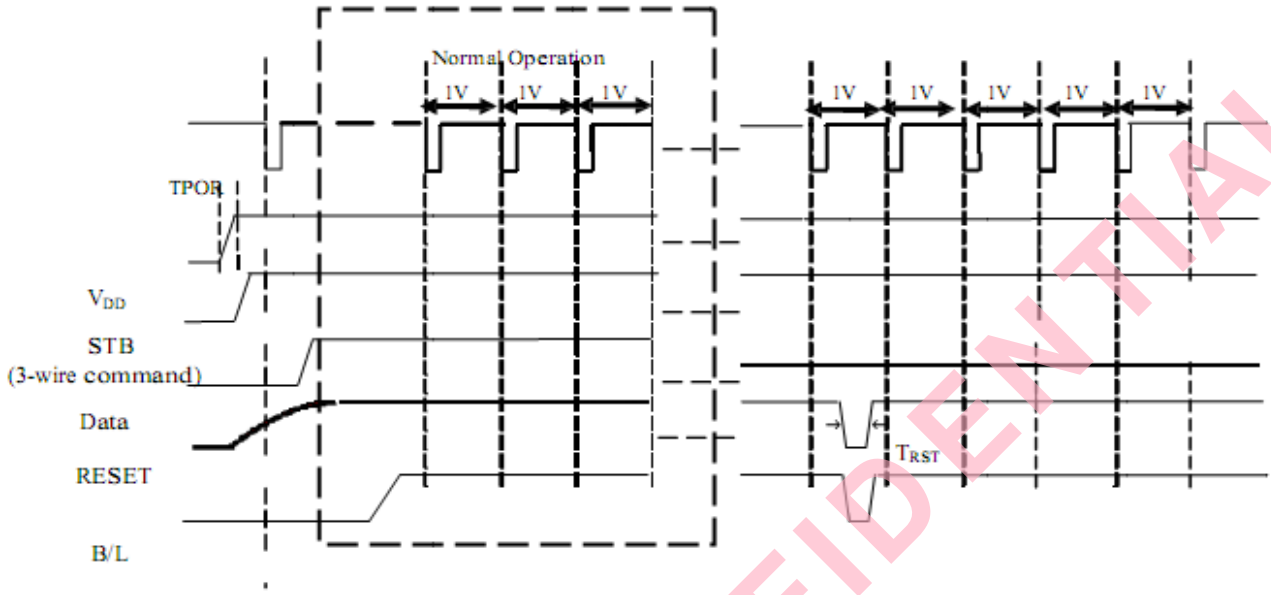
3.3. Backlight Driving Condition

Item	Symbol	Values			Unit	Remark
		Min.	Typ.	Max.		
Voltage for LED backlight	V_L	18.6	19.8	21	V	
Current for LED Backlight	I_L	18	20	22	mA	
LED life time	-	20,000	-	-	Hr	Note 1

Note 1:The "LED life time" is defined as the module brightness decreases to 50% original brightness that the ambient temperature is 25℃ and I_L =20mA. The LED lifetime could be decreased if operating I_L is larger than 20 mA.

3.4. Power Sequence

3.4.1. Power on:

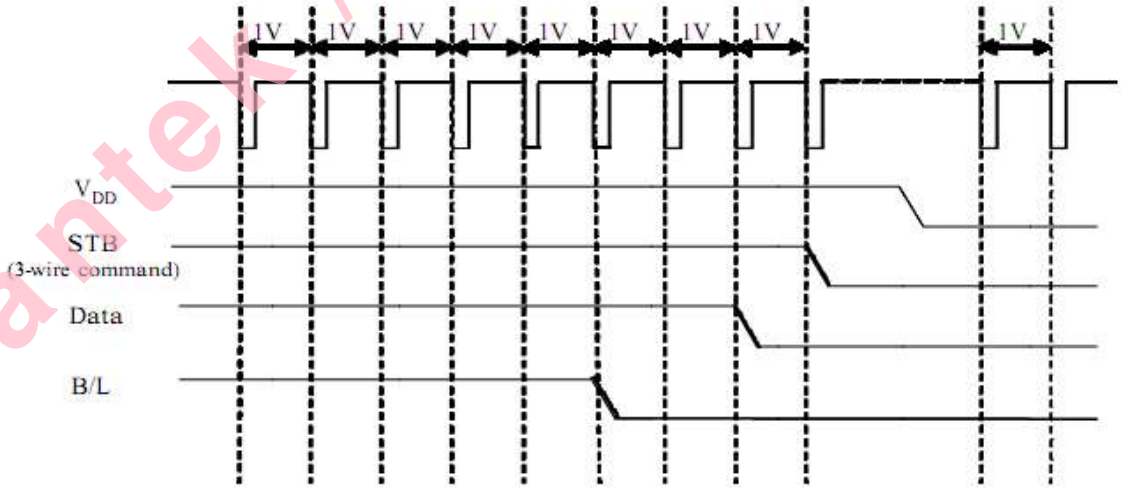


V_{DD}→STB→Data→B/L

Note: External Reset(RESET)

To prevent from abnormal reset condition, a glitch filter for RESET is embedded in this chip. The external reset signal should keep active for large then reset time(T_{RST}).

3.4.2. Power off:



B/L→Data→STB→V_{DD}

Note: Data include R[5:0],G[5:0],B[5:0],SPENA, SPCK, SPDA, Hsync, Vsync, DCLK, DE.

3.5. Timing Characteristics

3.5.1. AC Electrical Characteristics

3.5.1.1 AC Electrical Characteristics

(Test Condition: (V_{DD}=3.3V,GND= 0V, TA= 25℃))

Item	Symbol	Values			Unit.	Remark
		Min.	Typ.	Max.		
System Operation Timing						
V_{DD} power on slew time	TPOR	-	-	1000	us	From 0V to 90% V_{DD}
RESET active pulse width	T_{RST}	40			us	V_{DD}=3.3V
Input / Output Timing						
DCLK clock time	Tclk	125	-	-	ns	
Hsync to DCLK	Thc	-	-	1	Tclk	
Hsync width	Thwh	1	-	-	Tclk	
Vsync width	Tvwh	1	-	-	Th	
Hsync period time	Th	-	63.56	-	us	
Vsync setup time	Tvst	12	-	-	ns	
Vsync hold time	Tvhd	12	-	-	ns	
Hsync setup time	Thst	12	-	-		
Hsync setup time	Thhd	12	-	-	ns	
Data setup time	Tdsu	12	-	-	ns	
Data hold time	Tdhd	12	-	-	ns	
DE setup time	Tesu	12	-	-	ns	
Time that Vsync to 1st line data input	Tvs	2	13	127	Th	

3.5.1.2 Timing Table

18 Bit RGB Mode

ITEM	Symbol	Value			Unit	Remark
		Min.	Typ.	Max.		
DCLK frequency	Fclk	-	6.4	8.0	Mhz	V_{DD} =3.2~3.4V
DCLK cycle time	Tclk	-	156	-	ns	-
DCLK pulse duty	Tcwh	40	50	60	%	Tclk
Time that Hsync to 1'st data input(NTSC)	Ths	40	70	255	-	

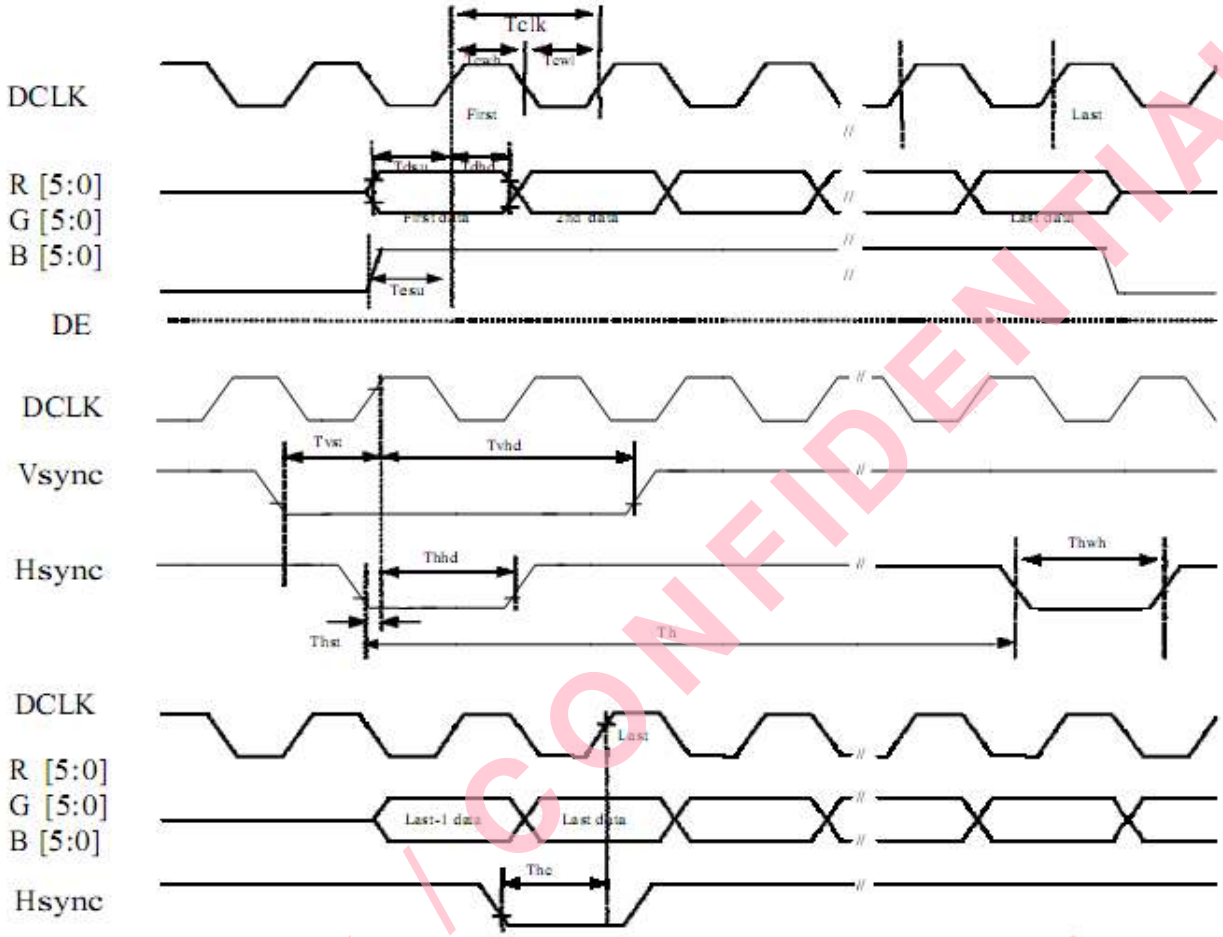
3.5.1.3 3-wire serial communication AC timing

Item	Symbol	Values			Unit	Remark
		Min.	Typ.	Max.		
Serial clock	Tspck	320	-	-	ns	
SPCK pulse duty	-	40	50	60	%	
Serial data setup time	Tisu	120	-	-	ns	
Serial data hold time	Tihd	120	-	-	ns	
Serial clock high/low	Tckh/l	120	-	-	ns	
Chip select distinguish	Tcd	1	-	-	us	
SPENB to Vsync	Tcv	1	-	-	us	
SPENB setup time	Teck	150	-	-	ns	
SPENB hold time	Tcke	150	-	-	ns	

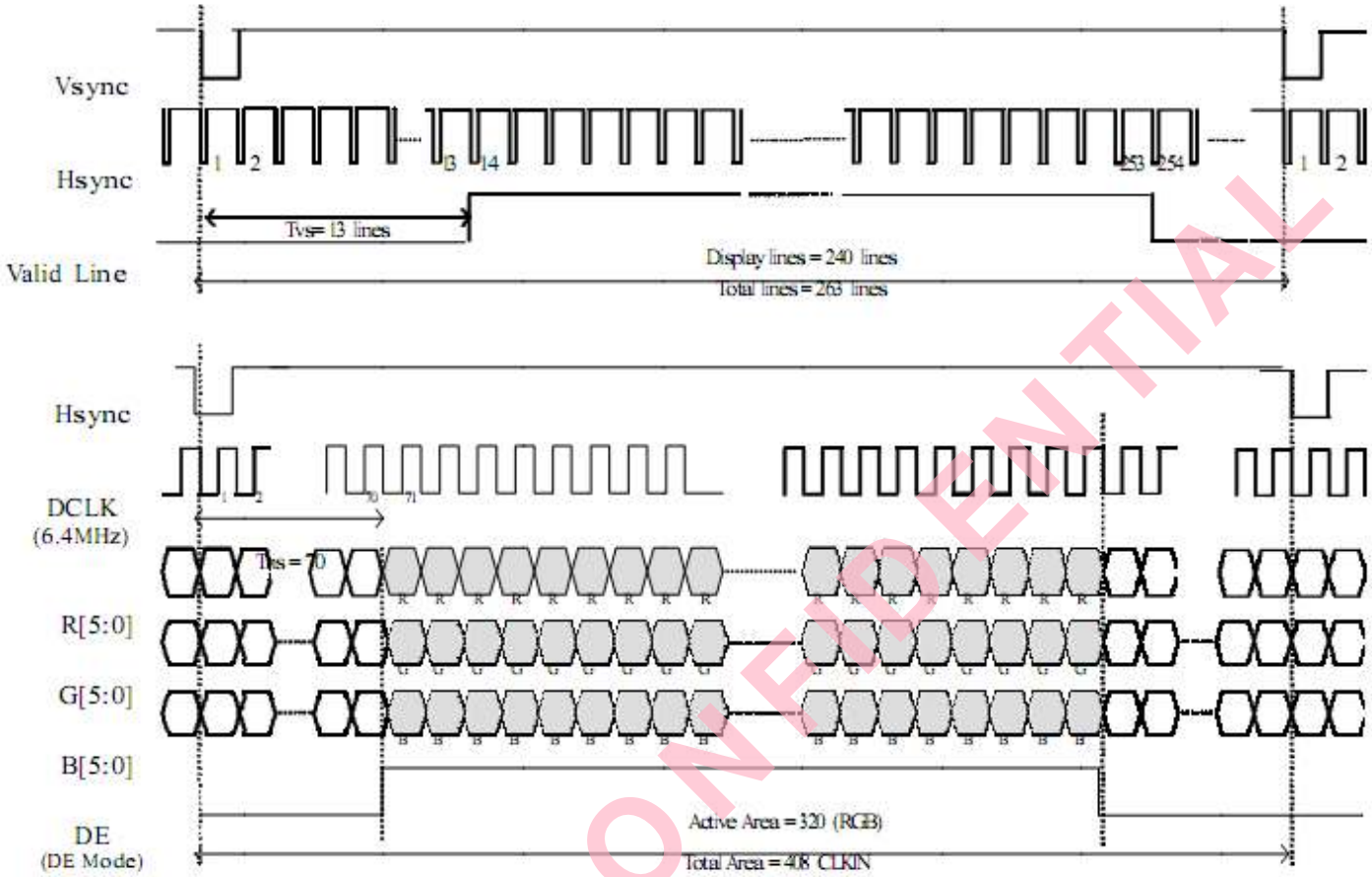
3.5.2. Timing Diagram

Input Data Timing

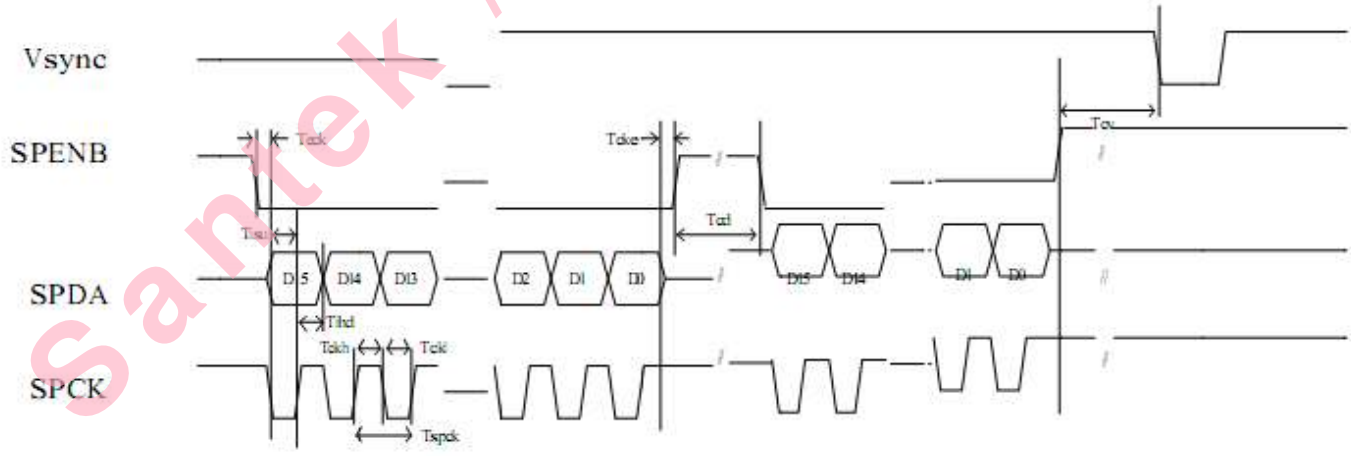
1. Clock and Data Input Timing Diagram



2. 18 bit RGB mode for 960 x 240



3. 3-Wire Timing Diagram



Note: 3-Wire Writer Format

MSB															LSB
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Register Address[5:0]						1	X	DATA(Issue by external controller)							

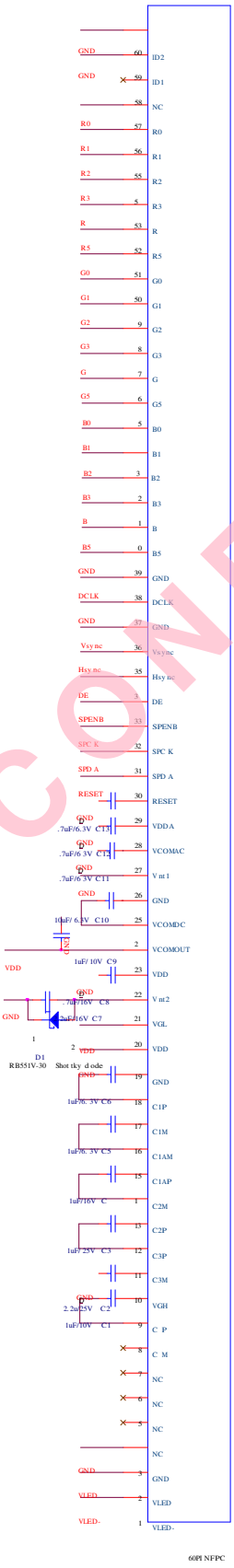
D9 : W/R control bit. "1" for Write ; "0" for Read
D8 : Hi-Z bit during read mode

Note: 3-Wire Control Registers List

3-Wire Register		Register Description		
D[15:10]	Name	Init	R/W	Function Description
000000b	R00	07h	R/W	System control register
000001b	R01	00h	R/W	Timing controller function register
000010b	R02	03h	R/W	Operation control register
000011b	R03	CCh	R/W	Input data format control register
000100b	R04	46h	R/W	Source Timing delay control register
000101b	R05	0Dh	R/W	Gate Timing delay control register
000110b	R06	00h	R/W	Reserved
000111b	R07	00h	R/W	Internal function control register
001000b	R08	08h	R/W	RGB contrast control register
001001b	R09	40h	R/W	RGB brightness control register
001010b	R0A	88h	R/W	Hue/Saturation control register
001011b	R0B	88h	R/W	R/B Sub-contrast control register
001100b	R0C	20h	R/W	R Sub-brightness control register
001101b	R0D	20h	R/W	B Sub-brightness control register

3.5.3. Reference circuit

The positive(VGH) and negative(VGL) power supplies for LCD are generated through build-in DC-DC charge pump circuit, an elegant design with only several passive power-setting capacitors are required.



4. Optical Specifications

Item	Symbol	Condition	Values			Unit	Remark
			Min.	Typ.	Max.		
Viewing angle (CR≥ 10)	θ_L	Φ=180°(9 o'clock)	55	65	-	degree	Note 1
	θ_R	Φ=0°(3 o'clock)	55	65	-		
	θ_T	Φ=90°(12 o'clock)	40	50	-		
	θ_B	Φ=270°(6 o'clock)	55	65	-		
Response time	T_{ON}	Normal θ=Φ=0°	-	9	20	msec	Note 3
	T_{OFF}		-	16	30	msec	Note 3
Contrast ratio	CR		400	500	-	-	Note 4
Color chromaticity	W_X		0.26	0.31	0.36	-	Note 2 Note 5 Note 6
	W_Y		0.28	0.33	0.38	-	
Luminance	L		350	400	-	cd/m²	Note 6
Luminance uniformity	Y_U		70	75	-	%	Note 7

Test Conditions:

1. V_{DD}=3.3V, I_L=20mA (Backlight current), the ambient temperature is 25℃.
2. The test systems refer to Note 2.

Note 1: Definition of viewing angle range

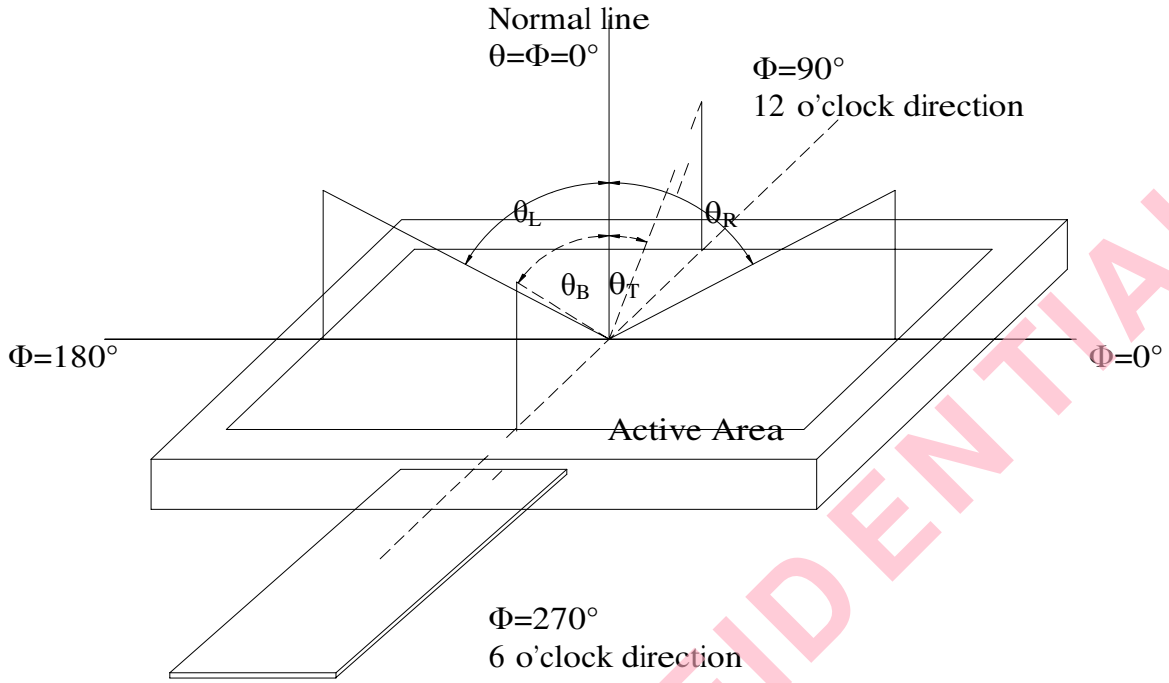


Fig. 5-1 Definition of viewing angle

Note 2: Definition of optical measurement system.

The optical characteristics should be measured in dark room. The optical properties are measured at the center point of the LCD screen. (Response time is measured by Photo detector TOPCON BM-7, other items are measured by BM-5A/Field of view: 1° /Height: 500mm.)

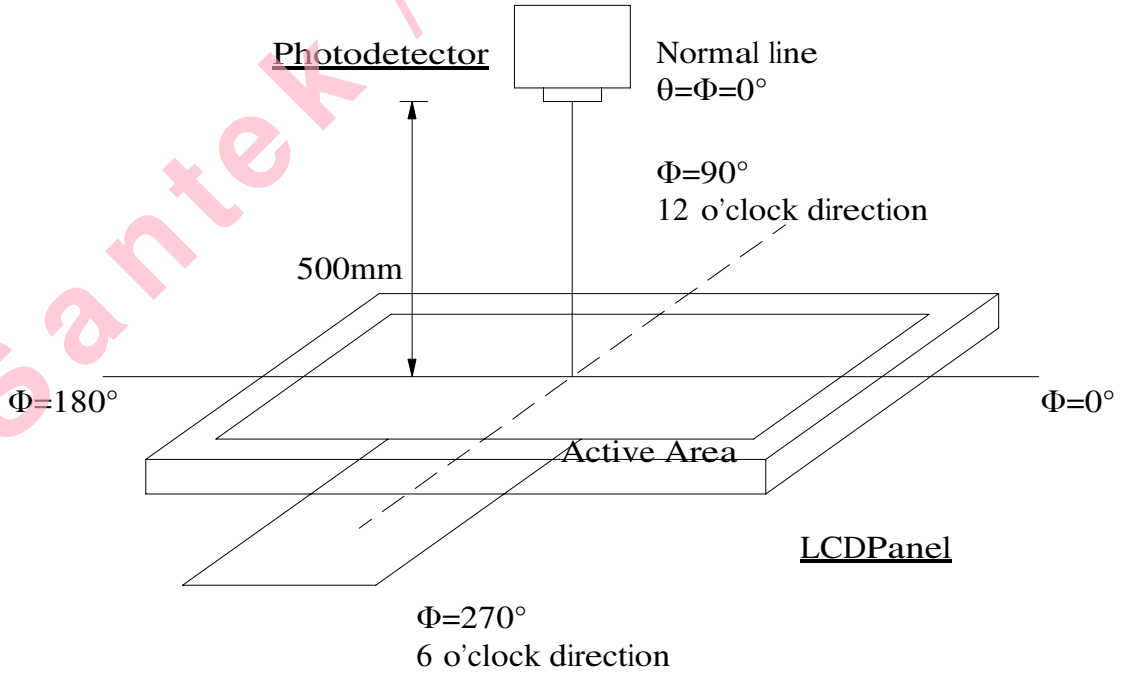


Fig. 5-2 Optical measurement system setup

Note 3: Definition of response t ime

The response time is defined as the LCD optical switching time interval between "White" state and "Black" state. Rise time (T_{ON}) is the time between photo detector output intensity changed from 90% to 10%. And fall time (T_{OFF}) is the time between photo detector output intensity changed from 10% to 90%.

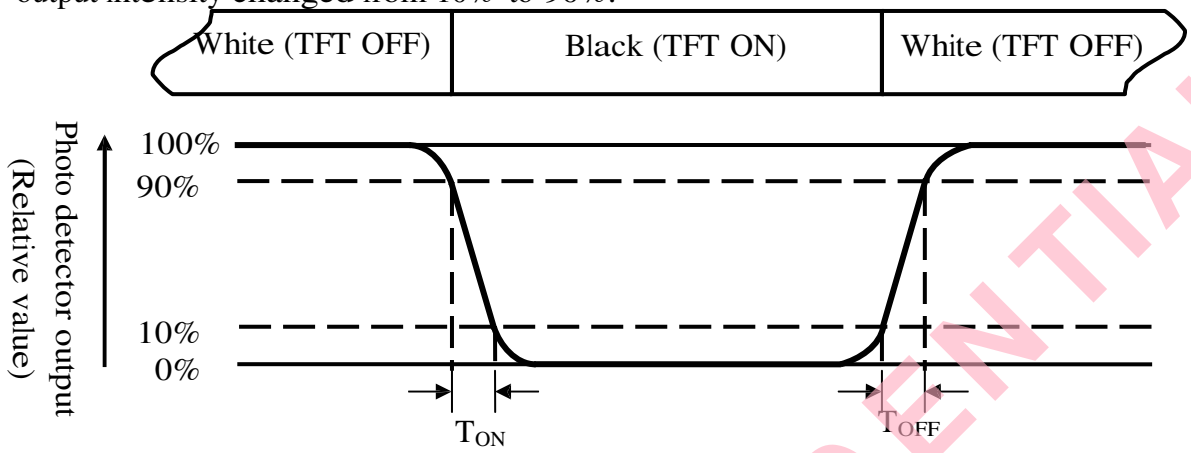


Fig. 5-3 Definition of response time

$T_{ON} + T_{OFF} \leq 25$ ms

Note 4: Definition of contrast ratio

$$\text{Contrast ratio (CR)} = \frac{\text{Luminance measured when LCD is on the "White" state}}{\text{Luminance measured when LCD is on the "Black" state}}$$

Note 5: Definition of color chromaticity (CIE1931)
Color coordinates measured at center point of LCD.

Note 6: All input terminals LCD panel must be ground when measuring the center area of the panel. The LED driving condition is I_L=20mA.

Note 7: Definition of luminance uniformity

To test for uniformity, the tested area, which is inside the active area, is divided into 3 rows and 3 columns. The measurement spot is placed at the center of each box.

$$\text{Luminance Uniformity (Yu)} = \frac{B_{min}}{B_{max}}$$

L-------Active area length W----- Active area width

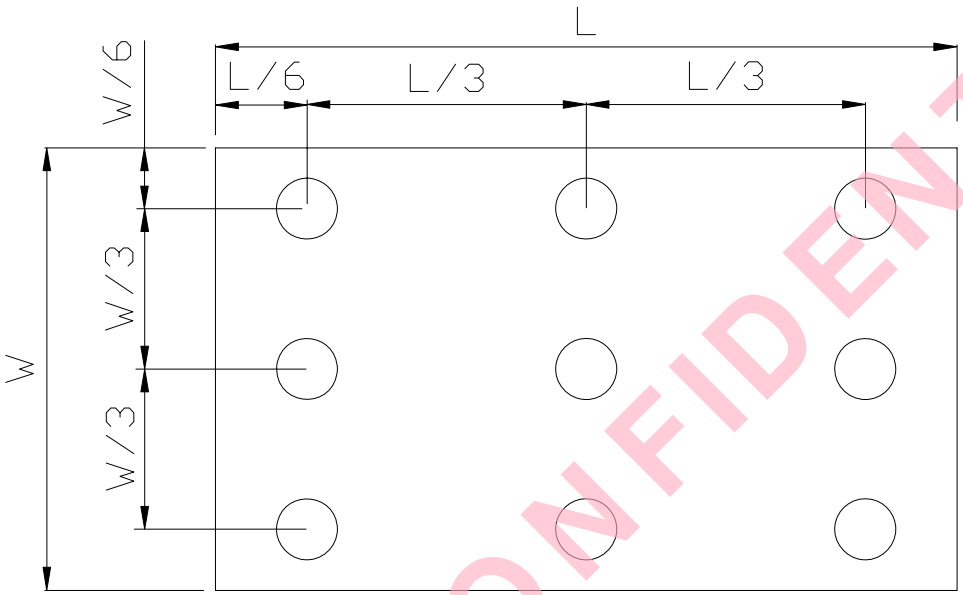


Fig. 5-4 Definition of uniformity

B_{max}: The measured maximum luminance of all measurement position.

B_{min}: The measured minimum luminance of all measurement position.

5. Reliability Test Items

(Note3)

Item	Test Conditions	Remark
High Temperature Storage	Ta = 80℃ 240 hrs	Note 1,Note 4
Low Temperature Storage	Ta = -30℃ 240hrs	Note 1,Note 4
High Temperature Operation	Ts = 70℃ 240hrs	Note 2,Note 4
Low Temperature Operation	Ta = -20℃ 240hrs	Note 1,Note 4
Operate at High Temperature and Humidity	+60℃, 90%RH 240 hrs	Note 4
Thermal Shock	-30℃/30 min ~ +80℃/30 min for total 100 cycles, start with cold temperature and end with high temperature	Note 4
Vibration Test	Frequency range:10~55Hz Stroke:1.5mm Sweep:10Hz~55Hz~10Hz 2 hours for each direction of X. Y. Z. (6 hours for total)	
Mechanical Shock	100G 6ms,±X, ±Y, ±Z 3 times for each direction	
Package Vibration Test	Random Vibration : 0.015G*G/Hz from 5-200HZ, -6dB/Octave from 200-500HZ 2 hours for each direction of X. Y. Z. (6 hours for total)	
Package Drop Test	Height:60 cm 1 corner, 3 edges, 6 surfaces	
Electro Static Discharge	± 2KV, Human Body Mode, 100pF/1500Ω	

Note 1: Ta is the ambient temperature of samples.
Note 2: Ts is the temperature of panel's surface.
Note 3: In the standard condition, there shall be no practical problem that may affect the display function. After the reliability test, the product only guarantees operation, but doesn't guarantee all the cosmetic specification.
Note 4: Before cosmetic and function test, the product must have enough recovery time, at least 2 hours at room temperature.

6. Handling Precautions

6.1. Safety

Liquid crystal is poisonous. Do not put it in your mouth. If liquid crystal touches your skin or clothes, wash it off immediately by using soap and water.

6.2. Handling

1. The LCD panel is plate glass. Do not subject the panel to mechanical shock or to excessive force on its surface.
2. The attached polarizer to the display is easily damaged. Please handle it carefully to avoid scratch or other damages.
3. To avoid contamination on the display surface, do not touch the module surface with bare hands.
4. Keep a space so that the LCD panels do not touch other components.
5. Put cover board such as acrylic board on the surface of LCD panel to protect panel from damages.
6. Transparent electrodes may be disconnected if you use the LCD panel under environmental conditions where the condensation of dew occurs.
7. Do not leave module in direct sunlight to avoid malfunction of the ICs.

6.3. Static Electricity

1. Be sure to ground module before turning on power or operating module.
2. Do not apply voltage which exceeds the absolute maximum rating value.

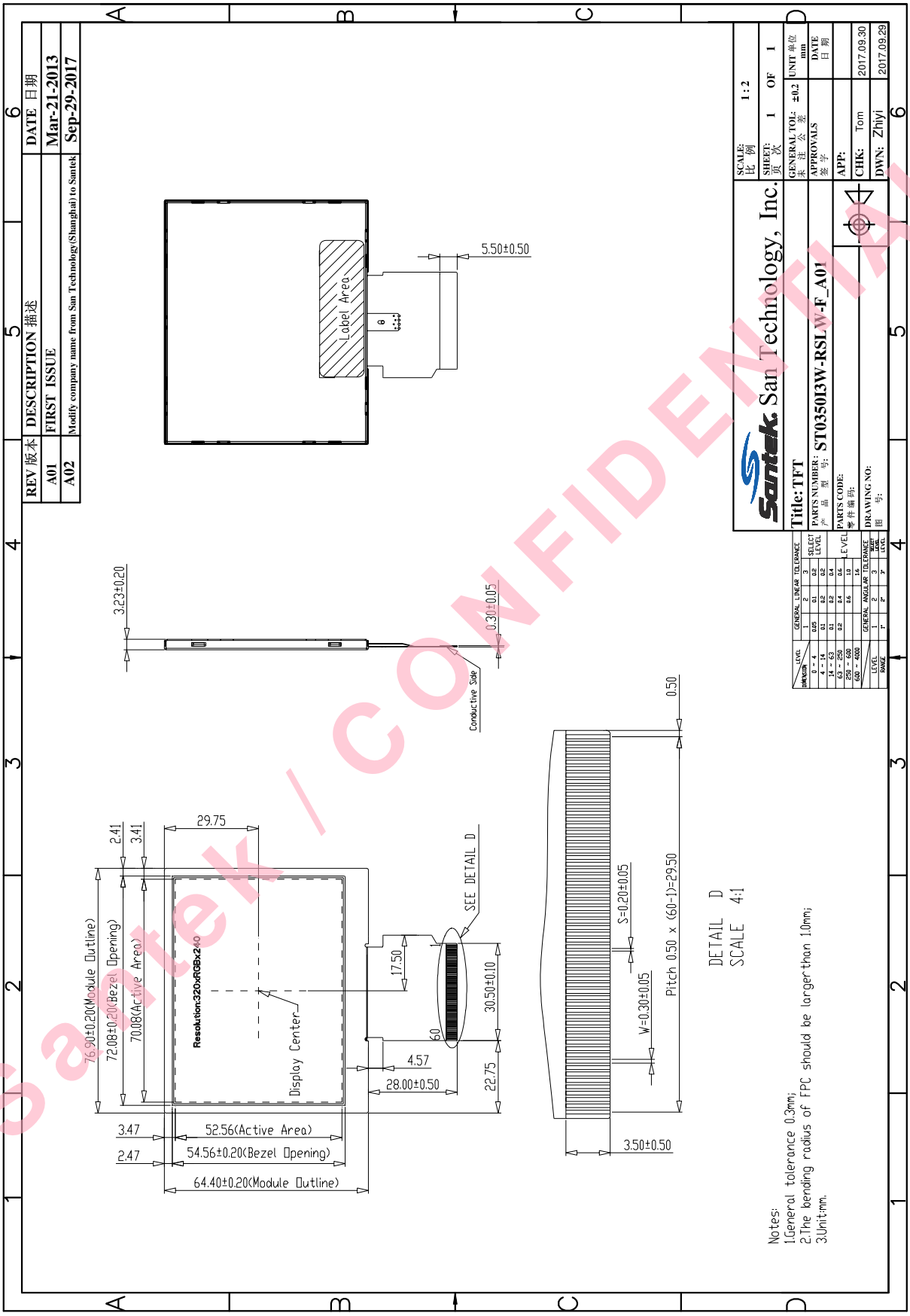
6.4. Storage

1. Store the module in a dark room where must keep at +25±10℃ and 65%RH or less.
2. Do not store the module in surroundings containing organic solvent or corrosive gas.
3. Store the module in an anti-electrostatic container or bag.

6.5. Cleaning

1. Do not wipe the polarizer with dry cloth. It might cause scratch.
2. Only use a soft sloth with IPA to wipe the polarizer, other chemicals might permanent damage to the polarizer.

7. Mechanical Drawing



8. Package Drawing

8.1. Packaging Material Table

No.	Item	Model (Material)	Dimensions (mm)	Unit Weight (kg)	Quantity (pcs)	Remark
1	LCM module	ST0350I3W-RSLW-F	76.9 × 64.4 × 3.23	0.034	240	
2	Tray	PET	505 x 338 x 16.5	0.250	21	Anti-static
3	DUST-PROOF BAG	PE	700 x 530	0.060	1	
4	Partition	CORRUGATED PAPER	512 x 350 x 225	0.500	1	
5	Carton	CORRUGATED PAPER	530 x 355 x 255	1.100	1	
6	Total weight	15.070±5%Kg				

8.2. Packaging Quantity

(1) LCM quantity per tray (pcs): 3 row x 4 column = 12
(2) Total LCM quantity in Carton (pcs): NO. of PS trays 20 x quantity per tray 12 = 240

8.3. Packaging Drawing