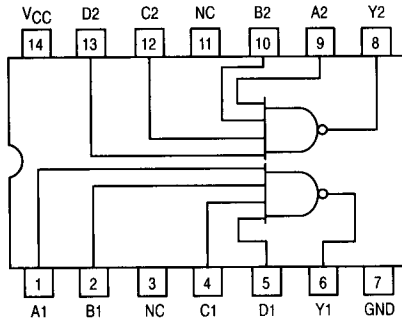




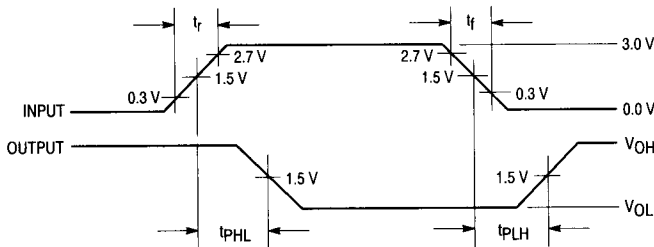
Dual 4-Input NAND Gate

ELECTRICALLY TESTED PER:
MIL-M-38510/33004

LOGIC DIAGRAM



WAVEFORMS



Military 54F20



AVAILABLE AS:

- 1) JAN: JM38510/33004BXA
- 2) SMD: N/A
- 3) 883: 54F20/BXAJC

X = CASE OUTLINE AS FOLLOWS:
PACKAGE: CERDIP: C
CERFLAT: D
LCC: 2

THE LETTER "M" APPEARS
BEFORE THE / ON LCC.

PIN ASSIGNMENTS

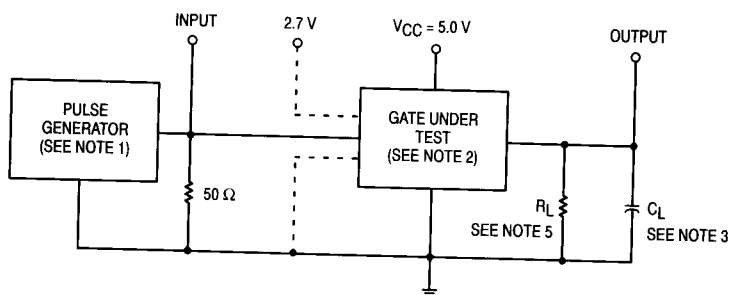
FUNCT.	DIL 632-08	FLATS 717-04	LCC 756A-02	BURN-IN (COND. A)
A1	1	1	2	VCC
B1	2	2	3	VCC
NC	3	3	4	OPEN
C1	4	4	6	VCC
D1	5	5	8	VCC
Y1	6	6	9	OPEN
GND	7	7	10	GND
Y2	8	8	12	OPEN
A2	9	9	13	VCC
B2	10	10	14	VCC
NC	11	11	16	OPEN
C2	12	12	18	VCC
D2	13	13	19	VCC
VCC	14	14	20	VCC

BURN-IN CONDITIONS:
VCC = 5.0 V MIN/6.0 V MAX

54F20

TRUTH TABLE				
A	B	C	D	Y
0	0	0	0	1
0	0	0	1	1
0	0	1	0	1
0	0	1	1	1
0	1	0	0	1
0	1	0	1	1
0	1	1	0	1
0	1	1	1	1
1	0	0	0	1
1	0	0	1	1
1	0	1	0	1
1	0	1	1	1
1	1	0	0	1
1	1	0	1	1
1	1	1	0	1
1	1	1	1	0

AC TEST CIRCUIT



NOTES:

1. Pulse generator has the following characteristics: $t_r = t_f \leq 2.5$ ns, PRR = 1.0 MHz, and $Z_{OUT} \approx 50 \Omega$.
2. Terminal conditions (pins not designated may be high ≥ 2.0 V, low ≤ 0.8 V, or open).
3. $C_L = 50$ pF $\pm 10\%$, including scope probe, wiring and stray capacitance, without package in test fixture.
4. Voltage measurements are to be made with respect to network ground terminal.
5. $R_L = 500 \Omega \pm 5.0\%$.

54F20

Symbol	Parameter	Limits						Unit	Test Condition (Unless Otherwise Specified)
		+ 25°C		+ 125°C		- 55°C			
		Subgroup 1		Subgroup 2		Subgroup 3			
		Min	Max	Min	Max	Min	Max		
V _{OH}	Logical "1" Output Voltage	2.5		2.5		2.5		V	V _{CC} = 4.5 V, I _{OH} = -1.0 mA, V _{IL} = 0.8 V, other inputs = 5.5 V.
V _{OL}	Logical "0" Output Voltage		0.5		0.5		0.5	V	V _{CC} = 4.5 V, I _{OL} = 20 mA, V _{IH} = 2.0 V other inputs = 2.0 V.
V _{IC}	Input Clamping Voltage		-1.2					V	V _{CC} = 4.5 V, I _{IN} = -18 mA, other inputs are open.
I _{IH1}	Logical "1" Input Voltage		20		20		20	μA	V _{CC} = 5.5 V, V _{IN} = 2.7 V,, all other inputs = 0 V.
I _{IH2}	Logical "1" Input Current		100		100		100	μA	V _{CC} = 5.5 V, V _{IN} = 7.0 V, other inputs 0 V.
I _{IL}	Logical "0" Input Current	-0.03	-0.6	-0.03	-0.6	-0.03	-0.6	mA	V _{CC} = 5.5 V, V _{IN} = 0.5 V, other inputs = 5.5 V.
I _{OS}	Output Short Circuit Current	-60	-150	-60	-150	-60	-150	mA	V _{CC} = 5.5 V, V _{IN} = 0 V (all inputs), V _{OUT} = 0 V.
I _{OD}	Diode Current	60		60		60		mA	V _{CC} = 4.5 V, all inputs = 5.5 V, V _{OUT} = 2.5 V.
I _{CCH}	Power Supply Current		1.4		1.4		1.4	mA	V _{CC} = 5.5 V, V _{IN} = 0 V, (all inputs).
I _{CCL}	Power Supply Current		5.1		5.1		5.1	mA	V _{CC} = 5.5 V, V _{IN} = 5.5 V (all inputs).
V _{IH}	Logical "1" Input Voltage	2.0		2.0		2.0		V	V _{CC} = 4.5 V.
V _{IL}	Logical "0" Input Voltage		0.8		0.8		0.8	V	V _{CC} = 4.5 V.
	Functional Tests	Subgroup 7		Subgroup 8A		Subgroup 8B			per Truth Table with V _{CC} = 5.0 V, V _{INL} = 0.5 V, and V _{INH} = 2.5 V.

Symbol	Parameter	Limits						Unit	Test Condition (Unless Otherwise Specified)
		+ 25°C		+ 125°C		- 55°C			
		Subgroup 9		Subgroup 10		Subgroup 11			
		Min	Max	Min	Max	Min	Max		
t _{PHL}	Propagation Delay /Data-Output Output High-Low	1.5	4.3	1.5	6.5	1.5	6.5	ns	V _{CC} = 5.0 V, C _L = 50 pF, R _L = 500 Ω.
t _{PLH}	Propagation Delay /Data-Output Output Low-High	2.4	5.0	2.0	7.0	2.0	7.0	ns	V _{CC} = 5.0 V, C _L = 50 pF, R _L = 500 Ω.