TPS61169 38-V High Current-Boost WLED Driver With PWM Control

1 Features

- 2.7-V to 5.5-V Input Voltage
- Integrated 40-V, 1.8-A MOSFET
- Drives LED String up to 38 V
- 1.2-A Minimum Switch Current Limit
- 1.2-MHz Switching Frequency
- 204-mV Reference Voltage
- Internal Compensation
- PWM Brightness Control
- Open LED Protection
- Undervoltage Protection
- Built-in Soft-Start
- Thermal Shutdown
- Up to 90% Efficiency

2 Applications

- Smartphone Backlighting
- Tablet Backlighting
- PDAs, Handheld Computers, GPS Receivers
- Portable Media Players, Portable TVs
- White LED Backlighting for Small and Media Form-Factor Displays
- Handheld Data Terminals (EPOS)
- Handheld Medical Equipment
- Thermostat Display
- Blood Glucose Meters
- Flashlights
- Refrigerators and Ovens

3 Description

With a 40-V rated integrated switch FET, the TPS61169 is a boost converter that drives LEDs in series. The boost converter has a 40-V, 1.8-A internal MOSFET with minimum 1.2-A current limit; thus it can drive single or parallel LED strings for small- to large-size panel backlighting. The default white LED current is set with the external sensor resistor, R_{SET}, and the feedback voltage is regulated to 204 mV, as shown in the *Simplified Schematic*. During the operation, the LED current can be controlled by using a pulse width modulation (PWM) signal applied to the CTRL pin, through which the duty cycle determines the feedback reference voltage. The TPS61169 does not burst the LED current; therefore, it does not generate audible noises on the output capacitor. For maximum protection, the device features integrated open LED protection that disables the TPS61169 to prevent the output voltage from exceeding the absolute maximum voltage ratings of the device during open LED conditions.

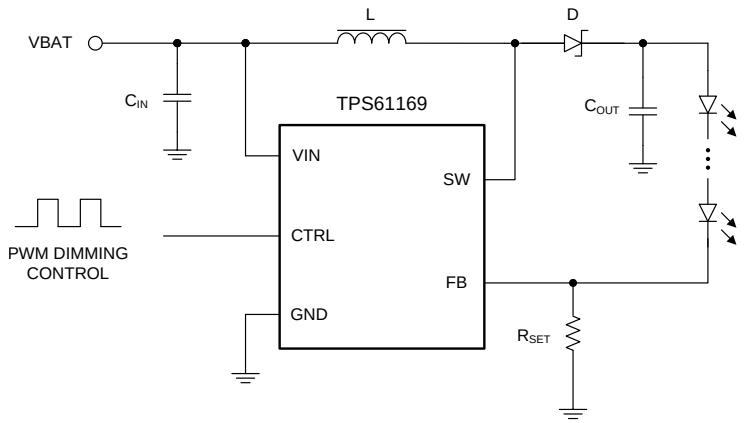
The TPS61169 is available in a space-saving 5-pin SC70 package.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS61169	SOT (5)	2.00 mm × 1.25 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

4 Simplified Schematic



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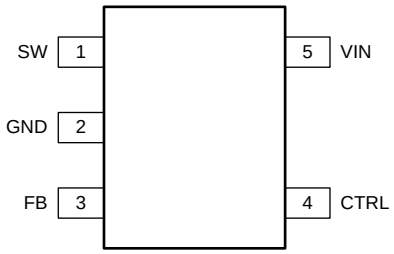
5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (October 2014) to Revision A	Page
• Added new items to "Applications" on page 1	1
• Changed *Handling Ratings* to *ESD Ratings* table; move storage temperature range from *Handling Ratings* to *Abs Max* table	4

6 Pin Configuration and Functions

DCK Package
5-Pin SC70
(Top View)



Pin Functions

PIN		I/O	DESCRIPTION
NUMBER	NAME		
1	SW	I	Drain connection of the internal power FET.
2	GND	O	Ground
3	FB	I	Feedback pin for current. Connect the sense resistor from FB to GND.
4	CTRL	I	PWM dimming signal input
5	VIN	I	Supply input pin

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Voltage(2)	VIN, CTRL, PWM, FB	–0.3	7	V
	SW	–0.3	40	
P_D	Continuous power dissipation	See Thermal Information Table		
T_J	Operating junction temperature	–40	150	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
V_{IN}	Input voltage	2.7		5.5	V
V_{OUT}	Output voltage	V_{IN}		38	V
L	Inductor	4.7		10	µH
C_I	Input capacitor	1			µF
C_O	Output capacitor	1		10	µF
F_{PWM}	PWM dimming signal frequency	5		100	kHz
D_{PWM}	PWM dimming signal duty cycle	1%		100%	
T_J	Operating junction temperature	–40		125	°C

7.4 Thermal Information

THERMAL METRIC(1)		TPS61169 DCK (SC70) 5 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance(2)	263.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance(3)	76.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance(4)	51.4	°C/W
ψ_{JT}	Junction-to-top characterization parameter(5)	1.1	°C/W
ψ_{JB}	Junction-to-board characterization parameter(6)	50.7	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.
(2) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
(3) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
(4) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
(5) The junction-to-top characterization parameter, ψ_{JT}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining $R_{\theta JA}$, using a procedure described in JESD51-2a (sections 6 and 7).
(6) The junction-to-board characterization parameter, ψ_{JB}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining $R_{\theta JA}$, using a procedure described in JESD51-2a (sections 6 and 7).

7.5 Electrical Characteristics

Over operating free-air temperature range, V_{IN} = 3.6 V, CTRL = V_{IN} (unless otherwise specified).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLY						
V_{IN}	Input voltage range		2.7		5.5	V
V_{VIN_UVLO}	Undervoltage lockout threshold	V_{IN} falling V_{IN} rising		2	2.3 2.6	V
V_{VIN_HYS}	V_{IN} UVLO hysteresis			200		mV
I_{Q_VIN}	Operating quiescent current into V_{IN}	Device enable, switching 1.2 MHz and no load,		0.3	0.45	mA
I_{SD}	Shutdown current	CTRL = GND		1	2	µA
CONTROL LOGIC AND TIMING						
V_H	CTRL Logic high voltage		1.2			V
V_L	CTRL Logic Low voltage				0.4	V
R_{PD}	CTRL pin internal pull-down resistor			300		KΩ
t_{SD}	CTRL logic low time to shutdown	CTRL high to low	2.5			ms
VOLTAGE AND CURRENT REGULATION						
V_{REF}	Voltage feedback regulation voltage	Duty = 100%, $T_A \geq 25°C$	188	204	220	mV
I_{FB}	FB pin bias current	V_{FB} = 204 mV			2.5	µA
t_{REF}	V_{REF} filter time constant			1		ms
POWER SWITCH						
$R_{DS(ON)}$	N-channel MOSFET on-resistance			0.35	0.7	Ω
I_{LN_NFET}	N-channel leakage current	V_{SW} = 35 V			1	µA
SWITCHING FREQUENCY						
f_{SW}	Switching frequency	V_{IN} = 3 V	0.75	1.2	1.5	MHz
PROTECTION AND SOFT START						
I_{LIM}	Switching MOSFET current limit	$D = D_{MAX}$, $T_A \leq 85°C$	1.2	1.8	2.4	A
I_{LIM_Start}	Switching MOSFET start-up current limit	$T_A \leq 85°C$		0.72		A
t_{Half_LIM}	Time step for half current limit			6.5		ms
V_{OVP_SW}	Output voltage overvoltage threshold		36	37.5	39	V
THERMAL SHUTDOWN						
$T_{shutdown}$	Thermal shutdown threshold			160		°C
T_{hys}	Thermal shutdown hysteresis			15		°C

7.6 Typical Characteristics

At T_A = 25°C, unless otherwise noted.

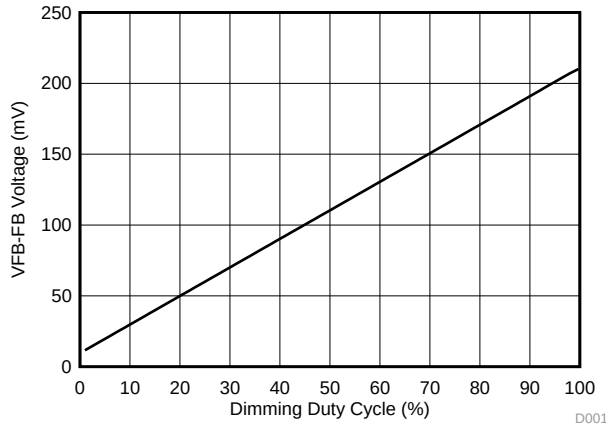


Figure 1. FB Voltage vs Dimming Duty Cycle

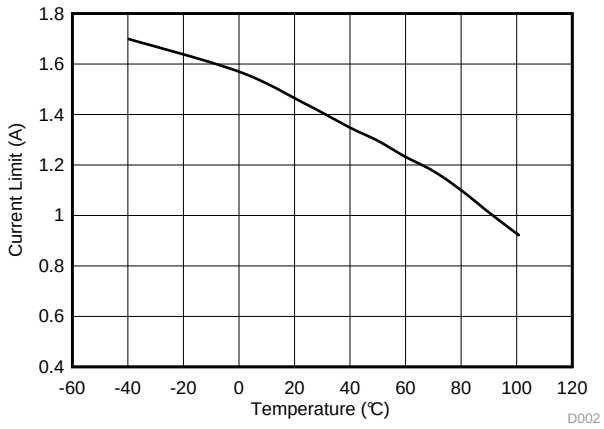


Figure 2. Current Limit vs Temperature

8 Detailed Description

8.1 Overview

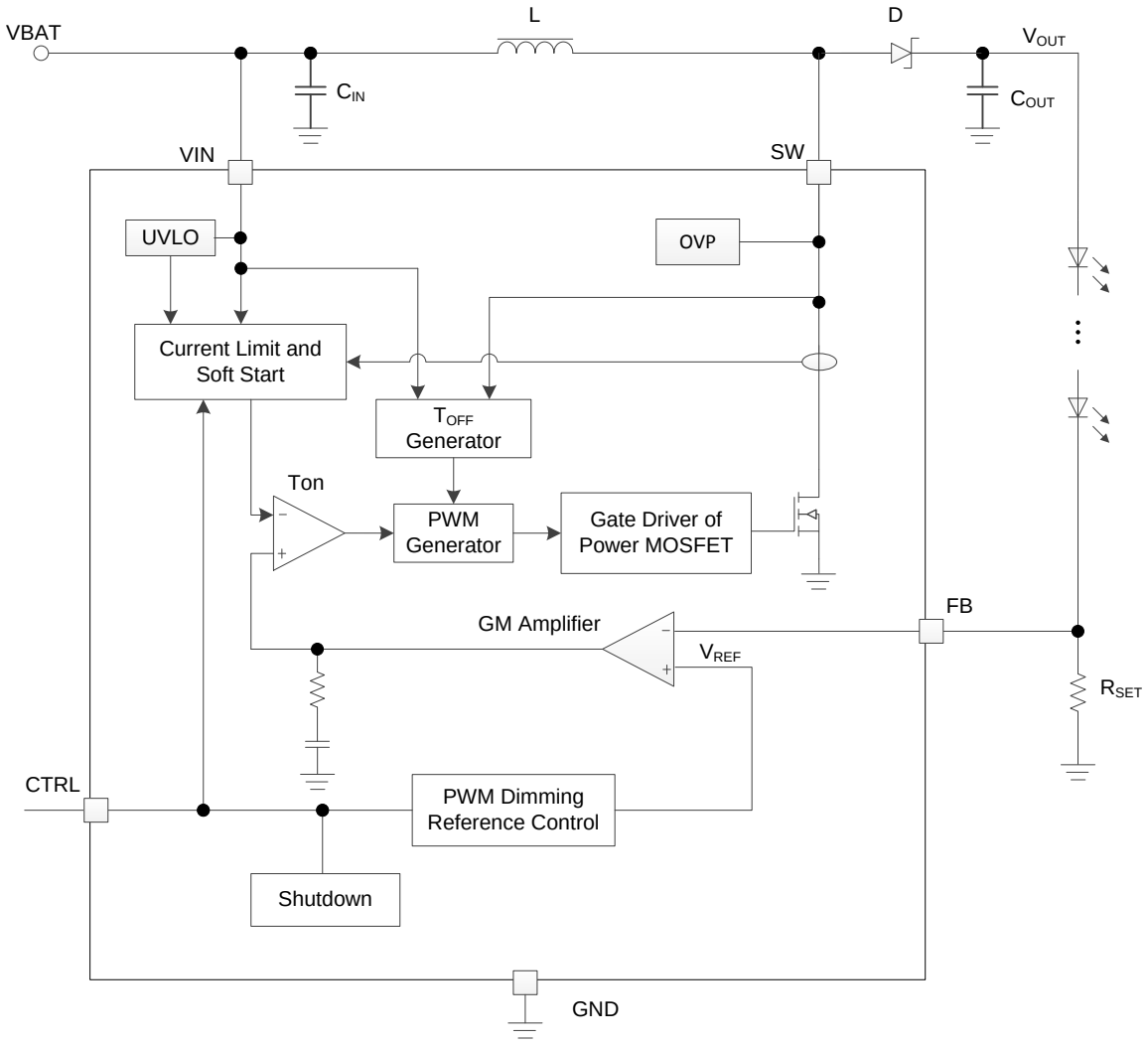
The TPS61169 is a high-efficiency, high-output voltage boost converter in small package size. The device integrates 40-V/1.8-A switch FET and is designed for output voltage up to 39 V with a switch peak current limit of 1.2 A minimum. Its large driving capability can drive single or parallel LED strings for small to large size panel backlighting.

The TPS61169 operates in a current mode scheme with quasi-constant frequency. It is internally compensated for maximum flexibility and stability. The switching frequency is 1.2 MHz, and the minimum input voltage is 2.7 V. During the on-time, the current rises into the inductor. When the current reaches a threshold value set by the internal GM amplifier, the power switch MOSFET is turned off. The polarity of the inductor changes and forward biases the schottky diode which lets the current flow towards the output of the boost converter. The off-time is fixed for a certain V_{IN} and V_{OUT}, and therefore maintains the same frequency when varying these parameters.

However, for different output loads, the frequency slightly changes due to the voltage drop across the RDS(ON) of the power switch MOSFET, this has an effect on the voltage across the inductor and thus on t_{ON} (t_{OFF} remains fixed). The fixed off-time maintains a quasi-fixed frequency that provides better stability for the system over a wider range of input and output voltages than conventional boost converters. The TPS61169 topology has also the benefits of providing very good load and line regulations, and excellent line and load transient responses.

The feedback loop regulates the FB pin to a low reference voltage (204 mV typical), reducing the power dissipation in the current sense resistor.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Soft Start-Up

Soft-start circuitry is integrated into the IC to avoid high inrush current spike during start-up. After the device is enabled, the GM amplifier output voltage ramps up very slowly, which ensures that the output voltage rises slowly to reduce the input current. During this period, the switch current limit is set to 0.72 A. After around 6.5 ms, the switch current limit changes back to I_{LIM}, and the FB pin voltage ramps up to the reference voltage slowly. These features ensure the smooth start-up and minimize the inrush current. See Figure 12 for a typical example.

8.3.2 Open LED Protection

Open LED protection circuitry prevents IC damage as the result of white LED disconnection. The TPS61169 monitors the voltage at the SW pin and FB pin during each switching cycle. The circuitry turns off the switch FET and shuts down the IC when both of the following conditions persist for 3 switching cycles: (1) the SW voltage exceeds the VOVP threshold, and (2) the FB voltage is less than 30 mV. As the result, the output voltage falls to the level of the input supply. The device remains in shutdown mode until it is enabled by toggling the CTRL pin.

Feature Description (continued)

8.3.3 Shutdown

The TPS61169 enters shutdown mode when the CTRL voltage is logic low for more than 2.5 ms. During shutdown, the input supply current for the device is less than 2 µA (max). Although the internal switch FET does not switch in shutdown, there is still a DC current path between the input and the LEDs through the inductor and Schottky diode. The minimum forward voltage of the LED array must exceed the maximum input voltage to ensure that the LEDs remain off in shutdown.

8.3.4 Current Program

The FB voltage is regulated by a low 204-mV reference voltage. The LED current is programmed externally using a current-sense resistor in series with the LED string(s). The value of the R_{SET} is calculated using:

$$I_{LED} = \frac{V_{FB}}{R_{SET}}$$

where

- I_{LED} = total output current of LED string(s)
- V_{FB} = regulated voltage of FB pin
- R_{SET} = current sense resistor (1)

The output current tolerance depends on the FB accuracy and the current sensor resistor accuracy.

8.3.5 LED Brightness Dimming

The TPS61169 receives PWM dimming signal at CTRL pin to control the total output current. When the CTRL pin is constantly high, the FB voltage is regulated to 204 mV typically. When the duty cycle of the input PWM signal is low, the regulation voltage at FB pin is reduced, and the total output current is reduced; therefore, it achieves LED brightness dimming. The relationship between the duty cycle and FB regulation voltage is given by:

$$V_{FB} = \text{Duty} \times 204\ \text{mV}$$

where

- Duty = Duty cycle of the PWM signal
- 204 mV = internal reference voltage (2)

Thus, the user can easily control the WLED brightness by controlling the duty cycle of the PWM signal.

As shown in Figure 3, the IC chops up the internal 204-mV reference voltage at the duty cycle of the PWM signal. The pulse signal is then filtered by an internal low-pass filter. The output of the filter is connected to the GM amplifier as the reference voltage for the FB pin regulation. Therefore, although a PWM signal is used for brightness dimming, only the WLED DC current is modulated, which is often referred as analog dimming. This eliminates the audible noise which often occurs when the LED current is pulsed in replica of the frequency and duty cycle of PWM control. Unlike other methods which filter the PWM signal for analog dimming, TPS61169 regulation voltage is independent of the PWM logic voltage level which often has large variations.

For optimum performance, use the PWM dimming frequency in the range of 5 kHz to 100 kHz. If the PWM frequency is lower than 5 kHz, it is out of the low pass filter's filter range, the FB regulation voltage ripple becomes large, causing large output ripple and may generate audible noise.

Feature Description (continued)

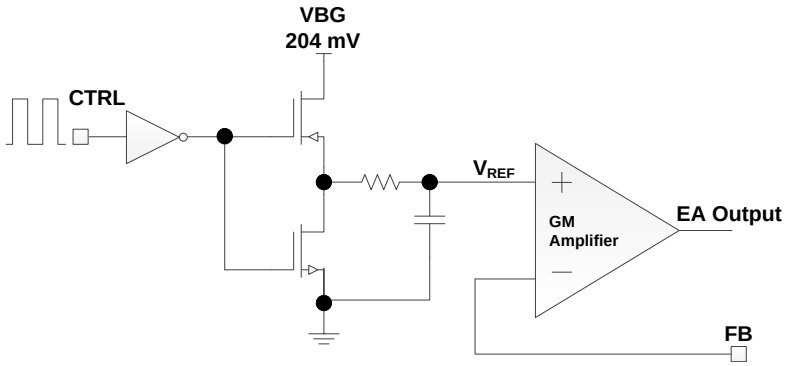


Figure 3. Programmable FB Voltage Using PWM Signal

8.3.6 Undervoltage Lockout

An undervoltage lockout prevents operation of the device at input voltages below typical 2 V. When the input voltage is below the undervoltage threshold, the device is shut down, and the internal switch FET is turned off. If the input voltage rises by undervoltage lockout hysteresis, the IC restarts.

8.3.7 Thermal Foldback and Thermal Shutdown

When TPS61169 drives heavy load for large size panel applications, the power dissipation increases a lot and the device junction temperature may reach a very high value, affecting the device function and reliability. In order to lower the thermal stress, the TPS61169 features a thermal foldback function. When the junction temperature is higher than 100°C, the switch current limit I_{LIM} is reduced automatically as Figure 2 shows. This thermal foldback mechanism controls the power dissipation and keeps the junction temperature from rising to a very high value. If the typical junction temperature of 160°C is exceeded, an internal thermal shutdown turns off the device. The device is released from shutdown automatically when the junction temperature decreases by 15°C.

8.4 Device Functional Modes

8.4.1 Operation With CTRL

The enable rising edge threshold voltage is 1.2 V. When the CTRL pin is held below that voltage the device is disabled and switching is inhibited. The IC quiescent current is reduced in this state. When input voltage is above the UVLO threshold, and the CTRL pin voltage is increased above the rising edge threshold, the device becomes active. Switching enables, and the soft-start sequence initiates.

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The TPS61169 device is a step-up DC-DC converter which can drive single or parallel LED strings for small- to large-size panel backlighting. This section includes a design procedure (*Detailed Design Procedure*) to select component values for the TPS61169 typical application (Figure 4).

9.2 Typical Application

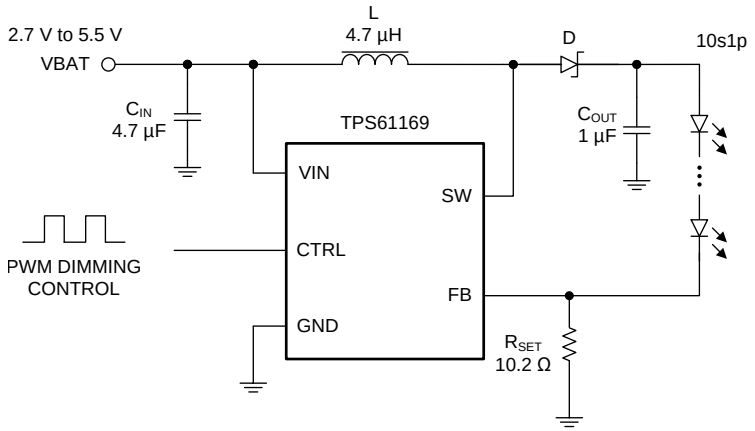


Figure 4. TPS61169 2.7-V to 5.5-V Input, 10 LEDs in Series Output Converter

9.2.1 Design Requirements

For this design example, use the parameters listed in Table 1 as the input parameters.

Table 1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage range	2.7 V to 5.5 V
Output, LED number in a string	10
Output, LED string number	1
Output, LED current per string	20 mA

9.2.2 Detailed Design Procedure

9.2.2.1 Inductor Selection

The selection of the inductor affects power efficiency, steady state operation as well as transient behavior and loop stability. These factors make it the most important component in power regulator design. There are three important inductor specifications, inductor value, DC resistance and saturation current. Considering inductor value alone is not enough. The inductor value determines the inductor ripple current. Choose an inductor that can handle the necessary peak current without saturating. Follow Equation 3 to Equation 4 to calculate the peak current of the inductor. To calculate the current in the worst case, use the minimum input voltage, maximum output voltage and maximum load current of application. In a boost regulator, the input DC current can be calculated as Equation 3.

$$I_{L(DC)} = \frac{V_{OUT} \times I_{OUT}}{V_{IN} \times \eta}$$

where

- V_{OUT} = boost output voltage
- I_{OUT} = boost output current
- V_{IN} = boost input voltage
- η = power conversion efficiency (3)

The inductor current peak to peak ripple can be calculated as Equation 4.

$$\Delta I_{L(P-P)} = \frac{1}{L \times \left(\frac{1}{V_{OUT} - V_{IN}} + \frac{1}{V_{IN}}\right) \times F_S}$$

where

- $\Delta I_{L(PP)}$ = inductor peak-to-peak ripple
- L = inductor value
- F_S = boost switching frequency
- V_{OUT} = boost output voltage
- V_{IN} = boost input voltage (4)

Therefore, the peak current $I_{L(P)}$ seen by the inductor is calculated with Equation 5.

$$I_{L(P)} = I_{L(DC)} + \frac{\Delta I_{L(P-P)}}{2} \quad (5)$$

Inductor values can have ±20% tolerance with no current bias. When the inductor current approaches saturation level, its inductance can decrease 20% to 35% from the 0-A value depending on how the inductor vendor defines saturation current. Using an inductor with a smaller inductance value forces discontinuous PWM when the inductor current ramps down to zero before the end of each switching cycle. This reduces the boost converter's maximum output current, causes large input voltage ripple and reduces efficiency. Large inductance value provides much more output current and higher conversion efficiency. For these reasons, a 4.7-µH to 10-µH inductor value range is recommended, and 4.7-µH inductor is recommended for higher than 5-V input voltage by considering inductor peak current and loop stability. Table 2 lists the recommended inductor for the TPS61169.

Table 2. Recommended Inductors for TPS61169

PART NUMBER	L (µH)	DCR MAX (mΩ)	SATURATION CURRENT (A)	SIZE (L x W x H mm)	VENDOR
LPS4018-472ML	4.7	125	1.9	4 × 4 × 1.8	Coilcraft
LPS4018-103ML	10	200	1.3	4 × 4 × 1.8	Coilcraft
PCMB051H-4R7M	4.7	85	4	5.4 × 5.2 × 1.8	Cyntec
PCMB051H-100M	10	155	3	5.4 × 5.2 × 1.8	Cyntec

9.2.2.2 Schottky Diode Selection

The TPS61169 demands a low forward voltage, high-speed and low capacitance Schottky diode for optimum efficiency. Ensure that the diode average and peak current rating exceeds the average output current and peak inductor current. In addition, the diode reverse breakdown voltage must exceed the open LED protection voltage. ONSemi NSR0240 is recommended for the TPS61169.

9.2.2.3 Output Capacitor Selection

The output capacitor is mainly selected to meet the requirement for the output ripple and loop stability. This ripple voltage is related to capacitor capacitance and its equivalent series resistance (ESR). Assuming a capacitor with zero ESR, the minimum capacitance needed for a given ripple can be calculated with Equation 6:

$$C_{OUT} = \frac{(V_{OUT} - V_{IN}) \times I_{OUT}}{V_{OUT} \times F_S \times V_{ripple}}$$

where

- V_{ripple} = peak-to-peak output ripple (6)

The additional part of the ripple caused by ESR is calculated using: $V_{ripple\_ESR} = I_{OUT} \times R_{ESR}$

Due to its low ESR, V_{ripple_ESR} could be neglected for ceramic capacitors, a 1-µF to 4.7-µF capacitor is recommended for typical application.

9.2.2.4 LED Current Set Resistor

The LED current set resistor can be calculated by Equation 1.

9.2.2.5 Thermal Considerations

The allowable IC junction temperature must be considered under normal operating conditions. This restriction limits the power dissipation of the TPS61169. The allowable power dissipation for the device can be determined by Equation 7:

$$P_D = \frac{T_J - T_A}{R_{\theta JA}}$$

where

- T_J is allowable junction temperature given in recommended operating conditions
- T_A is the ambient temperature for the application
- $R_{\theta JA}$ is the thermal resistance junction-to-ambient given in Power Dissipation Table (7)

The TPS61169 device also features a thermal foldback function to reduce the thermal stress automatically.

9.3 Application Curves

Typical application condition is as in Figure 4, V_{IN} = 3.6 V, R_{SET} = 10.2 Ω, L = 4.7 µH, C_{OUT} = 1 µF, 10 LEDs in series (unless otherwise specified).

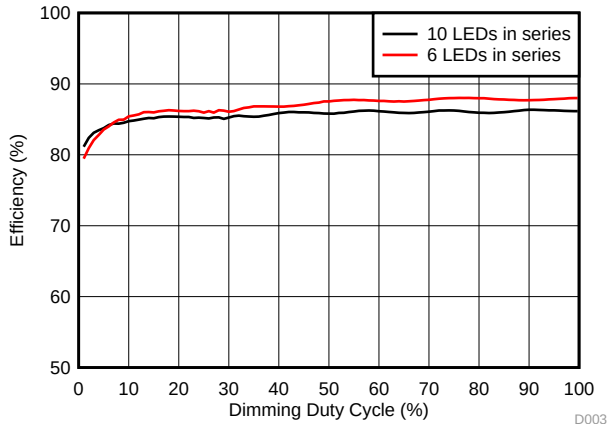


Figure 5. Efficiency vs Dimming Duty Cycle

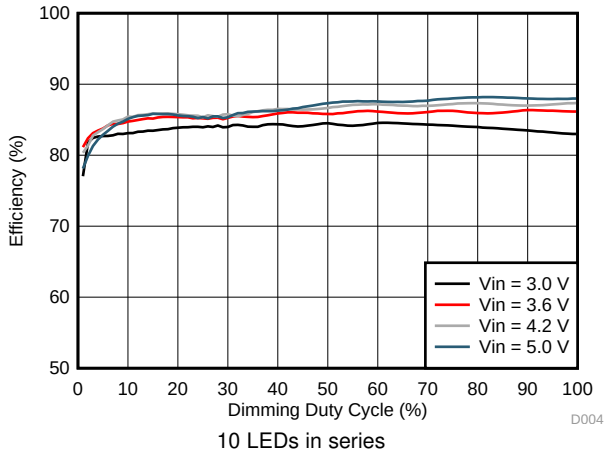


Figure 6. Efficiency vs Dimming Duty Cycle

Application Curves (continued)

Typical application condition is as in Figure 4, V_{IN} = 3.6 V, R_{SET} = 10.2 Ω, L = 4.7 µH, C_{OUT} = 1 µF, 10 LEDs in series (unless otherwise specified).

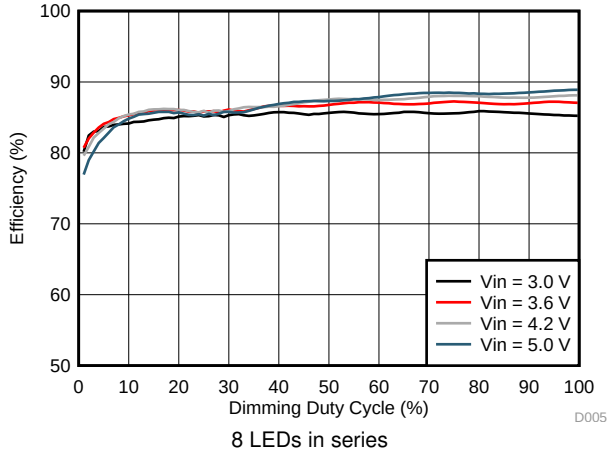


Figure 7. Efficiency vs Dimming Duty Cycle

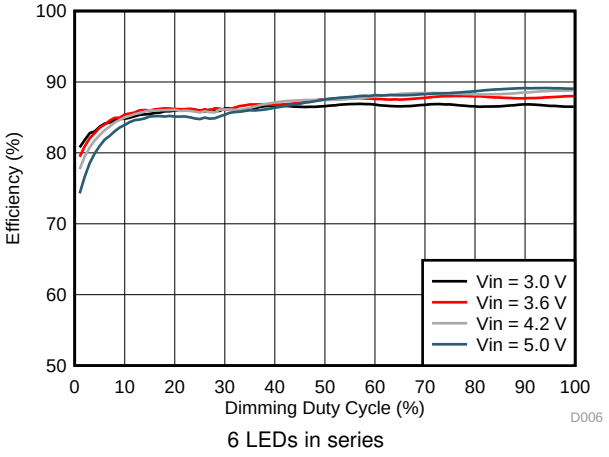


Figure 8. Efficiency vs Dimming Duty Cycle

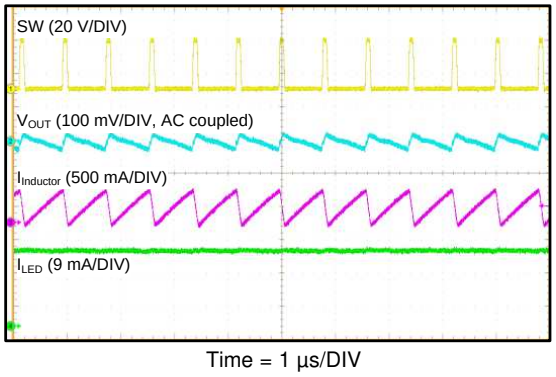


Figure 9. Switching-Dimming Duty = 100%

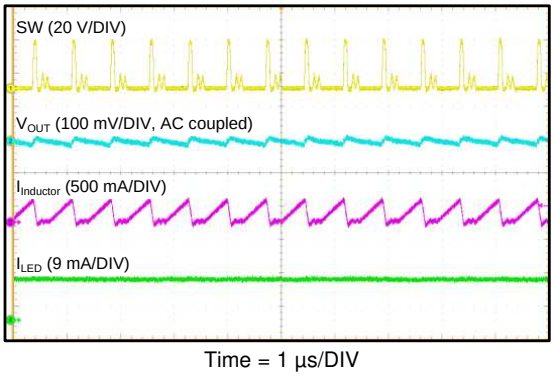


Figure 10. Switching-Dimming Duty = 50%

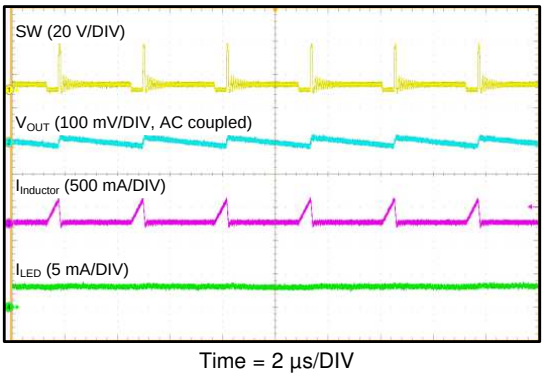


Figure 11. Switching-Dimming Duty = 10%

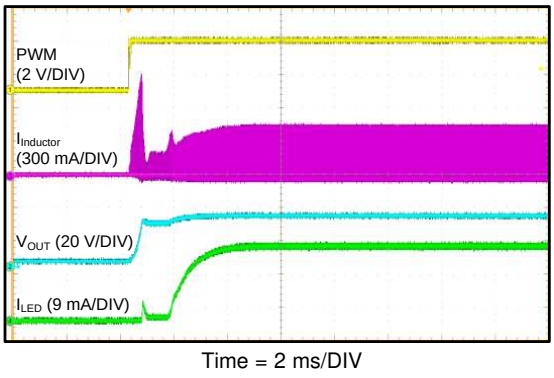
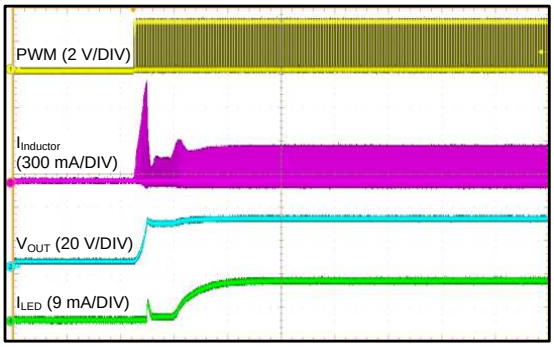


Figure 12. Start-Up Dimming Duty = 100%

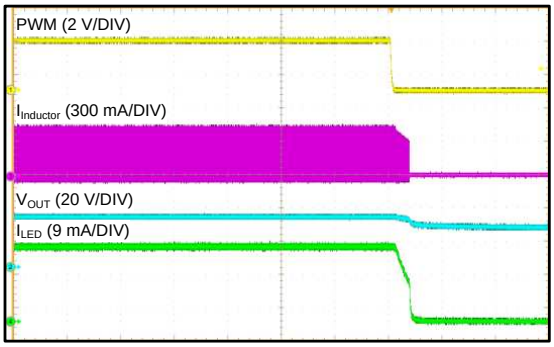
Application Curves (continued)

Typical application condition is as in Figure 4, V_{IN} = 3.6 V, R_{SET} = 10.2 Ω, L = 4.7 µH, C_{OUT} = 1 µF, 10 LEDs in series (unless otherwise specified).



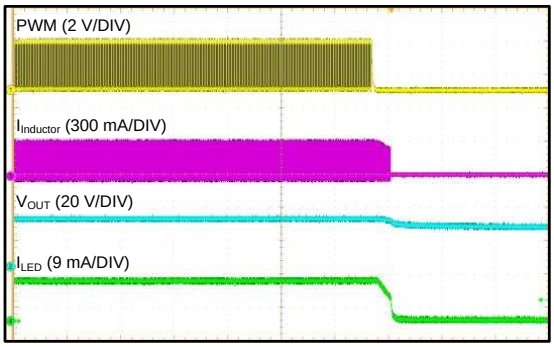
Time = 2 ms/DIV

Figure 13. Start-Up Dimming Duty = 50%



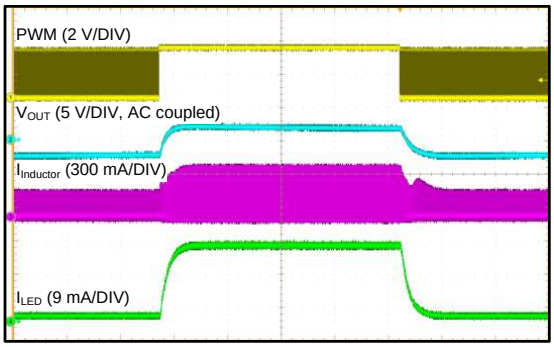
Time = 2 ms/DIV

Figure 14. Shutdown Dimming Duty = 100%



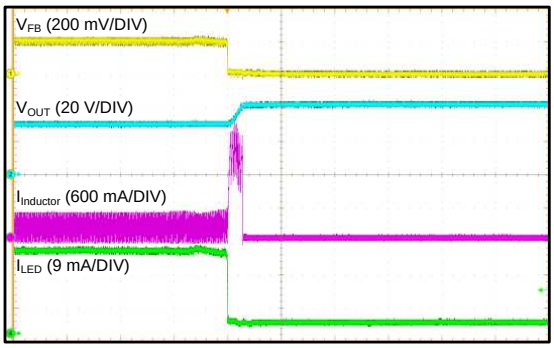
Time = 2 ms/DIV
Duty = 50%

Figure 15. Shutdown Dimming



Time = 5 ms/DIV
Duty = 1%-100%-1%

Figure 16. Dimming Transient-Dimming



Time = 50 µs/DIV

Figure 17. Open LED Protection

10 Power Supply Recommendations

The device is designed to operate from an input voltage supply range between 2.7 V and 5.5 V. This input supply must be well regulated. If the input supply is located more than a few inches from the TPS61169 device, additional bulk capacitance may be required in addition to the ceramic bypass capacitors.

11 Layout

11.1 Layout Guidelines

As for all switching power supplies, especially those high frequency and high current ones, layout is an important design step. If layout is not carefully done, the regulator could suffer from instability as well as noise problems. Therefore, use wide and short traces for high current paths. The input capacitor C_{IN} must be close to VIN pin and GND pin in order to reduce the input ripple seen by the device. If possible choose higher capacitance value for it. The SW pin carries high current with fast rising and falling edge; therefore, the connection between the SW pin to the inductor must be kept as short and wide as possible. The output capacitor C_{OUT} must be put close to VOUT pin. It is also beneficial to have the ground of C_{OUT} close to the GND pin because there is large ground return current flowing between them. FB resistor must be put close to FB pin. When laying out signal ground, TI recommends using short traces separated from power ground traces, and connect them together at a single point close to the GND pin.

11.2 Layout Example

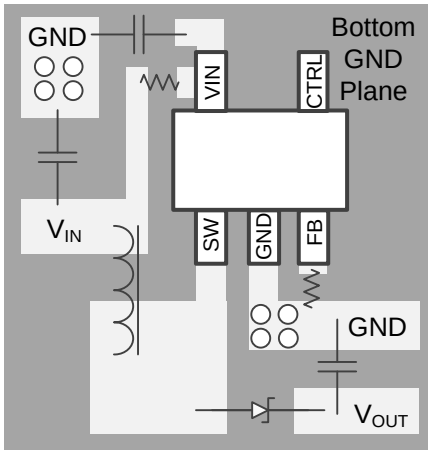


Figure 18. TPS61169 Board Layout

12 Device and Documentation Support

12.1 Device Support

12.1.1 Third-Party Products Disclaimer

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12.2 Community Resources

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Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.3 Trademarks

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All other trademarks are the property of their respective owners.

12.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS61169DCKR	ACTIVE	SC70	DCK	5	3000	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 85	SZL	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

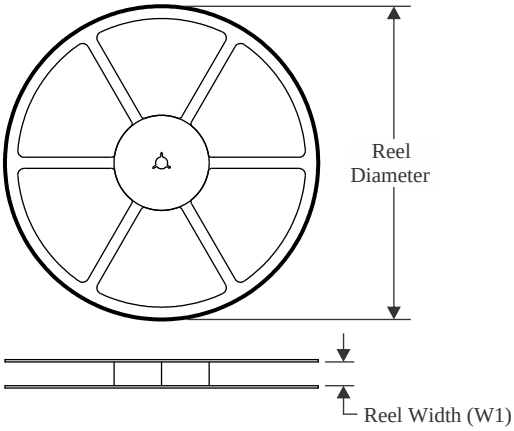
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

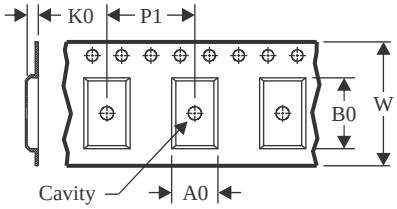
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

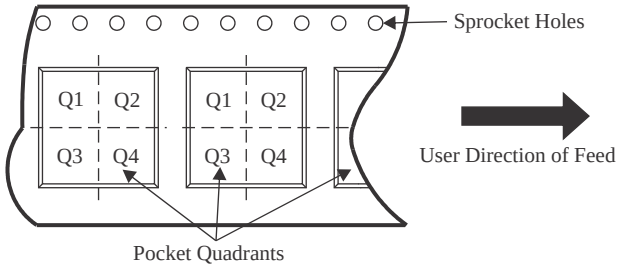


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

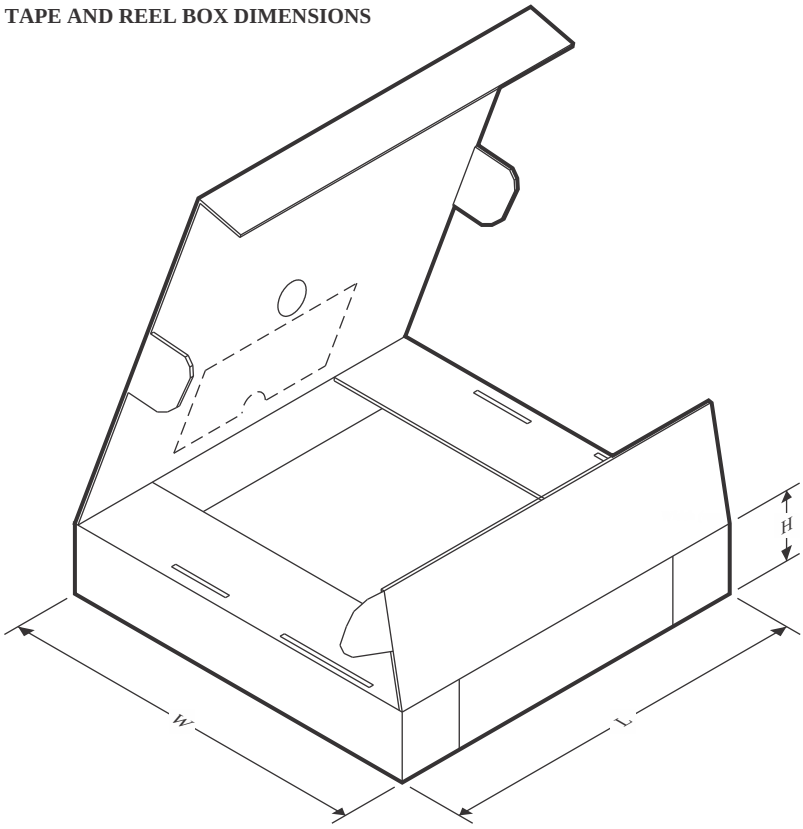
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS61169DCKR	SC70	DCK	5	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

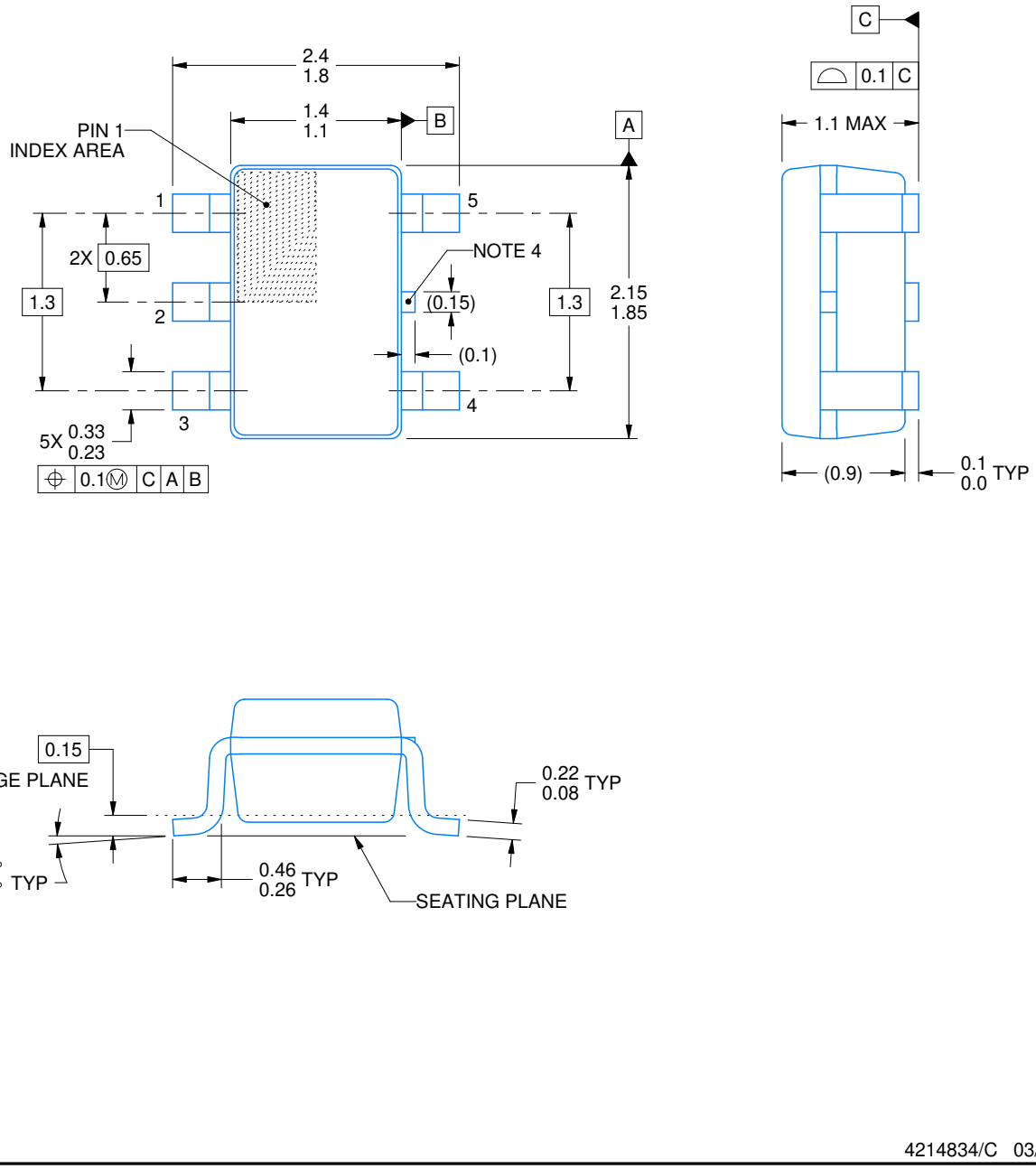
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS61169DCKR	SC70	DCK	5	3000	180.0	180.0	18.0

PACKAGE OUTLINE

DCK0005A

SOT - 1.1 max height

SMALL OUTLINE TRANSISTOR



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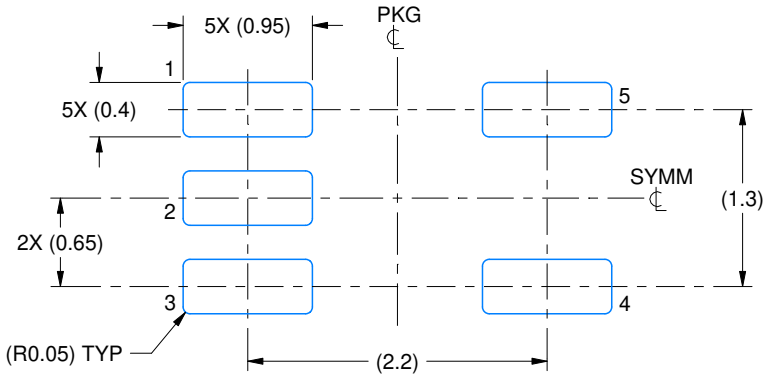
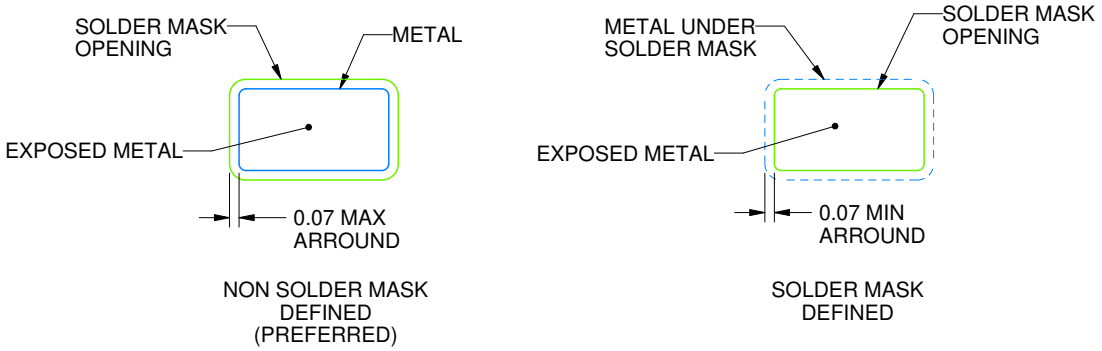
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-203.
4. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X



SOLDER MASK DETAILS

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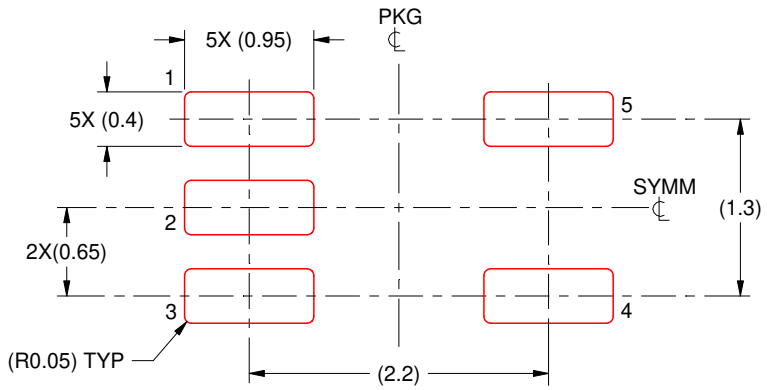
NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:18X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

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