
KSZ8863 Daughter Board Information Sheet

Abstract

The KSZ8863 Daughter Board (AC320004-7) enables Ethernet communication with a variety of Microchip starter kits. This information sheet provides an overview and a detailed schematic of the KSZ8863 Daughter Board.

This daughter board is designed specifically to be used with the PIC32 Ethernet Starter Kit II (DM320004-2) or the PIC32MZ Embedded Connectivity with Floating Point Unit (EF) Starter Kit (DM320007); however, it can also be used with other Microchip development hardware.

For additional information about the KSZ8863 Daughter Board, visit Microchip web site: <http://www.microchip.com>.

1 Features

The KSZ8863 Daughter Board features a 22-pin header for connecting the board into compatible PIC32 starter kits. The board has a KSZ8863 Ethernet Physical Layer Chip, configured to use RMII. The KSZ8863 Daughter Board is suitable for use with the PIC32 Ethernet Starter Kit II and PIC32MZ EF Starter Kit.

The following are features of the KSZ8863 Daughter Board:

- RMII interface with MDC/MDIO management interface for register configuration
- Fast start-up and link
- Loopback modes for diagnostics
- Integrated 3-Port 10/100 Managed Switch with PHYs
- IEEE 802.1q VLAN Support
- Optional SPI interface
- Compliant with IEEE 802.3u standard

2 Applications

- VoIP Phone
- Set-Top/Game Box
- Automotive
- Industrial Control
- IPTV POF
- SOHO Residential Gateway
- Broadband Gateway/Firewall/VPN
- Integrated DSL/Cable Modem

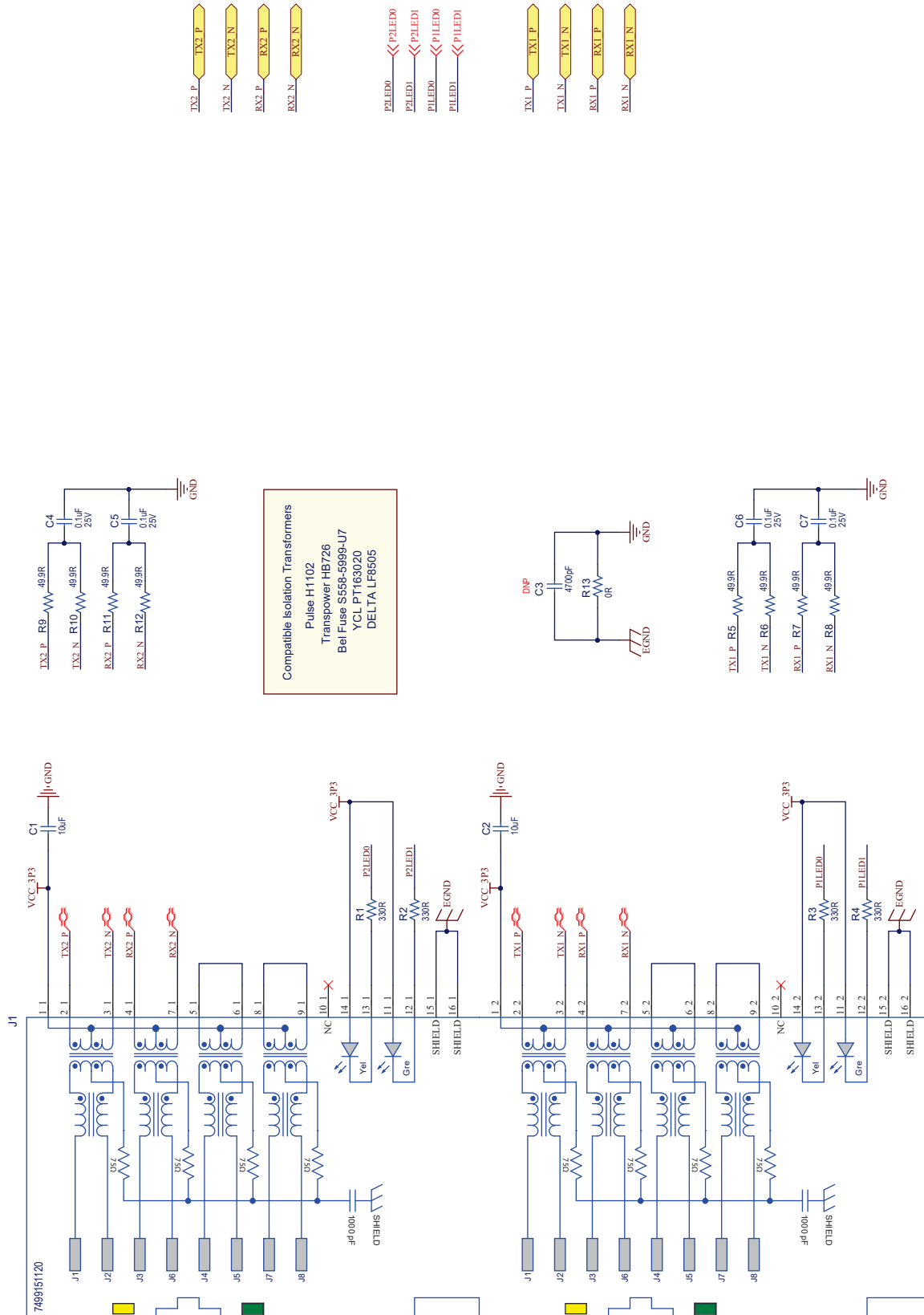
- Wireless LAN Access Point + Gateway
- Standalone 10/100 Switch

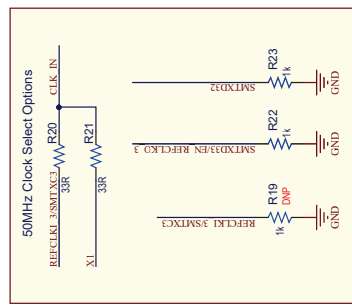
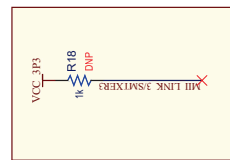
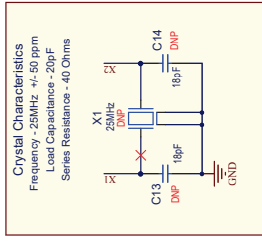
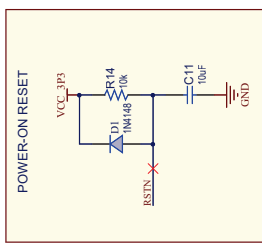
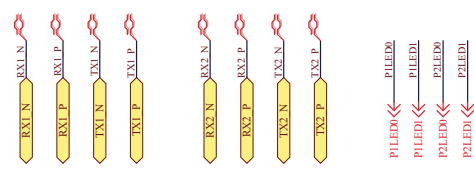
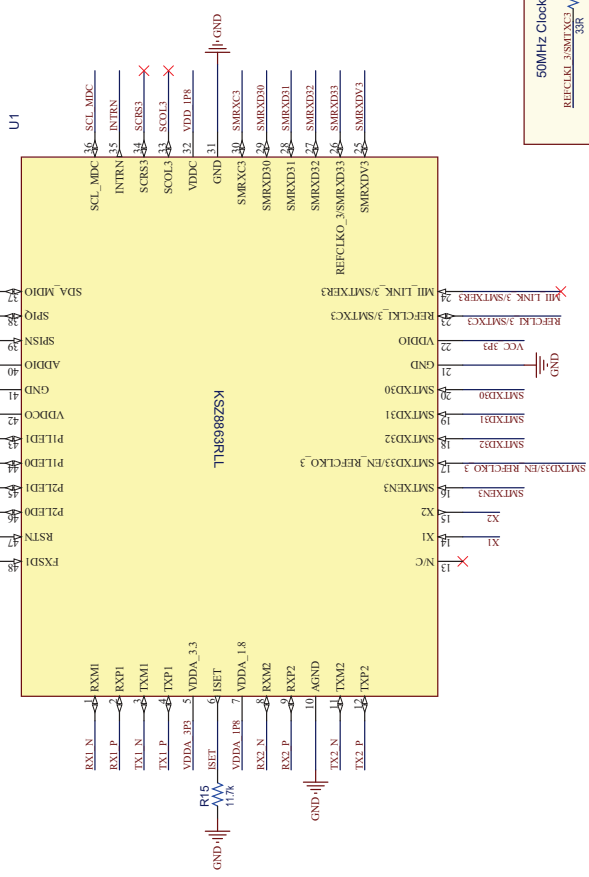
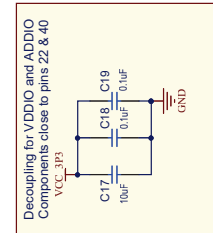
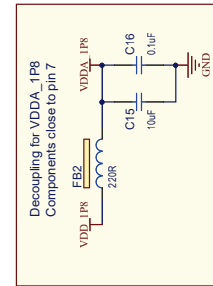
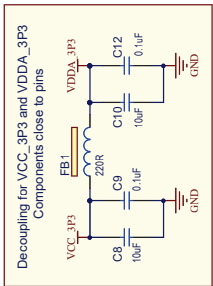
3 Additional Information

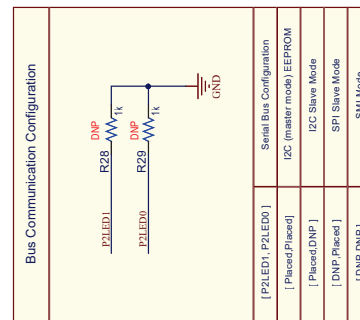
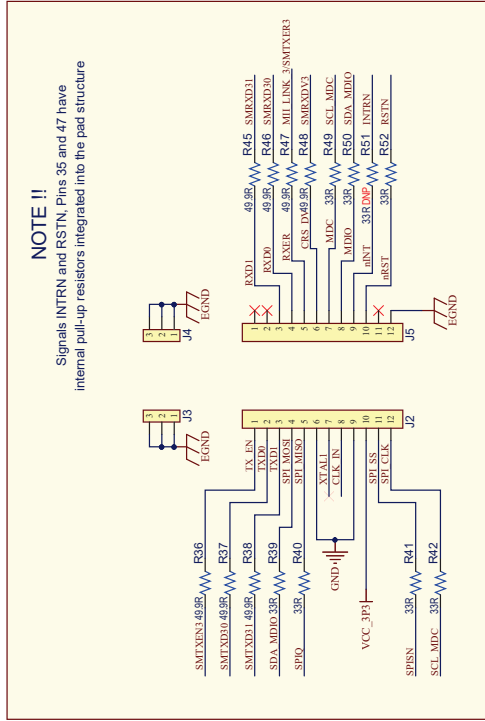
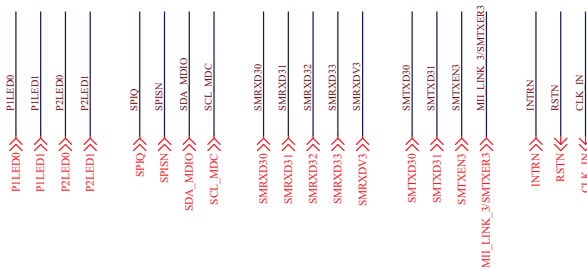
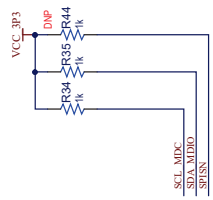
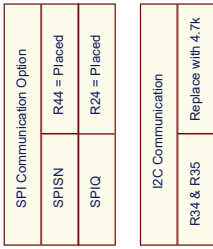
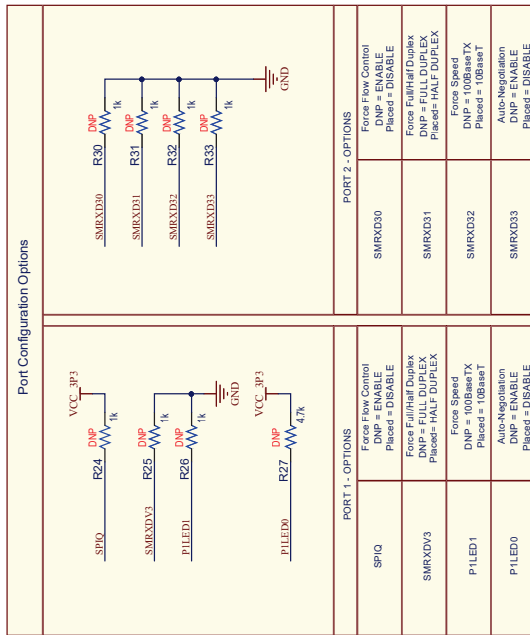
For additional information on drivers and examples, follow these links:

- <https://www.microchip.com/wwwproducts/en/KSZ8863>
- <http://www.microchip.com/mplab/mplab-harmony>

1. Schematics







Clock Source Configuration

Reg[19:bit[5]	Pin 17 SMTXD03 Internal Pull-Up (EN_REFCLK0_3)	Pin 18 SMTXD02 Internal Pull-Up (FORNVA3)	Clock Source	Note
0	0 (use 1k Pull-Down)	0 (use 1k Pull-Down)	External 50MHz OSC (not to SMTXC/REFCLK0_3 and X1 pin directly)	EN_REFCLK0_3 = 0 to Disable REFCLK0_3 for better EMI
0	1 (use 1k Pull-Down)	0 (use 1k Pull-Down)	50MHz on X1 pin is clock source. REFCLK0_3 to REFCLK0_3 externally	EN_REFCLK0_3 = 1 to Enable REFCLK0_3
0	1	1	25MHz on X1 pin is clock source. REFCLK0_3 to REFCLK0_3 externally	EN_REFCLK0_3 = 1 to Enable REFCLK0_3
1	0	0 or 1	25MHz on X1 pin is clock source. REFCLK0_3 to REFCLK0_3 internally	EN_REFCLK0_3 = 0 to Disable REFCLK0_3 for better EMI

2. Revision History

Revision B - March 2019

The following changes were implemented for this release:

- Updated the schematics:
 - Added the property and notation DNP to the resistor R51
- Updated document format

Revision A - June 2018

Initial release of this document.

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ISBN: 978-1-5224-4249-3

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