National Semiconductor

54F/74F161A • 54F/74F163A
Synchronous Presettable Binary Counter

General Description

The 'F161A and 'F163A are high-speed synchronous modulo-16 binary counters. They are synchronously presettable for application in programmable dividers and have two types of Count Enable inputs plus a Terminal Count output for versatility in forming synchronous multi-stage counters. The 'F161A has an asynchronous Master-Reset input that overrides all other inputs and forces the outputs LOW. The 'F163A has a Synchronous Reset input that overrides counting and parallel loading and allows the outputs to be simultaneously reset on the rising edge of the clock. The 'F161A and 'F163A are high-speed versions of the 'F161 and 'F163.

Features

- Synchronous counting and loading
- High-speed synchronous expansion
- Typical count frequency of 120 MHz
- Guaranteed 4000V minimum ESD protection

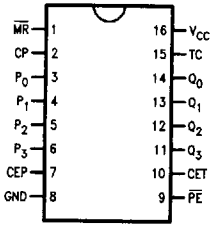
Ordering Code: See Section 11

Commercial	Military	Package Number	Package Description
74F161APC		N16E	16-Lead (0.300" Wide) Molded Dual-In-Line
	54F161ADM (Note 2)	J16A	16-Lead Ceramic Dual-In-Line
74F161ASC (Note 1)		M16A	16-Lead (0.150" Wide) Molded Small Outline, JEDEC
74F161ASJ (Note 1)		M16D	16-Lead (0.300" Wide) Molded Small Outline, EIAJ
	54F161AFM (Note 2)	W16A	16-Lead Cerpack
	54F161ALM (Note 2)	E20A	20-Lead Ceramic Leadless Chip Carrier, Type C
74F163APC		N16E	16-Lead (0.300" Wide) Molded Dual-In-Line
	54F163ADM (Note 2)	J16A	16-Lead Ceramic Dual-In-Line
74F163ASC (Note 1)		M16A	16-Lead (0.150" Wide) Molded Small Outline, JEDEC
74F163ASJ (Note 1)		M16D	16-Lead (0.300" Wide) Molded Small Outline, EIAJ
	54F163AFM (Note 2)	W16A	16-Lead Cerpack
	54F163ALM (Note 2)	E20A	20-Lead Ceramic Leadless Chip Carrier, Type C

Note 1: Devices also available in 13" reel. Use suffix = SCX and SJX.
Note 2: Military grade device with environmental and burn-in processing. Use suffix = DMQB, FMQB and LMQB.

Connection Diagrams

Pin Assignment for DIP, SOIC and Flatpak 'F161A



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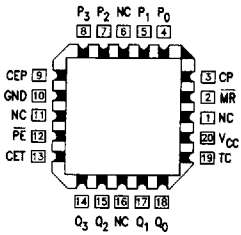
Pin Assignment for LCC 'F161A



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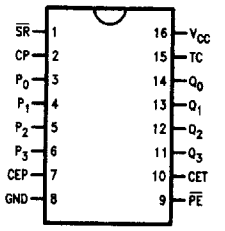
Pin Assignment for DIP, SOIC and Flatpak 'F163A



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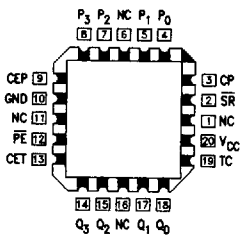
Pin Assignment for LCC 'F163A



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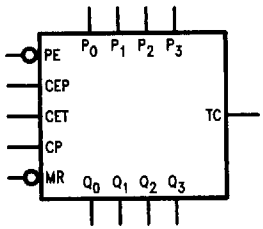
Logic Symbols

'F161A



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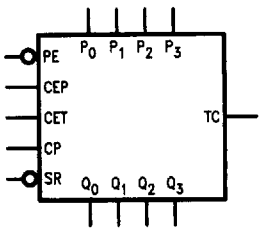
'F163A



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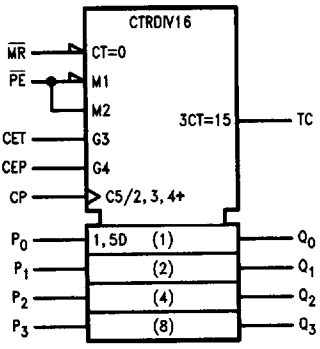
IEEE/IEC
'F161A



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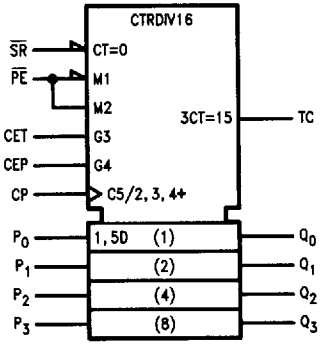
IEEE/IEC
'F163A



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Unit Loading/Fan Out: See Section 2 for U.L. Definitions

Pin Names	Description	54F/74F	
		U.L. HIGH/LOW	Input I_{IH}/I_{IL} Output I_{OH}/I_{OL}
CEP	Count Enable Parallel Input	1.0/1.0	20 μA/−0.6 mA
CET	Count Enable Trickle Input	1.0/2.0	20 μA/−1.2 mA
CP	Clock Pulse Input (Active Rising Edge)	1.0/1.0	20 μA/−0.6 mA
$\overline{MR}$ ('F161A)	Asynchronous Master Reset Input (Active LOW)	1.0/1.0	20 μA/−0.6 mA
$\overline{SR}$ ('F163A)	Synchronous Reset Input (Active LOW)	1.0/2.0	20 μA/−1.2 mA
P_0–P_3	Parallel Data Inputs	1.0/1.0	20 μA/−0.6 mA
$\overline{PE}$	Parallel Enable Input (Active LOW)	1.0/2.0	20 μA/−1.2 mA
Q_0–Q_3	Flip-Flop Outputs	50/33.3	−1 mA/20 mA
TC	Terminal Count Output	50/33.3	−1 mA/20 mA

Functional Description

The 'F161A and 'F163A count in modulo-16 binary sequence. From state 15 (HHHH) they increment to state 0 (LLLL). The clock inputs of all flip-flops are driven in parallel through a clock buffer. Thus all changes of the Q outputs (except due to Master Reset of the 'F161A) occur as a result of, and synchronous with, the LOW-to-HIGH transition of the CP input signal. The circuits have four fundamental modes of operation, in order of precedence: asynchronous reset ('F161A), synchronous reset ('F163A), parallel load, count-up and hold. Five control inputs—Master Reset ($\overline{MR}$, 'F161A), Synchronous Reset ($\overline{SR}$, 'F163A), Parallel Enable ($\overline{PE}$), Count Enable Parallel (CEP) and Count Enable Trickle (CET)—determine the mode of operation, as shown in the Mode Select Table. A LOW signal on $\overline{MR}$ overrides all other inputs and asynchronously forces all outputs LOW. A LOW signal on $\overline{SR}$ overrides counting and parallel loading and allows all outputs to go LOW on the next rising edge of CP. A LOW signal on $\overline{PE}$ overrides counting and allows information on the Parallel Data (P_n) inputs to be loaded into the flip-flops on the next rising edge of CP. With $\overline{PE}$ and $\overline{MR}$ ('F161A) or $\overline{SR}$ ('F163A) HIGH, CEP and CET permit counting when both are HIGH. Conversely, a LOW signal on either CEP or CET inhibits counting.

The 'F161A and 'F163A use D-type edge triggered flip-flops and changing the $\overline{SR}$, $\overline{PE}$, CEP and CET inputs when the CP is in either state does not cause errors, provided that the recommended setup and hold times, with respect to the rising edge of CP, are observed.

The Terminal Count (TC) output is HIGH when CET is HIGH and the counter is in state 15. To implement synchronous multi-stage counters, the TC outputs can be used with the CEP and CET inputs in two different ways. Please refer to the 'F568 data sheet. The TC output is subject to decoding spikes due to internal race conditions and is therefore not recommended for use as a clock or asynchronous reset for flip-flops, counters or registers.

Logic Equations: Count Enable = CEP • CET • $\overline{PE}$

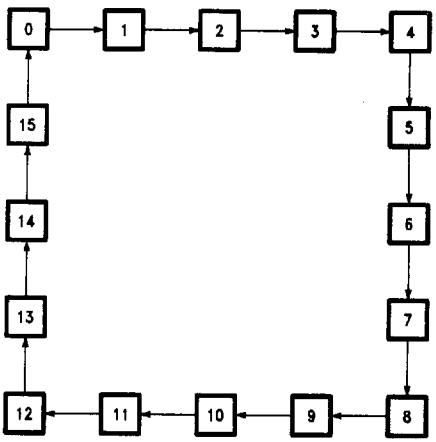
$$TC = Q_0 \bullet Q_1 \bullet Q_2 \bullet Q_3 \bullet CET$$

Mode Select Table

*$\overline{SR}$	$\overline{PE}$	CET	CEP	Action on the Rising Clock Edge (↗)
L	X	X	X	Reset (Clear)
H	L	X	X	Load ($P_n \rightarrow Q_n$)
H	H	H	H	Count (Increment)
H	H	L	X	No Change (Hold)
H	H	X	L	No Change (Hold)

*For 'F163A only
H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

State Diagram



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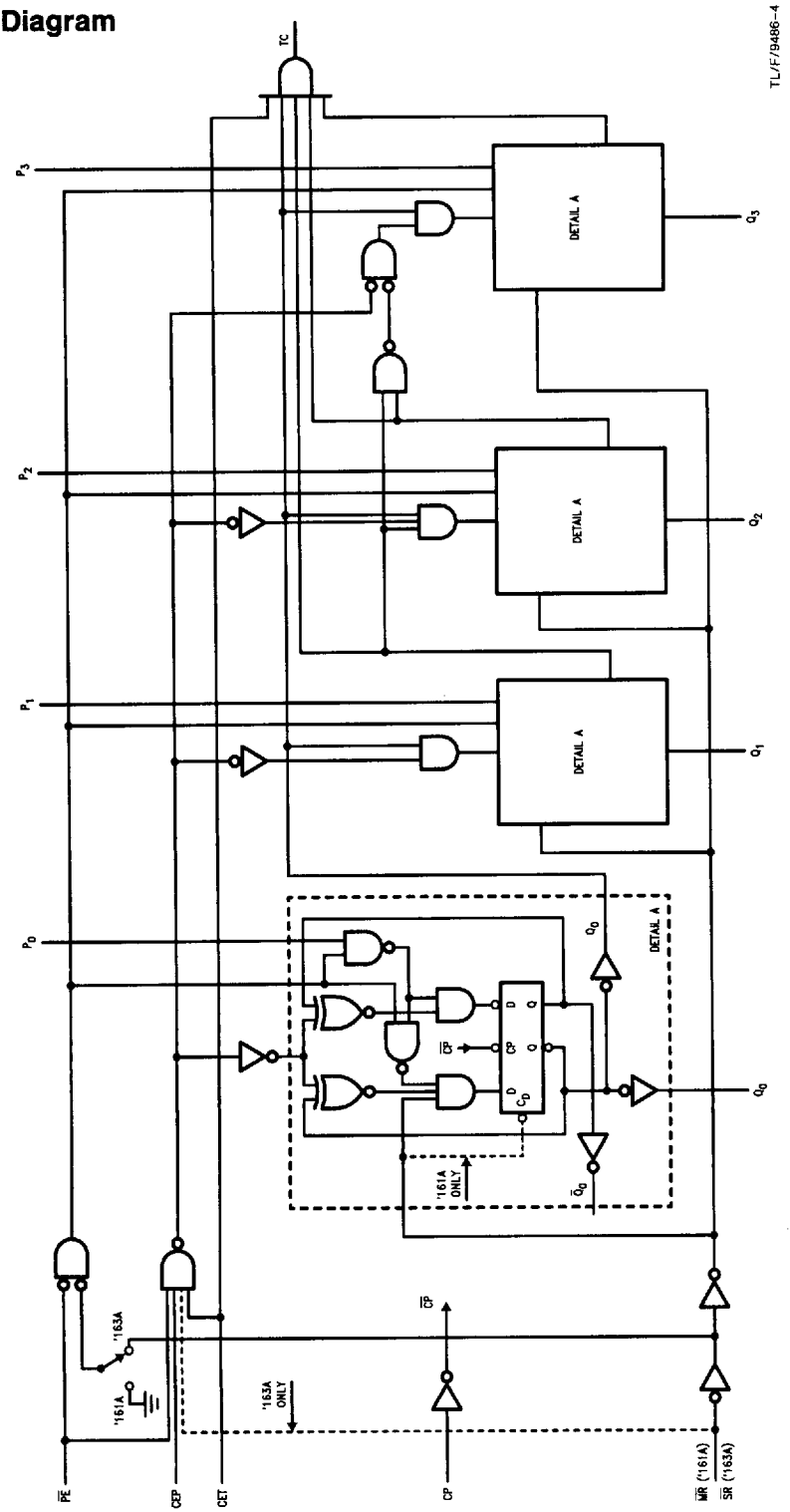
Block Diagram



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Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
Ambient Temperature under Bias	−55°C to +125°C
Junction Temperature under Bias	−55°C to +175°C
Plastic	−55°C to +150°C
V_{CC} Pin Potential to Ground Pin	−0.5V to +7.0V
Input Voltage (Note 2)	−0.5V to +7.0V
Input Current (Note 2)	−30 mA to +5.0 mA
Voltage Applied to Output in HIGH State (with V_{CC} = 0V)	
Standard Output	−0.5V to V_{CC}
TRI-STATE® Output	−0.5V to +5.5V
Current Applied to Output in LOW State (Max)	twice the rated I_{OL} (mA)
ESD Last Passing Voltage (Min)	4000V

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

Recommended Operating Conditions

Free Air Ambient Temperature	
Military	−55°C to +125°C
Commercial	0°C to +70°C
Supply Voltage	
Military	+4.5V to +5.5V
Commercial	+4.5V to +5.5V

DC Electrical Characteristics

Symbol	Parameter		54F/74F Min	54F/74F Typ	54F/74F Max	Units	V_{CC}	Conditions
V_{IH}	Input HIGH Voltage		2.0			V		Recognized as a HIGH Signal
V_{IL}	Input LOW Voltage				0.8	V		Recognized as a LOW Signal
V_{CD}	Input Clamp Diode Voltage				−1.2	V	Min	I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	54F 10% V_{CC}	2.5			V	Min	I_{OH} = −1 mA
		74F 10% V_{CC}	2.5					
		74F 5% V_{CC}	2.7					
V_{OL}	Output LOW Voltage	54F 10% V_{CC}			0.5	V	Min	I_{OL} = 20 mA
		74F 10% V_{CC}			0.5			
I_{IH}	Input HIGH Current	54F			20.0	μA	Max	V_{IN} = 2.7V
		74F			5.0			
I_{BVI}	Input HIGH Current Breakdown Test	54F			100	μA	Max	V_{IN} = 7.0V
		74F			7.0			
I_{CEX}	Output HIGH Leakage Current	54F			250	μA	Max	V_{OUT} = V_{CC}
		74F			50			
V_{ID}	Input Leakage Test	74F	4.75			V	0.0	I_{ID} = 1.9 μA All Other Pins Grounded
I_{OD}	Output Leakage Circuit Current	74F			3.75	μA	0.0	V_{IOD} = 150 mV All Other Pins Grounded
I_{IL}	Input LOW Current				−0.6	mA	Max	V_{IN} = 0.5V (CEP, CP, $\overline{MR}$, P_0–P_3)
					−1.2	mA	Max	V_{IN} = 0.5V (CET, $\overline{PE}$, $\overline{SR}$)
I_{OS}	Output Short-Circuit Current		−60		−150	mA	Max	V_{OUT} = 0V
I_{CC}	Power Supply Current			37	55	mA	Max	

AC Electrical Characteristics: See Section 2 for Waveforms and Load Configurations

Symbol	Parameter	74F $T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50\ pF$			54F $T_A, V_{CC} = Mil$ $C_L = 50\ pF$		74F $T_A, V_{CC} = Com$ $C_L = 50\ pF$		Units	Fig. No.
		Min	Typ	Max	Min	Max	Min	Max		
f_{max}	Maximum Count Frequency	100	120		75		90		MHz	2-1
t_{PLH} t_{PHL}	Propagation Delay CP to Q_n ($\overline{PE}$ Input HIGH)	3.5 3.5	5.5 7.5	7.5 10.0	3.5 3.5	9.0 11.5	3.5 3.5	8.5 11.0	ns	2-3
t_{PLH} t_{PHL}	Propagation Delay CP to Q_n ($\overline{PE}$ Input LOW)	4.0 4.0	6.0 6.0	8.5 8.5	4.0 4.0	10.0 10.0	4.0 4.0	9.5 9.5		
t_{PLH} t_{PHL}	Propagation Delay CP to TC	5.0 5.0	10.0 10.0	14.0 14.0	5.0 5.0	16.5 15.5	5.0 5.0	15.0 15.0	ns	2-3
t_{PLH} t_{PHL}	Propagation Delay CET to TC	2.5 2.5	4.5 4.5	7.5 7.5	2.5 2.5	9.0 9.0	2.5 2.5	8.5 8.5	ns	2-3
t_{PHL}	Propagation Delay $\overline{MR}$ to Q_n ('F161A)	5.5	9.0	12.0	5.5	14.0	5.5	13.0	ns	2-3
t_{PHL}	Propagation Delay $\overline{MR}$ to TC ('F161A)	4.5	8.0	10.5	4.5	12.5	4.5	11.5	ns	2-3

AC Operating Requirements: See Section 2 for Waveforms

Symbol	Parameter	74F $T_A = +25°C$ $V_{CC} = +5.0V$		54F $T_A, V_{CC} = Mil$		74F $T_A, V_{CC} = Com$		Units	Fig. No.
		Min	Max	Min	Max	Min	Max		
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW P_n to CP	5.0 5.0		5.5 5.5		5.0 5.0		ns	2-6
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW P_n to CP	2.0 2.0		2.5 2.5		2.0 2.0			
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW $\overline{PE}$ or $\overline{SR}$ to CP	11.0 8.5		13.5 10.5		11.5 9.5		ns	2-6
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW $\overline{PE}$ or $\overline{SR}$ to CP	2.0 0		3.6 0		2.0 0			
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW CEP or CET to CP	11.0 5.0		13.0 6.0		11.5 5.0		ns	2-6
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW CEP or CET to CP	0 0		0 0		0 0			
$t_w(H)$ $t_w(L)$	Clock Pulse Width (Load) HIGH or LOW	5.0 5.0		5.0 5.0		5.0 5.0		ns	2-4
$t_w(H)$ $t_w(L)$	Clock Pulse Width (Count) HIGH or LOW	4.0 6.0		5.0 8.0		4.0 7.0		ns	2-4
$t_w(L)$	$\overline{MR}$ Pulse Width, LOW ('F161A)	5.0		5.0		5.0		ns	2-4
t_{rec}	Recovery Time $\overline{MR}$ to CP ('F161A)	6.0		6.0		6.0		ns	2-6