

# RF LDMOS Wideband Integrated Power Amplifiers

The MD7IC21100N wideband integrated circuit is designed with on-chip matching that makes it usable from 2110 to 2170 MHz. This multi-stage structure is rated for 24 to 32 Volt operation and covers all typical cellular base station modulation formats including TD-SCDMA.

- Typical Single-Carrier W-CDMA Performance:  $V_{DD} = 28$  Volts,  $I_{DQ1A} + I_{DQ1B} = 190$  mA,  $I_{DQ2A} + I_{DQ2B} = 925$  mA,  $P_{out} = 32$  Watts Avg.,  $f = 2167.5$  MHz, IQ Magnitude Clipping, Channel Bandwidth = 3.84 MHz, Input Signal PAR = 7.5 dB @ 0.01% Probability on CCDF.  
Power Gain — 28.5 dB  
Power Added Efficiency — 30%  
Device Output Signal PAR — 6.1 dB @ 0.01% Probability on CCDF  
ACPR @ 5 MHz Offset — -38 dBc in 3.84 MHz Channel Bandwidth
- Capable of Handling 5:1 VSWR, @ 32 Vdc, 2140 MHz,  $P_{out} = 110$  Watts CW (3 dB Input Overdrive from Rated  $P_{out}$ )
- Stable into a 5:1 VSWR. All Spurs Below -60 dBc @ 1 mW to 100 Watts CW  $P_{out}$ .
- Typical  $P_{out}$  @ 1 dB Compression Point  $\approx 110$  Watts CW

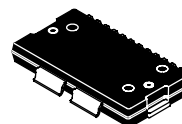
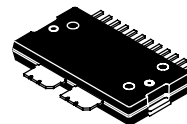
## Features

- 100% PAR Tested for Guaranteed Output Power Capability
- Characterized with Series Equivalent Large-Signal Impedance Parameters and Common Source S-Parameters
- On-Chip Matching (50 Ohm Input, on a per side basis, DC Blocked)
- Internally Matched for Ease of Use
- Integrated Quiescent Current Temperature Compensation with Enable/Disable Function (1)
- Integrated ESD Protection
- 225°C Capable Plastic Package
- In Tape and Reel. R1 Suffix = 500 Units, 44 mm Tape Width, 13 inch Reel.

**MD7IC21100NR1**  
**MD7IC21100GNR1**  
**MD7IC21100NBR1**

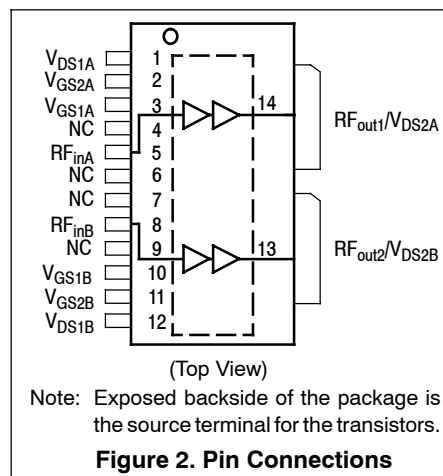
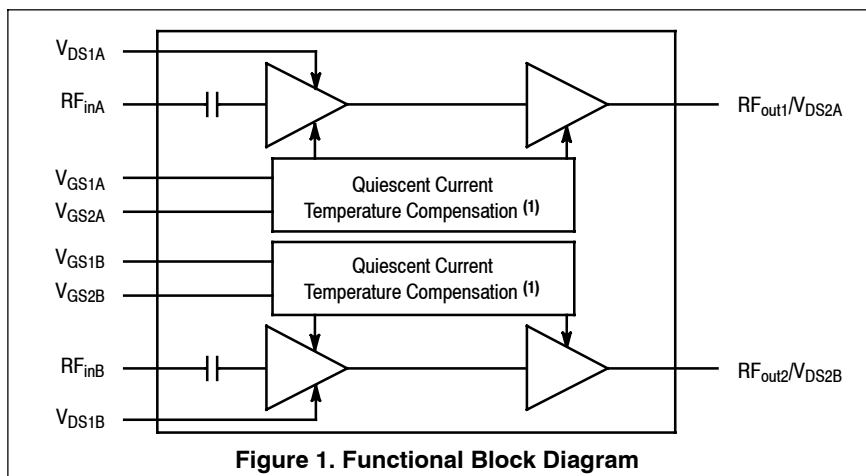
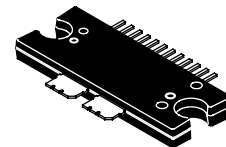
**2110-2170 MHz, 32 W AVG., 28 V**  
**SINGLE W-CDMA**  
**RF LDMOS WIDEBAND**  
**INTEGRATED POWER AMPLIFIERS**

**CASE 1618-02**  
**TO-270 WB-14**  
**PLASTIC**  
**MD7IC21100NR1**



**CASE 1621-02**  
**TO-270 WB-14 GULL**  
**PLASTIC**  
**MD7IC21100GNR1**

**CASE 1617-02**  
**TO-272 WB-14**  
**PLASTIC**  
**MD7IC21100NBR1**



1. Refer to AN1977, *Quiescent Current Thermal Tracking Circuit in the RF Integrated Circuit Family* and to AN1987, *Quiescent Current Control for the RF Integrated Circuit Device Family*. Go to <http://www.freescale.com/rf>. Select Documentation/Application Notes - AN1977 or AN1987.

**Table 1. Maximum Ratings**

Rating	Symbol	Value	Unit
Drain-Source Voltage	$V_{DSS}$	-0.5, +65	Vdc
Gate-Source Voltage	$V_{GS}$	-0.5, +6.0	Vdc
Operating Voltage	$V_{DD}$	32, +0	Vdc
Storage Temperature Range	$T_{stg}$	-65 to +150	°C
Case Operating Temperature	$T_C$	150	°C
Operating Junction Temperature (1,2)	$T_J$	225	°C
Input Power	$P_{in}$	29	dBm

**Table 2. Thermal Characteristics**

Characteristic	Symbol	Value (2,3)	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$		°C/W
(Case Temperature 76°C, 32 W CW) Stage 1, 28 Vdc, $I_{DQ1A} + I_{DQ1B} = 190$ mA		2.7	
(Case Temperature 76°C, 32 W CW) Stage 2, 28 Vdc, $I_{DQ2A} + I_{DQ2B} = 925$ mA		0.7	

**Table 3. ESD Protection Characteristics**

Test Methodology	Class
Human Body Model (per JESD22-A114)	0
Machine Model (per EIA/JESD22-A115)	A
Charge Device Model (per JESD22-C101)	III

**Table 4. Moisture Sensitivity Level**

Test Methodology	Rating	Package Peak Temperature	Unit
Per JESD22-A113, IPC/JEDEC J-STD-020	3	260	°C

**Table 5. Electrical Characteristics** ( $T_A = 25^\circ\text{C}$  unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
----------------	--------	-----	-----	-----	------

**Stage 1 — Off Characteristics (4)**

Zero Gate Voltage Drain Leakage Current ( $V_{DS} = 65$ Vdc, $V_{GS} = 0$ Vdc)	$I_{DSS}$	—	—	10	$\mu\text{Adc}$
Zero Gate Voltage Drain Leakage Current ( $V_{DS} = 28$ Vdc, $V_{GS} = 0$ Vdc)	$I_{DSS}$	—	—	1	$\mu\text{Adc}$
Gate-Source Leakage Current ( $V_{GS} = 1.5$ Vdc, $V_{DS} = 0$ Vdc)	$I_{GSS}$	—	—	1	$\mu\text{Adc}$

**Stage 1 — On Characteristics (4)**

Gate Threshold Voltage ( $V_{DS} = 10$ Vdc, $I_D = 50$ $\mu\text{Adc}$ )	$V_{GS(th)}$	1	2	3	Vdc
Gate Quiescent Voltage ( $V_{DS} = 28$ Vdc, $I_{DQ1A} + I_{DQ1B} = 190$ mAdc)	$V_{GS(Q)}$	—	2.9	—	Vdc
Fixture Gate Quiescent Voltage ( $V_{DD} = 28$ Vdc, $I_{DQ1A} + I_{DQ1B} = 190$ mAdc, Measured in Functional Test)	$V_{GG(Q)}$	5.5	6.3	7	Vdc

1. Continuous use at maximum temperature will affect MTTF.
2. MTTF calculator available at <http://www.freescale.com/rf>. Select Software & Tools/Development Tools/Calculators to access MTTF calculators by product.
3. Refer to AN1955, *Thermal Measurement Methodology of RF Power Amplifiers*. Go to <http://www.freescale.com/rf>. Select Documentation/Application Notes - AN1955.
4. Each side of device measured separately.

(continued)

**Table 5. Electrical Characteristics** ( $T_A = 25^\circ\text{C}$  unless otherwise noted) (continued)

Characteristic	Symbol	Min	Typ	Max	Unit
<b>Stage 2 — Off Characteristics</b> (1)					
Zero Gate Voltage Drain Leakage Current ( $V_{DS} = 65\text{ Vdc}$ , $V_{GS} = 0\text{ Vdc}$ )	$I_{DSS}$	—	—	10	$\mu\text{Adc}$
Zero Gate Voltage Drain Leakage Current ( $V_{DS} = 28\text{ Vdc}$ , $V_{GS} = 0\text{ Vdc}$ )	$I_{DSS}$	—	—	1	$\mu\text{Adc}$
Gate-Source Leakage Current ( $V_{GS} = 1.5\text{ Vdc}$ , $V_{DS} = 0\text{ Vdc}$ )	$I_{GSS}$	—	—	1	$\mu\text{Adc}$

**Stage 2 — On Characteristics** (1)

Gate Threshold Voltage ( $V_{DS} = 10\text{ Vdc}$ , $I_D = 270\ \mu\text{Adc}$ )	$V_{GS(th)}$	1	2	3	Vdc
Gate Quiescent Voltage ( $V_{DS} = 28\text{ Vdc}$ , $I_{DQ2A} + I_{DQ2B} = 925\text{ mAdc}$ )	$V_{GS(Q)}$	—	2.8	—	Vdc
Fixture Gate Quiescent Voltage ( $V_{DD} = 28\text{ Vdc}$ , $I_{DQ2A} + I_{DQ2B} = 925\text{ mAdc}$ , Measured in Functional Test)	$V_{GG(Q)}$	5.3	5.9	6.8	Vdc
Drain-Source On-Voltage ( $V_{GS} = 10\text{ Vdc}$ , $I_D = 1\text{ Adc}$ )	$V_{DS(on)}$	0.1	0.3	0.8	Vdc

**Stage 2 — Dynamic Characteristics** (1,2)

Output Capacitance ( $V_{DS} = 28\text{ Vdc} \pm 30\text{ mV(rms)ac}$ @ 1 MHz, $V_{GS} = 0\text{ Vdc}$ )	$C_{oss}$	—	380	—	pF
---	-----------	---	-----	---	----

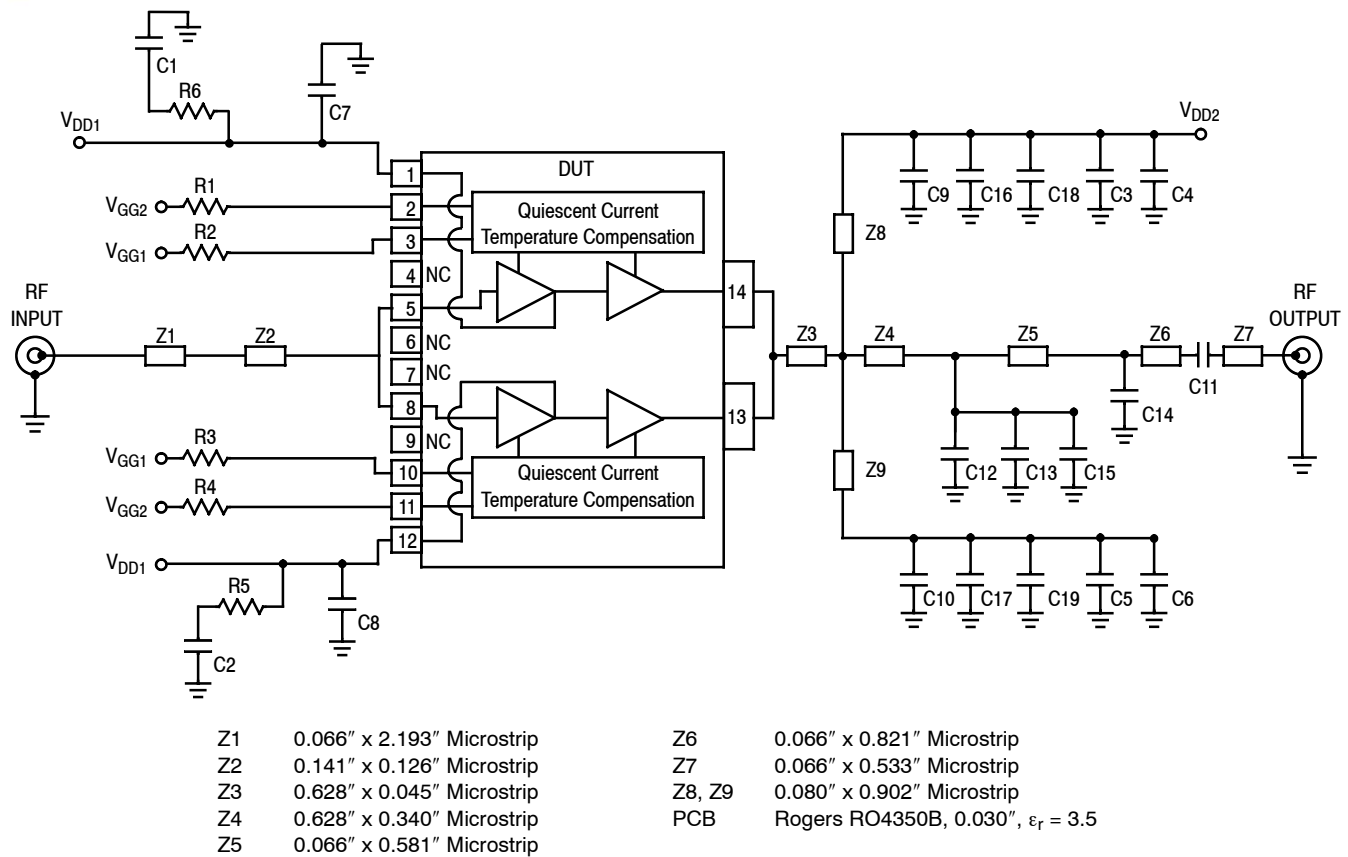
**Functional Tests** (3) (In Freescale Wideband 2110–2170 MHz Test Fixture, 50 ohm system)  $V_{DD} = 28\text{ Vdc}$ ,  $I_{DQ1A} + I_{DQ1B} = 190\text{ mA}$ ,  $I_{DQ2A} + I_{DQ2B} = 925\text{ mA}$ ,  $P_{out} = 32\text{ W Avg.}$ ,  $f = 2167.5\text{ MHz}$ , Single-Carrier W-CDMA, IQ Magnitude Clipping, Input Signal PAR = 7.5 dB @ 0.01% Probability on CCDF. ACPR measured in 3.84 MHz Channel Bandwidth @  $\pm 5\text{ MHz}$  Offset.

Power Gain	$G_{ps}$	27	28.5	32	dB
Power Added Efficiency	PAE	27	30	—	%
Output Peak-to-Average Ratio @ 0.01% Probability on CCDF	PAR	5.6	6.1	—	dB
Adjacent Channel Power Ratio	ACPR	—	-38	-36	dBc
Input Return Loss	IRL	—	-15	-9	dB

**Typical Performances** (3) (In Freescale Test Fixture, 50 ohm system)  $V_{DD} = 28\text{ Vdc}$ ,  $I_{DQ1A} + I_{DQ1B} = 190\text{ mA}$ ,  $I_{DQ2A} + I_{DQ2B} = 925\text{ mA}$ , 2110–2170 MHz Bandwidth

$P_{out}$ @ 1 dB Compression Point, CW	$P1dB$	—	110	—	W
IMD Symmetry @ 112 W PEP, $P_{out}$ where IMD Third Order Intermodulation $\cong 30\text{ dBc}$ (Delta IMD Third Order Intermodulation between Upper and Lower Sidebands > 2 dB)	$IMD_{sym}$	—	50	—	MHz
VBW Resonance Point (IMD Third Order Intermodulation Inflection Point)	$VBW_{res}$	—	50	—	MHz
Gain Flatness in 60 MHz Bandwidth @ $P_{out} = 32\text{ W Avg.}$	$G_F$	—	0.3	—	dB
Quiescent Current Accuracy over Temperature with 4.7 k $\Omega$ Gate Feed Resistors (-30 to 85°C) (4)	$\Delta I_{QT}$	—	$\pm 3$	—	%
Average Deviation from Linear Phase in 60 MHz Bandwidth @ $P_{out} = 110\text{ W CW}$	$\Phi$	—	0.6	—	°
Average Group Delay @ $P_{out} = 110\text{ W CW}$ , $f = 2140\text{ MHz}$	Delay	—	2.6	—	ns
Part-to-Part Insertion Phase Variation @ $P_{out} = 110\text{ W CW}$ , $f = 2140\text{ MHz}$ , Six Sigma Window	$\Delta\Phi$	—	35	—	°
Gain Variation over Temperature (-30°C to +85°C)	$\Delta G$	—	0.042	—	dB/°C
Output Power Variation over Temperature (-30°C to +85°C)	$\Delta P1dB$	—	0.003	—	dB/°C

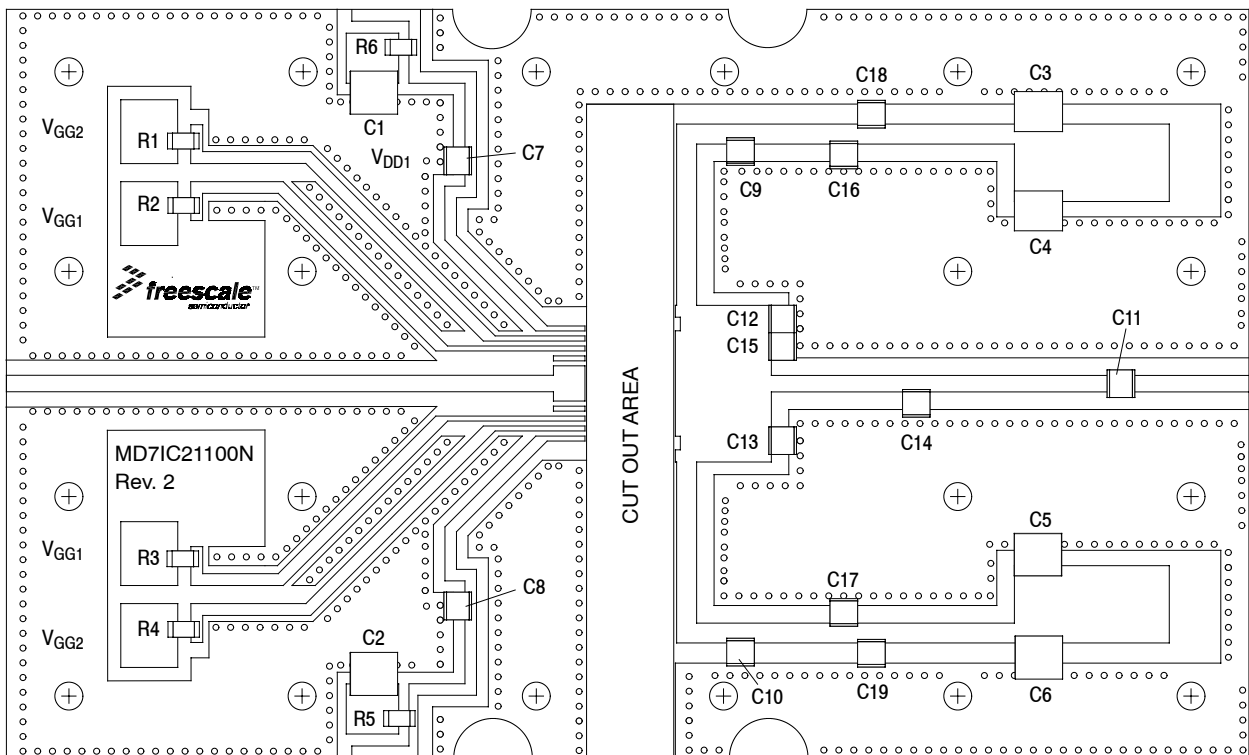
- Each side of device measured separately.
- Part internally matched both on input and output.
- Measurement made with device in a single-ended configuration.
- Refer to AN1977, *Quiescent Current Thermal Tracking Circuit in the RF Integrated Circuit Family* and to AN1987, *Quiescent Current Control for the RF Integrated Circuit Device Family*. Go to <http://www.freescale.com/rf>. Select Documentation/Application Notes - AN1977 or AN1987.



**Figure 3. MD7IC21100NR1(GNR1)(NBR1) Test Circuit Schematic**

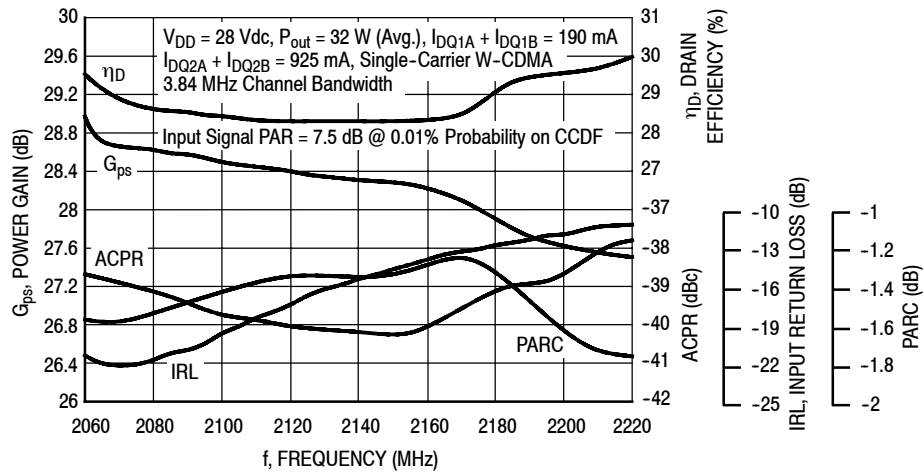
**Table 6. MW7IC2220NR1(GNR1)(NBR1) Test Circuit Component Designations and Values**

Part	Description	Part Number	Manufacturer
C1, C2, C3, C4, C5, C6	10 $\mu$ F, 50 V Chip Capacitors	GRM55DR61H106KA88B	Murata
C7, C8, C9, C10	5.1 pF Chip Capacitors	ATC100B5R1CT500XT	ATC
C11	10 pF Chip Capacitor	ATC100B100JT500XT	ATC
C12, C13, C14	1.2 pF Chip Capacitors	ATC100B1R2CT500XT	ATC
C15	0.5 pF Chip Capacitor	ATC100B0R5CT500XT	ATC
C16, C17	0.1 $\mu$ F, 100 V Chip Capacitors	GRM32NR72A104KA01B	Murata
C18, C19	1 $\mu$ F, 100 V Chip Capacitors	GRM32EER72A105KA01L	Murata
R1, R2, R3, R4	4.7 k $\Omega$ , 1/4 W Chip Resistors	CRCW12064701FKEA	Vishay
R5, R6	2 $\Omega$ , 1/2 W Chip Resistors	CRCW12102R00FKEA	Vishay

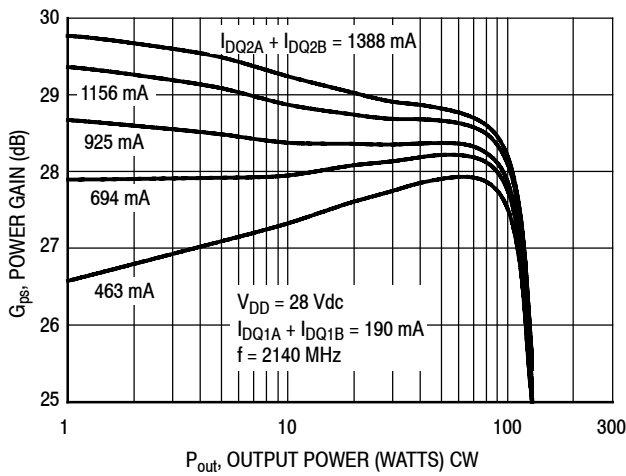


**Figure 4. MD7IC21100NR1(GNR1)(NBR1) Test Circuit Component Layout**

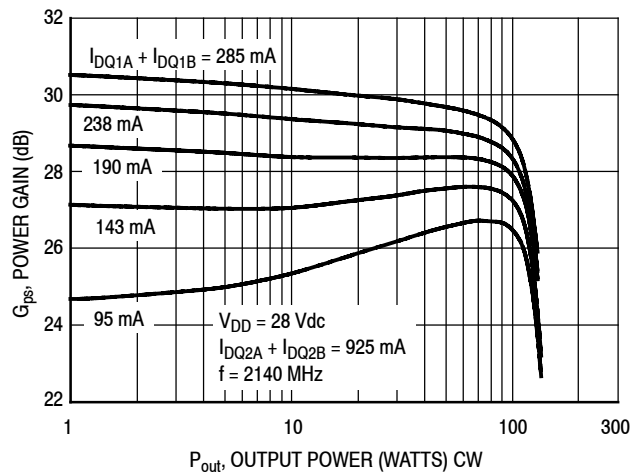
## TYPICAL CHARACTERISTICS



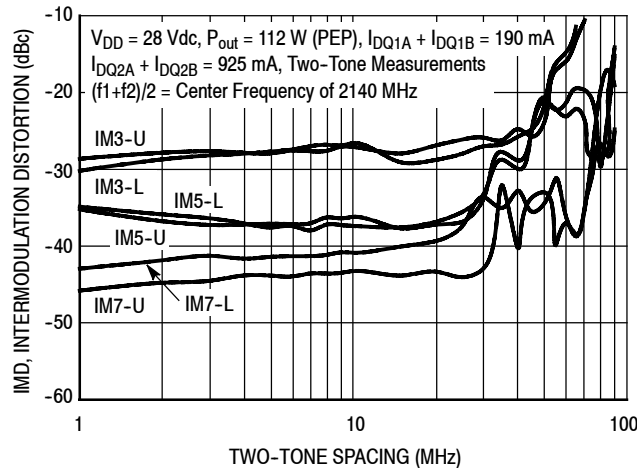
**Figure 5. Output Peak-to-Average Ratio Compression (PARC) versus Broadband Performance @  $P_{out} = 32$  Watts Avg.**



**Figure 6. Power Gain versus Output Power @  $I_{DQ1A} + I_{DQ1B} = 190 \text{ mA}$**

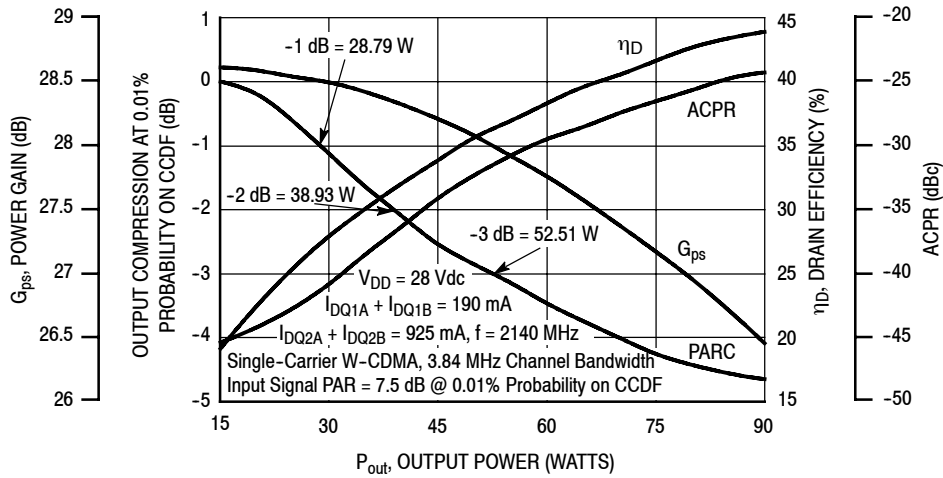


**Figure 7. Power Gain versus Output Power @  $I_{DQ2A} + I_{DQ2B} = 925 \text{ mA}$**

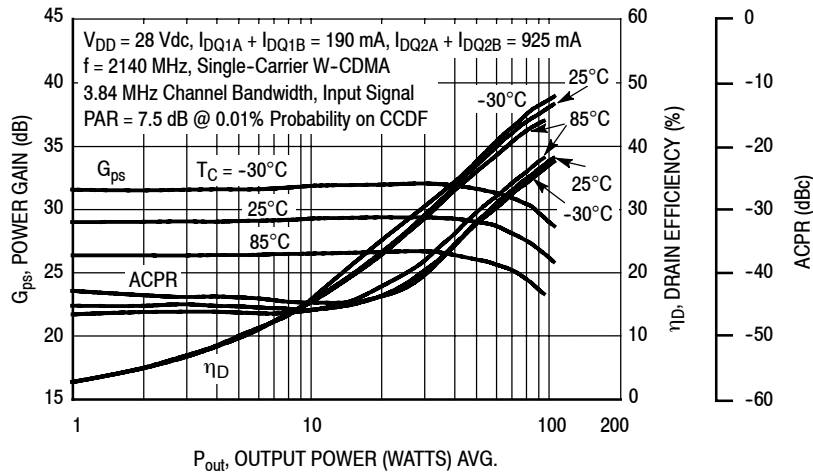


**Figure 8. Intermodulation Distortion Products versus Tone Spacing**

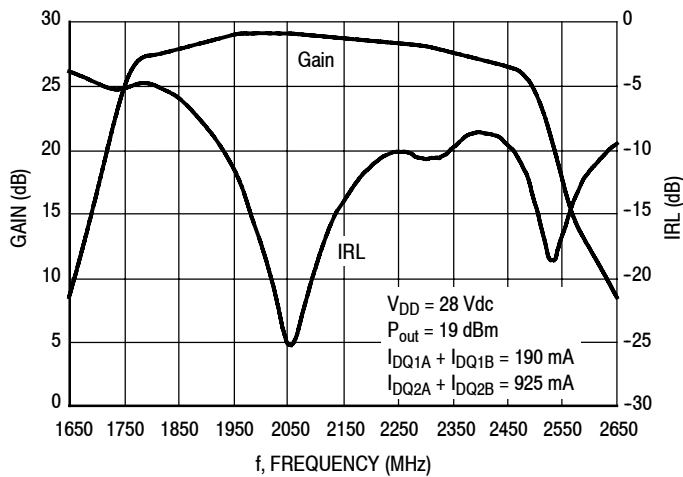
### TYPICAL CHARACTERISTICS



**Figure 9. Output Peak-to-Average Ratio Compression (PARC) versus Output Power**

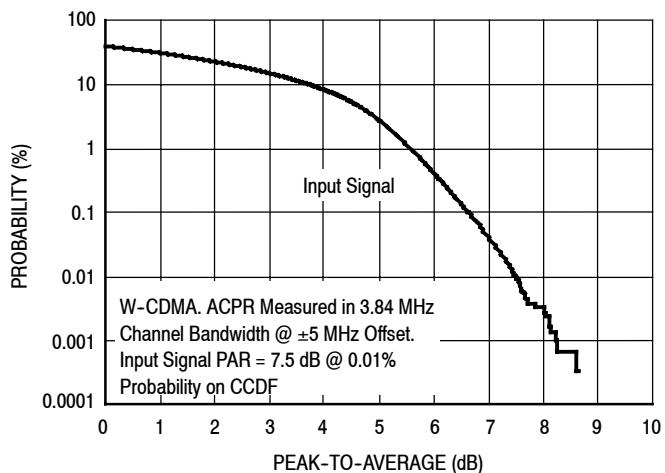


**Figure 10. Single-Carrier W-CDMA Power Gain, Drain Efficiency and ACPR versus Output Power**

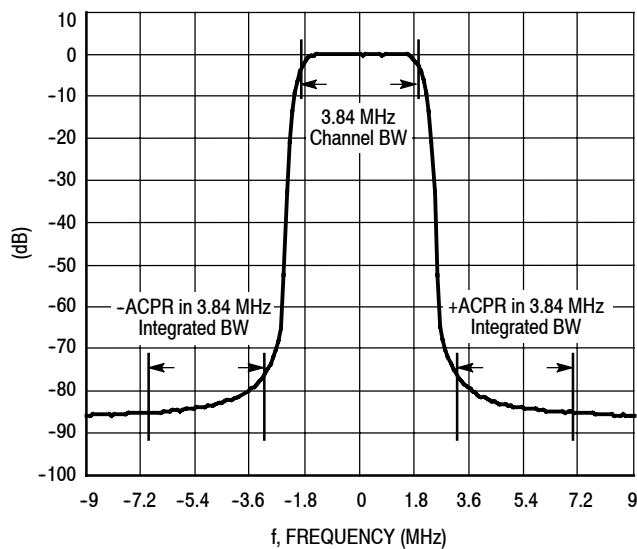


**Figure 11. Broadband Frequency Response**

### W-CDMA TEST SIGNAL

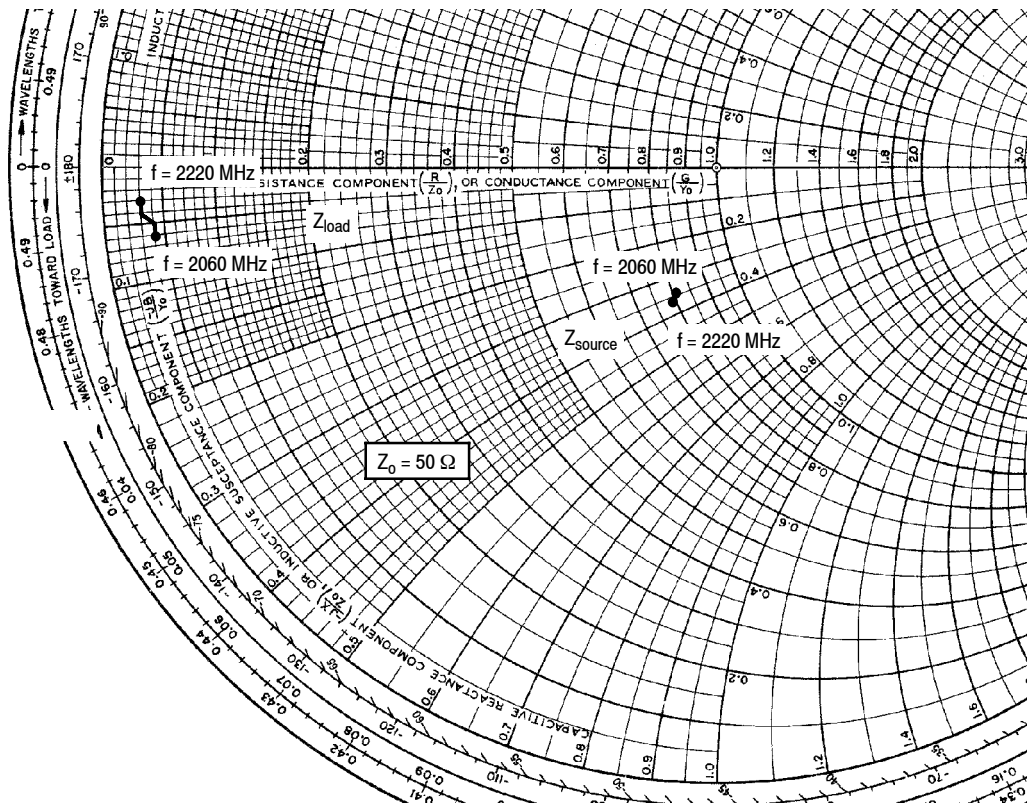


**Figure 12. CCDF W-CDMA IQ Magnitude Clipping, Single-Carrier Test Signal**



**Figure 13. Single-Carrier W-CDMA Spectrum**





$V_{DD} = 28 \text{ Vdc}$ ,  $I_{DQ1A} + I_{DQ1B} = 190 \text{ mA}$ ,  $I_{DQ2A} + I_{DQ2B} = 925 \text{ mA}$ ,  $P_{out} = 32 \text{ W Avg.}$

f MHz	$Z_{source}^{(1)}$ $\Omega$	$Z_{load}$ $\Omega$
2060	40.60 - j16.80	1.99 - j2.90
2080	40.51 - j16.95	1.90 - j2.74
2100	40.42 - j17.10	1.82 - j2.58
2120	40.32 - j17.26	1.75 - j2.41
2140	40.21 - j17.42	1.68 - j2.24
2160	40.10 - j17.58	1.62 - j2.08
2180	39.97 - j17.75	1.55 - j1.92
2200	39.84 - j17.91	1.48 - j1.77
2220	39.70 - j18.08	1.41 - j1.60

(1) Both 50  $\Omega$  inputs in parallel as per the product test fixture.

$Z_{source}$  = Test circuit impedance as measured from gate to ground.

$Z_{load}$  = Test circuit impedance as measured from drain to ground.

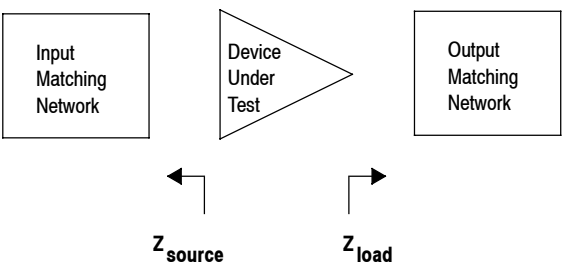
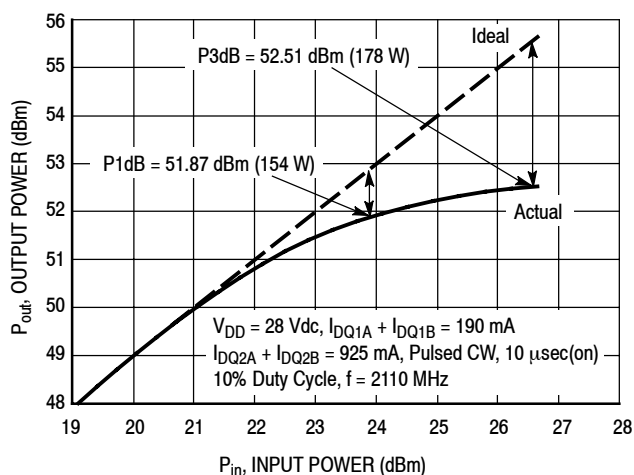


Figure 14. Series Equivalent Source and Load Impedance

## ALTERNATIVE PEAK TUNE LOAD PULL CHARACTERISTICS

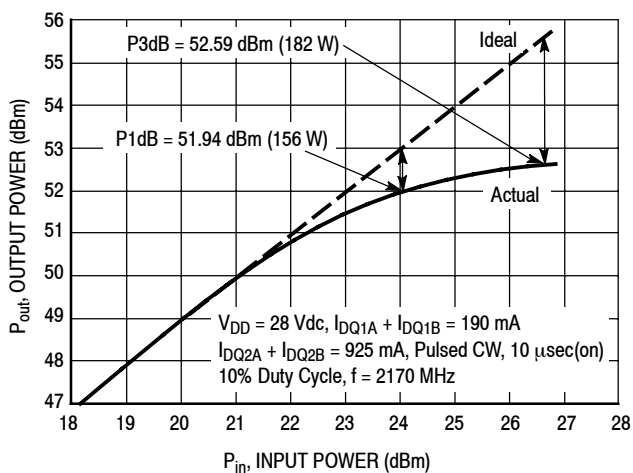


NOTE: Load Pull Test Fixture Tuned for Peak P1dB Output Power @ 28 V

Test Impedances per Compression Level

	$Z_{source}$ $\Omega$	$Z_{load}$ $\Omega$
P1dB	48.64 - j0.94	1.02 - j3.36

**Figure 15. Pulsed CW Output Power versus Input Power @ 28 V @ 2110 MHz**



NOTE: Load Pull Test Fixture Tuned for Peak P1dB Output Power @ 28 V

Test Impedances per Compression Level

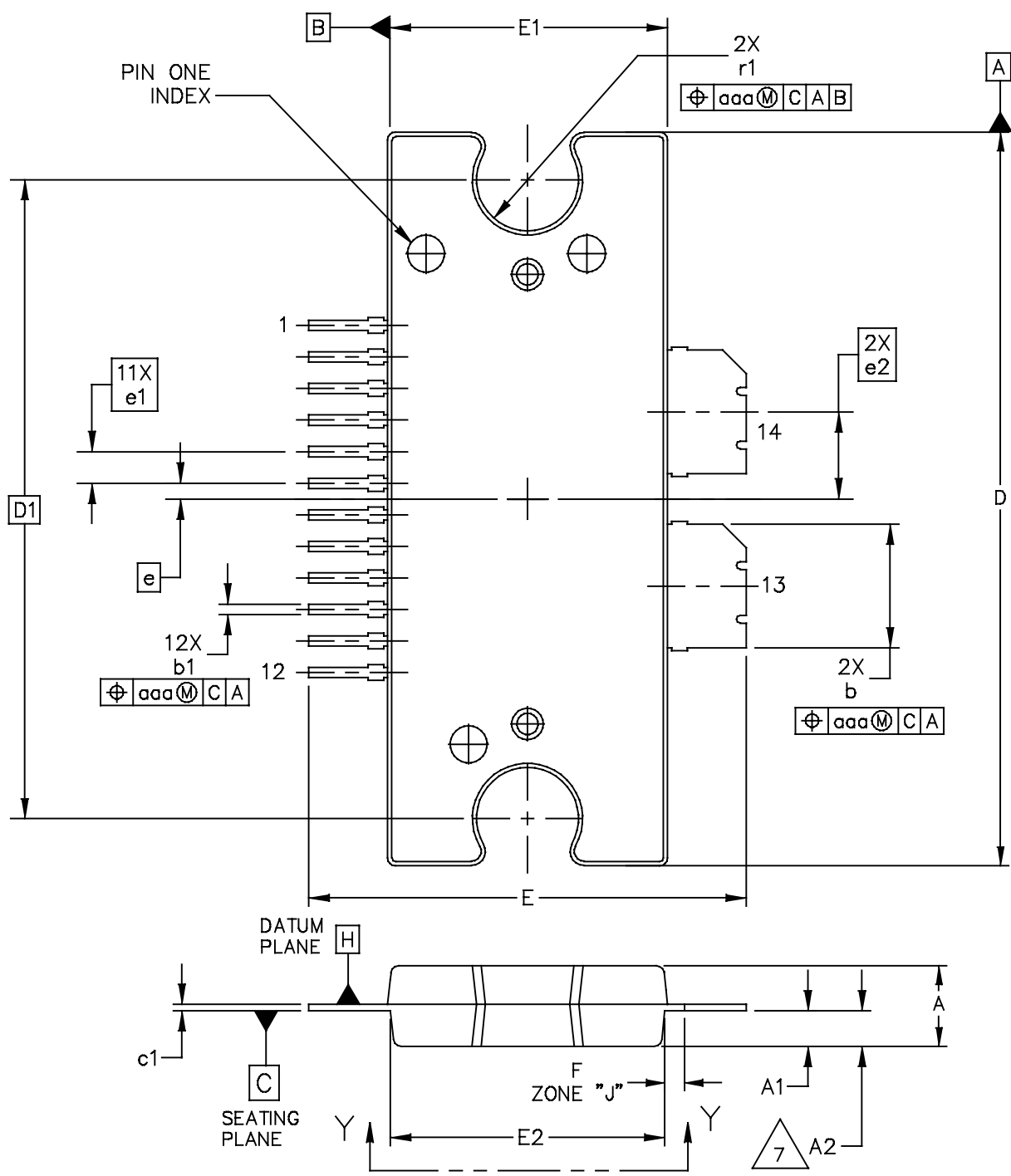
	$Z_{source}$ $\Omega$	$Z_{load}$ $\Omega$
P1dB	51.04 + j0.32	0.92 - j3.48

**Figure 16. Pulsed CW Output Power versus Input Power @ 28 V @ 2170 MHz**

**Table 7. Common Source S-Parameters** ( $V_{DD} = 28\text{ V}$ ,  $I_{DQ1A} + I_{DQ1B} = 190\text{ mA}$ ,  $I_{DQ2A} + I_{DQ2B} = 925\text{ mA}$ ,  $T_A = 25^\circ\text{C}$ , 50 Ohm System)

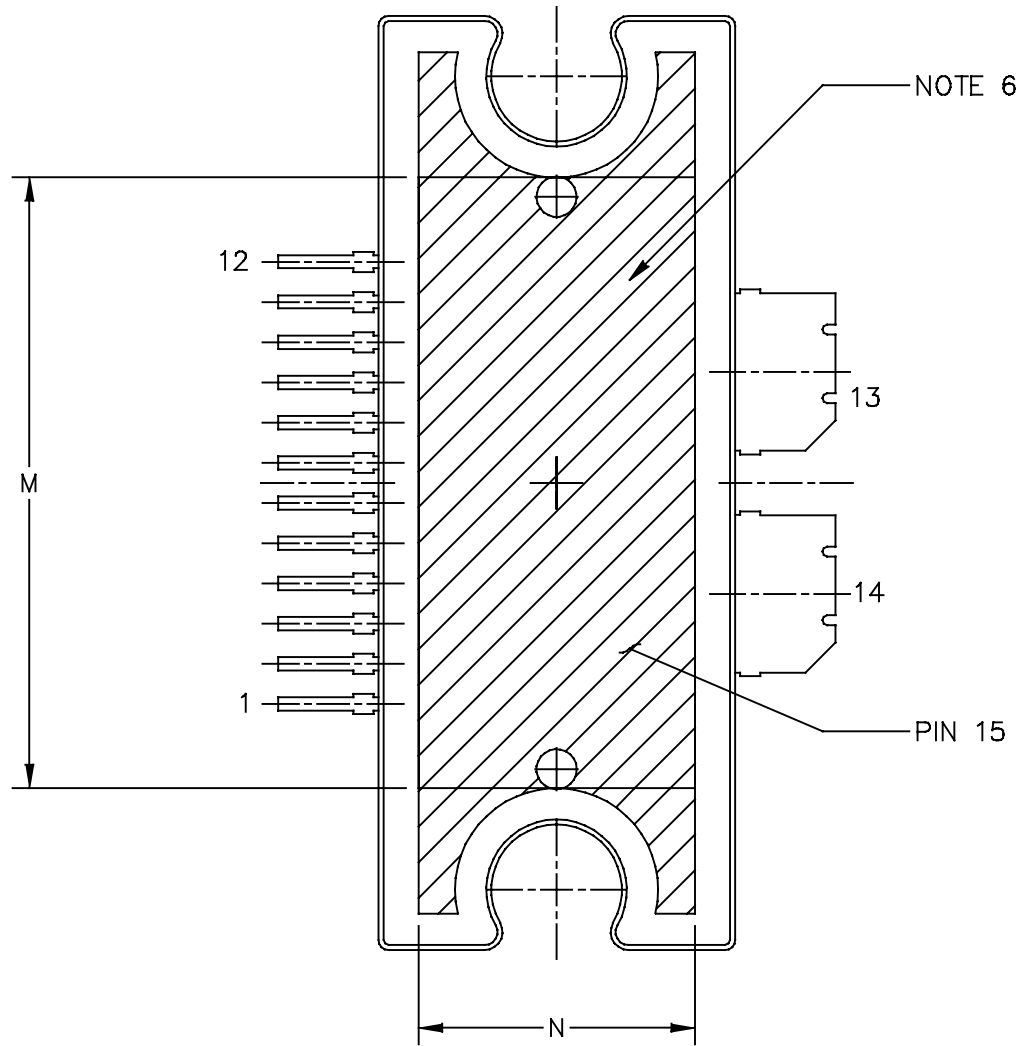
f MHz	S <sub>11</sub>		S <sub>21</sub>		S <sub>12</sub>		S <sub>22</sub>	
	S <sub>11</sub>	∠ φ	S <sub>21</sub>	∠ φ	S <sub>12</sub>	∠ φ	S <sub>22</sub>	∠ φ
1700	0.652	137.6	2.264	127.9	0.000338	110.1	0.986	170.7
1750	0.584	141.8	6.373	105.7	0.00176	-161.5	0.962	166.0
1800	0.967	149.5	22.975	30.1	0.00809	148.5	0.633	163.7
1850	0.830	109.6	14.760	-54.3	0.00544	88.8	0.872	-179.3
1900	0.609	93.0	12.528	-81.7	0.00445	92.7	0.891	175.2
1950	0.376	73.2	12.727	-115.4	0.00571	97.8	0.848	172.6
2000	0.159	50.5	11.639	-142.6	0.00781	75.0	0.785	177.3
2050	0.093	-129.9	11.706	-174.5	0.00711	50.8	0.863	-178.8
2100	0.200	-148.4	10.735	159.4	0.00593	37.7	0.921	179.9
2150	0.304	-156.5	9.872	135.1	0.00461	28.3	0.950	177.7
2200	0.386	-169.3	8.929	113.7	0.00366	28.3	0.958	176.2
2250	0.432	178.3	8.421	94.5	0.00304	33.7	0.960	175.5
2300	0.459	163.6	8.238	75.8	0.00281	41.0	0.962	175.2
2350	0.406	145.8	9.041	52.8	0.00253	46.3	0.963	175.5
2400	0.334	134.7	8.312	21.8	0.00255	54.7	0.971	175.7
2450	0.238	120.3	7.167	-5.1	0.00262	60.5	0.977	175.8
2500	0.133	110.4	5.879	-28.8	0.00270	65.2	0.981	175.8
2550	0.020	149.0	4.788	-50.7	0.00304	66.7	0.982	175.8
2600	0.102	-116.2	3.837	-70.6	0.00319	68.5	0.982	175.7
2650	0.204	-121.9	3.053	-89.3	0.00356	67.3	0.982	175.5
2700	0.280	-129.7	2.415	-105.9	0.00369	66.9	0.981	175.2
2750	0.342	-135.1	1.931	-121.3	0.00397	66.4	0.981	174.7
2800	0.392	-138.0	1.551	-135.6	0.00446	67.5	0.979	174.0
2850	0.455	-140.7	1.231	-148.0	0.00466	57.7	0.980	173.3
2900	0.503	-145.9	1.016	-160.1	0.00445	52.3	0.980	172.6
2950	0.531	-147.9	0.831	-172.2	0.00434	53.4	0.980	171.8
3000	0.566	-148.9	0.677	176.6	0.00437	54.8	0.981	171.1
3050	0.601	-149.7	0.550	166.3	0.00453	56.6	0.982	170.4
3100	0.634	-150.5	0.449	156.9	0.00486	57.6	0.982	170.0

**PACKAGE DIMENSIONS**



© FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED.	MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE	
TITLE: TO-272 WIDE BODY 14 LEAD	DOCUMENT NO: 98ASA10649D	REV: A	
	CASE NUMBER: 1617-02	27 JUN 2007	
	STANDARD: NON-JEDEC		

MD7IC21100NR1 MD7IC21100GNR1 MD7IC21100NBR1



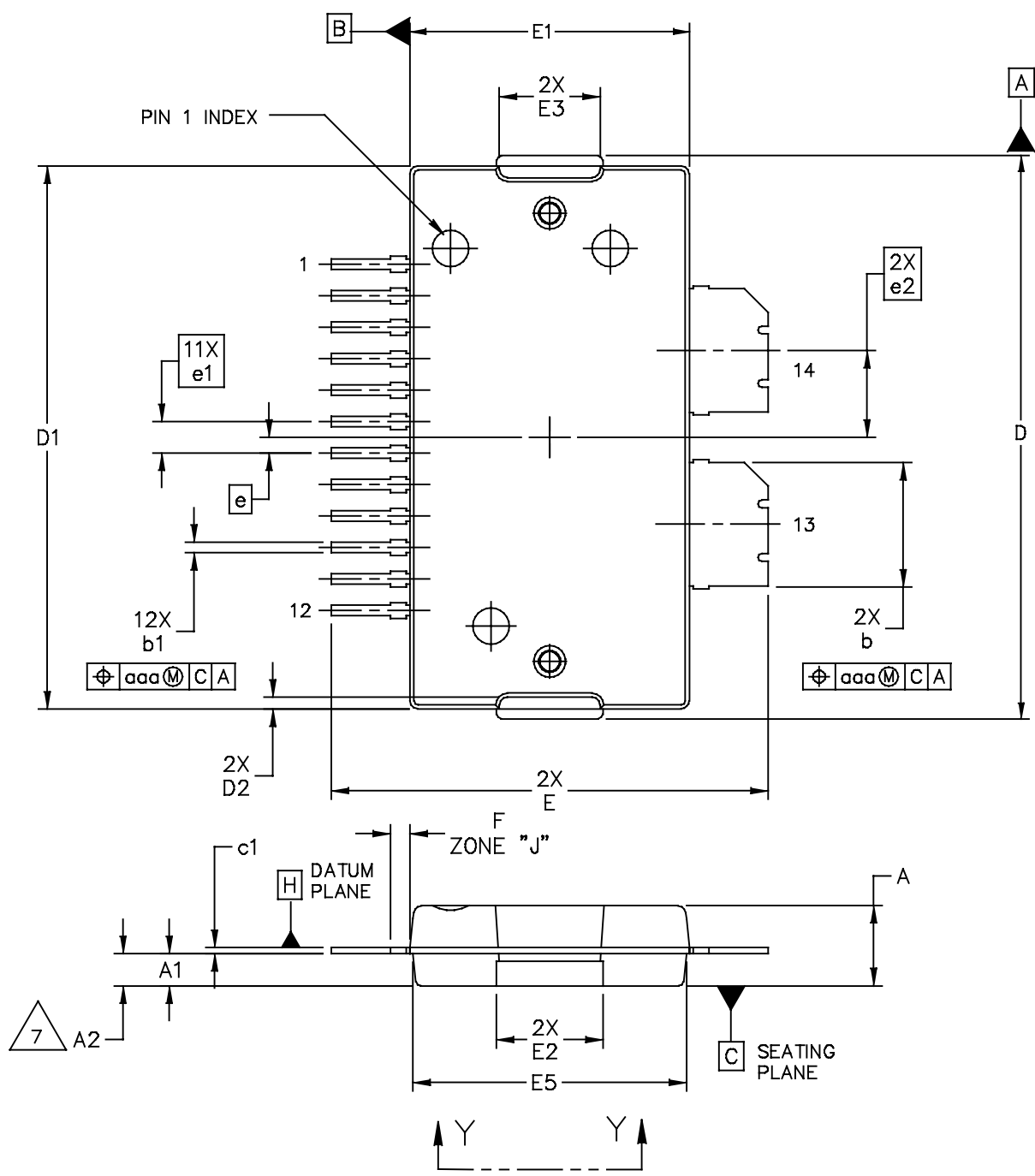
VIEW Y-Y

© FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED.	MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE	
TITLE: TO-272 WIDE BODY 14 LEAD	DOCUMENT NO: 98ASA10649D	REV: A	
	CASE NUMBER: 1617-02	27 JUN 2007	
	STANDARD: NON-JEDEC		

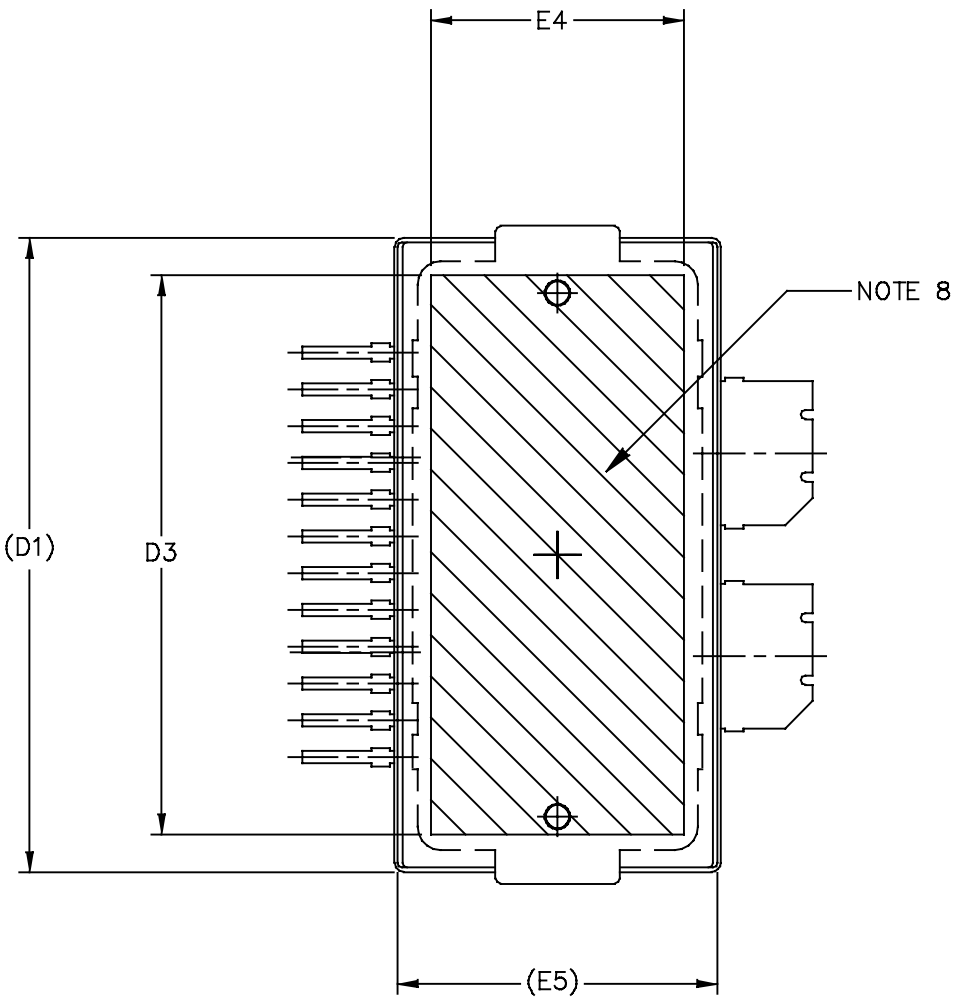
NOTES:

1. CONTROLLING DIMENSION: INCH
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M-1994.
3. DATUM PLANE -H- IS LOCATED AT THE TOP OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE TOP OF THE PARTING LINE.
4. DIMENSIONS "D" AND "E1" DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS .006 (0.15) PER SIDE. DIMENSIONS "D" AND "E1" DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE -H-.
5. DIMENSIONS "b" AND "b1" DO NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE .005 (0.13) TOTAL IN EXCESS OF THE "b" AND "b1" DIMENSIONS AT MAXIMUM MATERIAL CONDITION.
6. HATCHING REPRESENTS THE EXPOSED AREA OF THE HEAT SLUG.
7. DIM A2 APPLIES WITHIN ZONE "J" ONLY.

DIM	INCH		MILLIMETER		DIM	INCH		MILLIMETER	
	MIN	MAX	MIN	MAX		MIN	MAX	MIN	MAX
A	.100	.104	2.54	2.64	b	.154	.160	3.91	4.06
A1	.039	.043	0.99	1.09	b1	.010	.016	0.25	0.41
A2	.040	.042	1.02	1.07	c1	.007	.011	0.18	0.28
D	.928	.932	23.57	23.67	e	.020 BSC		0.51 BSC	
D1	.810 BSC		20.57 BSC		e1	.040 BSC		1.02 BSC	
E	.551	.559	14.00	14.20	e2	.1105 BSC		2.807 BSC	
E1	.353	.357	8.97	9.07	r1	.063	.068	1.6	1.73
E2	.346	.350	8.79	8.89					
F	.025 BSC		0.64 BSC		aaa	.004		0.10	
M	.600	----	15.24	----					
N	.270	----	6.86	----					
© FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED.			MECHANICAL OUTLINE			PRINT VERSION NOT TO SCALE			
TITLE:  TO-272 WIDE BODY 14 LEAD					DOCUMENT NO: 98ASA10649D			REV: A	
					CASE NUMBER: 1617-02			27 JUN 2007	
					STANDARD: NON-JEDEC				



© FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED.	MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE	
TITLE: TO-270 WIDE BODY 14 LEAD	DOCUMENT NO: 98ASA10650D	REV: A	
	CASE NUMBER: 1618-02	19 JUN 2007	
	STANDARD: NON-JEDEC		



VIEW Y-Y

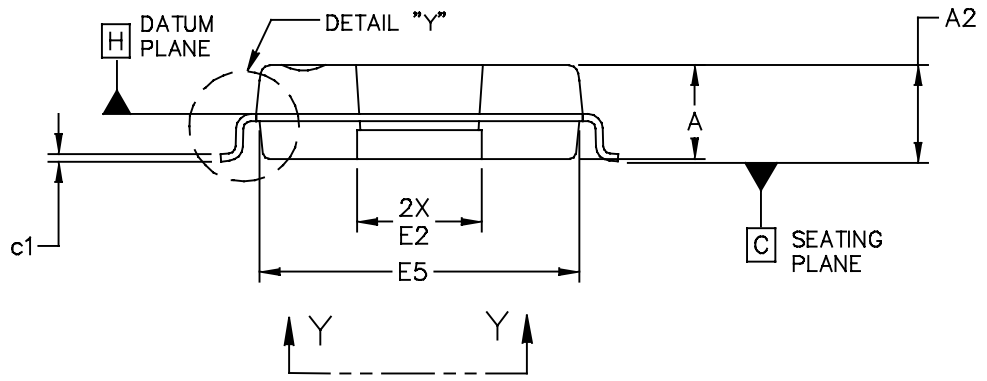
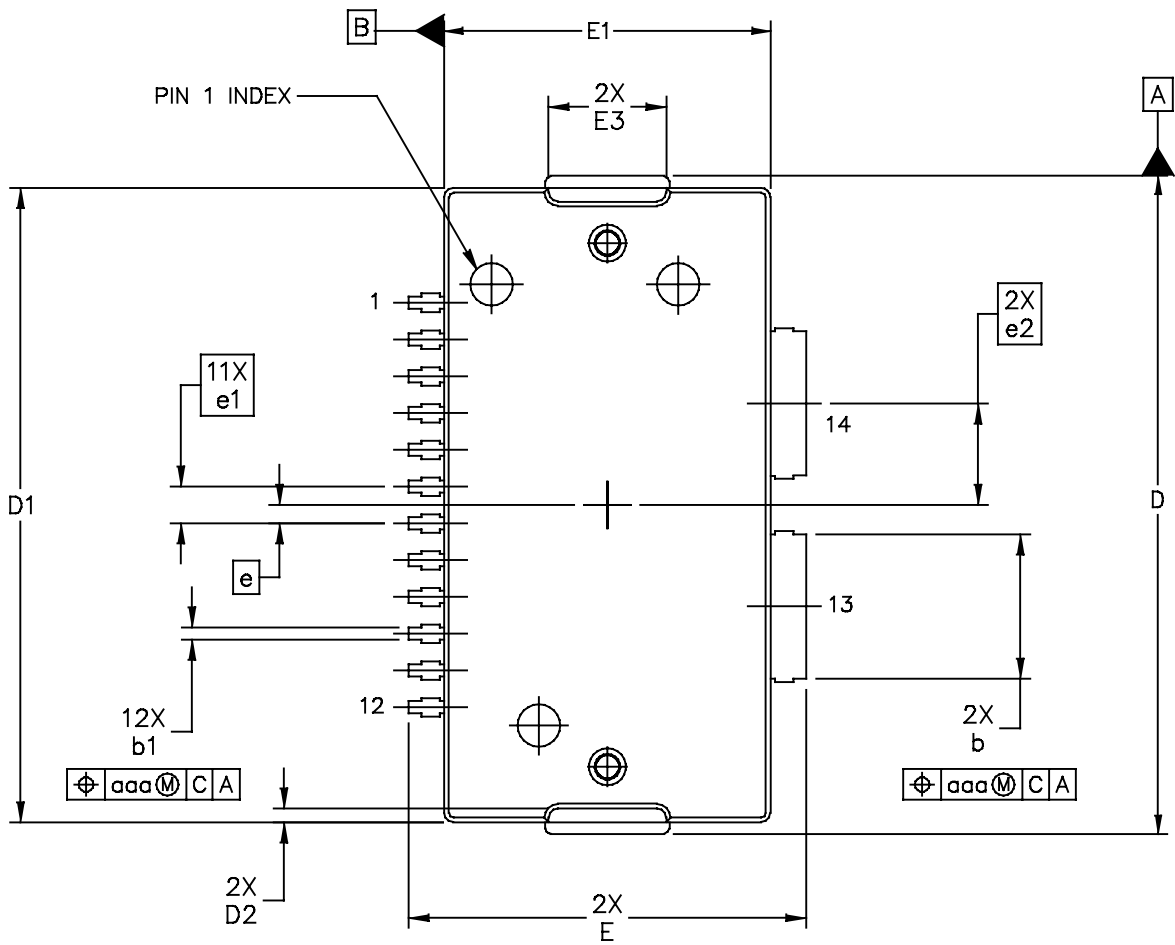
© FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED.	MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE	
TITLE: TO-270 WIDE BODY 14 LEAD		DOCUMENT NO: 98ASA10650D	REV: A
		CASE NUMBER: 1618-02	19 JUN 2007
		STANDARD: NON-JEDEC	



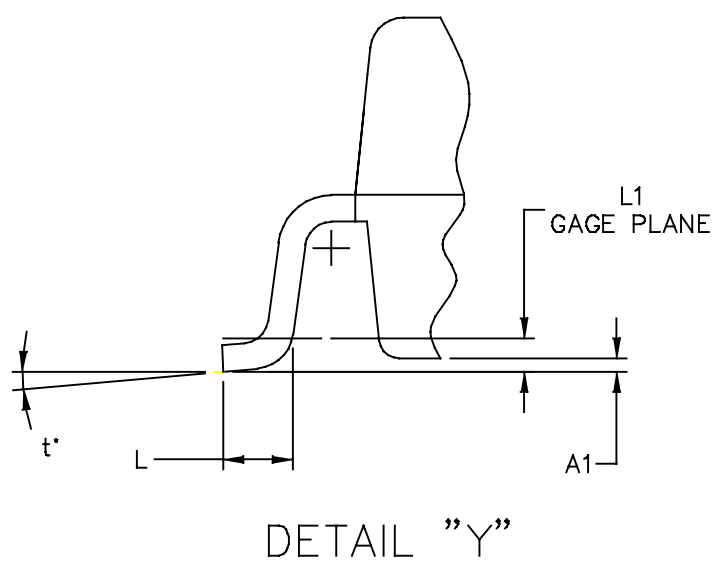
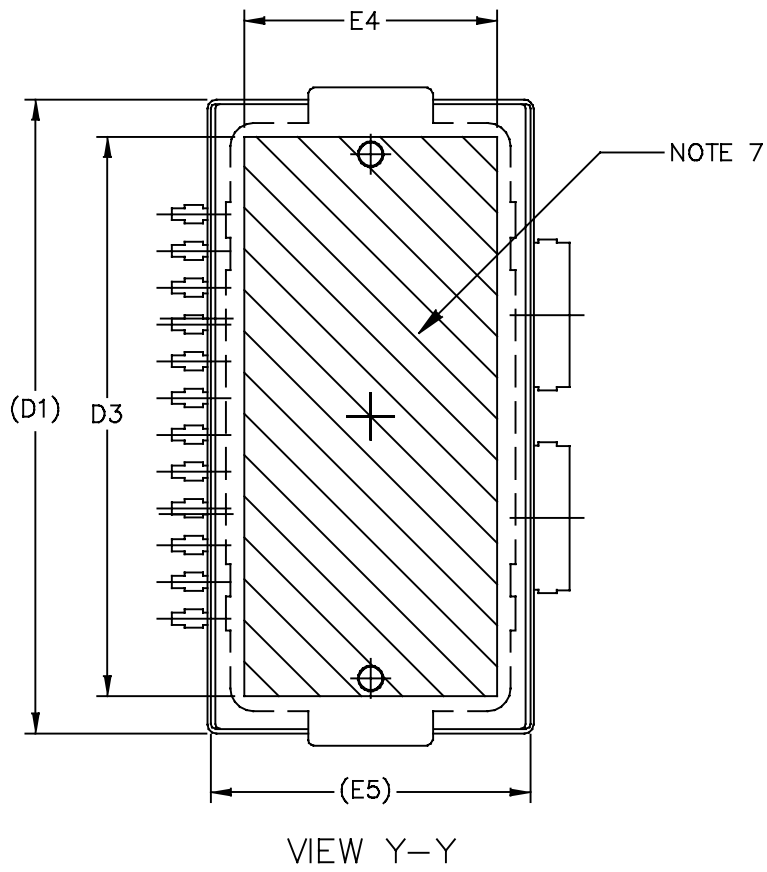
NOTES:

1. CONTROLLING DIMENSION: INCH
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M-1994.
3. DATUM PLANE -H- IS LOCATED AT THE TOP OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE TOP OF THE PARTING LINE.
4. DIMENSIONS "D" AND "E1" DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS .006 PER SIDE. DIMENSIONS "D" AND "E1" DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE -H-.
5. DIMENSIONS "b" AND "b1" DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE .005 TOTAL IN EXCESS OF THE "b" AND "b1" DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. DATUMS -A- AND -B- TO BE DETERMINED AT DATUM PLANE -H-.
7. DIMENSION A2 APPLIES WITHIN ZONE "J" ONLY.
8. HATCHING REPRESENTS THE EXPOSED AREA OF THE HEAT SLUG.

DIM	INCH		MILLIMETER		DIM	INCH		MILLIMETER	
	MIN	MAX	MIN	MAX		MIN	MAX	MIN	MAX
A	.100	.104	2.54	2.64	F	.025 BSC		0.64 BSC	
A1	.039	.043	0.99	1.09	b	.154	.160	3.91	4.06
A2	.040	.042	1.02	1.07	b1	.010	.016	0.25	0.41
D	.712	.720	18.08	18.29	c1	.007	.011	.18	.28
D1	.688	.692	17.48	17.58	e	.020 BSC		0.51 BSC	
D2	.011	.019	0.28	0.48	e1	.040 BSC		1.02 BSC	
D3	.600	---	15.24	---	e2	.1105 BSC		2.807 BSC	
E	.551	.559	14	14.2					
E1	.353	.357	8.97	9.07	aaa	.004		.10	
E2	.132	.140	3.35	3.56					
E3	.124	.132	3.15	3.35					
E4	.270	---	6.86	---					
E5	.346	.350	8.79	8.89					
© FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED.			MECHANICAL OUTLINE			PRINT VERSION NOT TO SCALE			
TITLE: TO-270 WIDE BODY 14 LEAD					DOCUMENT NO: 98ASA10650D			REV: A	
					CASE NUMBER: 1618-02			19 JUN 2007	
					STANDARD: NON-JEDEC				



© FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED.	MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE	
TITLE: TO-270 WIDE BODY 14 LEAD GULL WING		DOCUMENT NO: 98ASA10653D	REV: A
		CASE NUMBER: 1621-02	19 JUN 2007
		STANDARD: NON-JEDEC	



© FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED.	MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE	
TITLE: TO-270 WIDE BODY 14 LEAD GULL WING	DOCUMENT NO: 98ASA10653D	REV: A	
	CASE NUMBER: 1621-02	19 JUN 2007	
	STANDARD: NON-JEDEC		

NOTES:

1. CONTROLLING DIMENSION: INCH
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M-1994.
3. DATUM PLANE -H- IS LOCATED AT THE TOP OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE TOP OF THE PARTING LINE.
4. DIMENSIONS "D" AND "E1" DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS .006 PER SIDE. DIMENSIONS "D" AND "E1" DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE -H-.
5. DIMENSIONS "b" AND "b1" DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE .005 TOTAL IN EXCESS OF THE "b" AND "b1" DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. DATUMS -A- AND -B- TO BE DETERMINED AT DATUM PLANE -H-.
7. HATCHING REPRESENTS THE EXPOSED AREA OF THE HEAT SLUG.

DIM	INCH		MILLIMETER		DIM	INCH		MILLIMETER	
	MIN	MAX	MIN	MAX		MIN	MAX	MIN	MAX
A	.100	.104	2.54	2.64	L	.018	.024	0.46	0.61
A1	.001	.004	0.02	0.10	L1	.010 BSC		0.25 BSC	
A2	.099	.110	2.51	2.79	b	.154	.160	3.91	4.06
D	.712	.720	18.08	18.29	b1	.010	.016	0.25	0.41
D1	.688	.692	17.48	17.58	c1	.007	.011	.18	.28
D2	.011	.019	0.28	0.48	e	.020 BSC		0.51 BSC	
D3	.600	---	15.24	---	e1	.040 BSC		1.02 BSC	
E	.429	.437	10.9	11.1	e2	.1105 BSC		2.807 BSC	
E1	.353	.357	8.97	9.07	t	2'	8'	2'	8'
E2	.132	.140	3.35	3.56					
E3	.124	.132	3.15	3.35	aaa	.004		.10	
E4	.270	---	6.86	---					
E5	.346	.350	8.79	8.89					
© FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED.			MECHANICAL OUTLINE			PRINT VERSION NOT TO SCALE			
TITLE: TO-270 WIDE BODY 14 LEAD GULL WING					DOCUMENT NO: 98ASA10653D			REV: A	
					CASE NUMBER: 1621-02			19 JUN 2007	
					STANDARD: NON-JEDEC				

## PRODUCT DOCUMENTATION AND SOFTWARE

Refer to the following documents and software to aid your design process.

### Application Notes

- AN1907: Solder Reflow Attach Method for High Power RF Devices in Over-Molded Plastic Packages
- AN1955: Thermal Measurement Methodology of RF Power Amplifiers
- AN1977: Quiescent Current Thermal Tracking Circuit in the RF Integrated Circuit Family
- AN1987: Quiescent Current Control for the RF Integrated Circuit Device Family
- AN3263: Bolt Down Mounting Method for High Power RF Transistors and RFICs in Over-Molded Plastic Packages
- AN3789: Clamping of High Power RF Transistors and RFICs in Over-Molded Plastic Packages

### Engineering Bulletins

- EB212: Using Data Sheet Impedances for RF LDMOS Devices

### Software

- Electromigration MTTF Calculator
- RF High Power Model

For Software, do a Part Number search at <http://www.freescale.com>, and select the “Part Number” link. Go to the Software & Tools tab on the part’s Product Summary page to download the respective tool.

## REVISION HISTORY

The following table summarizes revisions to this document.

Revision	Date	Description
0	Oct. 2008	<ul style="list-style-type: none"> <li>• Initial Release of Data Sheet</li> </ul>
1	June 2011	<ul style="list-style-type: none"> <li>• Changed ESD Human Body Model rating from Class 1C to Class 0 to reflect recent ESD test results of the device, p. 2</li> <li>• Fig. 13, MTTF versus Junction Temperature removed, p. 8. Refer to the device’s MTTF Calculator available at <a href="http://freescale.com/RFpower">freescale.com/RFpower</a>. Go to Design Resources &gt; Software and Tools.</li> <li>• Fig. 14, CCDF W-CDMA IQ Magnitude Clipping, Single-Carrier Test Signal and Fig. 15, Single-Carrier W-CDMA Spectrum updated to show the undistorted input test signal, p. 8 (renumbered as Fig. 13 and Fig. 14 after Fig. 13 removed)</li> <li>• Added AN3789, Clamping of High Power RF Transistors and RFICs in Over-Molded Plastic Packages to Product Documentation, Application Notes, p. 21</li> <li>• Added Electromigration MTTF Calculator and RF High Power Model availability to Product Software, p. 21</li> </ul>
2	Feb. 2012	<ul style="list-style-type: none"> <li>• Table 3, ESD Protection Characteristics, removed the word “Minimum” after the ESD class rating. ESD ratings are characterized during new product development but are not 100% tested during production. ESD ratings provided in the data sheet are intended to be used as a guideline when handling ESD sensitive devices, p. 2</li> <li>• Corrected bias conditions throughout the data sheet to reflect the true testing methodology. Changed <math>I_{DQ1A} = I_{DQ1B} = 190 \text{ mA}</math> to <math>I_{DQ1A} + I_{DQ1B} = 190 \text{ mA}</math> and changed <math>I_{DQ2A} = I_{DQ2B} = 925 \text{ mA}</math> to <math>I_{DQ2A} + I_{DQ2B} = 925 \text{ mA}</math>.</li> <li>• Removed Fig. 5, Possible Circuit Topologies, and renumbered all subsequent figures, p. 5-10</li> </ul>

## **How to Reach Us:**

### **Home Page:**

[www.freescale.com](http://www.freescale.com)

### **Web Support:**

<http://www.freescale.com/support>

### **USA/Europe or Locations Not Listed:**

Freescale Semiconductor, Inc.  
Technical Information Center, EL516  
2100 East Elliot Road  
Tempe, Arizona 85284  
1-800-521-6274 or +1-480-768-2130  
[www.freescale.com/support](http://www.freescale.com/support)

### **Europe, Middle East, and Africa:**

Freescale Halbleiter Deutschland GmbH  
Technical Information Center  
Schatzbogen 7  
81829 Muenchen, Germany  
+44 1296 380 456 (English)  
+46 8 52200080 (English)  
+49 89 92103 559 (German)  
+33 1 69 35 48 48 (French)  
[www.freescale.com/support](http://www.freescale.com/support)

### **Japan:**

Freescale Semiconductor Japan Ltd.  
Headquarters  
ARCO Tower 15F  
1-8-1, Shimo-Meguro, Meguro-ku,  
Tokyo 153-0064  
Japan  
0120 191014 or +81 3 5437 9125  
[support.japan@freescale.com](mailto:support.japan@freescale.com)

### **Asia/Pacific:**

Freescale Semiconductor China Ltd.  
Exchange Building 23F  
No. 118 Jianguo Road  
Chaoyang District  
Beijing 100022  
China  
+86 10 5879 8000  
[support.asia@freescale.com](mailto:support.asia@freescale.com)

### **For Literature Requests Only:**

Freescale Semiconductor Literature Distribution Center  
1-800-441-2447 or +1-303-675-2140  
Fax: +1-303-675-2150  
[LDCForFreescaleSemiconductor@hibbertgroup.com](mailto:LDCForFreescaleSemiconductor@hibbertgroup.com)

Information in this document is provided solely to enable system and software implementers to use Freescale Semiconductor products. There are no express or implied copyright licenses granted hereunder to design or fabricate any integrated circuits or integrated circuits based on the information in this document.

Freescale Semiconductor reserves the right to make changes without further notice to any products herein. Freescale Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does Freescale Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation consequential or incidental damages. "Typical" parameters that may be provided in Freescale Semiconductor data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals", must be validated for each customer application by customer's technical experts. Freescale Semiconductor does not convey any license under its patent rights nor the rights of others. Freescale Semiconductor products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the Freescale Semiconductor product could create a situation where personal injury or death may occur. Should Buyer purchase or use Freescale Semiconductor products for any such unintended or unauthorized application, Buyer shall indemnify and hold Freescale Semiconductor and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that Freescale Semiconductor was negligent regarding the design or manufacture of the part.

Freescale™ and the Freescale logo are trademarks of Freescale Semiconductor, Inc. All other product or service names are the property of their respective owners.

© Freescale Semiconductor, Inc. 2008, 2011-2012. All rights reserved.