

ON Semiconductor®

FDS6975

Dual P-Channel, Logic Level, PowerTrench™ MOSFET

General Description

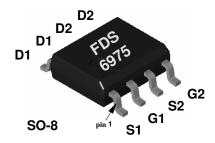
These P-Channel Logic Level MOSFETs are produced using ON Semiconductor's advanced PowerTrench process that has been especially tailored to minimize the on-state resistance and yet maintain low gate charge for superior switching performance.

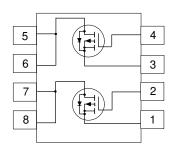
These devices are well suited for notebook computer applications: load switching and power management, battery charging circuits, and DC/DC conversion.

Features

- Low gate charge (14.5nC typical).
- High performance trench technology for extremely low R_{DS/ONI}.
- High power and current handling capability.







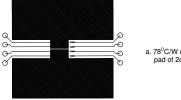
Absolute Maximum Ratings T_A = 25°C unless otherwise noted

Symbol	Parameter	Ratings	Units
V _{DSS}	Drain-Source Voltage	-30	V
V_{GSS}	Gate-Source Voltage	±20	V
I _D	Drain Current - Continuous (Note 1a)	-6	А
	- Pulsed	-20	
P _D	Power Dissipation for Dual Operation	2	W
	Power Dissipation for Single Operation (Note 1a)	1.6	
	(Note 1b)	1	
	(Note 1c)	0.9	
T_J, T_{STG}	Operating and Storage Temperature Range	-55 to 150	°C
THERMA	L CHARACTERISTICS		•
$R_{\theta^{JA}}$	Thermal Resistance, Junction-to-Ambient (Note 1a)	78	°C/W
R _{euc}	Thermal Resistance, Junction-to-Case (Note 1)	40	°C/W

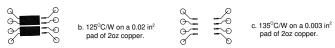
Symbol	Parameter	Conditions	Min	Тур	Max	Units
OFF CHAI	RACTERISTICS					
BV _{DSS}	Drain-Source Breakdown Voltage	$V_{GS} = 0 \text{ V}, \ I_D = -250 \ \mu\text{A}$	-30			V
$\Delta BV_{DSS}/\Delta T$	Breakdown Voltage Temp. Coefficient	$I_D = -250 \mu\text{A}$, Referenced to 25 °C		-21		mV/°C
DSS	Zero Gate Voltage Drain Current	$V_{DS} = -24 \text{ V}, \ V_{GS} = 0 \text{ V}$			-1	μΑ
		$T_{\text{J}} = 55^{\circ}\text{C}$			-10	μΑ
I _{GSSF}	Gate - Body Leakage, Forward	$V_{GS} = 20 \text{ V}, V_{DS} = 0 \text{ V}$			100	nA
I _{GSSR}	Gate - Body Leakage, Reverse	$V_{GS} = -20 \text{ V}, V_{DS} = 0 \text{ V}$			-100	nA
ON CHARA	ACTERISTICS (Note 2)		II.			
V _{GS(th)}	Gate Threshold Voltage	$V_{DS} = V_{GS}, \ I_{D} = -250 \ \mu A$	-1	-1.7	-3	V
$\Delta V_{GS(th)}/\Delta T_{J}$	Gate Threshold Voltage Temp. Coefficient	$I_D = 250 \mu\text{A}$, Referenced to 25°C		4		mV/°C
R _{DS(ON)}	Static Drain-Source On-Resistance	$V_{GS} = -10 \text{ V}, I_D = -6 \text{ A}$		0.025	0.032	Ω
		T _J =125°C		0.033	0.051	
		$V_{GS} = -4.5 \text{ V}, I_{D} = -5 \text{ A}$		0.034	0.045	
I _{D(ON)}	On-State Drain Current	$V_{GS} = -10 \text{ V}, \ V_{DS} = -5 \text{ V}$	-20			Α
g _{FS}	Forward Transconductance	$V_{DS} = -10 \text{ V}, I_{D} = -6 \text{ A}$		16		S
DYNAMIC	CHARACTERISTICS		•			
C _{iss}	Input Capacitance	$V_{DS} = -15 \text{ V}, \ V_{GS} = 0 \text{ V},$ f = 1.0 MHz		1540		рF
C _{oss}	Output Capacitance			400		рF
C _{rss}	Reverse Transfer Capacitance			170		pF
SWITCHIN	G CHARACTERISTICS (Note 2)					•
t _{D(on)}	Turn - On Delay Time	$V_{DS} = -15 \text{ V}, \ I_{D} = -1 \text{ A}$		13	24	ns
ţ	Turn - On Rise Time	$V_{GEN} = -10 \text{ V}, R_{GEN} = 6 \Omega$		22	35	ns
t _{D(off)}	Turn - Off Delay Time			47	75	ns
ţ,	Turn - Off Fall Time			18	30	ns
Q_g	Total Gate Charge	$V_{DS} = -10 \text{ V}, \ I_{D} = -6 \text{ A},$		14.5	20	nC
Q_{gs}	Gate-Source Charge	V _{GS} = -5 V		4		nC
Q_{qd}	Gate-Drain Charge			5		nC
DRAIN-SO	URCE DIODE CHARACTERISTICS AND MAXIM	IUM RATINGS	•	•	•	
I _s	Maximum Continuous Drain-Source Diode Forward Current				-1.3	Α
V_{SD}	Drain-Source Diode Forward Voltage	$V_{GS} = 0 \text{ V}, I_{S} = -1.3 \text{ A} \text{ (Note 2)}$		-0.73	-1.2	V

Notes:

^{1.} R_{BJA} is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. R_{BJC} is guaranteed by design while R_{BJC} is determined by the user's board design.



a. 78°C/W on a 0.5 in² pad of 2oz copper.

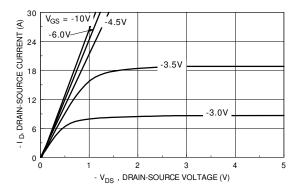




Scale 1: 1 on letter size paper

2. Pulse Test: Pulse Width \leq 300 μ s, Duty Cycle \leq 2.0%.

Typical Electrical Characteristics



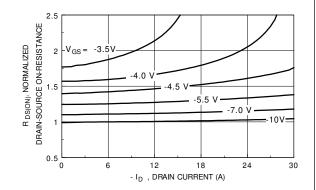
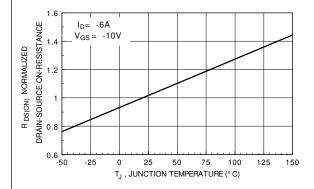


Figure 1. On-Region Characteristics.

Figure 2. On-Resistance Variation with Dain Current and Gate Voltage.



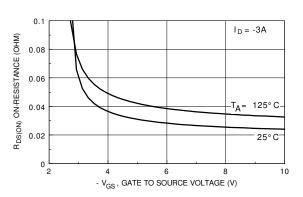
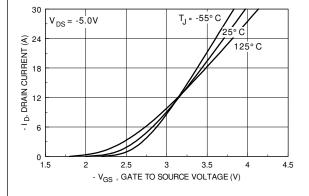


Figure 3. On-Resistance Variation with Temperature.

Figure 4. On-Resistance Variation with Gate-to-Source Voltage.



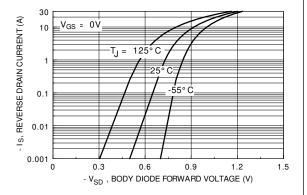
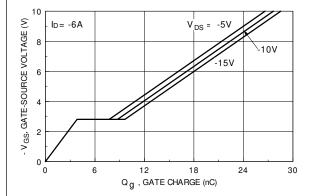


Figure 5. Transfer Characteristics.

Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.

Typical Electrical Characteristics (continued)



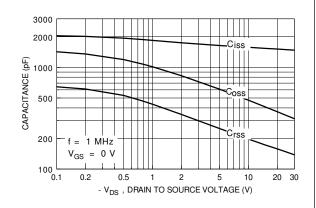
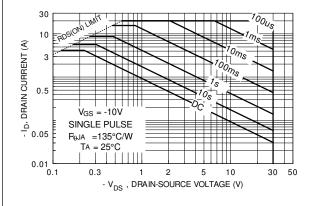


Figure 7. Gate Charge Characteristics.





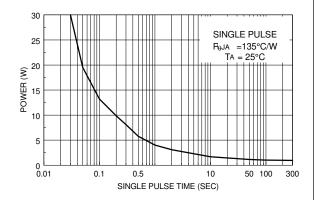


Figure 9. Maximum Safe Operating Area.

Figure 10. Single Pulse Maximum Power Dissipation.

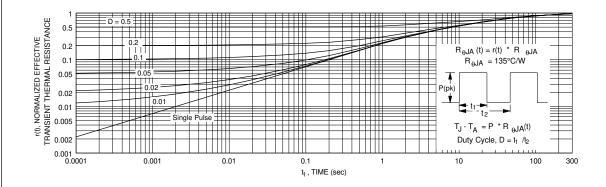


Figure 11. Transient Thermal Response Curve.

Thermal characterization performed using the conditions described in Note 1c. Transient thermal response will change depending on the circuit board design.

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