

74AC573, 74ACT573

Octal Latch with 3-STATE Outputs

The 74AC573 and 74ACT573 are high-speed octal latches with buffered common Latch Enable (LE) and buffered common Output Enable (\overline{OE}) inputs.

The 74AC573 and 74ACT573 are functionally identical to the 74AC373 and 74ACT373 but with inputs and outputs on opposite sides.

Rochester Electronics Manufactured Components

Rochester branded components are manufactured using either die/wafers purchased from the original suppliers or Rochester wafers recreated from the original IP. All re-creations are done with the approval of the Original Component Manufacturer (OCM).

Parts are tested using original factory test programs or Rochester developed test solutions to guarantee product meets or exceeds the OCM data sheet.

Quality Overview

- ISO-9001
- AS9120 certification
- Qualified Manufacturers List (QML) MIL-PRF-35835
 - Class Q Military
 - Class V Space Level
- Qualified Suppliers List of Distributors (QSLD)
 - Rochester is a critical supplier to DLA and meets all industry and DLA standards.

Rochester Electronics, LLC is committed to supplying products that satisfy customer expectations for quality and are equal to those originally supplied by industry manufacturers.

The original manufacturer's datasheet accompanying this document reflects the performance and specifications of the Rochester manufactured version of this device. Rochester Electronics guarantees the performance of its semiconductor products to the original OCM specifications. 'Typical' values are for reference purposes only. Certain minimum or maximum ratings may be based on product characterization, design, simulation, or sample testing.

FOR REFERENCE ONLY



74AC573, 74ACT573

Octal Latch with 3-STATE Outputs

Features

- I_{CC} and I_{OZ} reduced by 50%
- Inputs and outputs on opposite sides of package allowing easy interface with microprocessors
- Useful as input or output port for microprocessors
- Functionally identical to 74AC373 and 74ACT373
- 3-STATE outputs for bus interfacing
- Outputs source/sink 24mA
- 74ACT573 has TTL-compatible inputs

General Description

The 74AC573 and 74ACT573 are high-speed octal latches with buffered common Latch Enable (LE) and buffered common Output Enable (\overline{OE}) inputs.

The 74AC573 and 74ACT573 are functionally identical to the 74AC373 and 74ACT373 but with inputs and outputs on opposite sides.

Ordering Information

| Order Number | Package Number | Package Description |
|-------------------------------|----------------|---|
| 74AC573SC | M20B | 20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide |
| 74AC573SJ | M20D | 20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide |
| 74AC573MTC | MTC20 | 20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide |
| 74ACT573SC | M20B | 20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide |
| 74ACT573SCX_NL ⁽¹⁾ | M20B | 20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide |
| 74ACT573SJ | M20D | 20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide |
| 74ACT573MTC | MTC20 | 20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide |
| 74ACT573PC | N20A | 20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide |

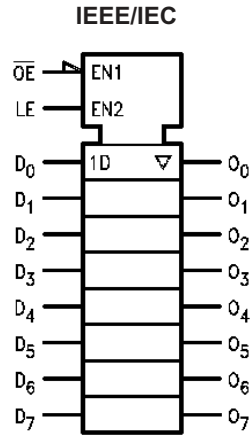
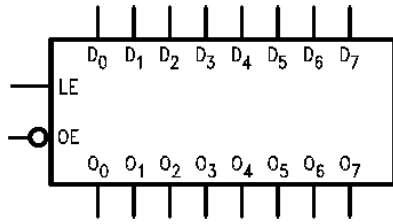
Device also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering number.
Pb-Free package per JEDEC J-STD-020B.

Note:

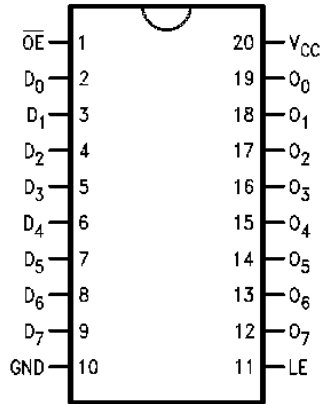
1. Device available in Tape and Reel only.

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Logic Symbols



Connection Diagram



Pin Descriptions

| Pin Names | Description |
|--------------------------------|-----------------------------|
| D ₀ -D ₇ | Data Inputs |
| LE | Latch Enable Input |
| \overline{OE} | 3-STATE Output Enable Input |
| O ₀ -O ₇ | 3-STATE Latch Outputs |

Truth Table

| Inputs | | | Outputs |
|-----------------|----|---|----------------|
| \overline{OE} | LE | D | O _n |
| L | H | H | H |
| L | H | L | L |
| L | L | X | O ₀ |
| H | X | X | Z |

H = HIGH Voltage

L = LOW Voltage

Z = High Impedance

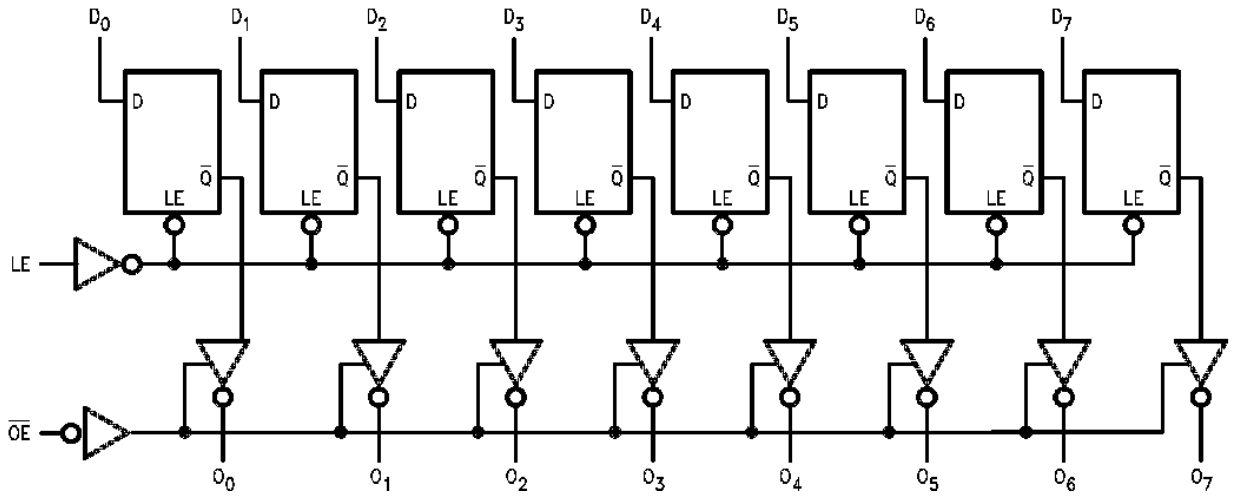
X = Immaterial

O₀ = Previous O₀ before HIGH-to-LOW transition of Latch Enable

Functional Description

The 74AC573 and 74ACT573 contain eight D-type latches with 3-STATE output buffers. When the Latch Enable (LE) input is HIGH, data on the D_n inputs enters the latches. In this condition the latches are transparent, i.e., a latch output will change state each time its D-type input changes. When LE is LOW the latches store the information that was present on the D-type inputs a setup time preceding the HIGH-to-LOW transition of LE. The 3-STATE buffers are controlled by the Output Enable (\overline{OE}) input. When \overline{OE} is LOW, the buffers are enabled. When \overline{OE} is HIGH the buffers are in the high impedance mode but this does not interfere with entering new data into the latches.

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

| Symbol | Parameter | Rating |
|-----------------------|---|--------------------------|
| V_{CC} | Supply Voltage | -0.5V to +7.0V |
| I_{IK} | DC Input Diode Current $V_I = -0.5V$ $V_I = V_{CC} + 0.5V$ | -20mA +20mA |
| V_I | DC Input Voltage | -0.5V to $V_{CC} + 0.5V$ |
| I_{OK} | DC Output Diode Current $V_O = -0.5V$ $V_O = V_{CC} + 0.5V$ | -20mA +20mA |
| V_O | DC Output Voltage | -0.5V to $V_{CC} + 0.5V$ |
| I_O | DC Output Source or Sink Current | $\pm 50mA$ |
| I_{CC} or I_{GND} | DC V_{CC} or Ground Current per Output Pin | $\pm 50mA$ |
| T_{STG} | Storage Temperature | -65°C to +150°C |
| T_J | Junction Temperature | 140°C |

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to absolute maximum ratings.

| Symbol | Parameter | Rating |
|-----------------------|--|------------------------------|
| V_{CC} | Supply Voltage AC ACT | 2.0V to 6.0V 4.5V to 5.5V |
| V_I | Input Voltage | 0V to V_{CC} |
| V_O | Output Voltage | 0V to V_{CC} |
| T_A | Operating Temperature | -40°C to +85°C |
| $\Delta V / \Delta t$ | Minimum Input Edge Rate, AC Devices: V_{IN} from 30% to 70% of V_{CC} , V_{CC} @ 3.0V, 4.5V, 5.5V | 125mV/ns |
| $\Delta V / \Delta t$ | Minimum Input Edge Rate, ACT Devices: V_{IN} from 0.8V to 2.0V, V_{CC} @ 4.5V, 5.5V | 125mV/ns |

DC Electrical Characteristics for AC

| Symbol | Parameter | V _{CC} (V) | Conditions | T _A = +25°C | | T _A = -40°C to +85°C | | Units | |
|--------------------------------|---|---------------------|--|---|-------------------|---------------------------------|------|-------|---|
| | | | | Typ. | Guaranteed Limits | | | | |
| V _{IH} | Minimum HIGH Level Input Voltage | 3.0 | V _{OUT} = 0.1V or V _{CC} - 0.1V | 1.5 | 2.1 | 2.1 | | V | |
| | | 4.5 | | 2.25 | 3.15 | 3.15 | | | |
| | | 5.5 | | 2.75 | 3.85 | 3.85 | | | |
| V _{IL} | Maximum LOW Level Input Voltage | 3.0 | V _{OUT} = 0.1V or V _{CC} - 0.1V | 1.5 | 0.9 | 0.9 | | V | |
| | | 4.5 | | 2.25 | 1.35 | 1.35 | | | |
| | | 5.5 | | 2.75 | 1.65 | 1.65 | | | |
| V _{OH} | Minimum HIGH Level Output Voltage | 3.0 | I _{OUT} = -50μA | 2.99 | 2.9 | 2.9 | | V | |
| | | 4.5 | | 4.49 | 4.4 | 4.4 | | | |
| | | 5.5 | | 5.49 | 5.4 | 5.4 | | | |
| | | | 3.0 | V _{IN} = V _{IL} or V _{IH} ; I _{OH} = -12mA | | | 2.56 | 2.46 | V |
| | | | 4.5 | I _{OH} = -24mA | | | 3.86 | 3.76 | |
| | | | 5.5 | I _{OH} = -24mA ⁽²⁾ | | | 4.86 | 4.76 | |
| V _{OL} | Maximum LOW Level Output Voltage | 3.0 | I _{OUT} = 50μA | 0.002 | 0.1 | 0.1 | | V | |
| | | 4.5 | | 0.001 | 0.1 | 0.1 | | | |
| | | 5.5 | | 0.001 | 0.1 | 0.1 | | | |
| | | | 3.0 | V _{IN} = V _{IL} or V _{IH} ; I _{OL} = 12mA | | | 0.36 | 0.44 | |
| | | | 4.5 | I _{OL} = 24mA | | | 0.36 | 0.44 | |
| | | | 5.5 | I _{OL} = 24mA ⁽²⁾ | | | 0.36 | 0.44 | |
| I _{IN} ⁽³⁾ | Maximum Input Leakage Current | 5.5 | V _I = V _{CC} , GND | | ±0.1 | ±1.0 | | μA | |
| I _{OLD} | Minimum Dynamic Output Current ⁽⁴⁾ | 5.5 | V _{OLD} = 1.65V Max. | | | 75 | | mA | |
| I _{OHD} | | 5.5 | V _{OHD} = 3.85V Min. | | | -75 | | mA | |
| I _{CC} ⁽³⁾ | Maximum Quiescent Supply Current | 5.5 | V _{IN} = V _{CC} or GND | | 4.0 | 40.0 | | μA | |
| I _{OZ} | Maximum 3-STATE Leakage Current | 5.5 | V _I (OE) = V _{IL} , V _{IH} ; V _I = V _{CC} , GND; V _O = V _{CC} , GND | | ±0.25 | ±2.5 | | μA | |

Notes:

- All outputs loaded; thresholds on input associated with output under test.
- I_{IN} and I_{CC} @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V_{CC}.
- Maximum test duration 2.0ms, one output loaded at a time.

DC Electrical Characteristics for ACT

| Symbol | Parameter | V _{CC} (V) | Conditions | T _A = +25°C | | T _A = -40°C to +85°C | | Units | |
|------------------|---|---------------------|--|------------------------|-------------------|---------------------------------|------|-------|--|
| | | | | Typ. | Guaranteed Limits | | | | |
| V _{IH} | Minimum HIGH Level Input Voltage | 4.5 | V _{OUT} = 0.1V or V _{CC} - 0.1V | 1.5 | 2.0 | 2.0 | | V | |
| | | 5.5 | | 1.5 | 2.0 | 2.0 | | | |
| V _{IL} | Maximum LOW Level Input Voltage | 4.5 | V _{OUT} = 0.1V or V _{CC} - 0.1V | 1.5 | 0.8 | 0.8 | | V | |
| | | 5.5 | | 5.5 | 1.5 | 0.8 | | | |
| V _{OH} | Minimum HIGH Level Output Voltage | 4.5 | I _{OUT} = -50 μA | 4.49 | 4.4 | 4.4 | | V | |
| | | 5.5 | | 5.49 | 5.4 | 5.4 | | | |
| | | 4.5 | V _{IN} = V _{IL} or V _{IH} ; I _{OH} = -24mA | | | 3.86 | 3.76 | | |
| | | 5.5 | I _{OH} = -24mA ⁽⁵⁾ | | | 4.86 | 4.76 | | |
| V _{OL} | Maximum LOW Level Output Voltage | 4.5 | I _{OUT} = 50 μA | 0.001 | 0.1 | 0.1 | | V | |
| | | 5.5 | | 0.001 | 0.1 | 0.1 | | | |
| | | 4.5 | V _{IN} = V _{IL} or V _{IH} ; I _{OL} = 24mA | | | 0.36 | 0.44 | | |
| | | 5.5 | I _{OL} = 24mA ⁽⁵⁾ | | | 0.36 | 0.44 | | |
| I _{IN} | Maximum Input Leakage Current | 5.5 | V _I = V _{CC} , GND | | ±0.1 | ±1.0 | | μA | |
| I _{OZ} | Maximum 3-STATE Leakage Current | 5.5 | V _I = V _{IL} , V _{IH} ; V _O = V _{CC} , GND | | ±0.25 | ±2.5 | | μA | |
| I _{CCT} | Maximum I _{CC} /Input | 5.5 | V _I = V _{CC} - 2.1V | 0.6 | | 1.5 | | mA | |
| I _{OLD} | Minimum Dynamic Output Current ⁽⁶⁾ | 5.5 | V _{OLD} = 1.65V Max. | | | 75 | | mA | |
| I _{OHD} | | 5.5 | V _{OHD} = 3.85V Min. | | | -75 | | mA | |
| I _{CC} | Maximum Quiescent Supply Current | 5.5 | V _{IN} = V _{CC} or GND | | 4.0 | 40.0 | | μA | |

Notes:

5. All outputs loaded; thresholds on input associated with output under test.
6. Maximum test duration 2.0ms, one output loaded at a time.

AC Electrical Characteristics for AC

| Symbol | Parameter | V _{CC} (V) ⁽⁷⁾ | T _A = +25°C, C _L = 50pF | | | T _A = -40°C to +85°C, C _L = 50pF | | Units |
|------------------|--|------------------------------------|--|------|------|---|------|-------|
| | | | Min. | Typ. | Max. | Min. | Max. | |
| t _{PHL} | Propagation Delay, D _n to O _n | 3.3 | 0.5 | 8.5 | 10.5 | 2.5 | 11.0 | ns |
| t _{PLH} | | 5.0 | 1.5 | 5.5 | 7.0 | 1.5 | 7.5 | |
| t _{PLH} | Propagation Delay, LE to O _n | 3.3 | 2.5 | 8.5 | 12.0 | 2.5 | 12.5 | ns |
| t _{PHL} | | 5.0 | 2.0 | 6.0 | 8.0 | 2.0 | 8.5 | |
| t _{PZL} | Output Enable Time | 3.3 | 2.5 | 8.5 | 13.0 | 2.5 | 13.5 | ns |
| t _{PZH} | | 5.0 | 1.5 | 6.0 | 8.5 | 1.5 | 9.0 | |
| t _{PHZ} | Output Disable Time | 3.3 | 1.0 | 9.0 | 14.5 | 1.0 | 15.0 | ns |
| t _{PLZ} | | 5.0 | 1.0 | 6.0 | 9.5 | 1.0 | 10.0 | |

Note:

7. Voltage range 5.0 is 5.0V ± 0.5V. Voltage range 3.3 is 3.3V ± 0.3V.

AC Operating Requirements for AC

| Symbol | Parameter | V _{CC} (V) ⁽⁸⁾ | T _A = +25°C, C _L = 50pF | | T _A = -40°C to +85°C, C _L = 50pF | Units |
|----------------|--|------------------------------------|--|--------------------|---|-------|
| | | | Typ. | Guaranteed Minimum | | |
| t _S | Setup Time, HIGH or LOW, D _n to LE | 3.3 | 0 | 3.0 | 3.0 | ns |
| | | 5.0 | 0 | 3.0 | 3.0 | |
| t _H | Hold Time, HIGH or LOW, D _n to LE | 3.3 | 0 | 1.5 | 1.5 | ns |
| | | 5.0 | 0 | 1.5 | 1.5 | |
| t _W | LE Pulse Width, HIGH | 3.3 | 2.0 | 4.0 | 4.0 | ns |
| | | 5.0 | 2.0 | 4.0 | 4.0 | |

Note:

8. Voltage range 5.0 is 5.0V ± 0.5V. Voltage range 3.3 is 3.3V ± 0.3V.

AC Electrical Characteristics for ACT

| Symbol | Parameter | V_{CC} (V) ⁽⁹⁾ | $T_A = +25^\circ\text{C}$, $C_L = 50\text{pF}$ | | | $T_A = -40^\circ\text{C to } +85^\circ\text{C}$, $C_L = 50\text{pF}$ | | Units |
|-----------|--------------------------------------|-----------------------------|--|------|------|--|------|-------|
| | | | Min. | Typ. | Max. | Min. | Max. | |
| t_{PLH} | Propagation Delay, D_n to O_n | 5.0 | 2.5 | 6.0 | 10.5 | 2.0 | 12.0 | ns |
| t_{PHL} | | | | | | | | |
| t_{PLH} | Propagation Delay, LE to O_n | 5.0 | 3.0 | 6.0 | 10.5 | 2.5 | 12.0 | ns |
| t_{PHL} | Propagation Delay, LE to O_n | 5.0 | 2.5 | 5.5 | 9.5 | 2.0 | 10.5 | ns |
| t_{PZH} | Output Enable Time | 5.0 | 2.0 | 5.5 | 10.0 | 1.5 | 11.0 | ns |
| t_{PZL} | Output Enable Time | 5.0 | 1.5 | 5.5 | 9.5 | 1.5 | 10.5 | ns |
| t_{PHZ} | Output Disable Time | 5.0 | 2.5 | 6.5 | 11.0 | 1.5 | 12.5 | ns |
| t_{PLZ} | Output Disable Time | 5.0 | 1.5 | 5.0 | 8.5 | 1.0 | 9.5 | ns |

Note:

9. Voltage range 5.0 is $5.0\text{V} \pm 0.5\text{V}$.

AC Operating Requirements for ACT

| Symbol | Parameter | V_{CC} (V) ⁽¹⁰⁾ | $T_A = +25^\circ\text{C}$, $C_L = 50\text{pF}$ | | $T_A = -40^\circ\text{C to } +85^\circ\text{C}$, $C_L = 50\text{pF}$ | | Units |
|--------|---|------------------------------|--|--------------------|--|--|-------|
| | | | Typ. | Guaranteed Minimum | | | |
| t_S | Setup Time, HIGH or LOW, D_n to LE | 5.0 | 1.5 | 3.0 | 3.5 | | ns |
| t_H | Hold Time, HIGH or LOW, D_n to LE | 5.0 | -1.5 | 0 | 0 | | ns |
| t_W | LE Pulse Width, HIGH | 5.0 | 2.0 | 3.5 | 4.0 | | ns |

Note:

10. Voltage range 5.0 is $5.0\text{V} \pm 0.5\text{V}$.

Capacitance

| Symbol | Parameter | Conditions | Typ. | Units |
|----------|-------------------------------|------------------------|--------------|-------|
| C_{IN} | Input Capacitance | $V_{CC} = \text{OPEN}$ | 5.0 | pF |
| C_{PD} | Power Dissipation Capacitance | $V_{CC} = 5.0\text{V}$ | 25.0 42.0 | pF |
| | AC | | | |
| | ACT | | | |

Physical Dimensions

Dimensions are in inches (millimeters) unless otherwise noted.

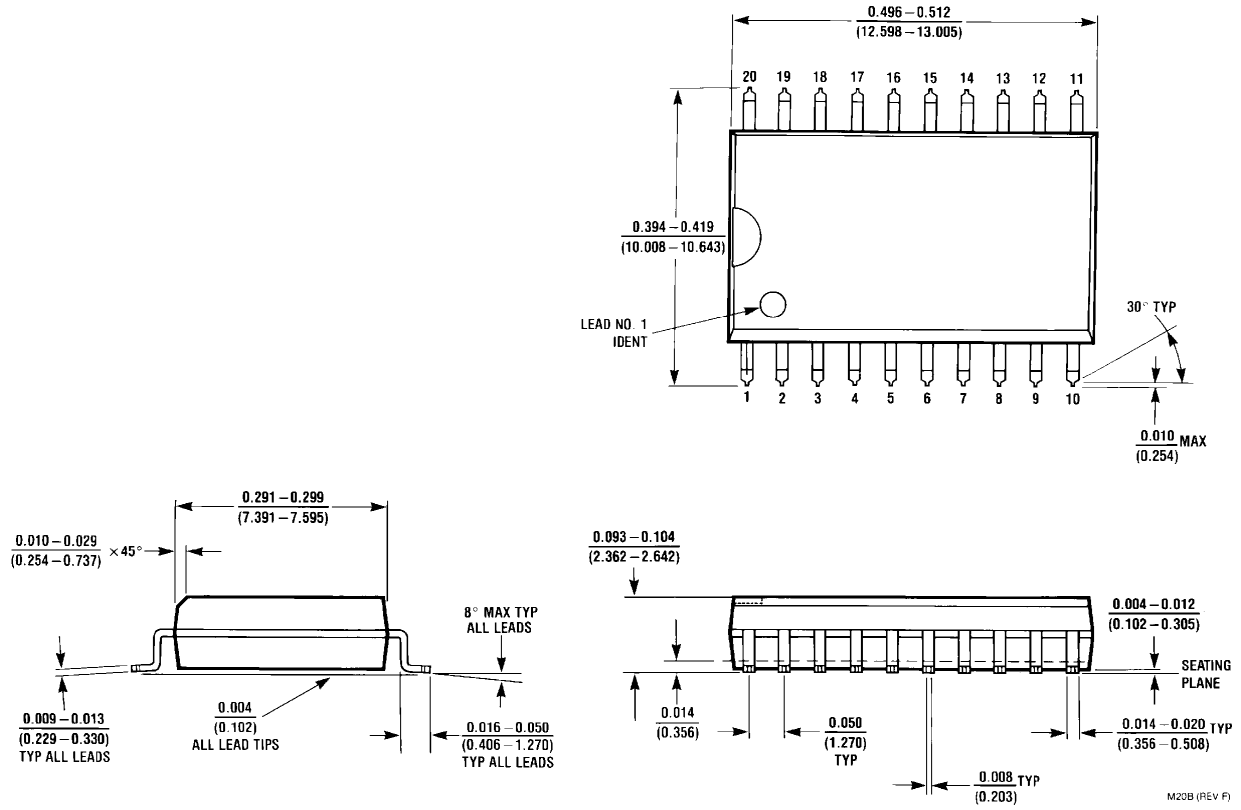
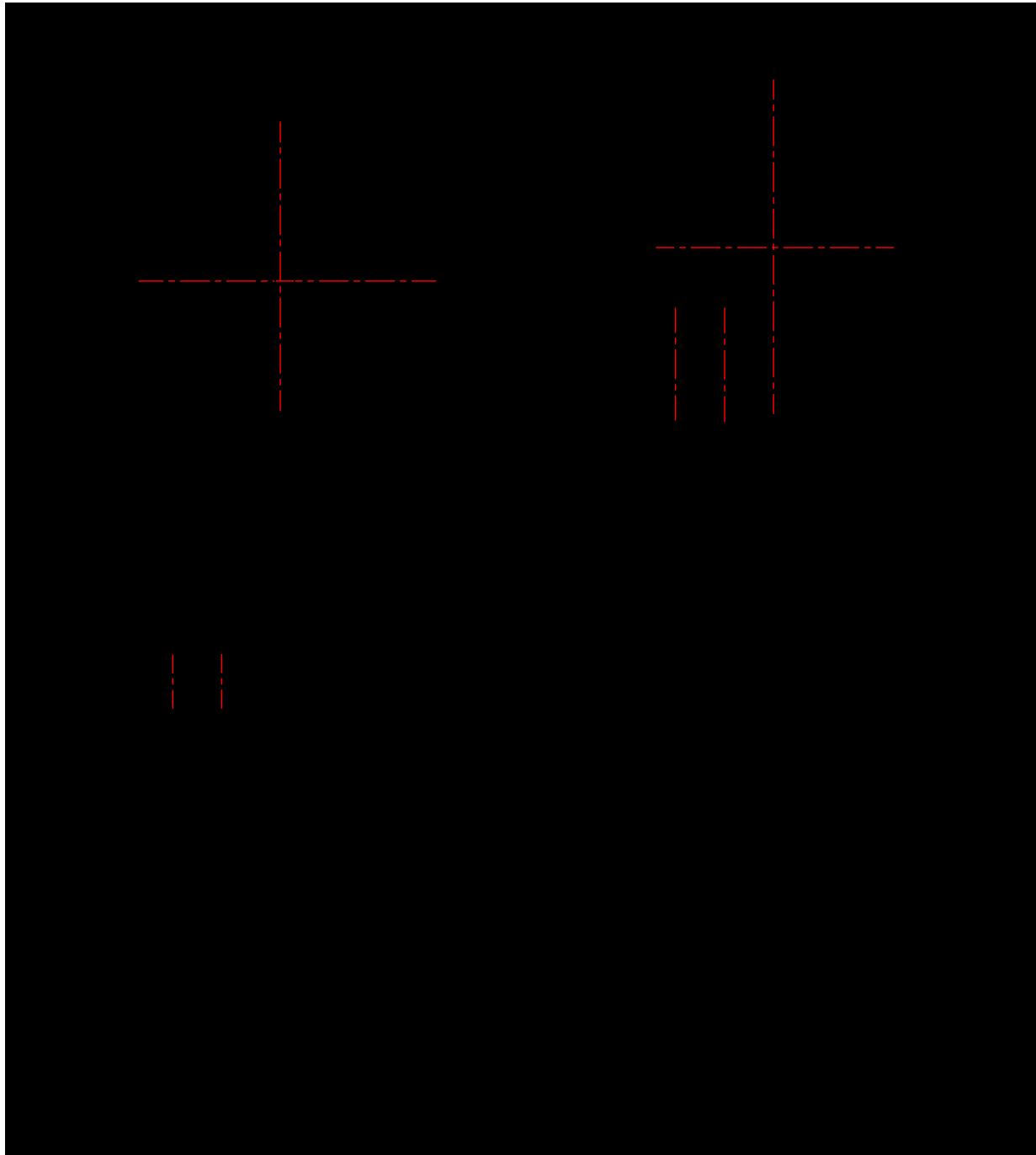


Figure 1. 20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide Package Number M20B

Physical Dimensions (Continued)

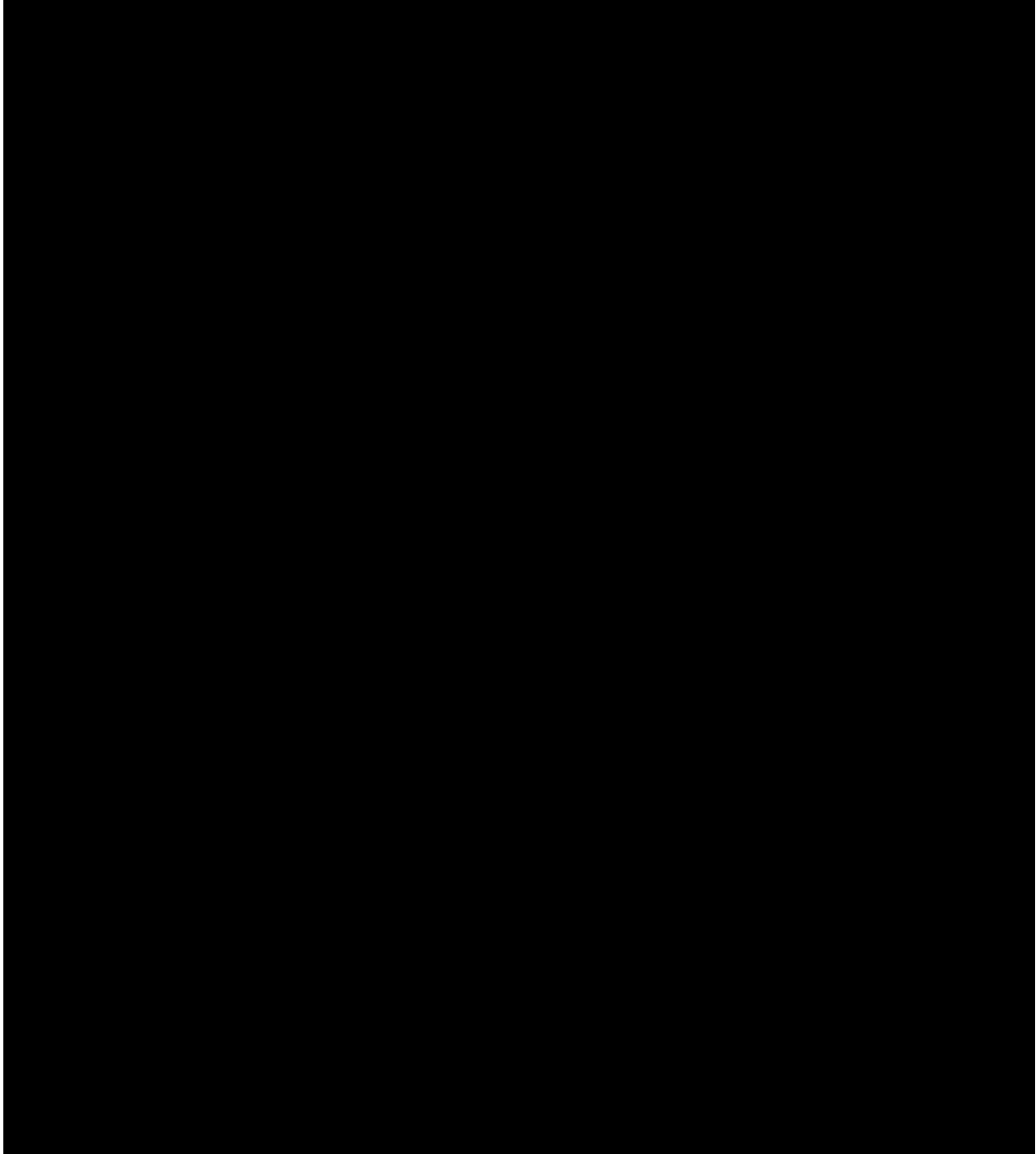
Dimensions are in millimeters unless otherwise noted.



**Figure 2. 20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
Package Number M20D**

Physical Dimensions (Continued)

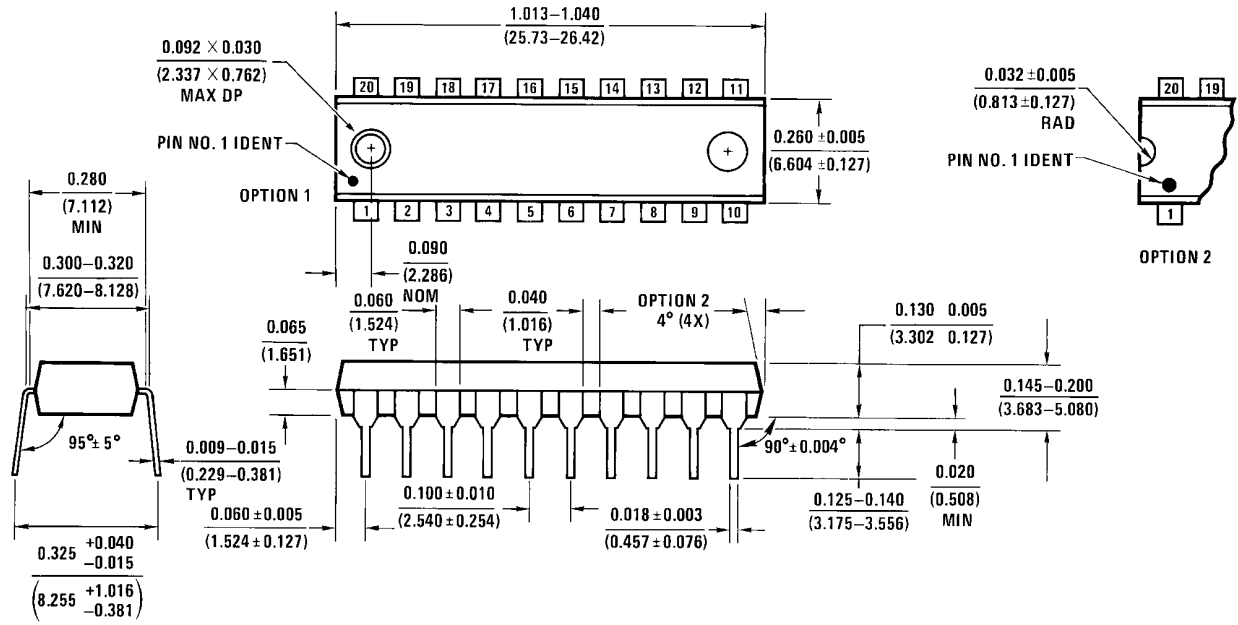
Dimensions are in millimeters unless otherwise noted.



**Figure 3. 20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
Package Number MTC20**

Physical Dimensions (Continued)

Dimensions are in inches (millimeters) unless otherwise noted.



N20A (REV G)

Figure 4. 20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide Package Number N20A



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