

## Features

- ESD/Surge Protection for 1 Line with Unidirectional.
- Provide ESD protection for each line to **IEC 61000-4-2 (ESD)  $\pm 30\text{kV}$  (air / contact)**  
**IEC 61000-4-4 (EFT) 80A (5/50ns)**  
**IEC 61000-4-5 (Lightning) 38A (8/20 $\mu\text{s}$ )**
- For operating voltage of **12V and below**
- **1.6mm x 1.0mm DFN package** saves board space
- Protect one I/O line or one power line
- Fast turn-on and Low clamping voltage
- Solid-state silicon-avalanche and active circuit triggering technology
- **Green Part**

## Applications

- Power Supply Protection
- USB VBUS Protection
- Cellular Handsets and Accessories
- Small Panel Modules
- PDA's
- Portable Devices
- Digital Cameras
- Touch Panels
- Notebooks and Handhelds
- MP3 Players
- Peripherals

## Description

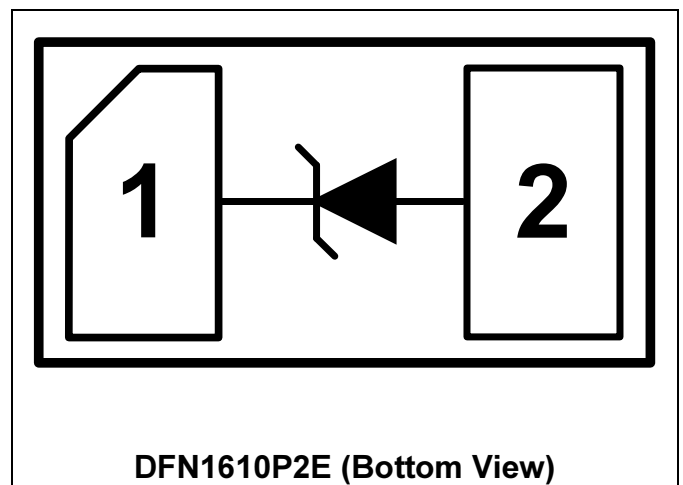
AZ4512-01F is a design which includes a unidirectional surge rated clamping cell to protect one power line, or one control line, or one low speed data line in an electronic systems. The AZ4512-01F has been specifically designed to protect sensitive components which are connected to power and control lines from

over-voltage damage and latch-up caused by Electrostatic Discharging (ESD), Electrical Fast Transients (EFT), Lightning, and Cable Discharge Event (CDE).

AZ4512-01F is a unique design which includes proprietary clamping cell in a single package. During transient conditions, the proprietary clamping cell prevents over-voltage on the power line or control/data lines, protecting any downstream components.

AZ4512-01F may be used to meet the ESD immunity requirements of IEC 61000-4-2, Level 4 ( $\pm 15\text{kV}$  air,  $\pm 8\text{kV}$  contact discharge).

## Circuit Diagram / Pin Configuration





## SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS			
PARAMETER	SYMBOL	RATING	UNITS
Peak Pulse Current (tp =8/20μs)	I <sub>PP</sub>	38	A
Operating Supply Voltage (pin-1 to pin-2)	V <sub>DC</sub>	13.2	V
pin-2 to pin-1 ESD per IEC 61000-4-2 (Air)	V <sub>ESD-1</sub>	±30	kV
pin-2 to pin-1 ESD per IEC 61000-4-2 (Contact)	V <sub>ESD-2</sub>	±30	kV
Lead Soldering Temperature	T <sub>SOL</sub>	260 (10 sec.)	°C
Operating Temperature	T <sub>OP</sub>	-55 to +85	°C
Storage Temperature	T <sub>STO</sub>	-55 to +150	°C

ELECTRICAL CHARACTERISTICS						
PARAMETER	SYMBOL	CONDITIONS	MINI	TYP	MAX	UNITS
Reverse Stand-Off Voltage	V <sub>RWM</sub>	pin-1 to pin-2, T=25 °C			12	V
Reverse Leakage Current	I <sub>Leak</sub>	V <sub>RWM</sub> = 12V, T=25 °C, pin-1 to pin-2			0.1	μA
Reverse Breakdown Voltage	V <sub>BV</sub>	I <sub>BV</sub> = 1mA, T=25 °C, pin-1 to pin-2	13.3		15.5	V
Forward Voltage	V <sub>F</sub>	I <sub>F</sub> = 15mA, T=25 °C, pin-2 to pin-1	0.6		1.2	V
Surge Clamping Voltage	V <sub>CL-surge</sub>	I <sub>PP</sub> =5A, tp=8/20μs, T=25 °C, pin-1 to pin-2		14.5		V
		I <sub>PP</sub> =38A, tp=8/20μs, T=25 °C, pin-1 to pin-2		18.5		V
ESD Clamping Voltage (Note 1)	V <sub>clamp</sub>	IEC 61000-4-2 +8kV (I <sub>TLP</sub> = 16A), T=25 °C, Contact mode, pin-1 to pin-2		15		V
ESD Dynamic Turn-on Resistance	R <sub>dynamic</sub>	IEC 61000-4-2 0~+8kV, T=25 °C, Contact mode, pin-1 to pin-2		0.04		Ω
Channel Input Capacitance	C <sub>IN</sub>	V <sub>R</sub> = 0V, f = 1MHz, T=25 °C, pin-1 to pin-2		440		pF

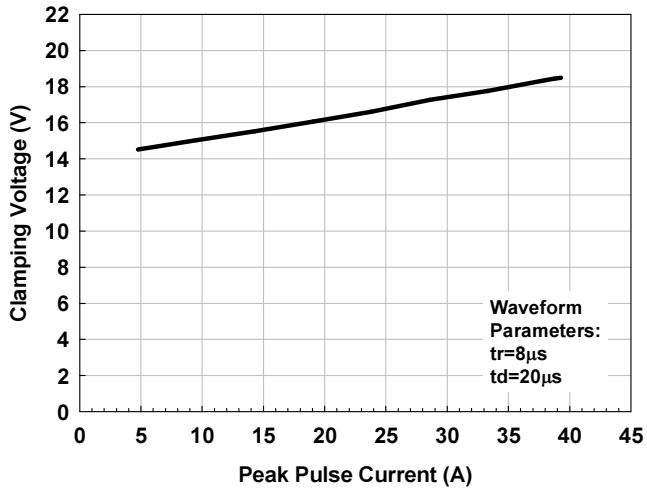
Note 1: ESD Clamping Voltage was measured by Transmission Line Pulsing (TLP) System.

TLP conditions: Z<sub>0</sub>= 50Ω, t<sub>p</sub>= 100ns, t<sub>r</sub>= 1ns.

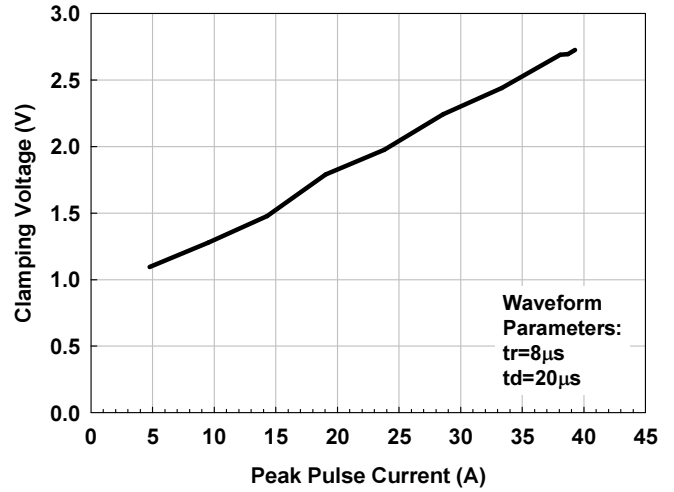


## Typical Characteristics

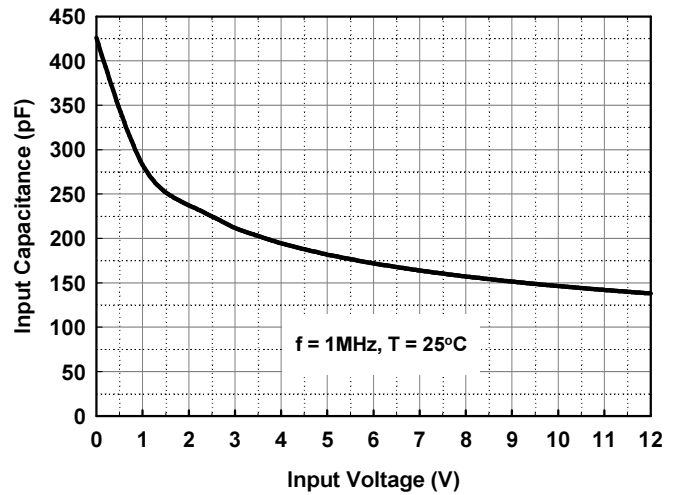
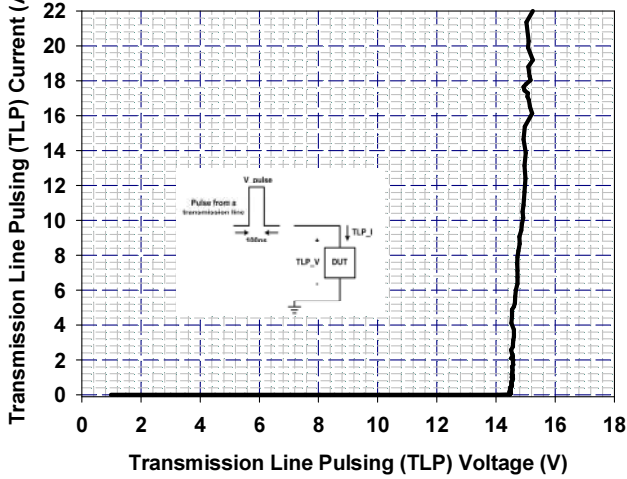
Reverse Clamping Voltage vs. Peak Pulse Current



Forward Clamping Voltage vs. Peak Pulse Current



Transmission Line Pulsing (TLP) Measurement



## Applications Information

The AZ4512-01F is designed to protect one line against System ESD/EFT/Lightning pulses by clamping them to an acceptable reference.

The usage of the AZ4512-01F is shown in Fig. 1. Protected lines, such as data lines, control lines, or power lines, are connected at pin 1. The pin 2 should be connected directly to a ground plane on the board. All path lengths connected to the pins of AZ4512-01F should be kept as short as possible to minimize parasitic inductance in the board traces.

In order to obtain enough suppression of ESD induced transient, good circuit board is critical.

Thus, the following guidelines are recommended:

- Minimize the path length between the protected lines and the AZ4512-01F.
- Place the AZ4512-01F near the input terminals or connectors to restrict transient coupling.
- The ESD current return path to ground should be kept as short as possible.
- Use ground planes whenever possible.
- NEVER route critical signals near board edges and near the lines which the ESD transient easily injects to.

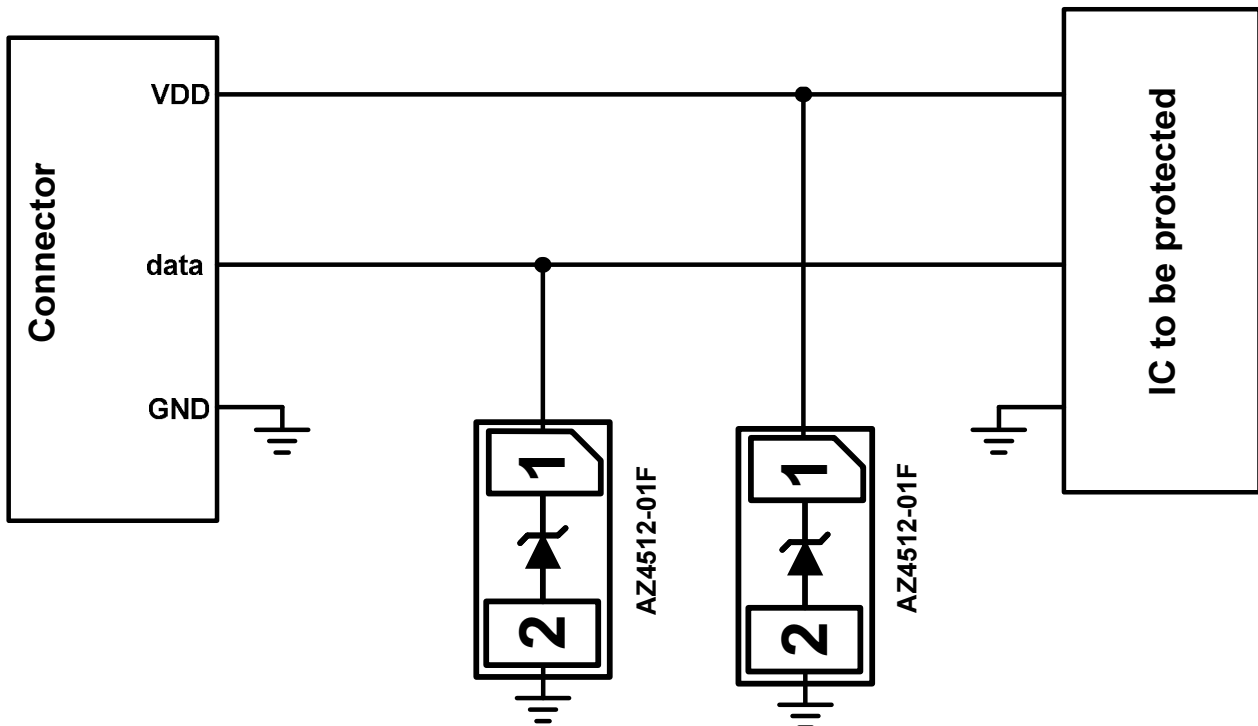


Fig. 1

Fig. 2 shows another simplified example of using AZ4512-01F to protect the control lines, low speed data lines, and power lines from ESD transient stress.

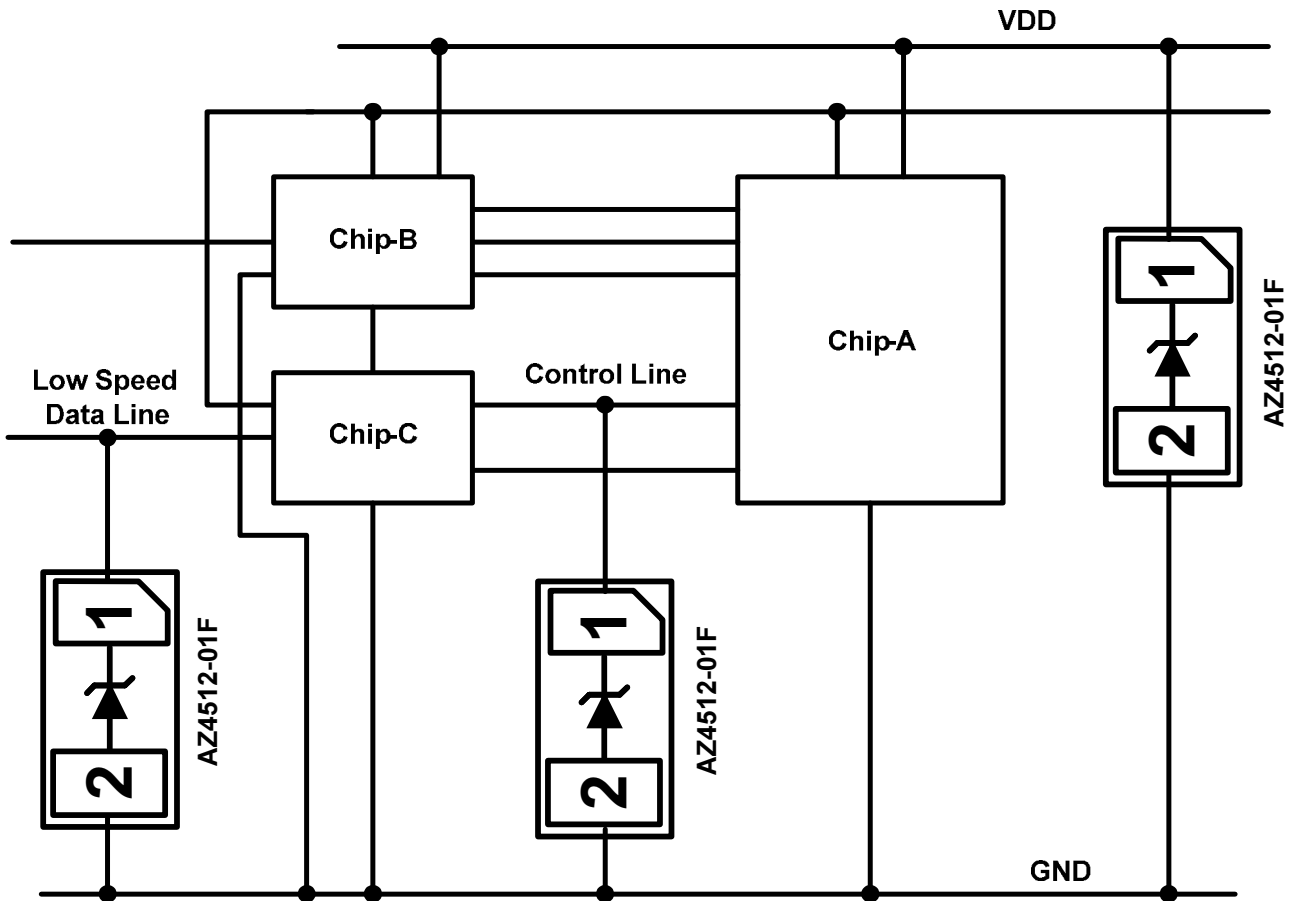
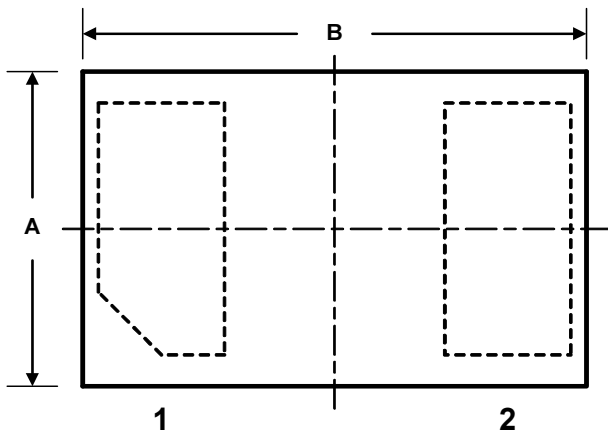


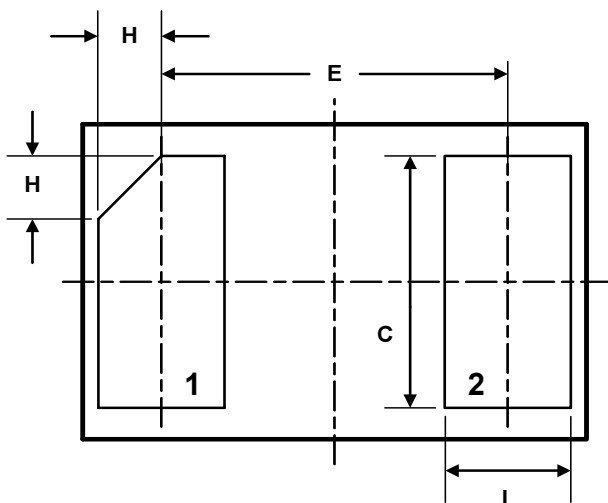
Fig. 2

## Mechanical Details

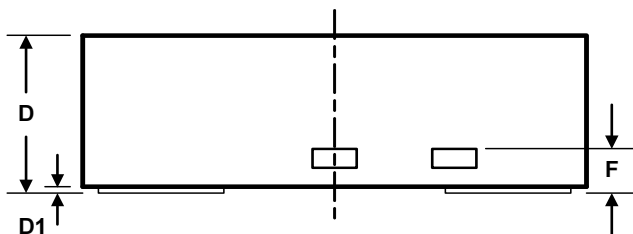
### DFN1610P2E PACKAGE DIAGRAMS



Top View



Bottom View

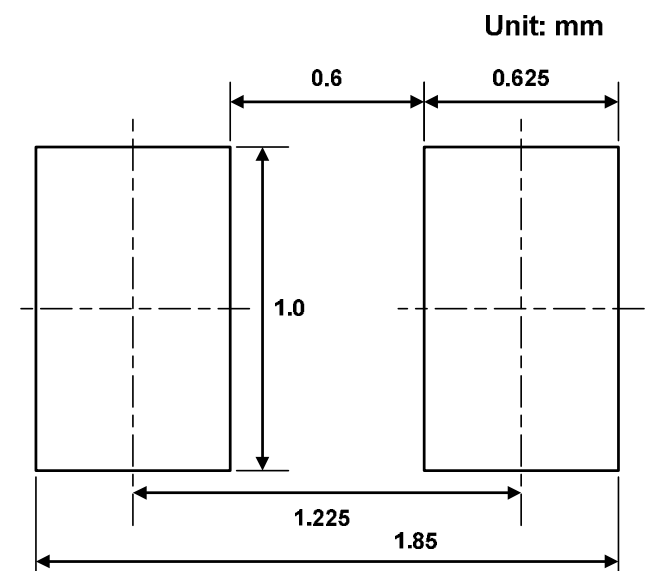


Side View

### PACKAGE DIMENSIONS

SYMBOL	Millimeter		
	Min.	Typ.	Max.
A	0.95	1.00	1.05
B	1.55	1.60	1.65
C	0.75	0.80	0.85
D	0.45	0.50	0.55
D1	-	0.02	0.05
E	1.10BSC		
F	0.10	0.15	0.20
H	0.15	0.20	0.25
L	0.35	0.40	0.45

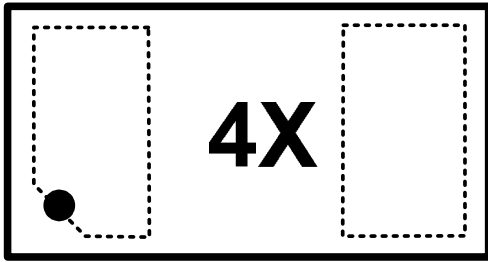
### LAND LAYOUT



#### Notes:

This LAND LAYOUT is for reference purposes only. Please consult your manufacturing partners to ensure your company's PCB design guidelines are met.

## MARKING CODE



Top View

4 = Device Code  
X = Control Code

Part Number	Marking Code
AZ4512-01F (Green Part)	4X

Note. Green means Pb-free, RoHS, and Halogen free compliant.

## Ordering Information

PN#	Material	Type	Reel size	MOQ	MOQ/internal box	MOQ/carton
AZ4512-01F.R7G	Green	T/R	7 inch	3,000/reel	4 reel= 12,000/box	6 box =72,000/carton

## Revision History

Revision	Modification Description
Revision 2015/03/12	Preliminary Release.
Revision 2015/12/07	Formal Release.