

# 74F251A

## 8-Input Multiplexer with 3-STATE Outputs

### General Description

The 74F251A is a high-speed 8-input digital multiplexer. It provides, in one package, the ability to select one bit of data from up to eight sources. It can be used as a universal function generator to generate any logic function of four variables. Both assertion and negation outputs are provided.

### Features

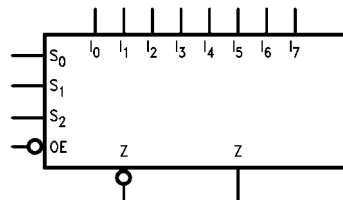
- Multifunctional capability
- On-chip select logic decoding
- Inverting and non-inverting 3-STATE outputs

### Ordering Code:

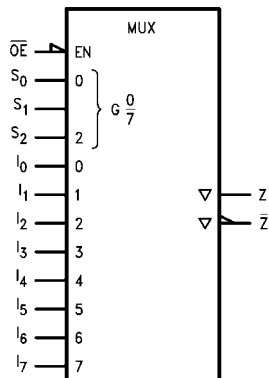
| Order Number | Package Number | Package Description   |
|--------------|----------------|---|
| 74F251ASC    | M16A           | 16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150 Narrow |
| 74F251ASJ    | M16D           | 16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide               |
| 74F251APC    | N16E           | 16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide       |

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

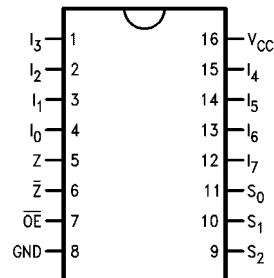
### Logic Symbols



IEEE/IEC



### Connection Diagram



### Unit Loading/Fan Out

| Pin Names       | Description                              | U.L.<br>HIGH/LOW | Input $I_{IH}/I_{IL}$<br>Output $I_{OH}/I_{OL}$ |
|-----------------|--|------------------|---|
| $S_0$ - $S_2$   | Select Inputs                            | 1.0/1.0          | 20 $\mu$ A/-0.6 mA                              |
| $\overline{OE}$ | 3-STATE Output Enable Input (Active LOW) | 1.0/1.0          | 20 $\mu$ A/-0.6 mA                              |
| $I_0$ - $I_7$   | Multiplexer Inputs                       | 1.0/1.0          | 20 $\mu$ A/-0.6 mA                              |
| Z               | 3-STATE Multiplexer Output               | 150/40 (33.3)    | -3 mA/24 mA (20 mA)                             |
| $\overline{Z}$  | Complementary 3-STATE Multiplexer Output | 150/40 (33.3)    | -3 mA/24 mA (20 mA)                             |

### Functional Description

This device is a logical implementation of a single-pole, 8-position switch with the switch position controlled by the state of three Select inputs,  $S_0$ ,  $S_1$ ,  $S_2$ . Both assertion and negation outputs are provided. The Output Enable input ( $\overline{OE}$ ) is active LOW. When it is activated, the logic function provided at the output is:

$$Z = \overline{OE} \cdot (I_0 \cdot \overline{S_0} \cdot \overline{S_1} \cdot \overline{S_2} + I_1 \cdot S_0 \cdot \overline{S_1} \cdot \overline{S_2} + I_2 \cdot \overline{S_0} \cdot S_1 \cdot \overline{S_2} + I_3 \cdot S_0 \cdot S_1 \cdot \overline{S_2} + I_4 \cdot \overline{S_0} \cdot \overline{S_1} \cdot S_2 + I_5 \cdot S_0 \cdot \overline{S_1} \cdot S_2 + I_6 \cdot \overline{S_0} \cdot S_1 \cdot S_2 + I_7 \cdot S_0 \cdot S_1 \cdot S_2)$$

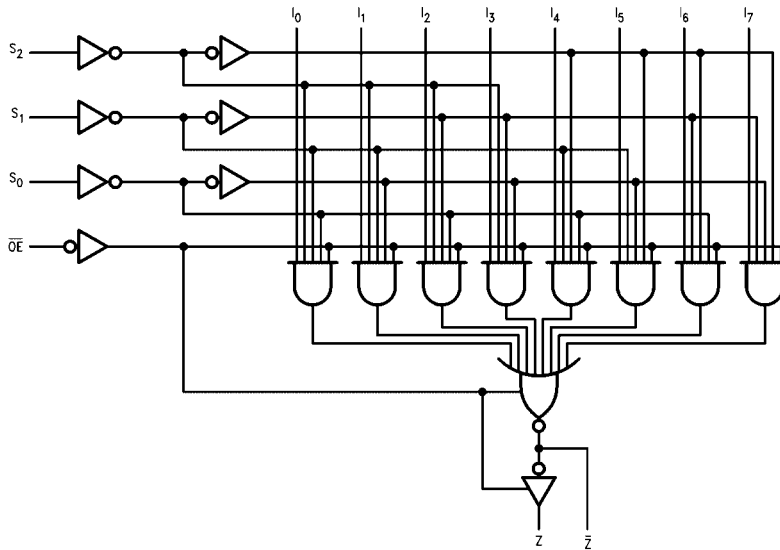
When the Output Enable is HIGH, both outputs are in the high impedance (High Z) state. This feature allows multiplexer expansion by tying the outputs of up to 128 devices together. When the outputs of the 3-STATE devices are tied together, all but one device must be in the high impedance state to avoid high currents that would exceed the maximum ratings. The Output Enable signals should be designed to ensure there is no overlap in the active LOW portion of the enable voltages.

### Truth Table

| Inputs          |       |       |       | Outputs          |       |
|-----------------|-------|-------|-------|------------------|-------|
| $\overline{OE}$ | $S_2$ | $S_1$ | $S_0$ | $\overline{Z}$   | Z     |
| H               | X     | X     | X     | Z                | Z     |
| L               | L     | L     | L     | $\overline{I_0}$ | $I_0$ |
| L               | L     | L     | H     | $\overline{I_1}$ | $I_1$ |
| L               | L     | H     | L     | $\overline{I_2}$ | $I_2$ |
| L               | L     | H     | H     | $\overline{I_3}$ | $I_3$ |
| L               | H     | L     | L     | $\overline{I_4}$ | $I_4$ |
| L               | H     | L     | H     | $\overline{I_5}$ | $I_5$ |
| L               | H     | H     | L     | $\overline{I_6}$ | $I_6$ |
| L               | H     | H     | H     | $\overline{I_7}$ | $I_7$ |

H = HIGH Voltage Level  
L = LOW Voltage Level  
X = Immaterial  
Z = High Impedance

### Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

**Absolute Maximum Ratings**(Note 1)

|  |                                      |
|--|--------------------------------------|
| Storage Temperature  | -65°C to +150°C                      |
| Ambient Temperature under Bias   | -55°C to +125°C                      |
| Junction Temperature under Bias  | -55°C to +150°C                      |
| V <sub>CC</sub> Pin Potential to Ground Pin                            | -0.5V to +7.0V                       |
| Input Voltage (Note 2)   | -0.5V to +7.0V                       |
| Input Current (Note 2)   | -30 mA to +5.0 mA                    |
| Voltage Applied to Output<br>in HIGH State (with V <sub>CC</sub> = 0V) |                                      |
| Standard Output  | -0.5V to V <sub>CC</sub>             |
| 3-STATE Output   | -0.5V to +5.5V                       |
| Current Applied to Output<br>in LOW State (Max)                        | twice the rated I <sub>OL</sub> (mA) |

**Recommended Operating Conditions**

|                              |                |
|------------------------------|----------------|
| Free Air Ambient Temperature | 0°C to +70°C   |
| Supply Voltage               | +4.5V to +5.5V |

**Note 1:** Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

**Note 2:** Either voltage limit or current limit is sufficient to protect inputs.

**DC Electrical Characteristics**

| Symbol           | Parameter                         | Min  | Typ                      | Max  | Units | V <sub>CC</sub> | Conditions   |
|------------------|-----------------------------------|--|--------------------------|------|-------|-----------------|--|
| V <sub>IH</sub>  | Input HIGH Voltage                | 2.0  |                          |      | V     |                 | Recognized as a HIGH Signal  |
| V <sub>IL</sub>  | Input LOW Voltage                 |  |                          | 0.8  | V     |                 | Recognized as a LOW Signal   |
| V <sub>CD</sub>  | Input Clamp Diode Voltage         |  |                          | -1.2 | V     | Min             | I <sub>IN</sub> = -18 mA   |
| V <sub>OH</sub>  | Output HIGH Voltage               | 10% V <sub>CC</sub><br>10% V <sub>CC</sub><br>5% V <sub>CC</sub><br>5% V <sub>CC</sub> | 2.5<br>2.4<br>2.7<br>2.7 |      | V     | Min             | I <sub>OH</sub> = -1 mA<br>I <sub>OH</sub> = -3 mA<br>I <sub>OH</sub> = -1 mA<br>I <sub>OH</sub> = -3 mA |
| V <sub>OL</sub>  | Output LOW Voltage                | 10% V <sub>CC</sub>  |                          | 0.5  | V     | Min             | I <sub>OL</sub> = 24 mA  |
| I <sub>IH</sub>  | Input HIGH Current                |  |                          | 5.0  | μA    | Max             | V <sub>IN</sub> = 2.7V   |
| I <sub>BVI</sub> | Input HIGH Current Breakdown Test |  |                          | 7.0  | μA    | Max             | V <sub>IN</sub> = 7.0V   |
| I <sub>CEX</sub> | Output HIGH Leakage Current       |  |                          | 50   | μA    | Max             | V <sub>OUT</sub> = V <sub>CC</sub>   |
| V <sub>ID</sub>  | Input Leakage Test                | 4.75   |                          |      | V     | 0.0             | I <sub>ID</sub> = 1.9 μA<br>All Other Pins Grounded  |
| I <sub>OD</sub>  | Output Leakage Circuit Current    |  |                          | 3.75 | μA    | 0.0             | V <sub>IOD</sub> = 150 mV<br>All Other Pins Grounded   |
| I <sub>IL</sub>  | Input LOW Current                 |  |                          | -0.6 | mA    | Max             | V <sub>IN</sub> = 0.5V   |
| I <sub>OZH</sub> | Output Leakage Current            |  |                          | 50   | μA    | Max             | V <sub>OUT</sub> = 2.7V  |
| I <sub>OZL</sub> | Output Leakage Current            |  |                          | -50  | μA    | Max             | V <sub>OUT</sub> = 0.5V  |
| I <sub>OS</sub>  | Output Short-Circuit Current      | -60  |                          | -150 | mA    | Max             | V <sub>OUT</sub> = 0V  |
| I <sub>ZZ</sub>  | Bus Drainage Test                 |  |                          | 500  | μA    | 0.0V            | V <sub>OUT</sub> = 5.25V   |
| I <sub>CC1</sub> | Power Supply Current              |  | 15                       | 22   | mA    | Max             | V <sub>O</sub> = LOW   |
| I <sub>CC2</sub> | Power Supply Current              |  | 16                       | 24   | mA    | Max             | V <sub>O</sub> = HIGH Z  |

## AC Electrical Characteristics

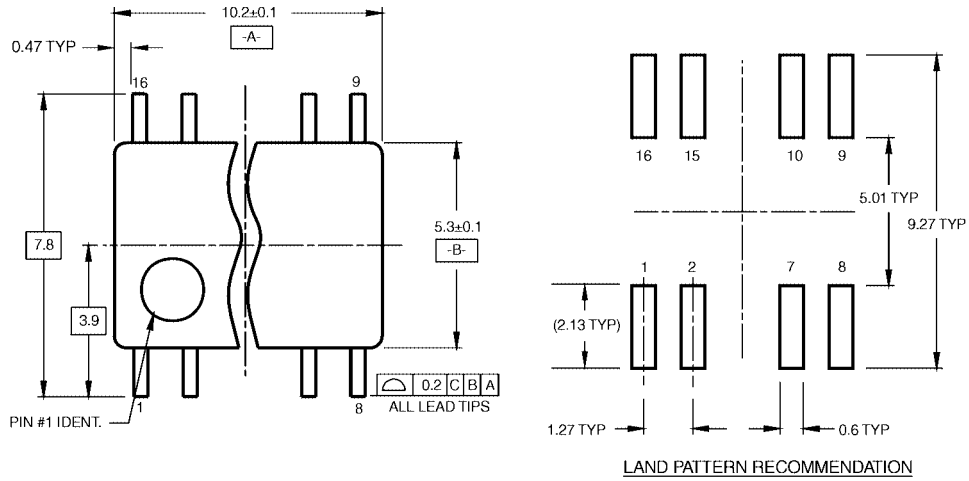
| Symbol    | Parameter                    | $T_A = +25^\circ\text{C}$<br>$V_{CC} = 5.0\text{V}$<br>$C_L = 50\text{ pF}$ |     |      | $T_A = -55^\circ\text{C to } +125^\circ\text{C}$<br>$V_{CC} = 5.0\text{V}$<br>$C_L = 50\text{ pF}$ |      | $T_A = 0^\circ\text{C to } +70^\circ\text{C}$<br>$V_{CC} = 5.0\text{V}$<br>$C_L = 50\text{ pF}$ |      | Units |
|-----------|------------------------------|---|-----|------|--|------|---|------|-------|
|           |                              | Min   | Typ | Max  | Min  | Max  | Min   | Max  |       |
| $t_{PLH}$ | Propagation Delay            | 3.5   | 6.0 | 9.0  | 3.5  | 11.5 | 3.5   | 9.5  | ns    |
| $t_{PHL}$ | $S_n$ to $\bar{Z}$           | 3.2   | 5.0 | 7.5  | 3.2  | 8.0  | 3.2   | 7.5  |       |
| $t_{PLH}$ | Propagation Delay            | 4.5   | 7.5 | 10.5 | 3.5  | 14.0 | 4.5   | 12.5 | ns    |
| $t_{PHL}$ | $S_n$ to Z                   | 4.0   | 6.0 | 8.5  | 3.0  | 10.5 | 4.0   | 9.0  |       |
| $t_{PLH}$ | Propagation Delay            | 3.0   | 5.0 | 6.5  | 2.5  | 8.0  | 3.0   | 7.0  | ns    |
| $t_{PHL}$ | $I_n$ to $\bar{Z}$           | 1.5   | 2.5 | 4.0  | 1.5  | 6.0  | 1.5   | 5.0  |       |
| $t_{PLH}$ | Propagation Delay            | 3.5   | 5.0 | 7.0  | 2.5  | 9.0  | 2.5   | 8.0  | ns    |
| $t_{PHL}$ | $I_n$ to Z                   | 3.5   | 5.5 | 7.0  | 3.5  | 9.0  | 3.5   | 7.5  |       |
| $t_{PZH}$ | Output Enable Time           | 2.5   | 4.3 | 6.0  | 2.0  | 7.0  | 2.5   | 7.0  | ns    |
| $t_{PZL}$ | $\overline{OE}$ to $\bar{Z}$ | 2.5   | 4.3 | 6.0  | 2.5  | 7.5  | 2.5   | 6.5  |       |
| $t_{PHZ}$ | Output Disable Time          | 2.5   | 4.0 | 5.5  | 2.5  | 6.0  | 2.5   | 6.0  |       |
| $t_{PLZ}$ | $\overline{OE}$ to $\bar{Z}$ | 1.5   | 3.0 | 4.5  | 1.5  | 5.0  | 1.5   | 4.5  | ns    |
| $t_{PZH}$ | Output Enable Time           | 3.5   | 5.0 | 7.0  | 3.0  | 8.5  | 3.0   | 7.5  |       |
| $t_{PZL}$ | $\overline{OE}$ to Z         | 3.5   | 5.5 | 7.5  | 3.5  | 9.0  | 3.5   | 8.0  |       |
| $t_{PHZ}$ | Output Disable Time          | 2.0   | 3.8 | 5.5  | 2.0  | 5.5  | 2.0   | 5.5  | ns    |
| $t_{PLZ}$ | $\overline{OE}$ to Z         | 1.5   | 3.0 | 4.5  | 1.5  | 5.5  | 1.5   | 4.5  |       |

**Physical Dimensions** inches (millimeters) unless otherwise noted



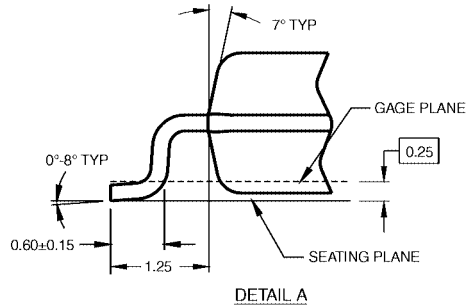
**16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150 Narrow Package Number M16A**

**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)



- NOTES:
- A. CONFORMS TO EIAJ EDR-7320 REGISTRATION, ESTABLISHED IN DECEMBER, 1998.
  - B. DIMENSIONS ARE IN MILLIMETERS.
  - C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

M16DRevB1



**16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide Package Number M16D**

**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)



**16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide Package Number N16E**

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