Quad Channel, 16-Bit, Serial Input, 4 mA to 20 mA Output DAC, Dynamic Power Control, HART Connectivity

Data Sheet

AD5757

FEATURES

16-bit resolution and monotonicity
Dynamic power control for thermal management or external PMOS mode
Current output ranges: 0 mA to 20 mA, 4 mA to 20 mA, or 0 mA to 24 mA
±0.05% total unadjusted error (TUE) maximum
User programmable offset and gain
On-chip diagnostics
On-chip reference (±10 ppm/°C maximum)
−40°C to +105°C temperature range

APPLICATIONS

Process control
Actuator control
Programmable logic controllers (PLCs)
HART network connectivity

GENERAL DESCRIPTION

The AD5757 is a quad, current output DAC that operates with a power supply range from 10.8 V to 33 V. On-chip dynamic power control minimizes package power dissipation by regulating the voltage on the output driver from 7.4 V to 29.5 V, using a dc-to-dc boost converter optimized for minimum on-chip power dissipation.

Each channel has a corresponding CHART pin so that HART signals can be coupled onto the current output of the AD5757.

The part uses a versatile 3-wire serial interface that operates at clock rates of up to 30 MHz and is compatible with standard SPI, QSPI™, MICROWIRE™, DSP, and microcontroller interface standards. The interface also features optional CRC-8 packet error checking, as well as a watchdog timer that monitors activity on the interface.

PRODUCT HIGHLIGHTS

1. Dynamic power control for thermal management.
2. 16-bit performance.
3. Multichannel.
4. HART compliant.

COMPANION PRODUCTS

Product Family: AD5755-1, AD5755
HART Modem: AD5700, AD5700-1
External References: ADR445, ADR02
Digital Isolators: ADuM1410, ADuM1411
Power: ADP2302, ADP2303
Additional companion products on the AD5757 product page

FUNCTIONAL BLOCK DIAGRAM

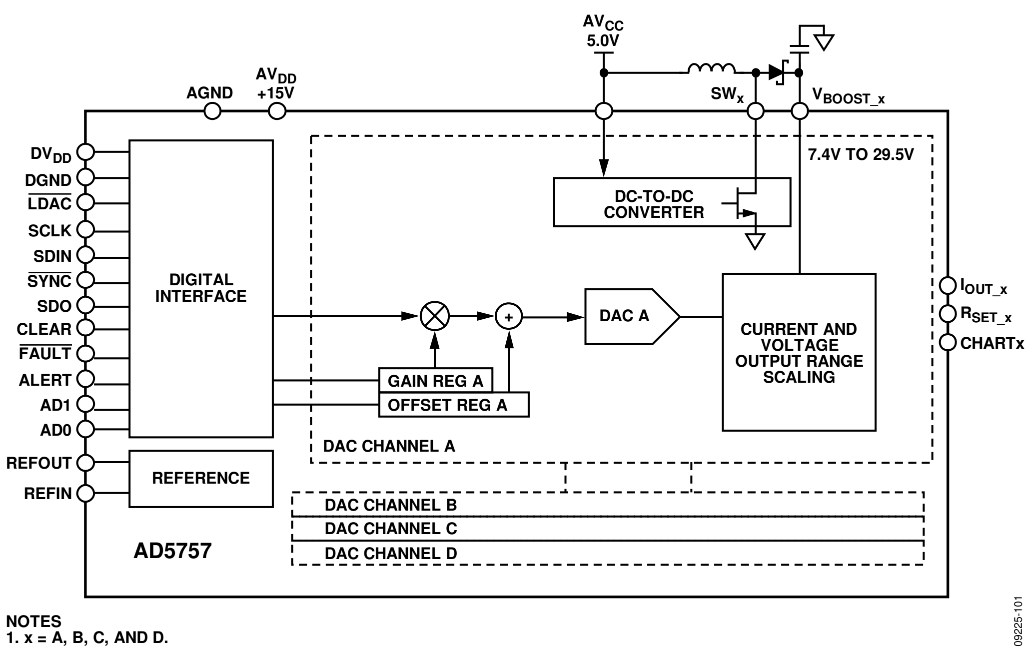

Figure 1.

Rev. G Document Feedback

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DETAILED FUNCTIONAL BLOCK DIAGRAM

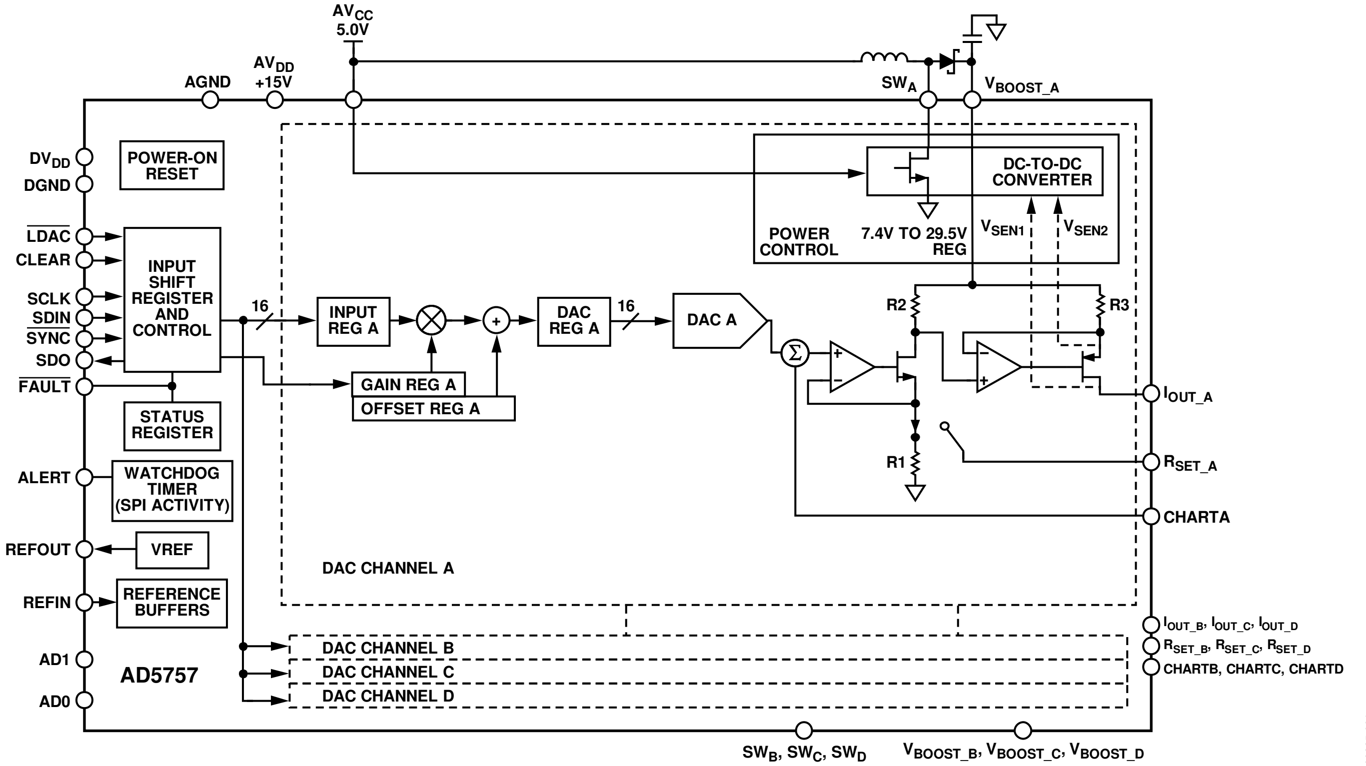


Figure 2.

SPECIFICATIONS

AV_{DD} = V_{BOOST_x} = 15 V; DV_{DD} = 2.7 V to 5.5 V; AV_{CC} = 4.5 V to 5.5 V; dc-to-dc converter disabled; AGND = DGND = $GNDSW_x$ = 0 V; REFIN = 5 V; R_L = 300 Ω; all specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 1.

Parameter[1]	Min	Typ	Max	Unit	Test Conditions/Comments
CURRENT OUTPUT					
Output Current Ranges	0		24	mA	
	0		20	mA	
	4		20	mA	
Resolution	16			Bits	
ACCURACY (EXTERNAL R_{SET})					Assumes ideal resistor; see the External Current Setting Resistor section for more information
Total Unadjusted Error (TUE)					
	−0.05	±0.009	+0.05	% FSR	
TUE Long-Term Stability		100		ppm FSR	Drift after 1000 hours, T_J = 150°C
Relative Accuracy (INL)	−0.006		+0.006	% FSR	
Differential Nonlinearity (DNL)	−1		+1	LSB	Guaranteed monotonic
Offset Error	−0.05	±0.005	+0.05	% FSR	
Offset Error Drift[2]		±4		ppm FSR/°C	
Gain Error	−0.05	±0.004	+0.05	% FSR	
Gain TC[2]		±3		ppm FSR/°C	
Full-Scale Error	−0.05	±0.008	+0.05	% FSR	
Full-Scale TC[2]		±5		ppm FSR/°C	
DC Crosstalk		0.0005		% FSR	External R_{SET}
ACCURACY (INTERNAL R_{SET})					
Total Unadjusted Error (TUE)[3, 4]	−0.14		+0.14	% FSR	
	−0.11	±0.009	+0.11	% FSR	T_A = 25°C
TUE Long-Term Stability		180		ppm FSR	Drift after 1000 hours, T_J = 150°C
Relative Accuracy (INL)	−0.006		+0.006	% FSR	
	−0.004		+0.004	% FSR	T_A = 25°C
Differential Nonlinearity (DNL)	−1		+1	LSB	Guaranteed monotonic
Offset Error[3,4]	−0.05		+0.05	% FSR	
	−0.04	±0.007	+0.04	% FSR	T_A = 25°C
Offset Error Drift[2]		±6		ppm FSR/°C	
Gain Error	−0.12		+0.12	% FSR	
	−0.06	±0.002	+0.06	% FSR	T_A = 25°C
Gain TC[2]		±9		ppm FSR/°C	
Full-Scale Error[3,4]	−0.14		+0.14	% FSR	
	−0.1	±0.007	+0.1	% FSR	T_A = 25°C
Full-Scale TC[2]		±14		ppm FSR/°C	
DC Crosstalk[4]		−0.011		% FSR	Internal R_{SET}
OUTPUT CHARACTERISTICS[2]					
Current Loop Compliance Voltage		V_{BOOST_x} − 2.4	V_{BOOST_x} − 2.7	V	
Output Current Drift vs. Time					Drift after 1000 hours, ¾ scale output, T_J = 150°C
		90		ppm FSR	External R_{SET}
		140		ppm FSR	Internal R_{SET}
Resistive Load			1000	Ω	The dc-to-dc converter has been characterized with a maximum load of 1 kΩ, chosen such that compliance is not exceeded; see Figure 32 and DC-DC MaxV bits in Table 24
Output Impedance		100		MΩ	
DC PSRR		0.02	1	µA/V	
REFERENCE INPUT/OUTPUT					
Reference Input[2]					
Reference Input Voltage	4.95	5	5.05	V	For specified performance
DC Input Impedance	45	150		MΩ	

Parameter[1]	Min	Typ	Max	Unit	Test Conditions/Comments
Reference Output					
Output Voltage	4.995	5	5.005	V	T_A = 25°C
Reference TC[2]	−10	±5	+10	ppm/°C	
Output Noise (0.1 Hz to 10 Hz)[2]		7		μV p-p	
Noise Spectral Density[2]		100		nV/√Hz	At 10 kHz
Output Voltage Drift vs. Time[2]		180		ppm	Drift after 1000 hours, T_J = 150°C
Capacitive Load[2]		1000		nF	
Load Current		9		mA	See Figure 43
Short-Circuit Current		10		mA	
Line Regulation[2]		3		ppm/V	See Figure 44
Load Regulation[2]		95		ppm/mA	See Figure 43
Thermal Hysteresis[2]		200		ppm	
DC-TO-DC					
Switch					
Switch On Resistance		0.425		Ω	
Switch Leakage Current		10		nA	
Peak Current Limit		0.8		A	
Oscillator					
Oscillator Frequency	11.5	13	14.5	MHz	This oscillator is divided down to give the dc-to-dc converter switching frequency
Maximum Duty Cycle		89.6		%	At 410 kHz dc-to-dc switching frequency
DIGITAL INPUTS[2]					JEDEC compliant
V_{IH}, Input High Voltage	2			V	
V_{IL}, Input Low Voltage			0.8	V	
Input Current	−1		+1	μA	Per pin
Pin Capacitance		2.6		pF	Per pin
DIGITAL OUTPUTS[2]					
SDO, ALERT					
V_{OL}, Output Low Voltage			0.4	V	Sinking 200 μA
V_{OH}, Output High Voltage	DVDD − 0.5			V	Sourcing 200 μA
High Impedance Leakage Current	−1		+1	μA	
High Impedance Output Capacitance		2.5		pF	
$\overline{FAULT}$					
V_{OL}, Output Low Voltage			0.4	V	10 kΩ pull-up resistor to DV_{DD}
V_{OL}, Output Low Voltage		0.6		V	At 2.5 mA
V_{OH}, Output High Voltage	3.6			V	10 kΩ pull-up resistor to DV_{DD}
POWER REQUIREMENTS					
AV_{DD}	9		33	V	
DV_{DD}	2.7		5.5	V	
AV_{CC}	4.5		5.5	V	
AI_{DD}		7	7.5	mA	
DI_{CC}		9.2	11	mA	V_{IH} = DV_{DD}, V_{IL} = DGND, internal oscillator running, over supplies
AI_{CC}			1	mA	Over supplies
I_{BOOST}[5]			1	mA	Per channel, current output mode, 0 mA output
Power Dissipation		155		mW	AV_{DD} = 15 V, DV_{DD} = 5 V, dc-to-dc converter enable, current output mode, outputs disabled

[1] Temperature range: −40°C to +105°C; typical at +25°C.
[2] Guaranteed by design and characterization; not production tested.
[3] For current outputs with internal R_{SET}, the offset, full-scale, and TUE measurements exclude dc crosstalk. The measurements are made with all four channels enabled loaded with the same code.
[4] See the Current Output Mode with Internal R_{SET} section for more explanation of the dc crosstalk.
[5] Efficiency plots in Figure 34, Figure 35, Figure 36, and Figure 37 include the I_{BOOST} quiescent current.

AC PERFORMANCE CHARACTERISTICS

$AV_{DD} = V_{BOOST\_x} = 15$ V; $DV_{DD} = 2.7$ V to 5.5 V; $AV_{CC} = 4.5$ V to 5.5 V; dc-to-dc converter disabled; AGND = DGND = $GNDSW_x = 0$ V; REFIN = 5 V; $R_L = 300\ \Omega$; all specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 2.

Parameter[1]	Min	Typ	Max	Unit	Test Conditions/Comments
DYNAMIC PERFORMANCE					
Current Output					
Output Current Settling Time		15		μs	To 0.1% FSR (0 mA to 24 mA)
		See test conditions/ comments		ms	See Figure 27, Figure 28, and Figure 29
Output Noise (0.1 Hz to 10 Hz Bandwidth)		0.15		LSB p-p	16-bit LSB, 0 mA to 24 mA range
Output Noise Spectral Density		0.5		nA/√Hz	Measured at 10 kHz, midscale output, 0 mA to 24 mA range

[1] Guaranteed by design and characterization; not production tested.

TIMING CHARACTERISTICS

$AV_{DD} = V_{BOOST\_x} = 15$ V; $DV_{DD} = 2.7$ V to 5.5 V; $AV_{CC} = 4.5$ V to 5.5 V; dc-to-dc converter disabled; AGND = DGND = $GNDSW_x = 0$ V; REFIN = 5 V; $R_L = 300\ \Omega$; all specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 3.

Parameter[1, 2, 3]	Limit at T_{MIN}, T_{MAX}	Unit	Description
t_1	33	ns min	SCLK cycle time
t_2	13	ns min	SCLK high time
t_3	13	ns min	SCLK low time
t_4	13	ns min	$\overline{\text{SYNC}}$ falling edge to SCLK falling edge setup time
t_5	13	ns min	$24^{th}/32^{nd}$ SCLK falling edge to $\overline{\text{SYNC}}$ rising edge (see Figure 55)
t_6	198	ns min	$\overline{\text{SYNC}}$ high time after a configuration write
	5	μs min	$\overline{\text{SYNC}}$ high time after a DAC update write
t_7	5	ns min	Data setup time
t_8	5	ns min	Data hold time
t_9	20	μs min	$\overline{\text{SYNC}}$ rising edge to $\overline{\text{LDAC}}$ falling edge (applies to any channel that has digital slew rate control enabled) (single DAC updated)
	5	μs min	$\overline{\text{SYNC}}$ rising edge to $\overline{\text{LDAC}}$ falling edge (single DAC updated)
t_{10}	10	ns min	$\overline{\text{LDAC}}$ pulse width low
t_{11}	500	ns max	$\overline{\text{LDAC}}$ falling edge to DAC output response time
t_{12}	See the AC Performance Characteristics section	μs max	DAC output settling time
t_{13}	10	ns min	CLEAR high time
t_{14}	5	μs max	CLEAR activation time
t_{15}	40	ns max	SCLK rising edge to SDO valid
t_{16}	5	μs min	$\overline{\text{SYNC}}$ rising edge to DAC output response time ($\overline{\text{LDAC}}$ = 0) (single DAC updated)
t_{17}	500	ns min	$\overline{\text{LDAC}}$ falling edge to $\overline{\text{SYNC}}$ rising edge
t_{18}	800	ns min	$\overline{\text{RESET}}$ pulse width
t_{19}	20	μs min	$\overline{\text{SYNC}}$ high to next $\overline{\text{SYNC}}$ low (digital slew rate control enabled) (single DAC updated)
	5	μs min	$\overline{\text{SYNC}}$ high to next $\overline{\text{SYNC}}$ low (digital slew rate control disabled) (single DAC updated)

[1] Guaranteed by design and characterization; not production tested.
[2] All input signals are specified with $t_{RISE} = t_{FALL} = 5$ ns (10% to 90% of DV_{DD}) and timed from a voltage level of 1.2 V.
[3] See Figure 3, Figure 4, Figure 6, and Figure 7.

Timing Diagrams

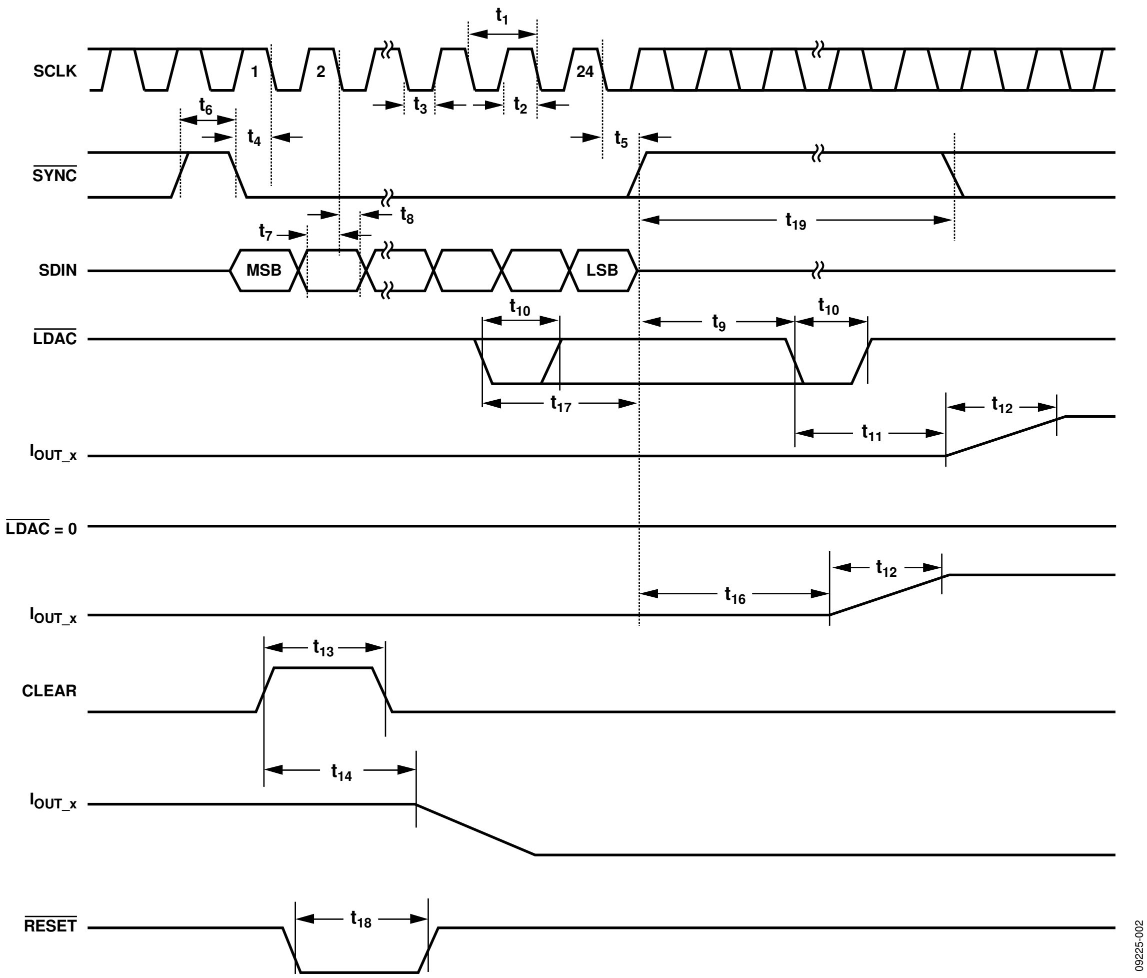


Figure 3. Serial Interface Timing Diagram

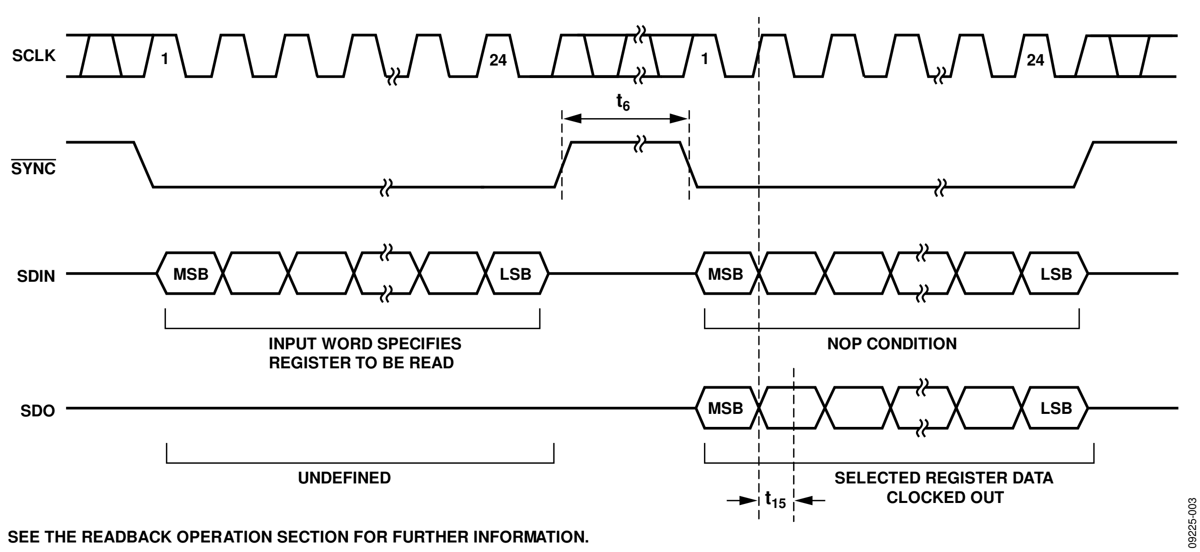


Figure 4. Readback Timing Diagram (Packet Error Checking Disabled)

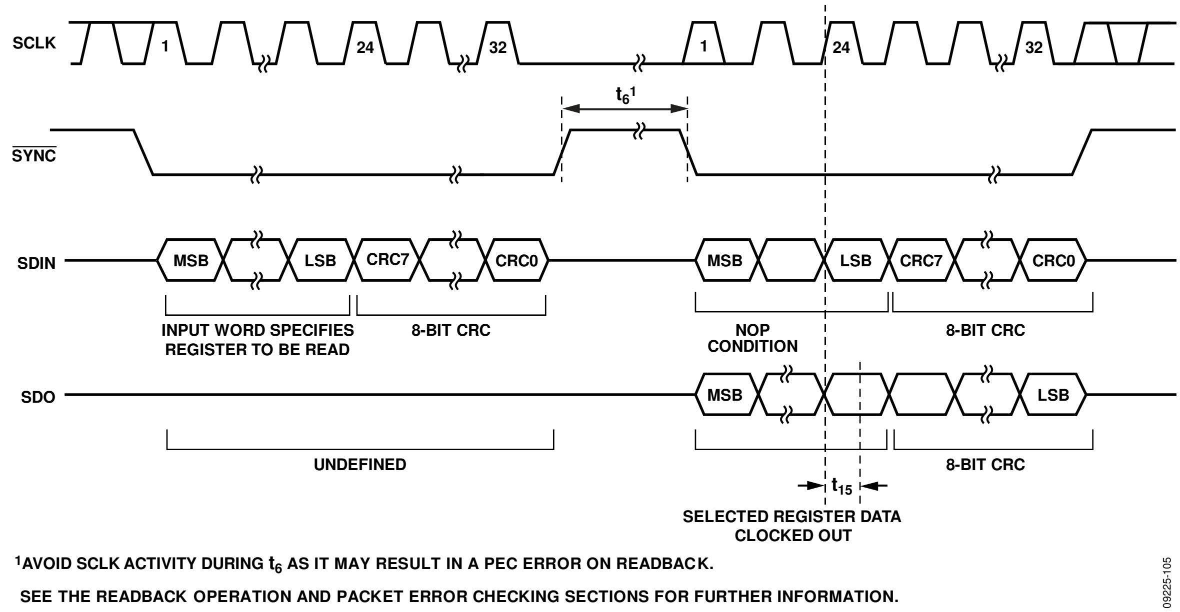


Figure 5. Readback Timing Diagram (Packet Error Checking Enabled)

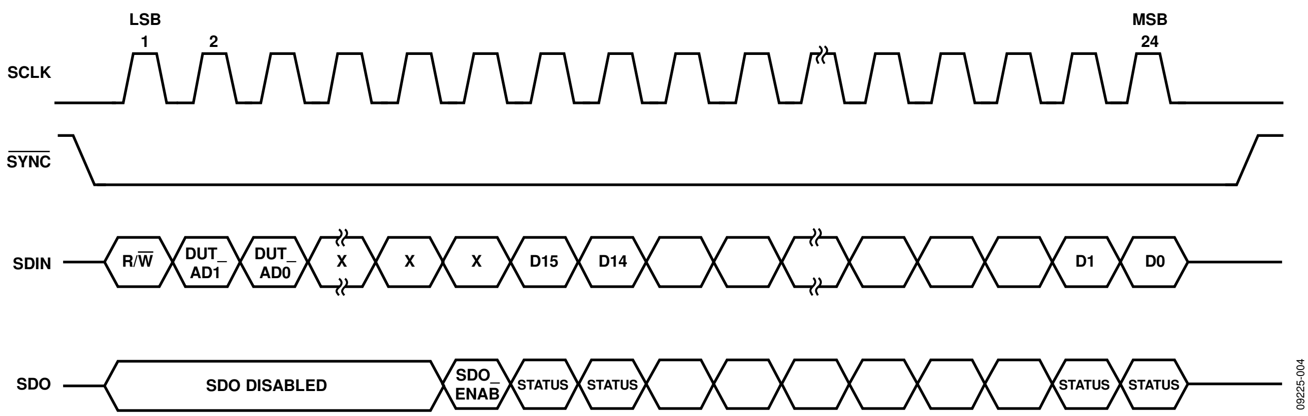


Figure 6. Status Readback During Write

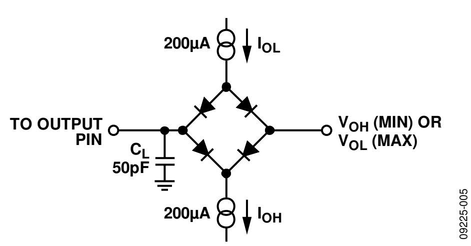


Figure 7. Load Circuit for SDO Timing Diagram

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted. Transient currents of up to 100 mA do not cause SCR latch-up.

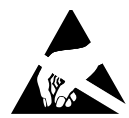
Table 4.

Parameter	Rating
AV_{DD}, V_{BOOST_x} to AGND, DGND	−0.3 V to +33 V
AV_{CC} to AGND	−0.3 V to +7 V
DV_{DD} to DGND	−0.3 V to +7 V
Digital Inputs to DGND	−0.3 V to DV_{DD} + 0.3 V or +7 V (whichever is less)
Digital Outputs to DGND	−0.3 V to DV_{DD} + 0.3 V or +7 V (whichever is less)
REFIN, REFOUT to AGND	−0.3 V to AV_{DD} + 0.3 V or +7 V (whichever is less)
I_{OUT_x} to AGND	AGND to V_{BOOST_x} or 33 V if using the dc-to-dc circuitry
SW_x to AGND	−0.3 V to +33 V
AGND, $GNDSW_x$ to DGND	−0.3 V to +0.3 V
Operating Temperature Range (T_A)	
Industrial[1]	−40°C to +105°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature (T_J max)	125°C
64-Lead LFCSP	
θ_{JA} Thermal Impedance[2]	28°C/W
Power Dissipation	(T_J max − T_A)/θ_{JA}
Lead Temperature	JEDEC industry standard
Soldering	J-STD-020

[1] Power dissipated on chip must be derated to keep the junction temperature below 125°C.
[2] Based on a JEDEC 4-layer test board.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

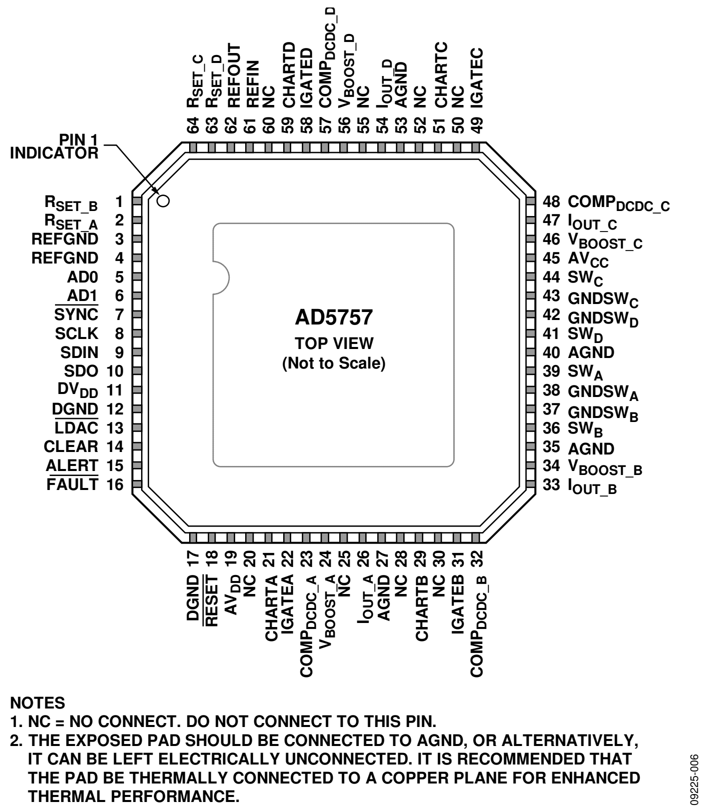


Figure 8. Pin Configuration

Table 5. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	R_{SET_B}	An external, precision, low drift 15 kΩ current setting resistor can be connected to this pin to improve the I_{OUT_B} temperature drift performance. See the Device Features section.
2	R_{SET_A}	An external, precision, low drift 15 kΩ current setting resistor can be connected to this pin to improve the I_{OUT_A} temperature drift performance. See the Device Features section.
3, 4	REFGND	Ground Reference Point for Internal Reference.
5	AD0	Address Decode for the Device Under Test (DUT) on the Board.
6	AD1	Address Decode for the DUT on the Board. It is not recommended to tie both AD1 and AD0 low when using PEC, see the Packet Error Checking section.
7	$\overline{\text{SYNC}}$	Active Low Input. This is the frame synchronization signal for the serial interface. While $\overline{\text{SYNC}}$ is low, data is transferred in on the falling edge of SCLK.
8	SCLK	Serial Clock Input. Data is clocked into the input shift register on the falling edge of SCLK. This pin operates at clock speeds of up to 30 MHz.
9	SDIN	Serial Data Input. Data must be valid on the falling edge of SCLK.
10	SDO	Serial Data Output. Used to clock data from the serial register in readback mode. See Figure 4 and Figure 6.
11	DV_{DD}	Digital Supply. The voltage range is from 2.7 V to 5.5 V.
12, 17	DGND	Digital Ground.
13	$\overline{\text{LDAC}}$	Load DAC, Active Low Input. This is used to update the DAC register and consequently the DAC outputs. When tied permanently low, the addressed DAC data register is updated on the rising edge of $\overline{\text{SYNC}}$. If $\overline{\text{LDAC}}$ is held high during the write cycle, the DAC input register is updated, but the DAC output update only takes place at the falling edge of $\overline{\text{LDAC}}$ (see Figure 3). Using this mode, all analog outputs can be updated simultaneously. The $\overline{\text{LDAC}}$ pin must not be left unconnected.
14	CLEAR	Active High, Edge Sensitive Input. Asserting this pin sets the output current and voltage to the preprogrammed clear code bit setting. Only channels enabled to be cleared are cleared. See the Device Features section for more information. When CLEAR is active, the DAC output register cannot be written to.

Pin No.	Mnemonic	Description
15	ALERT	Active High Output. This pin is asserted when there has been no SPI activity on the interface pins for a predetermined time. See the Device Features section for more information.
16	$\overline{\text{FAULT}}$	Active Low Output. This pin is asserted low when an open circuit in current mode is detected, a short circuit in voltage mode is detected, a PEC error is detected, or an overtemperature is detected (see the Device Features section). Open-drain output.
18	$\overline{\text{RESET}}$	Hardware Reset. Active Low Input.
19	AV$_{DD}$	Positive Analog Supply. The voltage range is from 10.8 V to 33 V.
20, 25, 28, 30, 50, 52, 55, 60	NC	No Connect. Do not connect to this pin.
21	CHARTA	HART Input Connection for DAC Channel A. For more information, see the HART section. If unused, leave as an open circuit.
22	IGATEA	Optional Connection for External Pass Transistor. Leave unconnected when using the dc-to-dc converter. See the External PMOS Mode section for more information.
23	COMP$_{DCDC_A}$	DC-to-DC Compensation Capacitor. Connect a 10 nF capacitor from this pin to ground. Used to regulate the feedback loop of the Channel A dc-to-dc converter. Alternatively, if using an external compensation resistor, place a resistor in series with a capacitor to ground from this pin (see the DC-to-DC Converter Compensation Capacitors and the AICC Supply Requirements—Slewing sections in the Device Features section for more information).
24	V$_{BOOST_A}$	Supply for Channel A Current Output Stage (see Figure 50). To use the dc-to-dc feature of the device, connect as shown in Figure 57.
26	I$_{OUT_A}$	Current Output Pin for DAC Channel A.
27, 40, 53	AGND	Ground Reference Point for Analog Circuitry. This must be connected to 0 V.
29	CHARTB	HART Input Connection for DAC Channel B. For more information, see the HART section. If unused, leave as an open circuit.
31	IGATEB	Optional Connection for External Pass Transistor. Leave unconnected when using the dc-to-dc converter. See the External PMOS Mode section for more information.
32	COMP$_{DCDC_B}$	DC-to-DC Compensation Capacitor. Connect a 10 nF capacitor from this pin to ground. Used to regulate the feedback loop of the Channel B dc-to-dc converter. Alternatively, if using an external compensation resistor, place a resistor in series with a capacitor to ground from this pin (see the DC-to-DC Converter Compensation Capacitors and AI$_{CC}$ Supply Requirements—Slewing sections in the Device Features section for more information).
33	I$_{OUT_B}$	Current Output Pin for DAC Channel B.
34	V$_{BOOST_B}$	Supply for Channel B Current Output Stage (see Figure 50). To use the dc-to-dc feature of the device, connect as shown in Figure 57.
35	AGND	Ground Reference Point for Analog Circuitry. This pin must be connected to 0 V.
36	SW$_B$	Switching Output for Channel B DC-to-DC Circuitry. To use the dc-to-dc feature of the device, connect as shown in Figure 57.
37	GNDSW$_B$	Ground Connection for DC-to-DC Switching Circuit. This pin must always be connected to ground.
38	GNDSW$_A$	Ground Connection for DC-to-DC Switching Circuit. This pin must always be connected to ground.
39	SW$_A$	Switching Output for Channel A DC-to-DC Circuitry. To use the dc-to-dc feature of the device, connect as shown in Figure 57.
41	SW$_D$	Switching Output for Channel D DC-to-DC Circuitry. To use the dc-to-dc feature of the device, connect as shown in Figure 57.
42	GNDSW$_D$	Ground Connections for DC-to-DC Switching Circuit. This pin must always be connected to ground.
43	GNDSW$_C$	Ground Connections for DC-to-DC Switching Circuit. This pin must always be connected to ground.
44	SW$_C$	Switching Output for Channel C DC-to-DC Circuitry. To use the dc-to-dc feature of the device, connect as shown in Figure 57.
45	AV$_{CC}$	Supply for DC-to-DC Circuitry.
46	V$_{BOOST_C}$	Supply for Channel C Current Output Stage (see Figure 50). To use the dc-to-dc feature of the device, connect as shown in Figure 57.
47	I$_{OUT_C}$	Current Output Pin for DAC Channel C.
48	COMP$_{DCDC_C}$	DC-to-DC Compensation Capacitor. Connect a 10 nF capacitor from this pin to ground. Used to regulate the feedback loop of the Channel C dc-to-dc converter. Alternatively, if using an external compensation resistor, place a resistor in series with a capacitor to ground from this pin (see the DC-to-DC Converter Compensation Capacitors and AICC Supply Requirements—Slewing sections in the Device Features section for more information).

Pin No.	Mnemonic	Description
49	IGATEC	Optional Connection for External Pass Transistor. Leave unconnected when using the dc-to-dc converter. See the External PMOS Mode section for more information.
51	CHARTC	HART Input Connection for DAC Channel C. For more information, see the HART section. If unused, leave as an open circuit.
54	I_{OUT_D}	Current Output Pin for DAC Channel D.
56	V_{BOOST_D}	Supply for Channel D Current Output Stage (see Figure 50). To use the dc-to-dc feature of the device, connect as shown in Figure 57.
57	$COMP_{DCDC\_D}$	DC-to-DC Compensation Capacitor. Connect a 10 nF capacitor from this pin to ground. Used to regulate the feedback loop of the Channel D dc-to-dc converter. Alternatively, if using an external compensation resistor, place a resistor in series with a capacitor to ground from this pin (see the DC-to-DC Converter Compensation Capacitors and AI_{CC} Supply Requirements—Slewing sections in t section for more information).
58	IGATED	Optional Connection for External Pass Transistor. Leave unconnected when using the dc-to-dc converter. See the External PMOS Mode section for more information.
59	CHARTD	HART Input Connection for DAC Channel D. For more information, see the HART section. If unused, leave as an open circuit.
61	REFIN	External Reference Voltage Input.
62	REFOUT	Internal Reference Voltage Output. It is recommended to place a 0.1 µF capacitor between REFOUT and REFGND. REFOUT must be connected to REFIN to use the internal reference.
63	R_{SET_D}	An external, precision, low drift 15 kΩ current setting resistor can be connected to this pin to improve the I_{OUT_D} temperature drift performance. See the Device Features section.
64	R_{SET_C}	An external, precision, low drift 15 kΩ current setting resistor can be connected to this pin to improve the I_{OUT_C} temperature drift performance. See the Device Features section.
	EPAD	Exposed Pad. This exposed pad must be connected to AGND, or, alternatively, it can be left electrically unconnected. It is recommended that the pad be thermally connected to a copper plane for enhanced thermal performance.

TYPICAL PERFORMANCE CHARACTERISTICS

CURRENT OUTPUTS

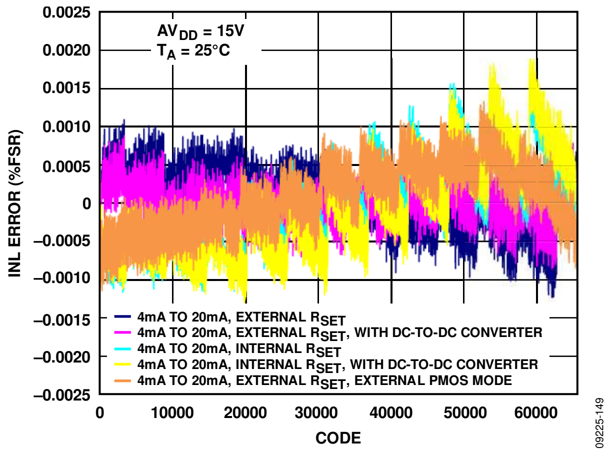


Figure 9. Integral Nonlinearity vs. Code

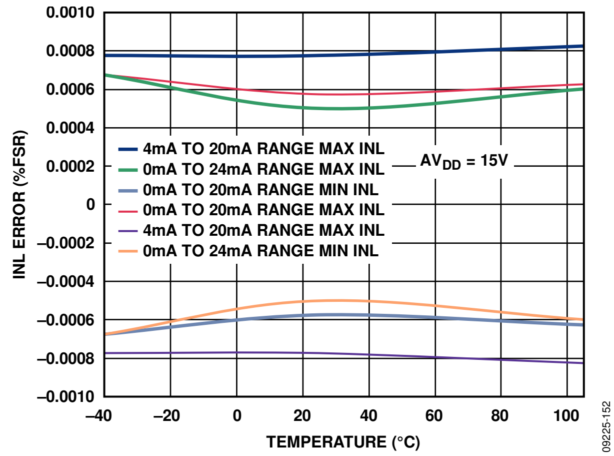


Figure 12. Integral Nonlinearity vs. Temperature, Internal R_{SET}

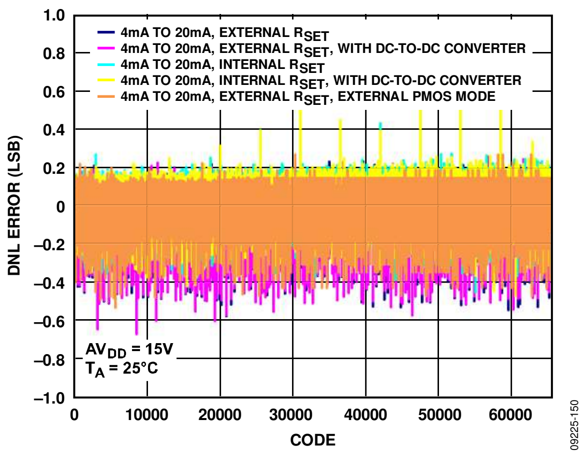


Figure 10. Differential Nonlinearity vs. Code

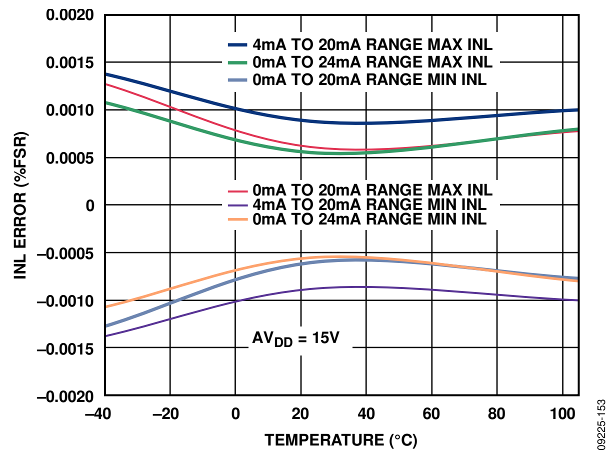


Figure 13. Integral Nonlinearity vs. Temperature, External R_{SET}

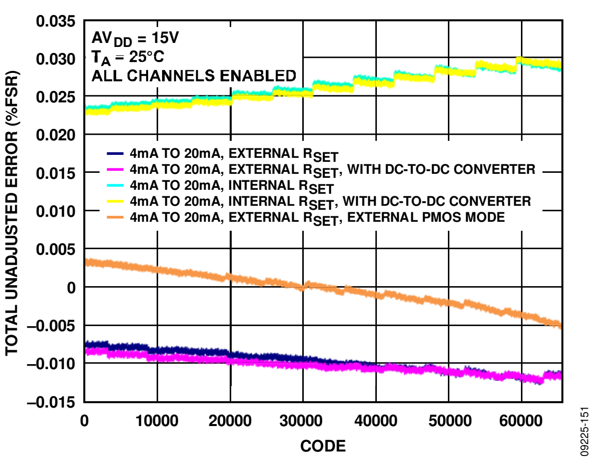


Figure 11. Total Unadjusted Error vs. Code

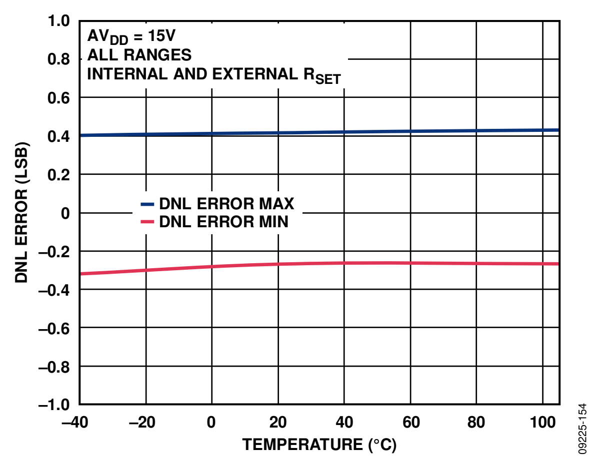


Figure 14. Differential Nonlinearity vs. Temperature

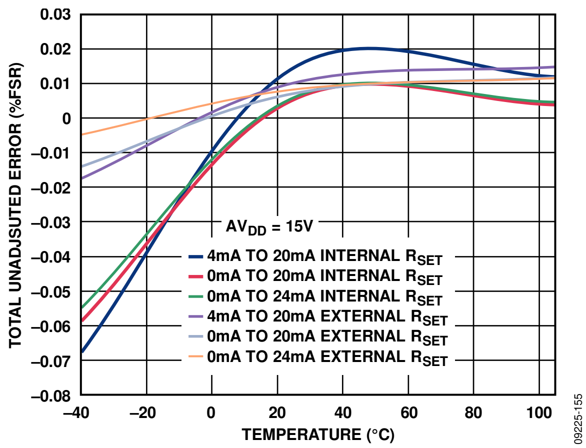


Figure 15. Total Unadjusted Error vs. Temperature

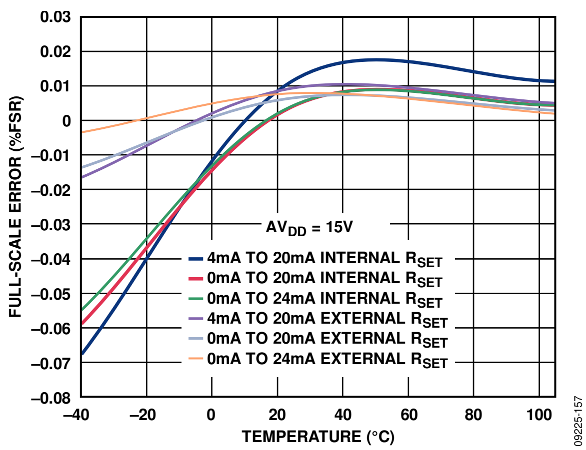


Figure 16. Full-Scale Error vs. Temperature

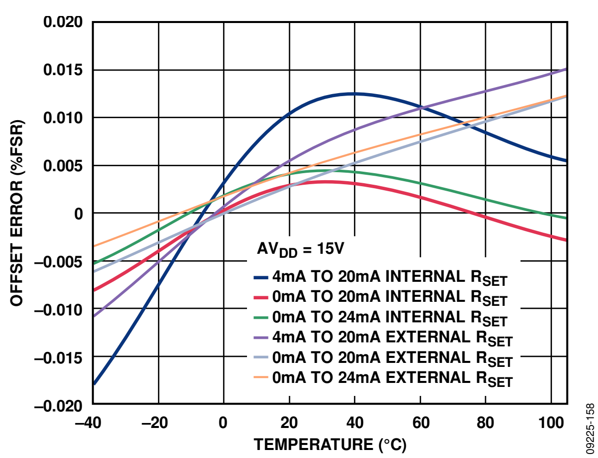


Figure 17. Offset Error vs. Temperature

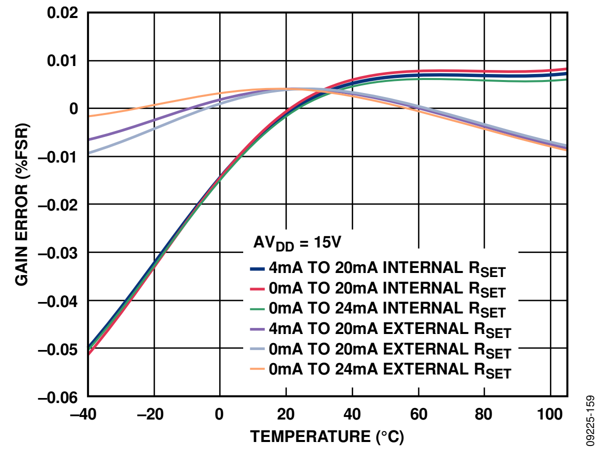


Figure 18. Gain Error vs. Temperature

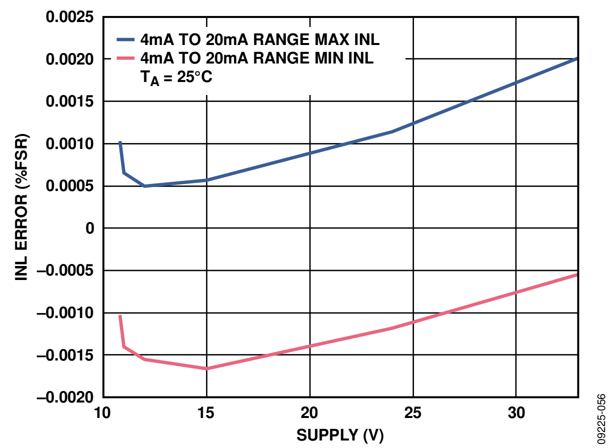


Figure 19. Integral Nonlinearity Error vs. AV_{DD}, Over Supply, External R_{SET}

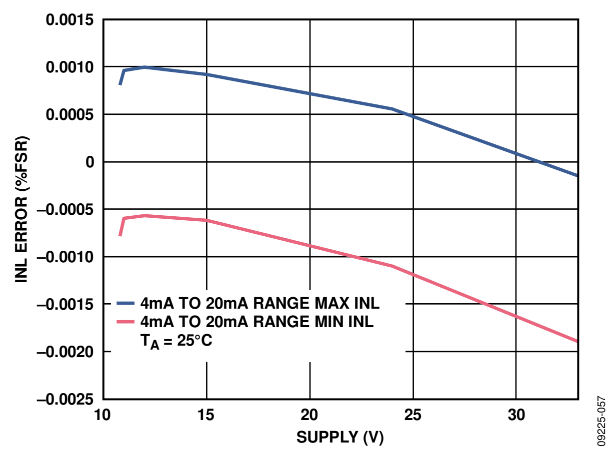


Figure 20. Integral Nonlinearity Error vs. AV_{DD}, Over Supply, Internal R_{SET}

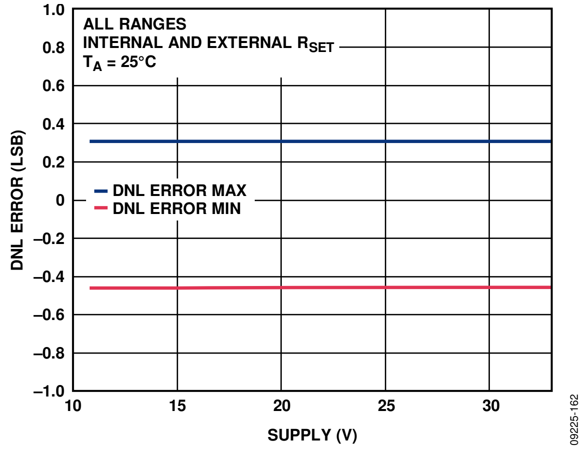


Figure 21. Differential Nonlinearity Error vs. AV_{DD}

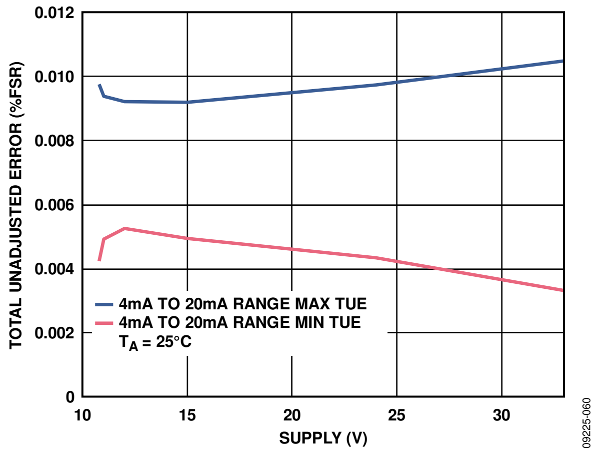


Figure 22. Total Unadjusted Error vs. AV_{DD}, External R_{SET}

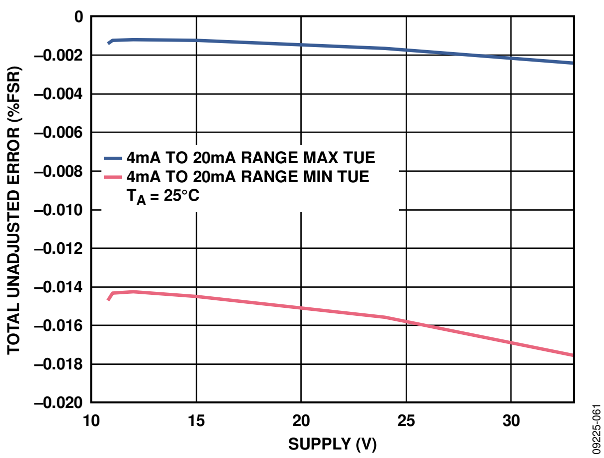


Figure 23. Total Unadjusted Error vs. AV_{DD}, Internal R_{SET}

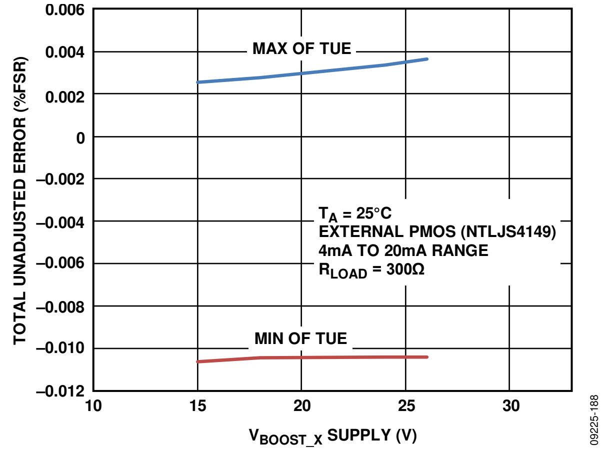


Figure 24. Total Unadjusted Error vs. V_{BOOST_x}, Using External PMOS Mode

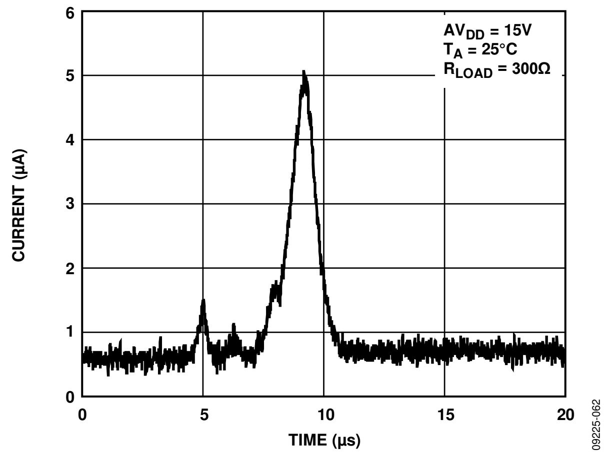


Figure 25. Output Current vs. Time on Power-Up

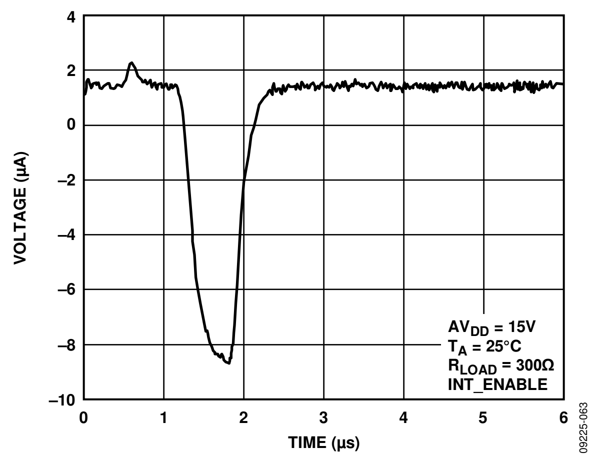


Figure 26. Output Current vs. Time on Output Enable

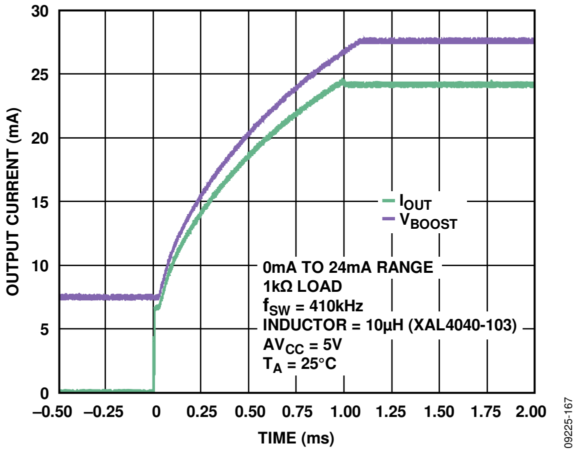


Figure 27. Output Current and V_{BOOST_x} Settling Time with DC-to-DC Converter (See Figure 57)

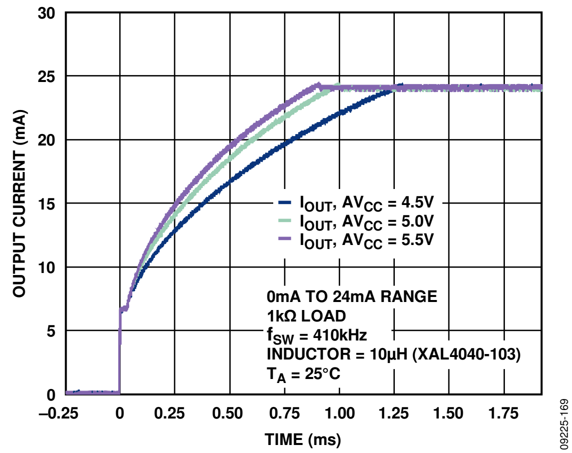


Figure 29. Output Current Settling with DC-to-DC Converter vs. Time and AV_{CC} (See Figure 57)

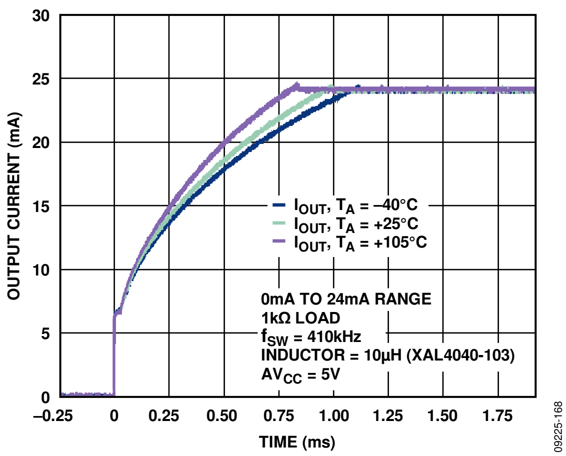


Figure 28. Output Current Settling with DC-to-DC Converter vs. Time and Temperature (See Figure 57)

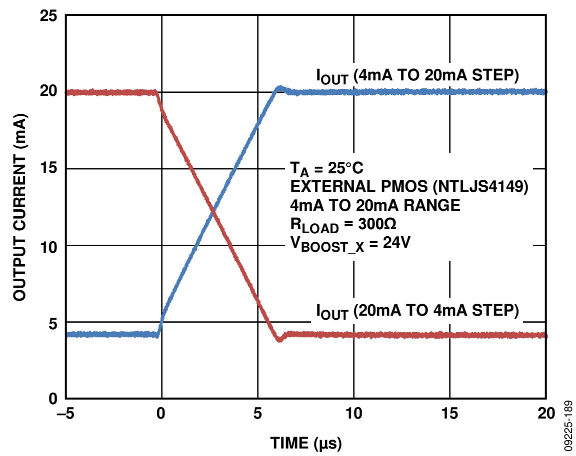


Figure 30. Output Current Settling Time with External PMOS Transistor

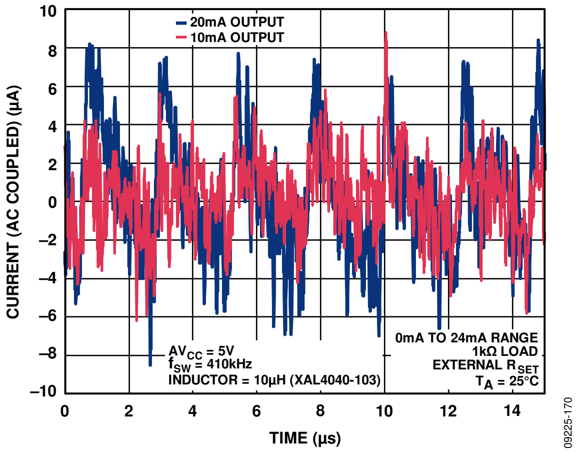


Figure 31. Output Current vs. Time with DC-to-DC Converter (See Figure 57)

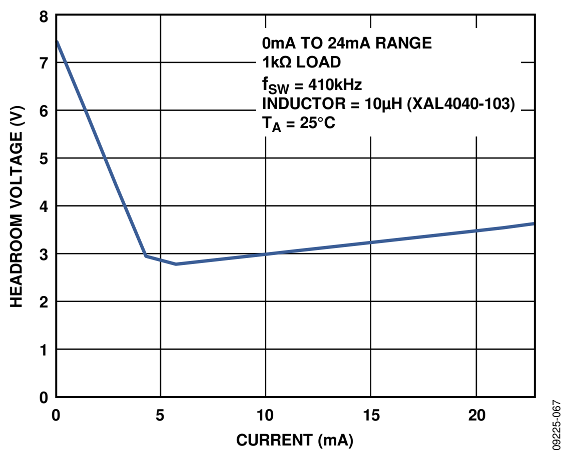


Figure 32. DC-to-DC Converter Headroom vs. Output Current (See Figure 57)

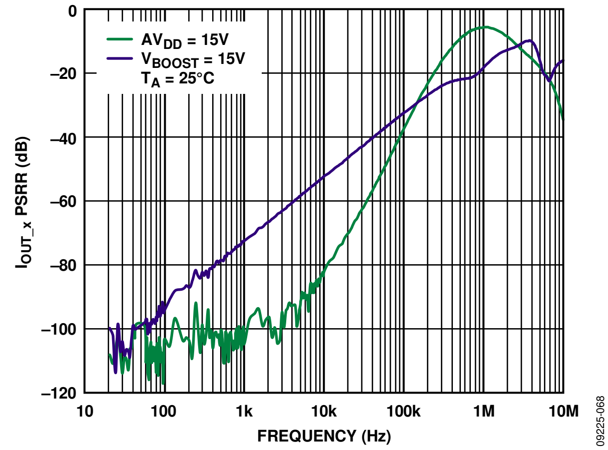


Figure 33. I_{OUT_x} PSRR vs. Frequency

DC-TO-DC BLOCK

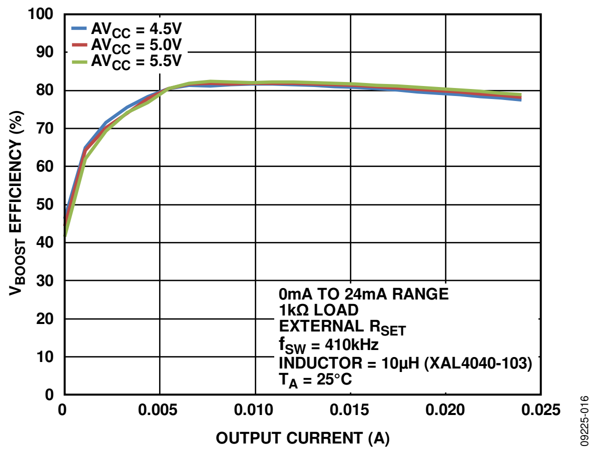


Figure 34. Efficiency at V_{BOOST_x} vs. Output Current (See Figure 57)

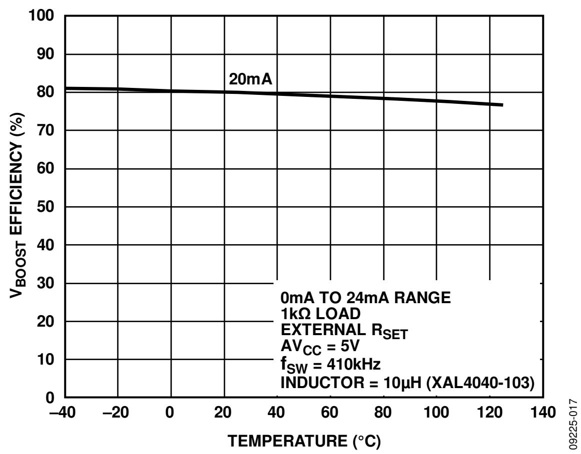


Figure 35. Efficiency at V_{BOOST_x} vs. Temperature (See Figure 57)

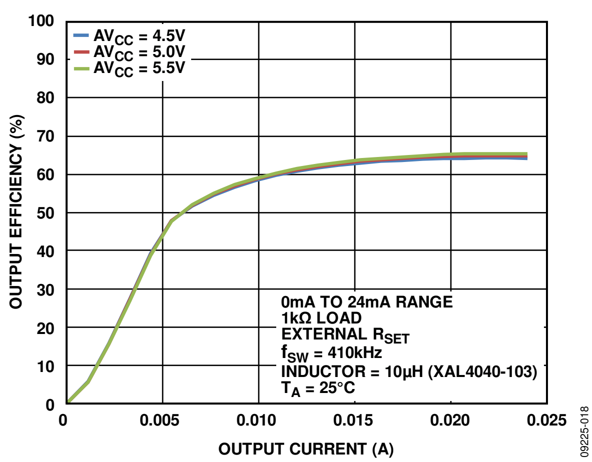


Figure 36. Output Efficiency vs. Output Current (See Figure 57)

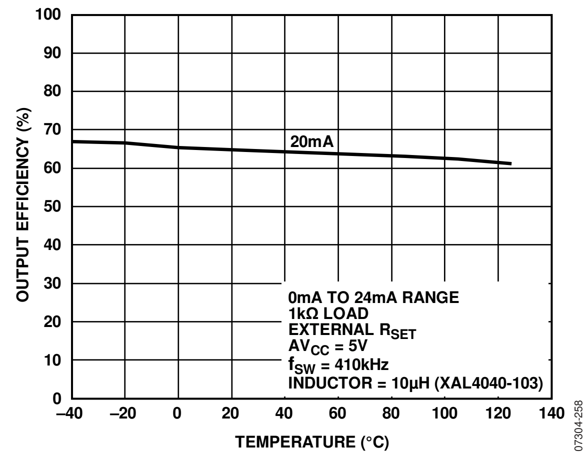


Figure 37. Output Efficiency vs. Temperature (See Figure 57)

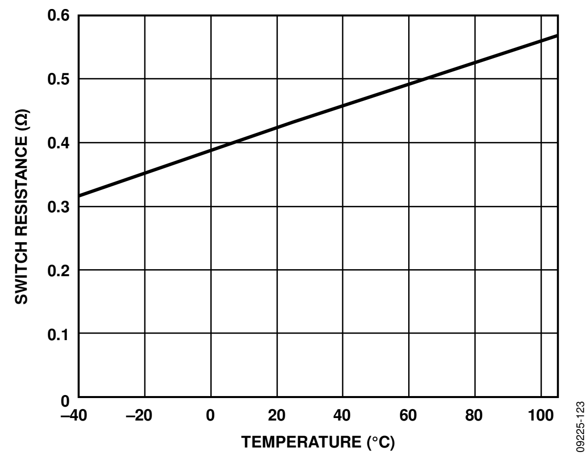


Figure 38. Switch Resistance vs. Temperature

REFERENCE

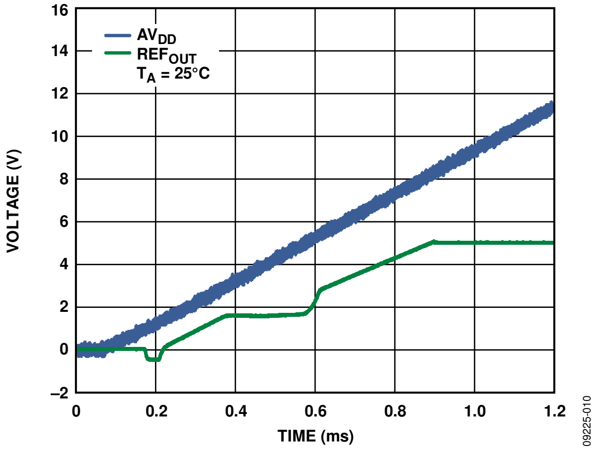


Figure 39. REFOUT Turn-On Transient

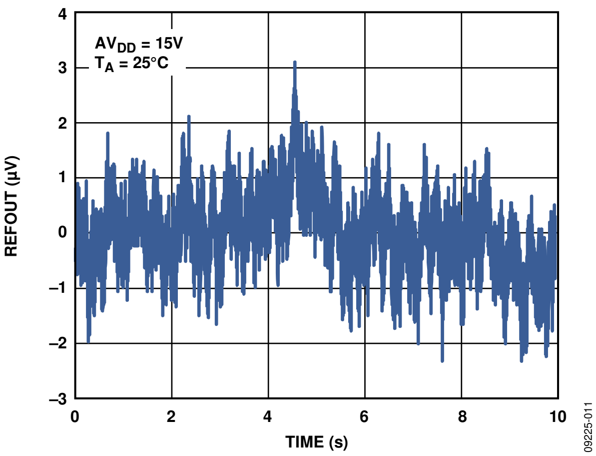


Figure 40. REFOUT Output Noise (0.1 Hz to 10 Hz Bandwidth)

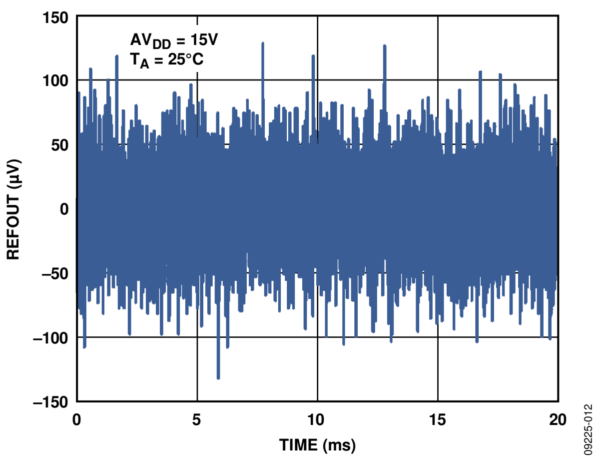


Figure 41. REFOUT Output Noise (100 kHz Bandwidth)

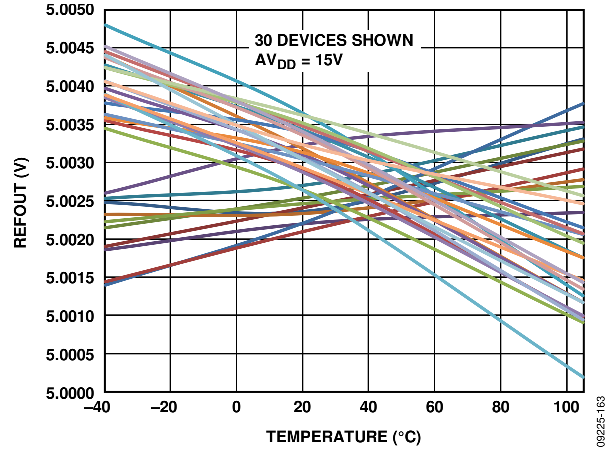


Figure 42. REFOUT vs. Temperature (When the AD5757 is soldered onto a PCB, the reference shifts due to thermal shock on the package. The average output voltage shift is –4 mV. Measurement of these parts after seven days shows that the outputs typically shift back 2 mV toward their initial values. This second shift is due to the relaxation of stress incurred during soldering.)

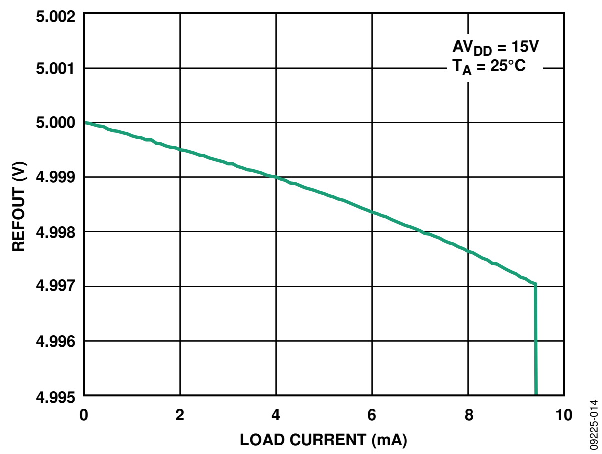


Figure 43. REFOUT vs. Load Current

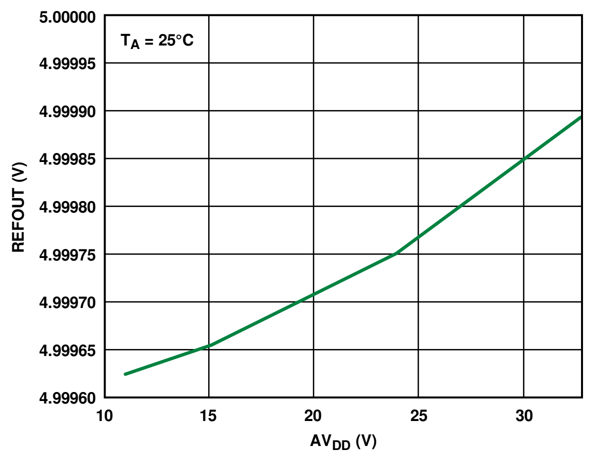


Figure 44. REFOUT vs. Supply

GENERAL

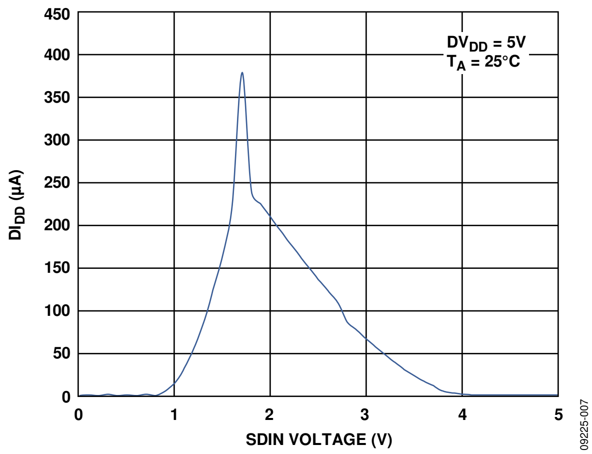


Figure 45. DI_{CC} vs. Logic Input Voltage

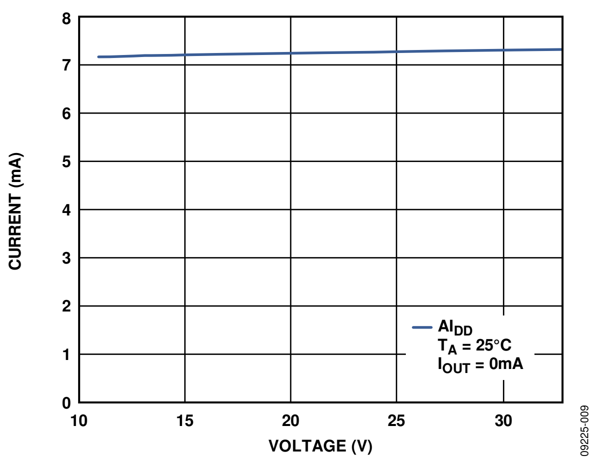


Figure 46. AI_{DD} vs. AV_{DD}

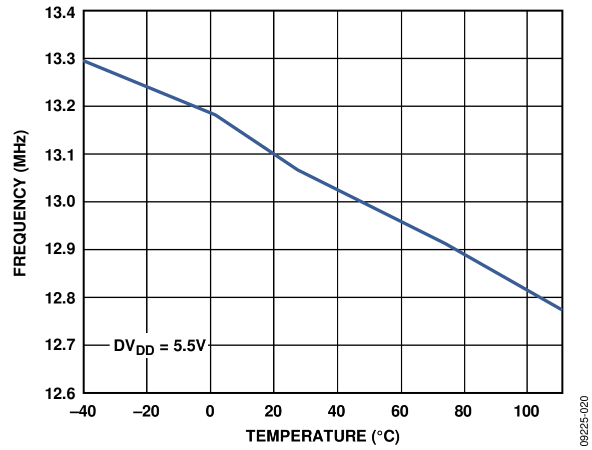


Figure 47. Internal Oscillator Frequency vs. Temperature

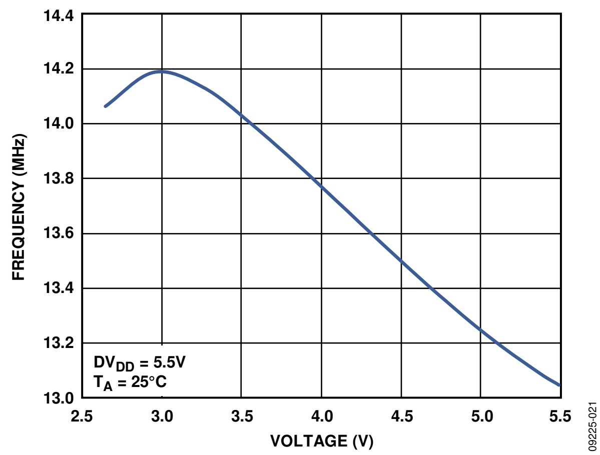


Figure 48. Internal Oscillator Frequency vs. DV_{DD} Supply Voltage

TERMINOLOGY

Relative Accuracy or Integral Nonlinearity (INL)

For the DAC, relative accuracy, or integral nonlinearity, is a measure of the maximum deviation, in LSBs, from the best fit line through the DAC transfer function. A typical INL vs. code plot is shown in Figure 9.

Differential Nonlinearity (DNL)

Differential nonlinearity (DNL) is the difference between the measured change and the ideal 1 LSB change between any two adjacent codes. A specified differential nonlinearity of ±1 LSB maximum ensures monotonicity. This DAC is guaranteed monotonic by design. A typical DNL vs. code plot is shown in Figure 10.

Monotonicity

A DAC is monotonic if the output either increases or remains constant for increasing digital input code. The AD5757 is monotonic over its full operating temperature range.

Offset Error

Offset error is the deviation of the analog output from the ideal zero-scale output when all DAC registers are loaded with 0x0000.

Gain Error

This is a measure of the span error of the DAC. It is the deviation in slope of the DAC transfer characteristic from the ideal, expressed in % FSR.

Gain TC

This is a measure of the change in gain error with changes in temperature. Gain TC is expressed in ppm FSR/°C.

Full-Scale Error

Full-scale error is a measure of the output error when full-scale code is loaded to the DAC register. Ideally, the output is full-scale − 1 LSB. Full-scale error is expressed in percent of full-scale range (% FSR).

Full-Scale TC

Full-scale TC is a measure of the change in full-scale error with changes in temperature and is expressed in ppm FSR/°C.

Total Unadjusted Error

Total unadjusted error (TUE) is a measure of the output error taking all the various errors into account, including INL error, offset error, gain error, temperature, and time. TUE is expressed in % FSR.

DC Crosstalk

This is the dc change in the output level of one DAC in response to a change in the output of another DAC. It is measured with a full-scale output change on one DAC while monitoring another DAC, which is at midscale.

Current Loop Compliance Voltage

The maximum voltage at the I_{OUT_x} pin for which the output current is equal to the programmed value.

Voltage Reference Thermal Hysteresis

Voltage reference thermal hysteresis is the difference in output voltage measured at +25°C compared to the output voltage measured at +25°C after cycling the temperature from +25°C to −40°C to +105°C and back to +25°C. The hysteresis is expressed in ppm.

Power-On Glitch Energy

Power-on glitch energy is the impulse injected into the analog output when the AD5757 is powered-on. It is specified as the area of the glitch in nV-sec. See Figure 25.

Power Supply Rejection Ratio (PSRR)

PSRR indicates how the output of the DAC is affected by changes in the power supply voltage.

Reference TC

Reference TC is a measure of the change in the reference output voltage with a change in temperature. It is expressed in ppm/°C.

Line Regulation

Line regulation is the change in reference output voltage due to a specified change in supply voltage. It is expressed in ppm/V.

Load Regulation

Load regulation is the change in reference output voltage due to a specified change in load current. It is expressed in ppm/mA.

DC-to-DC Converter Headroom

This is the difference between the voltage required at the current output and the voltage supplied by the dc-to-dc converter. See Figure 32.

Output Efficiency

$$\frac{I_{OUT}^2 \times R_{LOAD}}{AV_{CC} \times AI_{CC}}$$

This is defined as the power delivered to a channel's load vs. the power delivered to the channel's dc-to-dc input.

Efficiency at V_{BOOST_x}

$$\frac{I_{OUT} \times V_{BOOST\_x}}{AV_{CC} \times AI_{CC}}$$

This is defined as the power delivered to a channel's V_{BOOST_x} supply vs. the power delivered to the channel's dc-to-dc input. The V_{BOOST_x} quiescent current is considered part of the dc-to-dc converter's losses.

THEORY OF OPERATION

The AD5757 is a quad, precision digital-to-current loop converter designed to meet the requirements of industrial process control applications. It provides a high precision, fully integrated, low cost, single-chip solution for generating current loop outputs. The current ranges available are 0 mA to 20 mA, 0 mA to 24 mA, and 4 mA to 20 mA. The desired output configuration is user selectable via the DAC control register.

On-chip dynamic power control minimizes package power dissipation in current mode.

DAC ARCHITECTURE

The DAC core architecture of the AD5757 consists of two matched DAC sections. A simplified circuit diagram is shown in Figure 49. The four MSBs of the 16-bit data-word are decoded to drive 15 switches, E1 to E15. Each of these switches connects one of 15 matched resistors to either ground or the reference buffer output. The remaining 12 bits of the data-word drive Switch S0 to Switch S11 of a 12-bit voltage mode R-2R ladder network.

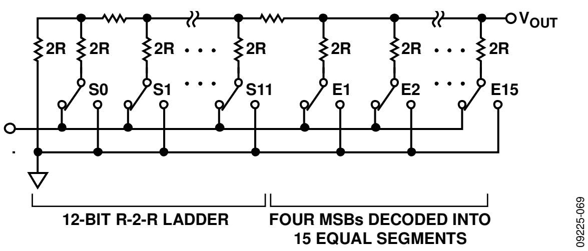


Figure 49. DAC Ladder Structure

The voltage output from the DAC core is converted to a current (see Figure 50), which is then mirrored to the supply rail so that the application simply sees a current source output. The current outputs are supplied by V_{BOOST_x}.

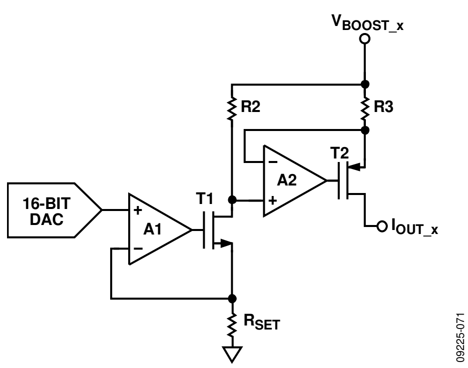


Figure 50. Voltage-to-Current Conversion Circuitry

Reference Buffers

The AD5757 can operate with either an external or internal reference. The reference input requires a 5 V reference for specified performance. This input voltage is then buffered before it is applied to the DAC.

POWER-ON STATE OF THE AD5757

On power-up of the AD5757, the I_{OUT_x} pins are in tristate mode.

After device power-on or a device reset, it is recommended to wait 100 µs or more before writing to the device to allow time for internal calibrations to take place.

SERIAL INTERFACE

The AD5757 is controlled over a versatile 3-wire serial interface that operates at clock rates of up to 30 MHz and is compatible with SPI, QSPI, MICROWIRE, and DSP standards. Data coding is always straight binary.

Input Shift Register

The input shift register is 24 bits wide. Data is loaded into the device MSB first as a 24-bit word under the control of a serial clock input, SCLK. Data is clocked in on the falling edge of SCLK.

If packet error checking, or PEC (see the Device Features section), is enabled, an additional eight bits must be written to the AD5757, creating a 32-bit serial interface.

There are two ways in which the DAC outputs can be updated: individual updating or simultaneous updating of all DACs.

Individual DAC Updating

In this mode, $\overline{\text{LDAC}}$ is held low while data is being clocked into the DAC data register. The addressed DAC output is updated on the rising edge of $\overline{\text{SYNC}}$. See Table 3 and Figure 3 for timing information.

Simultaneous Updating of All DACs

In this mode, $\overline{\text{LDAC}}$ is held high while data is being clocked into the DAC data register. Only the first write to each channel's DAC data register is valid after $\overline{\text{LDAC}}$ is brought high. Any subsequent writes while $\overline{\text{LDAC}}$ is still held high are ignored, although they are loaded into the DAC data register. All the DAC outputs are updated by taking $\overline{\text{LDAC}}$ low after $\overline{\text{SYNC}}$ is taken high.

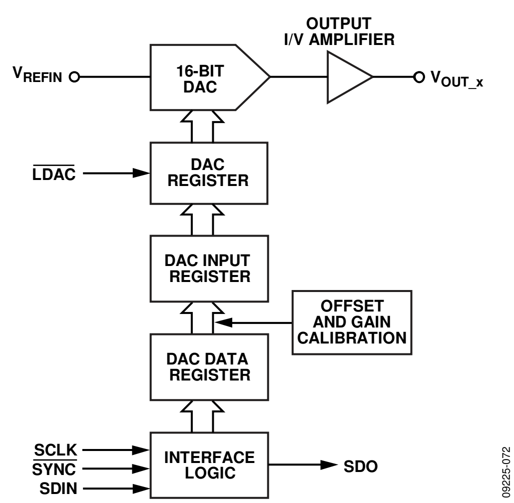


Figure 51. Simplified Serial Interface of Input Loading Circuitry for One DAC Channel

TRANSFER FUNCTION

For the 0 mA to 20 mA, 0 mA to 24 mA, and 4 mA to 20 mA current output ranges, the output current is respectively expressed as

$$I_{OUT} = \left[\frac{20\text{ mA}}{2^N}\right] \times D$$

$$I_{OUT} = \left[\frac{24\text{ mA}}{2^N}\right] \times D$$

$$I_{OUT} = \left[\frac{16\text{ mA}}{2^N}\right] \times D + 4\text{ mA}$$

where:
D is the decimal equivalent of the code loaded to the DAC.
N is the bit resolution of the DAC.

REGISTERS

Table 6 shows an overview of the registers for the AD5757.

Table 6. Data, Control, and Readback Registers for the AD5757

Register	Description
Data	
DAC Data Register (×4)	Used to write a DAC code to each DAC channel. AD5757 data bits = D15 to D0. There are four DAC data registers, one per DAC channel.
Gain Register (×4)	Used to program gain trim, on a per channel basis. AD5757 data bits = D15 to D0. There are four gain registers, one per DAC channel.
Offset Register (×4)	Used to program offset trim, on a per channel basis. AD5757 data bits = D15 to D0. There are four offset registers, one per DAC channel.
Clear Code Register (×4)	Used to program clear code on a per channel basis. AD5757 data bits = D15 to D0. There are four clear code registers, one per DAC channel.
Control	
Main Control Register	Used to configure the part for main operation. Sets functions such as status readback during write, enables output on all channels simultaneously, powers on all dc-to-dc converter blocks simultaneously, and enables and sets conditions of the watchdog timer. See the Device Features section for more details.
Software Register	Has three functions. Used to perform a reset, to toggle the user bit and, as part of the watchdog timer feature, to verify correct data communication operation.
Slew Rate Control Register (×4)	Used to program the slew rate of the output. There are four slew rate control registers, one per channel.
DAC Control Register (×4)	These registers are used to control the following:
	Set the output range, for example, 4 mA to 20 mA.
	Set whether an internal/external sense resistor is used.
	Enable/disable a channel for CLEAR.
	Enable/disable internal circuitry on a per channel basis.
	Enable/disable output on a per channel basis.
	Power on dc-to-dc converters on a per channel basis.
	There are four DAC control registers, one per DAC channel.
DC-to-DC Control Register	Use to set the dc-to-dc control parameters. Can control dc-to-dc maximum voltage, phase, and frequency.
Readback	
Status Register	This contains any fault information, as well as a user toggle bit.

PROGRAMMING SEQUENCE TO WRITE/ENABLE THE OUTPUT CORRECTLY

To correctly write to and set up the part from a power-on condition, use the following sequence:

1. Perform a hardware or software reset after initial power-on.
2. The dc-to-dc converter supply block must be configured. Set the dc-to-dc switching frequency, maximum output voltage allowed, and the phase that the four dc-to-dc channels clock at.
3. Configure the DAC control register on a per channel basis. The output range is selected, and the dc-to-dc converter block is enabled (DC_DC bit). Other control bits can be configured at this point. Set the INT_ENABLE bit; however, do not set the output enable bit (OUTEN).
4. Write the required code to the DAC data register. This implements a full DAC calibration internally. Allow at least 200 μs before Step 5 for reduced output glitch.
5. Write to the DAC control register again to enable the output (set the OUTEN bit).

A flowchart of this sequence is shown in Figure 52.

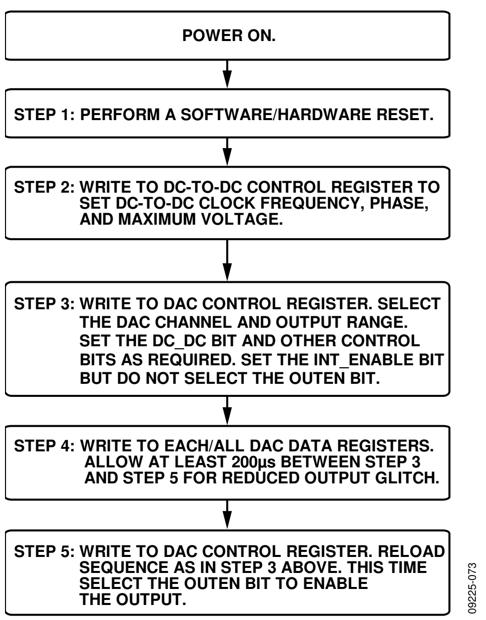


Figure 52. Programming Sequence for Enabling the Output Correctly

CHANGING AND REPROGRAMMING THE RANGE

When changing between ranges, the same sequence as described in the Programming Sequence to Write/Enable the Output Correctly section should be used. It is recommended to set the range to zero scale prior to disabling the output. Because the dc-to-dc switching frequency, maximum voltage, and phase are already selected, there is no need to reprogram these. A flowchart of this sequence is shown in Figure 53.

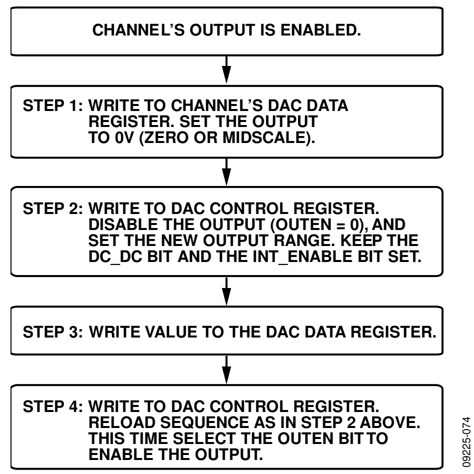


Figure 53. Steps for Changing the Output Range

DATA REGISTERS

The input register is 24 bits wide. When PEC is enabled, the input register is 32 bits wide, with the last eight bits corresponding to the PEC code (see the Packet Error Checking section for more information on PEC). When writing to a data register, the format in Table 7 must be used.

DAC Data Register

When writing to the AD5757 DAC data registers, D15 to D0 are used for the DAC data bits. Table 9 shows the register format and Table 8 describes the function of Bit D23 to Bit D16.

Table 7. Writing to a Data Register

MSB → LSB

D23	D22	D21	D20	D19	D18	D17	D16	D15 to D0
R/$\overline{W}$	DUT_AD1	DUT_AD0	DREG2	DREG1	DREG0	DAC_AD1	DAC_AD0	Data

Table 8. Input Register Decode

Bit	Description
R/$\overline{W}$	Indicates a read from or a write to the addressed register.
DUT_AD1, DUT_AD0	Used in association with the external pins, AD1 and AD0, to determine which AD5757 device is being addressed by the system controller. It is not recommended to tie both AD1 and AD0 low when using PEC (see the Packet Error Checking section).

DUT_AD1	DUT_AD0	Function
0	0	Addresses part with Pin AD1 = 0, Pin AD0 = 0
0	1	Addresses part with Pin AD1 = 0, Pin AD0 = 1
1	0	Addresses part with Pin AD1 = 1, Pin AD0 = 0
1	1	Addresses part with Pin AD1 = 1, Pin AD0 = 1

Bit	Description
DREG2, DREG1, DREG0	Selects whether a data register or a control register is written to. If a control register is selected, a further decode of CREG bits (see Table 16) is required to select the particular control register, as follows.

DREG2	DREG1	DREG0	Function
0	0	0	Write to DAC data register (individual channel write)
0	1	0	Write to gain register
0	1	1	Write to gain register (all DACs)
1	0	0	Write to offset register
1	0	1	Write to offset register (all DACs)
1	1	0	Write to clear code register
1	1	1	Write to a control register

Bit	Description
DAC_AD1, DAC_AD0	These bits are used to decode the DAC channel.

DAC_AD1	DAC_AD0	DAC Channel/Register Address
0	0	DAC A
0	1	DAC B
1	0	DAC C
1	1	DAC D
X	X	These are don't cares if they are not relevant to the operation being performed.

Table 9. Programming the DAC Data Registers

MSB → LSB

D23	D22	D21	D20	D19	D18	D17	D16	D15 to D0
R/$\overline{W}$	DUT_AD1	DUT_AD0	DREG2	DREG1	DREG0	DAC_AD1	DAC_AD0	DAC data

Gain Register

The 16-bit gain register, as shown in Table 10, allows the user to adjust the gain of each channel in steps of 1 LSB. This is done by setting the DREG[2:0] bits to 010. It is possible to write the same gain code to all four DAC channels at the same time by setting the DREG[2:0] bits to 011. The gain register coding is straight binary as shown in Table 11. The default code in the gain register is 0xFFFF. In theory, the gain can be tuned across the full range of the output. In practice, the maximum recommended gain trim is about 50% of programmed range to maintain accuracy. See the Digital Offset and Gain Control section for more information.

Offset Register

The 16-bit offset register, as shown in Table 12, allows the user to adjust the offset of each channel by −32,768 LSBs to +32,767 LSBs in steps of 1 LSB. This is done by setting the DREG[2:0] bits to 100. It is possible to write the same offset code to all four DAC channels at the same time by setting the DREG[2:0] bits to 101. The offset register coding is straight binary as shown in Table 13. The default code in the offset register is 0x8000, which results in zero offset programmed to the output. See the Digital Offset and Gain Control section for more information.

Clear Code Register

The 16-bit clear code register allows the user to set the clear value of each channel as shown in Table 14. It is possible, via software, to enable or disable on a per channel basis which channels are cleared when the CLEAR pin is activated. The default clear code is 0x0000. See the Asynchronous Clear section for more information.

Table 10. Programming the Gain Register

R/$\overline{W}$	DUT_AD1	DUT_AD0	DREG2	DREG1	DREG0	DAC_AD1	DAC_AD0	D15 to D0
0	Device address		0	1	0	DAC channel address		Gain adjustment

Table 11. Gain Register

Gain Adjustment	G15	G14	G13	G12 to G4	G3	G2	G1	G0
+65,535 LSBs	1	1	1	1	1	1	1	1
+65,534 LSBs	1	1	1	1	1	1	1	0
…	…	…	…	…	…	…	…	…
1 LSB	0	0	0	0	0	0	0	1
0 LSBs	0	0	0	0	0	0	0	0

Table 12. Programming the Offset Register

R/$\overline{W}$	DUT_AD1	DUT_AD0	DREG2	DREG1	DREG0	DAC_AD1	DAC_AD0	D15 to D0
0	Device address		1	0	0	DAC channel address		Offset adjustment

Table 13. Offset Register Options

Offset Adjustment	OF15	OF14	OF13	OF12 to OF4	OF3	OF2	OF1	OF0
+32,767 LSBs	1	1	1	1	1	1	1	1
+32,766 LSBs	1	1	1	1	1	1	1	0
…	…	…	…	…	…	…	…	…
No Adjustment (Default)	1	0	0	0	0	0	0	0
…	…	…	…	…	…	…	…	…
−32,767 LSBs	0	0	0	0	0	0	0	1
−32,768 LSBs	0	0	0	0	0	0	0	0

Table 14. Programming the Clear Code Register

R/$\overline{W}$	DUT_AD1	DUT_AD0	DREG2	DREG1	DREG0	DAC_AD1	DAC_AD0	D15 to D0
0	Device address		1	1	0	DAC channel address		Clear code

CONTROL REGISTERS

When writing to a control register, the format shown in Table 15 must be used. See Table 8 for information on the configuration of Bit D23 to Bit D16. The control registers are addressed by setting the DREG[2:0] bits to 111 and then setting the CREG[2:0] bits to the appropriate decode address for that register, according to Table 16. These CREG bits select among the various control registers.

Main Control Register

The main control register options are shown in Table 17 and Table 18. See the Device Features section for more information on the features controlled by the main Control Register.

Table 15. Writing to a Control Register

MSB ... LSB

D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12 to D0
R/$\overline{W}$	DUT_AD1	DUT_AD0	1	1	1	DAC_AD1	DAC_AD0	CREG2	CREG1	CREG0	Data

Table 16. Register Access Decode

CREG2 (D15)	CREG1 (D14)	CREG0 (D13)	Function
0	0	0	Slew rate control register (one per channel)
0	0	1	Main control register
0	1	0	DAC control register (one per channel)
0	1	1	DC-to-dc control register
1	0	0	Software register

Table 17. Programming the Main Control Register

MSB ... LSB

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3 to D0
0	0	1	0	STATREAD	EWD	WD1	WD0	X[1]	X[1]	OUTEN_ALL	DCDC_ALL	X[1]

[1] X = don't care.

Table 18. Main Control Register Functions

Bit	Description		
STATREAD	Enable status readback during a write. See the Device Features section. STATREAD = 1, enable. STATREAD = 0, disable (default).		
EWD	Enable watchdog timer. See the Device Features section for more information. EWD = 1, enable watchdog. EWD = 0, disable watchdog (default).		
WD1, WD0	Timeout select bits. Used to select the timeout period for the watchdog timer.		
	WD1	**WD0**	**Timeout Period (ms)**
	0	0	5
	0	1	10
	1	0	100
	1	1	200
OUTEN_ALL	Enables the output on all four DACs simultaneously. Do not use the OUTEN_ALL bit when using the OUTEN bit in the DAC control register.		
DCDC_ALL	When set, powers up the dc-to-dc converter on all four channels simultaneously. To power down the dc-to-dc converters, all channel outputs must first be disabled. Do not use the DCDC_ALL bit when using the DC_DC bit in the DAC control register.		

DAC Control Register

The DAC control register is used to configure each DAC channel. The DAC control register options are shown in Table 19 and Table 20.

Table 19. Programming DAC Control Register

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	X[1]	X[1]	X[1]	X[1]	INT_ENABLE	CLR_EN	OUTEN	RSET	DC_DC	X[1]	R2	R1	R0

[1] X = don't care.

Table 20. DAC Control Register Functions

Bit	Description			
INT_ENABLE	Powers up the dc-to-dc converter, DAC, and internal amplifiers for the selected channel. Does not enable the output. Can only be done on a per channel basis. It is recommended to set this bit and allow a >200 µs delay before enabling the output because this results in a reduced output enable glitch. Plots of this glitch can be found in Figure 26.			
CLR_EN	Per channel clear enable bit. Selects if this channel clears when the CLEAR pin is activated. CLR_EN = 1, channel clears when the part is cleared. CLR_EN = 0, channel does not clear when the part is cleared (default).			
OUTEN	Enables/disables the selected output channel. OUTEN = 1, enables the channel. OUTEN = 0, disables the channel (default).			
RSET	Selects an internal or external current sense resistor for the selected DAC channel. RSET = 0, selects the external resistor (default). RSET = 1, selects the internal resistor.			
DC_DC	Powers the dc-to-dc converter on the selected channel. DC_DC = 1, power up the dc-to-dc converter. DC_DC = 0, power down the dc-to-dc converter (default). This allows per channel dc-to-dc converter power-up/power-down. To power down the dc-to-dc converter, the OUTEN and INT_ENABLE bits must also be set to 0. All dc-to-dc converters can also be powered up simultaneously using the DCDC_ALL bit in the main control register.			
R2, R1, R0	Selects the output range to be enabled.			
	R2	**R1**	**R0**	**Output Range Selected**
	1	0	0	4 mA to 20 mA current range
	1	0	1	0 mA to 20 mA current range
	1	1	0	0 mA to 24 mA current range

Software Register

The software register has three functions. It allows the user to perform a software reset to the part. It can be used to set the user toggle bit, D11, in the status register. It is also used as part of the watchdog feature when it is enabled. This feature is useful to ensure that communication has not been lost between the MCU and the AD5757 and that the datapath lines are working properly (that is, SDIN, SCLK, and SYNC).

When the watchdog feature is enabled, the user must write 0x195 to the software register within the timeout period. If this command is not received within the timeout period, the ALERT pin signals a fault condition. This is only required when the watchdog timer function is enabled.

DC-to-DC Control Register

The dc-to-dc control register allows the user control over the dc-to-dc switching frequency and phase, as well as the maximum allowable dc-to-dc output voltage. The dc-to-dc control register options are shown in Table 23 and Table 24.

Table 21. Programming the Software Register

MSB				LSB
D15	D14	D13	D12	D11 to D0
1	0	0	User program	Reset code/SPI code

Table 22. Software Register Functions

Bit	Description	
User Program	This bit is mapped to Bit D11 of the status register. When this bit is set to 1, Bit D11 of the status register is set to 1. Likewise, when D12 is set to 0, Bit D11 of the status register is also set to 0. This feature can be used to ensure that the SPI pins are working correctly by writing a known bit value to this register and reading back the corresponding bit from the status register.	
Reset Code/SPI Code	**Option**	**Description**
	Reset code	Writing 0x555 to D[11:0] performs a reset of the AD5757.
	SPI code	If the watchdog timer feature is enabled, 0x195 must be written to the software register (D11 to D0) within the programmed timeout period.

Table 23. Programming the DC-to-DC Control Register

MSB							LSB
D15	D14	D13	D12 to D7	D6	D5 to D4	D3 to D2	D1 to D0
0	1	1	X[1]	DC-DC Comp	DC-DC phase	DC-DC Freq	DC-DC MaxV

[1] X = don't care.

Table 24. DC-to-DC Control Register Options

Bit	Description
DC-DC Comp	Selects between an internal and external compensation resistor for the dc-to-dc converter. See the DC-to-DC Converter Compensation Capacitors and AICC Supply Requirements—Slewing sections in the Device Features section for more information. 0 = selects the internal 150 kΩ compensation resistor (default). 1 = bypasses the internal compensation resistor for the dc-to-dc converter. In this mode, an external dc-to-dc compensation resistor must be used; this is placed at the $COMP_{DCDC\_x}$ pin in series with the 10 nF dc-to-dc compensation capacitor to ground. Typically, a ~50 kΩ resistor is recommended.
DC-DC Phase	User programmable dc-to-dc converter phase (between channels). 00 = all dc-to-dc converters clock on the same edge (default). 01 = Channel A and Channel B clock on the same edge, Channel C and Channel D clock on opposite edges. 10 = Channel A and Channel C clock on the same edge, Channel B and Channel D clock on opposite edges. 11 = Channel A, Channel B, Channel C, and Channel D clock 90° out of phase from each other.
DC-DC Freq	DC-to-dc switching frequency; these are divided down from the internal 13 MHz oscillator (see Figure 47 and Figure 48). 00 = 250 ± 10% kHz. 01 = 410 ± 10% kHz (default). 10 = 650 ± 10% kHz.
DC-DC MaxV	Maximum allowed V_{BOOST_x} voltage supplied by the dc-to-dc converter. 00 = 23 V + 1 V/−1.5 V (default). 01 = 24.5 V ± 1 V. 10 = 27 V ± 1 V. 11 = 29.5 V ± 1V.

Slew Rate Control Register

This register is used to program the slew rate control for the selected DAC channel. The slew rate control is enabled/ disabled and programmed on a per channel basis. See Table 25 and the Digital Slew Rate Control section for more information.

READBACK OPERATION

Readback mode is invoked by setting the R/$\overline{W}$ bit to 1 in the serial input register write. See Table 26 and Table 27 for the bits associated with a readback operation. The DUT_AD1 bit and DUT_AD0 bit, in association with bits RD[4:0], select the register to be read. The remaining data bits in the write sequence are don't cares.

During the next SPI transfer (see Figure 4), either a NOP or a request to read another register must be issued. Meanwhile the SDO returns 24 bits, the 8 MSBs are don't cares, and the 16 LSBs contain the data from the addressed register. The SDO is loaded on each rising edge of SCLK and read on each falling edge of SCLK.

If PEC is enabled, the SDO returns 32 bits (Figure 5), with 8 CRC bits appended to the data readback. There must be no activity on SCLK between read command and NOP command, or an incorrect PEC may be read back.

Readback Example

To read back the gain register of Device 1, Channel A on the AD5757, implement the following sequence:

1. Write 0xA80000 to the AD5757 input register. This configures the AD5757 Device Address 1 for read mode with the gain register of Channel A selected. All the data bits, [D15:D0], are don't cares.
2. Follow with another read command or a no operation command (0x3CE000). During this command, the data from the Channel A gain register is clocked out on the SDO line.

Table 25. Programming the Slew Rate Control Register

D15	D14	D13	D12	D11 to D7	D6 to D3	D2 to D0
0	0	0	SREN	X[1]	SR_CLOCK	SR_STEP

[1] X = don't care.

Table 26. Input Shift Register Contents for a Read Operation

D23	D22	D21	D20	D19	D18	D17	D16	D15 to D0
R/$\overline{W}$	DUT_AD1	DUT_AD0	RD4	RD3	RD2	RD1	RD0	X[1]

[1] X = don't care.

Table 27. Read Address Decoding

RD4	RD3	RD2	RD1	RD0	Function
0	0	0	0	0	Read DAC A data register
0	0	0	0	1	Read DAC B data register
0	0	0	1	0	Read DAC C data register
0	0	0	1	1	Read DAC D data register
0	0	1	0	0	Read DAC A control register
0	0	1	0	1	Read DAC B control register
0	0	1	1	0	Read DAC C control register
0	0	1	1	1	Read DAC D control register
0	1	0	0	0	Read DAC A gain register
0	1	0	0	1	Read DAC B gain register
0	1	0	1	0	Read DAC C gain register
0	1	0	1	1	Read DAC D gain register
0	1	1	0	0	Read DACA offset register
0	1	1	0	1	Read DAC B offset register
0	1	1	1	0	Read DAC C offset register
0	1	1	1	1	Read DAC D offset register
1	0	0	0	0	Clear DAC A code register
1	0	0	0	1	Clear DAC B code register
1	0	0	1	0	Clear DAC C code register
1	0	0	1	1	Clear DAC D code register
1	0	1	0	0	DAC A slew rate control register
1	0	1	0	1	DAC B slew rate control register
1	0	1	1	0	DAC C slew rate control register
1	0	1	1	1	DAC D slew rate control register
1	1	0	0	0	Read status register
1	1	0	0	1	Read main control register
1	1	0	1	0	Read dc-to-dc control register

Status Register

The status register is a read only register. This register contains any fault information as well as a ramp active bit, and shows the status of the packet error checking feature. When the STATREAD bit in the main control register is set, the status register contents can be read back on the SDO pin during every write sequence. Alternatively, if the STATREAD bit is not set, the status register can be read using the normal readback operation.

Table 28. Decoding the Status Register

MSB **LSB**

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
DC-DCD	DC-DCC	DC-DCB	DC-DCA	User toggle	PEC error	Ramp active	Over TEMP	X[1]	X[1]	X[1]	X[1]	I_{OUT_D} fault	I_{OUT_C} fault	I_{OUT_B} fault	I_{OUT_A} fault

[1] X = don't care.

Table 29. Status Register Options

Bit	Description
DC-DCD	This bit is set on Channel D if the dc-to-dc converter cannot maintain compliance (it may be reaching its V_{MAX} voltage). In this case, the I_{OUT_D} fault bit is also set. See the DC-to-DC Converter V_{MAX} Functionality section for more information on this bit's operation under this condition.
DC-DCC	This bit is set on Channel C if the dc-to-dc converter cannot maintain compliance (it may be reaching its V_{MAX} voltage). In this case, the I_{OUT_C} fault bit is also set. See the DC-to-DC Converter V_{MAX} Functionality section for more information on this bit's operation under this condition.
DC-DCB	This bit is set on Channel B if the dc-to-dc converter cannot maintain compliance (it may be reaching its V_{MAX} voltage). In this case, the I_{OUT_B} fault bit is also set. See the DC-to-DC Converter V_{MAX} Functionality section for more information on this bit's operation under this condition.
DC-DCA	This bit is set on Channel A if the dc-to-dc converter cannot maintain compliance (it may be reaching its V_{MAX} voltage). In this case, the I_{OUT_A} fault bit is also set. See the DC-to-DC Converter V_{MAX} Functionality section for more information on this bit's operation under this condition.
User Toggle	User toggle bit. This bit is set or cleared via the software register. This can be used to verify data communications if needed.
PEC Error	Denotes a PEC error on the last data-word received over the SPI interface.
Ramp Active	This bit is set while any one of the output channels is slewing (slew rate control is enabled on at least one channel).
Over TEMP	This bit is set if the AD5757 core temperature exceeds approximately 150°C.
I_{OUT_D} Fault	This bit is set if a fault is detected on the I_{OUT_D} pin.
I_{OUT_C} Fault	This bit is set if a fault is detected on the I_{OUT_C} pin.
I_{OUT_B} Fault	This bit is set if a fault is detected on the I_{OUT_B} pin.
I_{OUT_A} Fault	This bit is set if a fault is detected on the I_{OUT_A} pin.

DEVICE FEATURES

OUTPUT FAULT

The AD5757 is equipped with a FAULT pin, an active low open-drain output allowing several AD5757 devices to be connected together to one pull-up resistor for global fault detection. The FAULT pin is forced active by any one of the following fault scenarios:

- The voltage at I_{OUT_x} attempts to rise above the compliance range, due to an open-loop circuit or insufficient power supply voltage. The internal circuitry that develops the fault output avoids using a comparator with windowed limits because this requires an actual output error before the FAULT output becomes active. Instead, the signal is generated when the internal amplifier in the output stage has less than approximately 1 V of remaining drive capability. Thus, the FAULT output activates slightly before the compliance limit is reached.
- An interface error is detected due to a PEC failure. See the Packet Error Checking section.
- If the core temperature of the AD5757 exceeds approximately 150°C.

The I_{OUT_x} fault, PEC error, and over TEMP bits of the status register are used in conjunction with the FAULT output to inform the user which one of the fault conditions caused the FAULT output to be activated.

DIGITAL OFFSET AND GAIN CONTROL

Each DAC channel has a gain (M) and offset (C) register, which allow trimming out of the gain and offset errors of the entire signal chain. Data from the DAC data register is operated on by a digital multiplier and adder controlled by the contents of the M and C registers. The calibrated DAC data is then stored in the DAC input register.

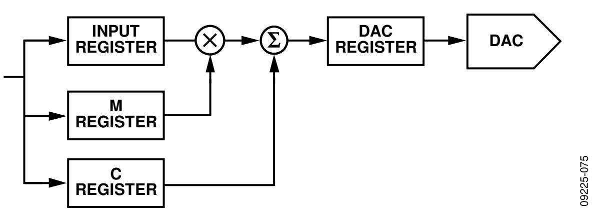


Figure 54. Digital Offset and Gain control

Although Figure 54 indicates a multiplier and adder for each channel, there is only one multiplier and one adder in the device, and they are shared among all four channels. This has implications for the update speed when several channels are updated at once (see Table 3).

Each time data is written to the M or C register, the output is not automatically updated. Instead, the next write to the DAC channel uses these M and C values to perform a new calibration and automatically updates the channel.

The output data from the calibration is routed to the DAC input register. This is then loaded to the DAC as described in the Theory of Operation section. Both the gain register and the offset register have 16 bits of resolution. The correct method to calibrate the gain/offset is to first calibrate out the gain, then calibrate the offset.

The value (in decimal) that is written to the DAC input register can be calculated by

$$Code_{DACRegister} = D \times \frac{(M+1)}{2^{16}} + C - 2^{15} \quad (1)$$

where:
D is the code loaded to the DAC channel's input register.
M is the code in the gain register (default code = $2^{16} - 1$).
C is the code in the offset register (default code = 2^{15}).

STATUS READBACK DURING A WRITE

The AD5757 has the ability to read back the status register contents during every write sequence. This feature is enabled via the STATREAD bit in the main control register. This allows the user to continuously monitor the status register and act quickly in the case of a fault.

When status readback during a write is enabled, the contents of the 16-bit status register (see Table 29) are output on the SDO pin, as shown in Figure 6.

The AD5757 powers up with this feature disabled. When this is enabled, the normal readback feature is not available, except for the status register. To read back any other register, clear the STATREAD bit first before following the readback sequence. STATREAD can be set high again after the register read.

If there are multiple units on the same SDO bus that have the STATREAD feature enabled, ensure that each unit is provided a unique physical address (AD1 and AD0) to prevent contention on the bus.

If packet error checking is enabled, ignore the PEC values returned on a status readback during a write operation. See the Packet Error Checking section for further information.

ASYNCHRONOUS CLEAR

CLEAR is an active high, edge-sensitive input that allows the output to be cleared to a preprogrammed 16-bit code. This code is user programmable via a per channel 16-bit clear code register.

For a channel to clear, that channel must be enabled to be cleared via the CLR_EN bit in the channel's DAC control register. If the channel is not enabled to be cleared, the output remains in its current state independent of the CLEAR pin level.

When the CLEAR signal is returned low, the relevant outputs remain cleared until a new value is programmed.

The CLEAR pin must not be asserted between the first and second commands of a normal SPI read when SYNC is high (represented by t6 in Figure 4). Failure to comply with this will result in the DAC outputs not being cleared and may cause the AD5757 SPI port to become unresponsive, requiring a hardware reset to restore SPI communications. If automatic readback of status registers is enabled then there are no restrictions to the use of the CLEAR pin.

PACKET ERROR CHECKING

To verify that data is received correctly in noisy environments, the AD5757 offers the option of packet error checking based on an 8-bit cyclic redundancy check (CRC-8). The device controlling the AD5757 generates an 8-bit frame check sequence using the polynomial

$$C(x) = x_8 + x_2 + x_1 + 1$$

This is added to the end of the data-word, and 32 bits are sent to the AD5757 before taking SYNC high. If the AD5757 sees a 32-bit frame, it performs the error check when SYNC goes high. If the check is valid, the data is written to the selected register.

If the error check fails, the FAULT pin goes low and the PEC error bit in the status register is set. After reading the status register, FAULT returns high (assuming there are no other faults), and the PEC error bit is cleared automatically. It is not recommended to tie both AD1 and AD0 low as a short low on SDIN could possibly lead to a zero-scale update for DAC A.

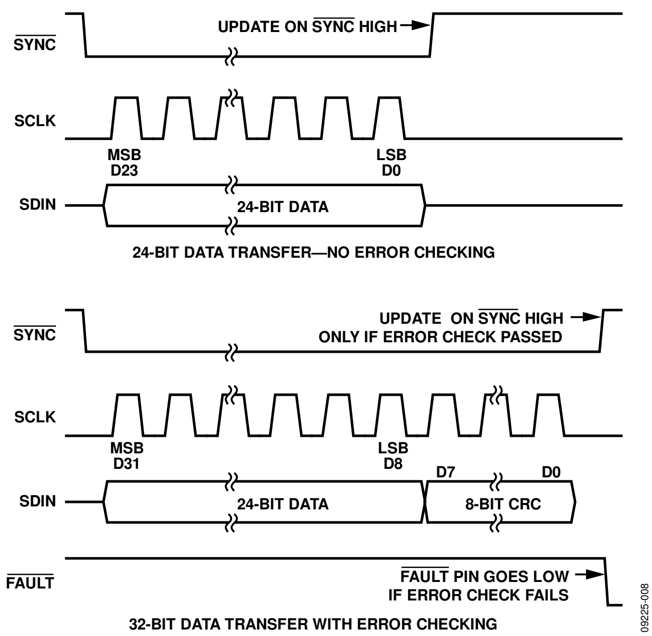


Figure 55. PEC Timing

The PEC can be used for both transmit and receive of data packets. If status readback during a write is enabled, ignore the PEC values returned during the status readback during a write operation. If status readback during a write is disabled, the user can still use the normal readback operation to monitor status register activity with PEC.

If PEC is enabled when receiving data packets, there must be no activity on SCLK between the read command and the NOP command, or an incorrect PEC may be read back. See Figure 5 and the Readback Operation section for further information.

WATCHDOG TIMER

When enabled, an on-chip watchdog timer generates an alert signal if 0x195 is not written to the software register within the programmed timeout period. This feature is useful to ensure that communication is not lost between the MCU and the AD5757 and that these datapath lines are working properly (that is, SDIN, SCLK, and SYNC). If 0x195 is not received by the software register within the timeout period, the ALERT pin signals a fault condition. The ALERT signal is active high and can be connected directly to the CLEAR pin to enable a CLEAR in the event that communication from the MCU is lost.

The watchdog timer is enabled, and the timeout period (5 ms, 10 ms, 100 ms, or 200 ms) is set in the main control register (see Table 17 and Table 18).

OUTPUT ALERT

The AD5757 is equipped with an ALERT pin. This is an active high CMOS output. The AD5757 also has an internal watchdog timer. When enabled, it monitors SPI communications. If 0x195 is not received by the software register within the timeout period, the ALERT pin goes active.

INTERNAL REFERENCE

The AD5757 contains an integrated 5 V voltage reference with initial accuracy of ±5 mV maximum and a temperature drift coefficient of ±10 ppm maximum. The reference voltage is buffered and externally available for use elsewhere within the system. REFOUT must be connected to REFIN to use the internal reference.

EXTERNAL CURRENT SETTING RESISTOR

Referring to Figure 50, R_{SET} is an internal sense resistor as part of the voltage to current conversion circuitry. The stability of the output current value over temperature is dependent on the stability of the value of R_{SET}. As a method of improving the stability of the output current over temperature, an external 15 kΩ low drift resistor can be connected to the R_{SET_x} pin of the AD5757 to be used instead of the internal resistor, R1. The external resistor is selected via the DAC control register (see Table 19).

Table 1 outlines the performance specifications of the AD5757 with both the internal R_{SET} resistor and an external, 15 kΩ R_{SET} resistor. Using an external R_{SET} resistor allows for improved performance over the internal R_{SET} resistor option. The external R_{SET} resistor specification assumes an ideal resistor; the actual performance depends on the absolute value and temperature coefficient of the resistor used. This directly affects the gain error of the output, and thus the total unadjusted error. To arrive at the gain/TUE error of the output with a particular external R_{SET} resistor, add the percentage absolute error of the R_{SET} resistor directly to the gain/TUE error of the AD5757 with the external R_{SET} resistor, shown in Table 1 (expressed in % FSR).

HART

The AD5757 has four CHART pins, one corresponding to each output channels. A HART signal can be coupled into these pins. The HART signal appears on the corresponding current output, if the output is enabled. Table 30 shows the recommended input voltages for the HART signal at the CHART pin. If these voltages are used, the current output meets the HART amplitude specifications. Figure 56 shows the recommended circuit for attenuating and coupling in the HART signal.

Table 30. CHART Input Voltage to HART Output Current

R_{SET}	CHART Input Voltage	Current Output (HART)
Internal R_{SET}	150 mV p-p	1 mA p-p
External R_{SET}	170 mV p-p	1 mA p-p

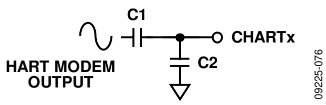


Figure 56. Coupling HART Signal

A minimum capacitance of C1 + C2 is required to ensure that the 1.2 kHz and 2.2 kHz HART frequencies are not significantly attenuated at the output. The recommended values are C1 = 22 nF, C2 = 47 nF.

Digitally controlling the slew rate of the output is necessary to meet the analog rate of change requirements for HART.

If the HART feature is not required, leave the CHARTx pins open circuit.

DIGITAL SLEW RATE CONTROL

The slew rate control feature of the AD5757 allows the user to control the rate at which the output value changes. With the slew rate control feature disabled, the output value changes at a rate limited by the output drive circuitry and the attached load. To reduce the slew rate, this can be achieved by enabling the slew rate control feature. With the feature enabled via the SREN bit of the slew rate control register (see Table 25), the output, instead of slewing directly between two values, steps digitally at a rate defined by two parameters accessible via the slew rate control register, as shown in Table 25. The parameters are SR_CLOCK and SR_STEP. SR_CLOCK defines the rate at which the digital slew is updated, for example, if the selected update rate is 8 kHz, the output updates every 125 µs. In conjunction with this, SR_STEP defines by how much the output value changes at each update. Together, both parameters define the rate of change of the output value. Table 31 and Table 32 outline the range of values for both the SR_CLOCK and SR_STEP parameters.

Table 31. Slew Rate Update Clock Options

SR_CLOCK	Update Clock Frequency (Hz)[1]
0000	64 k
0001	32 k
0010	16 k
0011	8 k
0100	4 k
0101	2 k
0110	1 k
0111	500
1000	250
1001	125
1010	64
1011	32
1100	16
1101	8
1110	4
1111	0.5

[1] These clock frequencies are divided down from the 13 MHz internal oscillator. See Table 1, Figure 47, and Figure 48.

Table 32. Slew Rate Step Size Options

SR_STEP	Step Size (LSBs)
000	1
001	2
010	4
011	16
100	32
101	64
110	128
111	256

The following equation describes the slew rate as a function of the step size, the update clock frequency, and the LSB size:

$$Slew\ Time = \frac{Output\ Change}{Step\ Size \times Update\ Clock\ Frequency \times LSB\ Size}$$

where:
Slew Time is expressed in seconds.
Output Change is expressed in amps for I_{OUT_x}.

When the slew rate control feature is enabled, all output changes occur at the programmed slew rate (see the DC-to-DC Converter Settling Time section for additional information). For example, if the CLEAR pin is asserted, the output slews to the clear value at the programmed slew rate (assuming that the clear channel is enabled to be cleared). If a number of channels are enabled for slew, care must be taken when asserting the CLEAR pin. If one of the channels is slewing when CLEAR is asserted, other channels may change directly to their clear values not under slew rate control. The update clock frequency for any given value is the same for all output ranges. The step size, however, varies across output ranges for a given value of step size because the LSB size is different for each output range.

POWER DISSIPATION CONTROL

The AD5757 contains integrated dynamic power control using a dc-to-dc boost converter circuit, allowing reductions in power consumption from standard designs.

In standard current input module designs, the load resistor values can range from typically 50 Ω to 750 Ω. Output module systems must source enough voltage to meet the compliance voltage requirement across the full range of load resistor values. For example, in a 4 mA to 20 mA loop when driving 20 mA, a compliance voltage of >15 V is required. When driving 20 mA into a 50 Ω load, only 1 V compliance is required.

The AD5757 circuitry senses the output voltage and regulates this voltage to meet compliance requirements plus a small headroom voltage. The AD5757 is capable of driving up to 24 mA through a 1 kΩ load.

DC-TO-DC CONVERTERS

The AD5757 contains four independent dc-to-dc converters. These are used to provide dynamic control of the V_{BOOST} supply voltage for each channel (see Figure 50). Figure 57 shows the discrete components needed for the dc-to-dc circuitry, and the following sections describe component selection and operation of this circuitry.

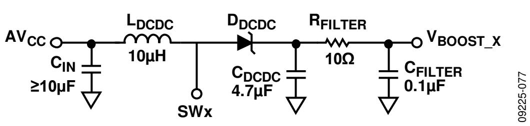


Figure 57. DC-to-DC Circuit

Table 33. Recommended DC-to-DC Components

Symbol	Component	Value	Manufacturer
L_{DCDC}	XAL4040-103	10 µH	Coilcraft®
C_{DCDC}	GRM32ER71H475KA88L	4.7 µF	Murata
D_{DCDC}	PD3S160-7	0.55 V_F	Diodes, Inc.

It is recommended to place a 10 Ω, 100 nF low-pass RC filter after C_{DCDC}. This consumes a small amount of power but reduces the amount of ripple on the V_{BOOST_x} supply.

DC-to-DC Converter Operation

The on-board dc-to-dc converters use a constant frequency, peak current mode control scheme to step up an AV_{CC} input of 4.5 V to 5.5 V to drive the AD5757 output channel. These are designed to operate in discontinuous conduction mode (DCM) with a duty cycle of <90% typical. Discontinuous conduction mode refers to a mode of operation where the inductor current goes to zero for an appreciable percentage of the switching cycle. The dc-to-dc converters are nonsynchronous; that is, they require an external Schottky diode.

DC-to-DC Converter Output Voltage

When a channel current output is enabled, the converter regulates the V_{BOOST_x} supply to 7.4 V (±5%) or (I_{OUT} × R_{LOAD} + Headroom), whichever is greater (see Figure 32 for a plot of headroom supplied vs. output current). When the output is disabled, the converter regulates the V_{BOOST_x} supply to 7.4 V (±5%).

DC-to-DC Converter Settling Time

The settling time for a step greater than ~1 V (I_{OUT} × R_{LOAD}) is dominated by the settling time of the dc-to-dc converter. The exception to this is when the required voltage at the I_{OUT_x} pin plus the compliance voltage is below 7.4 V (±5%). A typical plot of the output settling time can be found in Figure 27. This plot is for a 1 kΩ load. The settling time for smaller loads is faster. The settling time for current steps less than 24 mA is also faster.

DC-to-DC Converter V_{MAX} Functionality

The maximum V_{BOOST_x} voltage is set in the dc-to-dc control register (23 V, 24.5 V, 27 V, or 29.5 V; see Table 24). On reaching this maximum voltage, the dc-to-dc converter is disabled, and the V_{BOOST_x} voltage is allowed to decay by ~0.4 V. After the V_{BOOST_x} voltage has decayed by ~0.4 V, the dc-to-dc converter is reenabled, and the voltage ramps up again to V_{MAX}, if still required. This operation is shown in Figure 58.

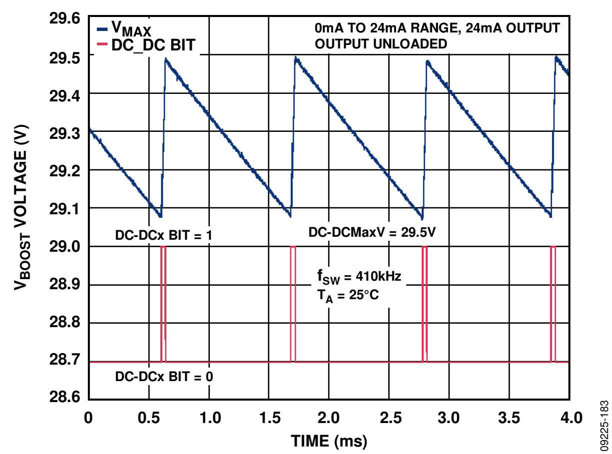


Figure 58. Operation on Reaching V_{MAX}

As shown in Figure 58, the DC-DCx bit in the status register asserts when the AD5757 is ramping to the V_{MAX} value but deasserts when the voltage is decaying to V_{MAX} − ~0.4 V.

DC-to-DC Converter On-Board Switch

The AD5757 contains a 0.425 Ω internal switch. The switch current is monitored on a pulse by pulse basis and is limited to 0.8 A peak current.

DC-to-DC Converter Switching Frequency and Phase

The AD5757 dc-to-dc converter switching frequency can be selected from the dc-to-dc control register. The phasing of the channels can also be adjusted so that the dc-to-dc converter can clock on different edges (see Table 24). For typical applications, a 410 kHz frequency is recommended. At light loads (low output current and small load resistor), the dc-to-dc converter enters a pulse-skipping mode to minimize switching power dissipation.

DC-to-DC Converter Inductor Selection

For typical 4 mA to 20 mA applications, a 10 µH inductor (such as the XAL4040-103 from Coilcraft), combined with a switching frequency of 410 kHz, allows up to 24 mA to be driven into a load resistance of up to 1 kΩ with an AV_{CC} supply of 4.5 V to 5.5 V. It is important to ensure that the inductor is able to handle the peak current without saturating, especially at the maximum ambient temperature. If the inductor enters into saturation mode, it results in a decrease in efficiency. The inductance value also drops during saturation and may result in the dc-to-dc converter circuit not being able to supply the required output power.

DC-to-DC Converter External Schottky Selection

The AD5757 requires an external Schottky for correct operation. Ensure that the Schottky is rated to handle the maximum reverse breakdown expected in operation and that the rectifier maximum junction temperature is not exceeded. The diode average current is approximately equal to the I_{LOAD} current. Diodes with larger forward voltage drops result in a decrease in efficiency.

DC-to-DC Converter Compensation Capacitors

As the dc-to-dc converter operates in DCM, the uncompensated transfer function is essentially a single-pole transfer function. The pole frequency of the transfer function is determined by the dc-to-dc converter's output capacitance, input and output voltage, and output load. The AD5757 uses an external capacitor in conjunction with an internal 150 kΩ resistor to compensate the regulator loop. Alternatively, an external compensation resistor can be used in series with the compensation capacitor by setting the DC-DC Comp bit in the dc-to-dc control register. In this case, a ~50 kΩ resistor is recommended. A description of the advantages of this can be found in the AI_{CC} Supply Requirements—Slewing section. For typical applications, a 10 nF dc-to-dc compensation capacitor is recommended.

DC-to-DC Converter Input and Output Capacitor Selection

The output capacitor affects ripple voltage of the dc-to-dc converter and indirectly limits the maximum slew rate at which the channel output current can rise. The ripple voltage is caused by a combination of the capacitance and equivalent series resistance (ESR) of the capacitor. For the AD5757, a ceramic capacitor of 4.7 µF is recommended for typical applications. Larger capacitors or paralleled capacitors improve the ripple at the expense of reduced slew rate. Larger capacitors also impact the AV_{CC} supplies current requirements while slewing (see the AI_{CC} Supply Requirements—Slewing section). This capacitance at the output of the dc-to-dc converter should be >3 µF under all operating conditions.

The input capacitor provides much of the dynamic current required for the dc-to-dc converter and should be a low ESR component. For the AD5757, a low ESR tantalum or ceramic capacitor of 10 µF is recommended for typical applications. Ceramic capacitors must be chosen carefully because they can exhibit a large sensitivity to dc bias voltages and temperature. X5R or X7R dielectrics are preferred because these capacitors remain stable over wider operating voltage and temperature ranges. Care must be taken if selecting a tantalum capacitor to ensure a low ESR value.

AI_{CC} SUPPLY REQUIREMENTS—STATIC

The dc-to-dc converter is designed to supply a V_{BOOST_x} voltage of

$$V_{BOOST} = I_{OUT} \times R_{LOAD} + Headroom \quad (2)$$

See Figure 32 for a plot of headroom supplied vs. output voltage. This means that, for a fixed load and output voltage, the dc-to-dc converter output current can be calculated by the following formula:

$$AI_{CC} = \frac{Power\ Out}{Efficiency \times AV_{CC}} = \frac{I_{OUT} \times V_{BOOST}}{\eta_{V_{BOOST}} \times AV_{CC}} \quad (3)$$

where:
I_{OUT} is the output current from I_{OUT_x} in amps.
$\eta_{V_{BOOST}}$ is the efficiency at V_{BOOST_x} as a fraction (see Figure 34 and Figure 35).

AI_{CC} SUPPLY REQUIREMENTS—SLEWING

The AI_{CC} current requirement while slewing is greater than in static operation because the output power increases to charge the output capacitance of the dc-to-dc converter. This transient current can be quite large (see Figure 59), although the methods described in the Reducing AI_{CC} Current Requirements section can reduce the requirements on the AV_{CC} supply. If not enough AI_{CC} current can be provided, the AV_{CC} voltage drops. Due to this AV_{CC} drop, the AI_{CC} current required to slew increases further. This means that the voltage at AV_{CC} drops further (see Equation 3) and the V_{BOOST_x} voltage, and thus the output voltage, may never reach its intended value. Because this AV_{CC} voltage is common to all channels, this may also affect other channels.

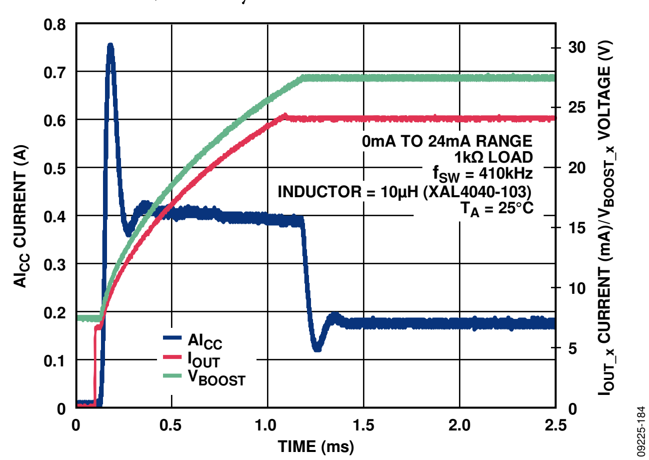


Figure 59. AI_{CC} Current vs. Time for 24 mA Step Through 1 kΩ Load with Internal Compensation Resistor

Reducing AI_{CC} Current Requirements

There are two main methods that can be used to reduce the AI_{CC} current requirements. One method is to add an external compensation resistor, and the other is to use slew rate control. Both of these methods can be used in conjunction.

A compensation resistor can be placed at the $COMP_{DCDC\_x}$ pin in series with the 10 nF compensation capacitor. A 51 kΩ external compensation resistor is recommended. This compensation increases the slew time of the current output but eases the AI_{CC} transient current requirements. Figure 60 shows a plot of AI_{CC} current for a 24 mA step through a 1 kΩ load when using a 51 kΩ compensation resistor. This method eases the current requirements through smaller loads even further, as shown in Figure 61.

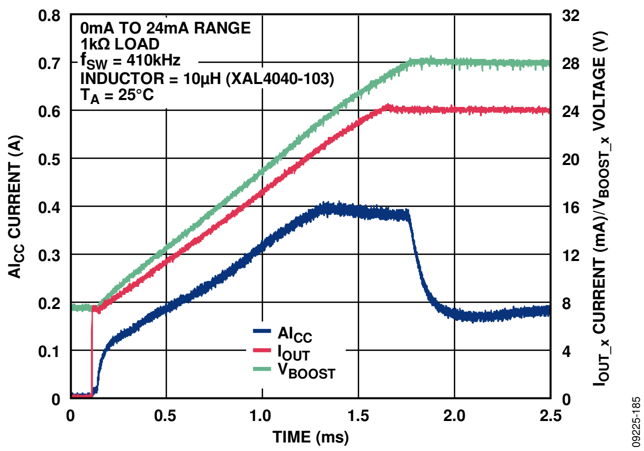


Figure 60. AI_{CC} Current vs. Time for 24 mA Step Through 1 kΩ Load with External 51 kΩ Compensation Resistor

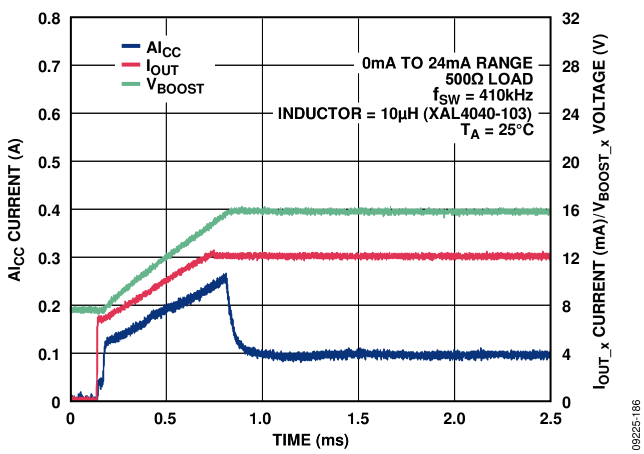


Figure 61. AI_{CC} Current vs. Time for 24 mA Step Through 500 Ω Load with External 51 kΩ Compensation Resistor

Using slew rate control can greatly reduce the AV_{CC} supplies current requirements, as shown in Figure 62. When using slew rate control, pay attention to the fact that the output cannot slew faster than the dc-to-dc converter. The dc-to-dc converter slews slowest at higher currents through large (for example, 1 kΩ) loads. This slew rate is also dependent on the configuration of the dc-to-dc converter. Two examples of the dc-to-dc converter's output slew are shown in Figure 60 and Figure 61 (V_{BOOST} corresponds to the dc-to-dc converter's output voltage).

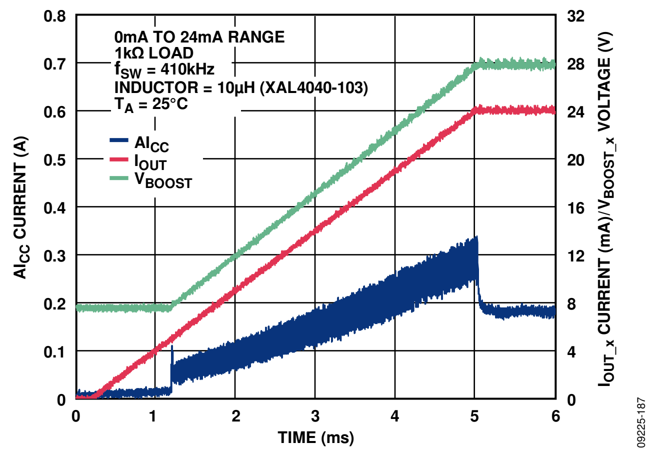


Figure 62. AI_{CC} Current vs. Time for 24 mA Step Through 1 kΩ Load with Slew Rate Control

EXTERNAL PMOS MODE

The AD5757 can also be used with an external PMOS transistor per channel, as shown in Figure 63. This mode can be used to limit the on-chip power dissipation of the AD5757, though this will not reduce the power dissipation of the total system. The IGATE functionality is not typically required when using the dynamic power control feature so Figure 63 shows the configuration of the device for a fixed V_{BOOST_x} supply.

In this configuration the SW_x pins are left floating and the $GNDSW_x$ pin is grounded. The V_{BOOST_x} pin is connected to a minimum supply of 7.5 V and a maximum supply of 33 V. This supply can be sized according to the maximum load required to be driven.

The IGATE functionality works by holding the gate of the external PMOS transistor at (V_{BOOST_x} − 5 V). This means that the majority of the channels power dissipation will take place in this external PMOS transistor.

The external PMOS transistor should be chosen tolerate a V_{DS} voltage of at least $-V_{BOOST\_x}$, as well as to handle the power dissipation required. Choose the V_{GS} to accommodate for the I_{OUT} headroom. This external PMOS transistor typically has minimal effect on the current output performance.

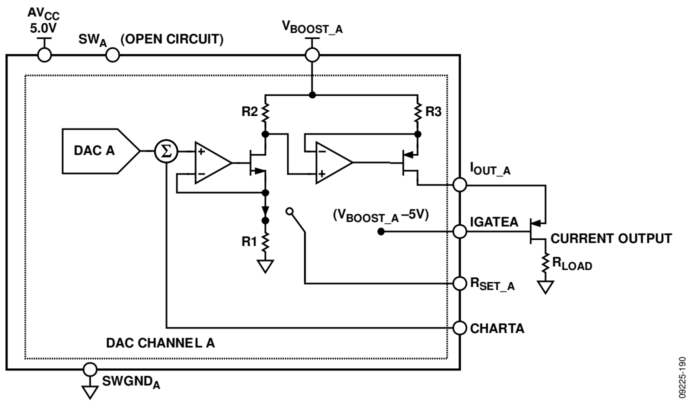


Figure 63. Configuration off a Particular Channel Using IGATE

APPLICATIONS INFORMATION

CURRENT OUTPUT MODE WITH INTERNAL R_{SET}

When using the internal R_{SET} resistor in current output mode, the output is significantly affected by how many other channels using the internal R_{SET} are enabled and by the dc crosstalk from these channels. The internal R_{SET} specifications in Table 1 are for all channels enabled with the internal R_{SET} selected and outputting the same code.

For every channel enabled with the internal R_{SET}, the offset error decreases. For example, with one current output enabled using the internal R_{SET}, the offset error is 0.075% FSR. This value decreases proportionally as more current channels are enabled; the offset error is 0.056% FSR on each of two channels, 0.029% on each of three channels, and 0.01% on each of four channels.

Similarly, the dc crosstalk when using the internal R_{SET} is proportional to the number of current output channels enabled with the internal R_{SET}. For example, with the measured channel at 0x8000 and one channel going from zero to full scale, the dc crosstalk is −0.011% FSR. With two channels going from zero to full scale, it is −0.019% FSR, and with all three other channels going from zero to full scale, it is −0.025% FSR.

For the full-scale error measurement in Table 1, all channels are at 0xFFFF. This means that, as any channel goes to zero scale, the full-scale error increases due to the dc crosstalk. For example, with the measured channel at 0xFFFF and three channels at zero scale, the full-scale error is 0.025%. Similarly, if only one channel is enabled in current output mode with the internal R_{SET}, the full-scale error is 0.025% FSR + 0.075% FSR = 0.1% FSR.

PRECISION VOLTAGE REFERENCE SELECTION

To achieve the optimum performance from the AD5757 over its full operating temperature range, a precision voltage reference must be used. Give thought to the selection of a precision voltage reference. The voltage applied to the reference inputs is used to provide a buffered reference for the DAC cores. Therefore, any error in the voltage reference is reflected in the outputs of the device.

There are four possible sources of error to consider when choosing a voltage reference for high accuracy applications: initial accuracy, temperature coefficient of the output voltage, long-term drift, and output voltage noise.

Initial accuracy error on the output voltage of an external reference can lead to a full-scale error in the DAC. Therefore, to minimize these errors, a reference with low initial accuracy error specification is preferred. Choosing a reference with an output trim adjustment, such as the ADR425, allows a system designer to trim system errors out by setting the reference voltage to a voltage other than the nominal. The trim adjustment can be used at any temperature to trim out any error.

Long-term drift is a measure of how much the reference output voltage drifts over time. A reference with a tight long-term drift specification ensures that the overall solution remains relatively stable over its entire lifetime.

The temperature coefficient of a reference's output voltage affects INL, DNL, and TUE. Choose a reference with a tight temperature coefficient specification to reduce the dependence of the DAC output voltage to ambient temperature.

In high accuracy applications, which have a relatively low noise budget, reference output voltage noise must be considered. Choosing a reference with as low an output noise voltage as practical for the system resolution required is important. Precision voltage references such as the ADR435 (XFET design) produce low output noise in the 0.1 Hz to 10 Hz region. However, as the circuit bandwidth increases, filtering the output of the reference may be required to minimize the output noise.

DRIVING INDUCTIVE LOADS

When driving inductive or poorly defined loads, a capacitor may be required between I_{OUT_x} and AGND to ensure stability. A 0.01 µF capacitor between I_{OUT_x} and AGND ensures stability of a load of 50 mH. The capacitive component of the load may cause slower settling, although this may be masked by the settling time of the AD5757. There is no maximum capacitance limit for the current output of the AD5757.

Table 34. Recommended Precision References

Part No.	Initial Accuracy (mV Maximum)	Long-Term Drift (ppm Typical)	Temperature Drift (ppm/°C Maximum)	0.1 Hz to 10 Hz Noise (µV p-p Typical)
ADR445	±2	50	3	2.25
ADR02	±3	50	3	10
ADR435	±2	40	3	8
ADR395	±5	50	9	8
AD586	±2.5	15	10	4

TRANSIENT VOLTAGE PROTECTION

The AD5757 contains ESD protection diodes that prevent damage from normal handling. The industrial control environment can, however, subject I/O circuits to much higher transients. To protect the AD5757 from excessively high voltage transients, external power diodes and a surge current limiting resistor (R_P) are required, as shown in Figure 64. A typical value for R_P is 10 Ω. The two protection diodes and the resistor (R_P) must have appropriate power ratings.

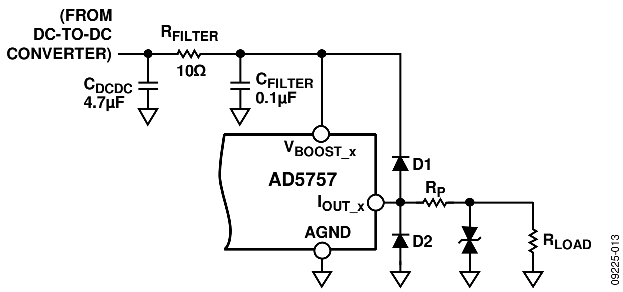


Figure 64. Output Transient Voltage Protection

Additional protection can be provided using transient voltage suppressors (TVSs), also referred to as transorbs. These components are available as unidirectional suppressors, which protect against positive high voltage transients, and as bidirectional suppressors, which protect against both positive and negative high voltage transients. Transient voltage suppressors are available in a wide range of standoff and breakdown voltage ratings. The TVS must be sized with the lowest breakdown voltage possible while not conducting in the functional range of the current output.

It is recommended that all field connected nodes be protected.

MICROPROCESSOR INTERFACING

Microprocessor interfacing to the AD5757 is via a serial bus that uses a protocol compatible with microcontrollers and DSP processors. The communications channel is a 3-wire minimum interface consisting of a clock signal, a data signal, and a latch signal. The AD5757 requires a 24-bit data-word with data valid on the falling edge of SCLK.

The DAC output update is initiated on either the rising edge of LDAC or, if LDAC is held low, on the rising edge of SYNC. The contents of the registers can be read using the readback function.

AD5757-TO-ADSP-BF527 INTERFACE

The AD5757 can be connected directly to the SPORT interface of the ADSP-BF527, an Analog Devices, Inc., Blackfin® DSP. Figure 65 shows how the SPORT interface can be connected to control the AD5757.

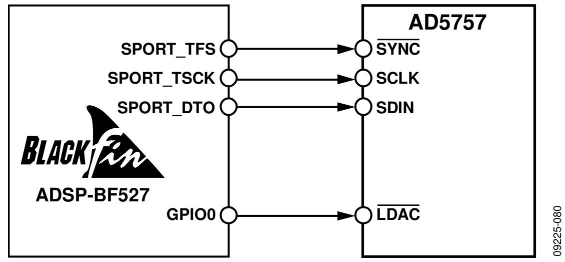


Figure 65. AD5757-to-ADSP-BF527 SPORT Interface

LAYOUT GUIDELINES

Grounding

In any circuit where accuracy is important, careful consideration of the power supply and ground return layout helps to ensure the rated performance. The printed circuit board on which the AD5757 is mounted should be designed so that the analog and digital sections are separated and confined to certain areas of the board. If the AD5757 is in a system where multiple devices require an AGND-to-DGND connection, make the connection at one point only. Establish the star ground point as close as possible to the device.

The $GNDSW_x$ and ground connection for the AV_{CC} supply are referred to as PGND. PGND must be confined to certain areas of the board, and the PGND-to-AGND connection must be made at one point only.

Supply Decoupling

The AD5757 must have ample supply bypassing of 10 µF in parallel with 0.1 µF on each supply located as close to the package as possible, ideally right up against the device. The 10 µF capacitors are the tantalum bead type. The 0.1 µF capacitor must have low effective series resistance (ESR) and low effective series inductance (ESL), such as the common ceramic types, which provide a low impedance path to ground at high frequencies to handle transient currents due to internal logic switching.

Traces

The power supply lines of the AD5757 must use as large a trace as possible to provide low impedance paths and reduce the effects of glitches on the power supply line. Fast switching signals such as clocks must be shielded with digital ground to prevent radiating noise to other parts of the board and must never be run near the reference inputs. A ground line routed between the SDIN and SCLK lines helps reduce crosstalk between them (not required on a multilayer board that has a separate ground plane, but separating the lines helps). It is essential to minimize noise on the REFIN line because it couples through to the DAC output.

Avoid crossover of digital and analog signals. Traces on opposite sides of the board must run at right angles to each other. This reduces the effects of feedthrough on the board. A microstrip technique is by far the best, but is not always possible with a double-sided board. In this technique, the component side of the board is dedicated to ground plane, whereas signal traces are placed on the solder side.

DC-to-DC Converters

To achieve high efficiency, good regulation, and stability, a well-designed printed circuit board layout is required.

Follow these guidelines when designing printed circuit boards (see Figure 57):

- Keep the low ESR input capacitor, C_{IN}, close to AV_{CC} and PGND.
- Keep the high current path from C_{IN} through the inductor, L_{DCDC}, to SW_X and PGND as short as possible.
- Keep the high current path from C_{IN} through L_{DCDC} and the rectifier, D_{DCDC}, to the output capacitor, C_{DCDC}, as short as possible.
- Keep high current traces as short and as wide as possible. The path from C_{IN} through the inductor, L_{DCDC}, to SW_X and PGND must be able to handle a minimum of 1 A.
- Place the compensation components as close as possible to $COMP_{DCDC\_x}$.
- Avoid routing high impedance traces near any node connected to SW_x or near the inductor to prevent radiated noise injection.

GALVANICALLY ISOLATED INTERFACE

In many process control applications, it is necessary to provide an isolation barrier between the controller and the unit being controlled to protect and isolate the controlling circuitry from any hazardous common-mode voltages that may occur. Analog Devices *i*Coupler® products can provide voltage isolation in excess of 2.5 kV. The serial loading structure of the AD5757 makes it ideal for isolated interfaces because the number of interface lines is kept to a minimum. Figure 66 shows a 4-channel isolated interface to the AD5757 using an ADuM1400. For more information, visit www.analog.com.

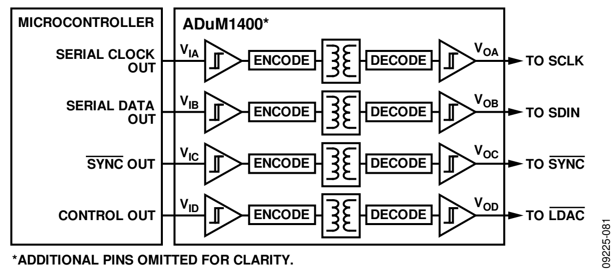


Figure 66. Isolated Interface

INDUSTRIAL HART CAPABLE ANALOG OUTPUT APPLICATION

Many industrial control applications have requirements for accurately controlled current output signals, and the AD5757 is ideal for such applications. Figure 67 shows the AD5757 in a circuit design for a HART-enabled output module, specifically for use in an industrial control application.

The design provides for a HART-enabled current output, with the HART capability provided by the AD5700/AD5700-1 HART modem, the industry's lowest power and smallest footprint HART-compliant IC modem. For additional space-savings, the AD5700-1 offers a 0.5% precision internal oscillator. The HART_OUT signal from the AD5700 is attenuated and ac-coupled into the CHARTx pin of the AD5757. Such a configuration results in the AD5700 HART modem output modulating the 4 mA to 20 mA analog current without affecting the dc level of the current. This circuit adheres to the HART physical layer specifications as defined by the HART Communication Foundation.

For transient overvoltage protection, a 24 V transient voltage suppressor (TVS) is placed on the I_{OUT}/V_{OUT} connection. For added protection, clamping diodes are connected from the I_{OUT_x}/V_{OUT_x} pin to the AV_{DD} and GND power supply pins. A 5 kΩ current limiting resistor is also placed in series with the +VSENSE_X input. This is to limit the current to an acceptable level during a transient event. The recommended external band-pass filter for the AD5700 HART modem includes a 150 kΩ resistor, which limits current to a sufficiently low level to adhere to intrinsic safety requirements. In this case, the input has higher transient voltage protection and, therefore, does not require additional protection circuitry, even in the most demanding of industrial environments.

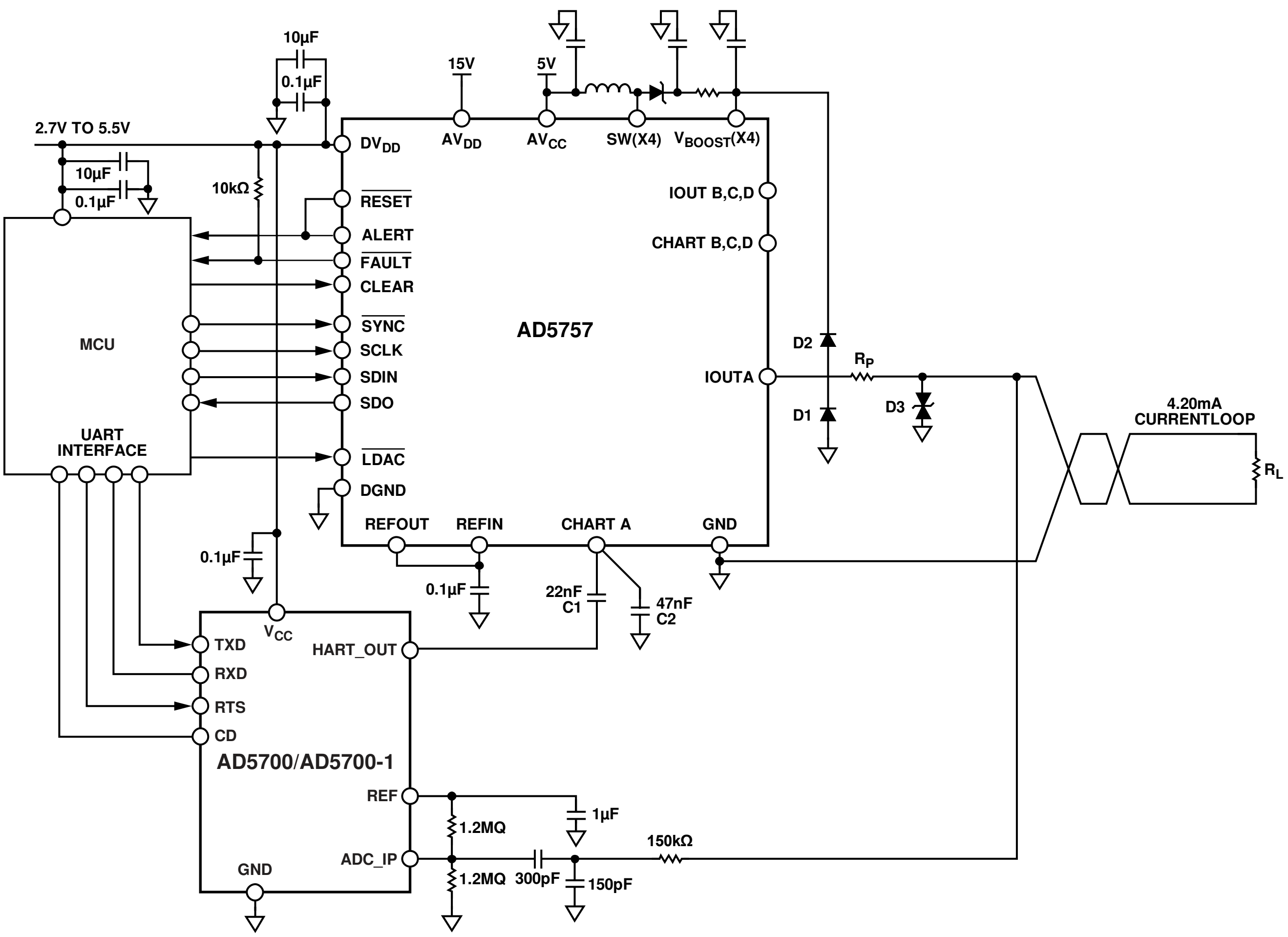


Figure 67. AD5757 in HART Configuration

OUTLINE DIMENSIONS

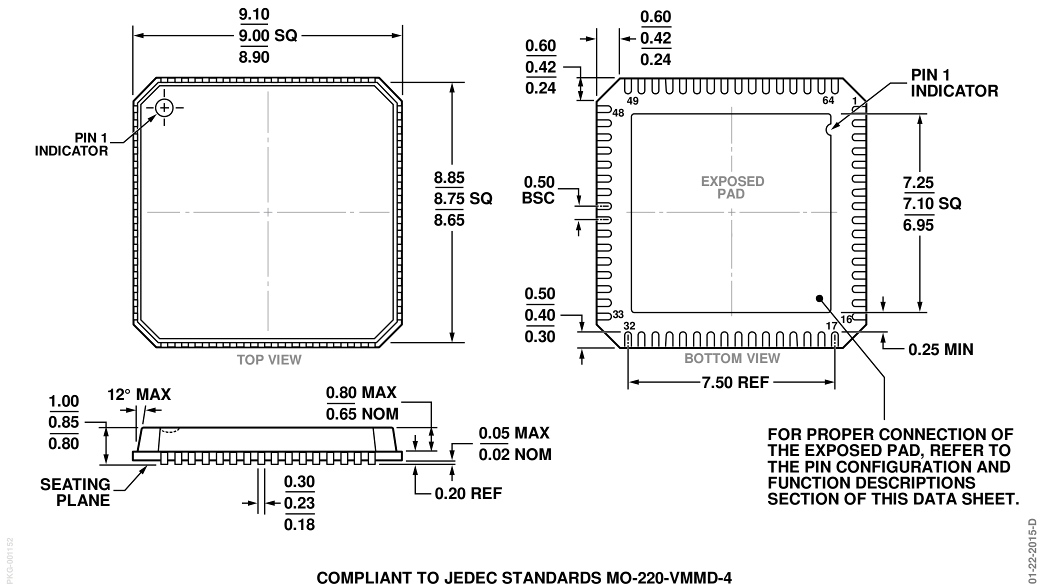


Figure 68. 64-Lead Lead Frame Chip Scale Package [LFCSP_VQ]
9 mm × 9 mm Body, Very Thin Quad
(CP-64-3)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1, 2]	Resolution (Bits)	Temperature Range	Package Description	Package Option
AD5757ACPZ	16	−40°C to +105°C	64-Lead Lead Frame Chip Scale Package [LFCSP_VQ]	CP-64-3
AD5757ACPZ-REEL7	16	−40°C to +105°C	64-Lead Lead Frame Chip Scale Package [LFCSP_VQ]	CP-64-3
EVAL-AD5755-1SDZ			Evaluation Board	

[1] Z = RoHS Compliant Part.
[2] The EVAL-AD5755-1SDZ can be used to evaluate the AD5757.

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