ASC Breakout Board User Guide

FPGA-EB-02023 Version 1.1, September 2018

Introduction

Thank you for choosing the Lattice Semiconductor ASC Breakout Board.

This guide describes how to begin using the L-ASC10 (ASC) Breakout Board, an easy-to-use platform for evaluating and designing with the ASC programmable hardware management expander. This board is designed for use with a Lattice FPGA evaluation board such as the Platform Manager 2 evaluation board. The board cannot be used stand-alone as the ASC works with an FPGA to function as a programmable hardware management controller.

The contents of this user guide include a description of the various portions of the evaluation board, the complete set of schematics and the bill of material for the ASC Breakout Board. The ASC Breakout Board is also known as the L-ASC10 Evaluation Board.

Features

The ASC Breakout Board features the following on-board components and circuits:

- L-ASC10 (ASC) Hardware Management Expander
- Two Potentiometers for Voltage Monitor Testing
- One Push-Button Switch as GPIO Input
- One 8-bit DIP Switch for I^2C Address Selection
- Nine LEDs for GPIO Output
- Two PNP Transistors for Temperature Monitoring
- Jumpers for Reset and Voltage Configuration
- Header for Connection to FPGA Breakout Board
- Footprints for 4 x DC-DC Converters and Components for Trimming Evaluation
- Footprints for 5 V Hot Swap Circuit and 12 V Hot Swap Circuit
- Footprint for 12 V Input DC-DC Converter

The features are described in more detail in the Board Hardware Features.

ASC Breakout Board Photos

Photographs of the top and bottom of ASC Breakout Board are shown in Figure 1 and Figure 2 below. These photographs show the board with the Hot Swap and Trim circuits populated (which are not populated in the released version of the breakout board). See Board Hardware Features for more detail on which circuits are populated on the breakout board. Component location references are relative to the top of the board with the silk screen text in the readable orientation (as shown in the photo).

Figure 1. ASC Breakout Board - Top View

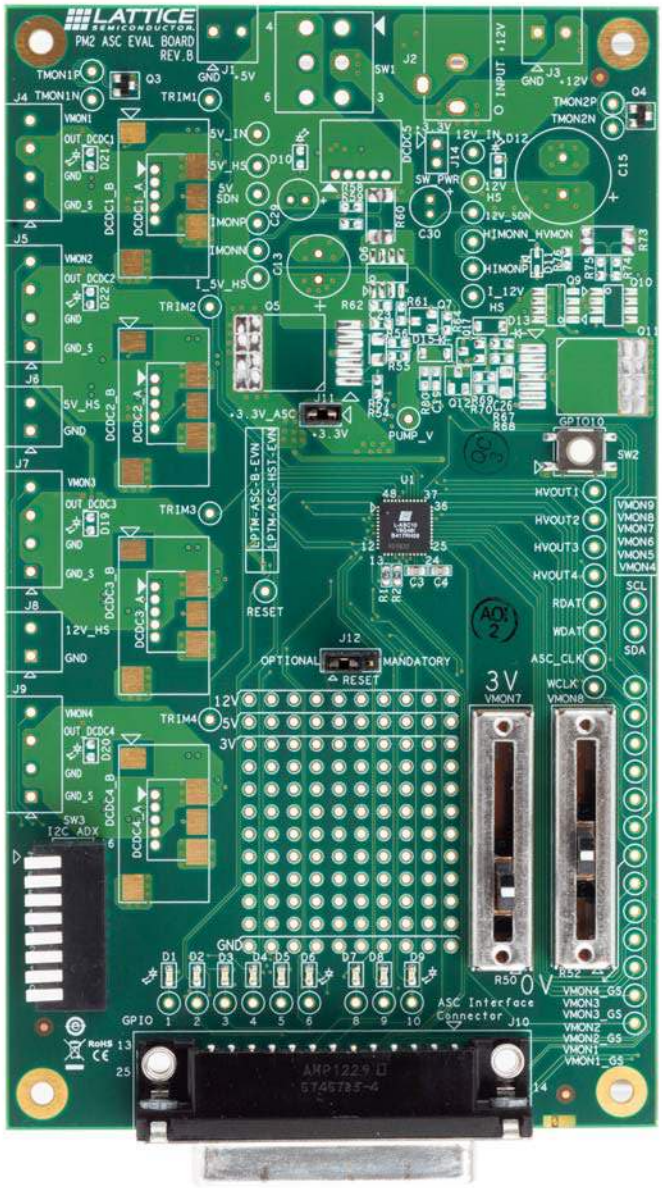
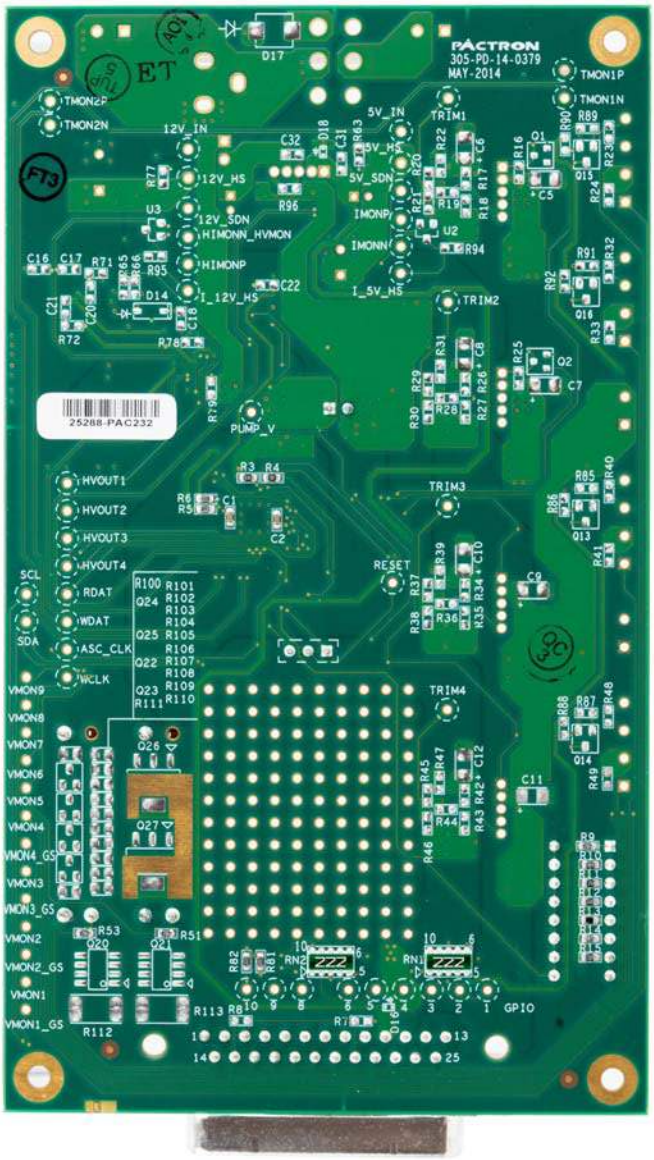


Figure 2. ASC Breakout Board - Bottom View



Board Hardware Features

The ASC Breakout Board is provided with a limited set of circuits populated. The circuits populated on the breakout board are described first. The breakout board also includes connections and footprints for evaluating the trimming and Hot Swap functions of the ASC. These unpopulated circuits are described in the later part of this section.

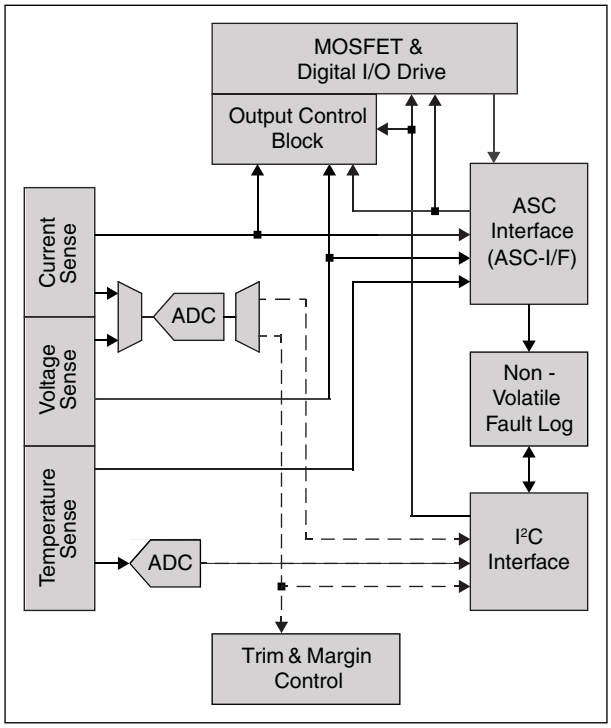
L-ASC10 (ASC) Device

The L-ASC10 (Analog Sense and Control - 10 rail) is a Hardware Management (Power, Thermal, and Control Plane Management) Expander designed to be used with Lattice FPGAs to implement the Hardware Management Control function in a circuit board. The L-ASC10 (referred to as ASC) enables seamless scaling of power supply voltage and current monitoring, temperature monitoring, sequence and margin control channels. The ASC includes dedicated interfaces supporting the exchange of monitor signal status and output control signals with these centralized hardware management controllers. Up to eight ASC devices can be used to implement a hardware management system.

The list below summarizes the hardware features of the ASC used on the breakout board. These features are also shown in the block diagram in Figure 3. For detailed information on the operation of each feature, see FPGA-DS-02038, L-ASC10 Data Sheet.

- Voltage Monitors (VMON) – Nine standard channels and one high voltage channel
- Current Monitors (IMON) – One standard voltage and one high voltage
- Temperature Monitors (TMON) – Two external and one internal
- Trim and Margin Circuits (TRIM) – Four channels
- General Purpose I/O (GPIO) – Nine channels
- High Voltage Outputs (HVOUT) – Four channels
- ASC Interface (ASC-I/F) – Connection to main FPGA
- I^2C Interface – A/D Converter measurement interface

Figure 3. ASC Block Diagram



Voltage Monitoring

There are 10 VMON inputs to the analog section of the device (including the HIMONN_HVMON pin). These are routed to slide potentiometers, board power supplies (not populated), and the on-board Hot Swap circuits (not populated).

Most of the voltage monitors on the breakout board have low value series resistors connected between the on-board components and the voltage monitors. These series resistors are populated so that the on-board voltage monitor test points can be driven by an off-board source without damaging the on-board components. These series resistors are not required for a real-world application board.

All voltages can be read out from the A/D converter using I^2C. The VMON signal connections and board components are described in Table 1. The schematic sheet location for the given components and signals are also listed (see the Appendix A. Schematics section).

Table 1. Voltage Monitor Components and Signals

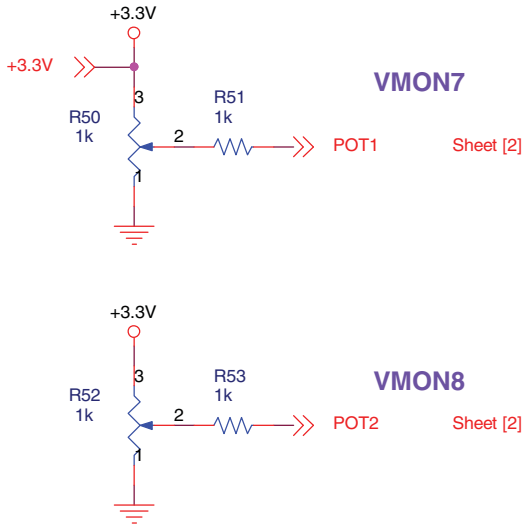
Component / Signals	Ref. Des.	Schematic Sheet	Description
Components Populated on Breakout Board			
Slider Potentiometers (POT1 and POT2)	R50, R52	5	1 kΩ slider pot: provides a variable Voltage from zero to 3.3 V. Connected to VMON7 and VMON8 of U1 with a 1k series resistor.
Series Resistors	R51, R53	5	1 kΩ resistor allows the user to safely drive VMON7 and VMON8 test points with an off-board Voltage source.
Series Resistors	R5[1], R6[1]	2	270 Ω resistor allows the user to safely drive VMON5 and VMON6 test points with an off-board Voltage source.

Component / Signals	Ref. Des.	Schematic Sheet	Description
Components Not Populated on Breakout Board			
Series Resistors	R23[1], R32[1]	3	270 Ω resistor allows the user to safely drive VMON1 and VMON2 test points with an off-board voltage source. (Only needed when DCDC1 and DCDC2 are populated.)
Ground Sense Resistors	R24[1], R33[1]	3	100 Ω resistor allows the user to safely drive the VMON1_GS and VMON2_GS test points with an off-board voltage source (such as remote load sensing) without adding or removing components. (Only needed when DCDC1 and DCDC2 are populated.)
Series Resistors	R40[1], R48[1]	4	270 Ω resistor allows the user to safely drive VMON3 and VMON4 test points with an off-board voltage source. (Only needed when DCDC3 and DCDC4 are populated.)
Ground Sense Resistors	R41[1], R49[1]	4	100 Ω resistor allows the user to safely drive the VMON3_GS and VMON4_GS test points with an off-board voltage source (such as remote load sensing) without adding or removing components. (Only needed when DCDC3 and DCDC4 are populated.)
Signals			
VMON1 / GS_VMON1		2, 3	Connected to DCDC1 output – 5 V – via R23 series resistor. Also connected to J4 terminal. See the Closed Loop Trimming (Not Populated) section for more details.
VMON2 / GS_VMON2		2, 3	Connected to DCDC2 output – 3.3 V – via R32 series resistor. Also connected to J5 terminal. See the Closed Loop Trimming (Not Populated) section for more details.
VMON3 / GS_VMON3		2, 4	Connected to DCDC3 output – 2.5 V – via R40 series resistor. Also connected to J4 terminal. See the Closed Loop Trimming (Not Populated) section for more details.
VMON4 / GS_VMON4		2, 4	Connected to DCDC4 output – 1.2 V – via R48 series resistor. Also connected to J4 terminal. See the Closed Loop Trimming (Not Populated) section for more details.
VMON5		2, (6), 9	5 V switched input supply to 5 V Hot Swap circuit via R5 series resistor. Connected to SW1 in Board Power circuit. See the 5 V Hot Swap (Not Populated) section for more details.
VMON6		2, (6)	5 V rail supply from either main FPGA board or Hot Swap output via R6 series resistor. See the 5 V Hot Swap (Not Populated) section for more details.
VMON7		2, 5	Potentiometer 1 (R50) via R51 series resistor
VMON8		2, 5	Potentiometer 2 (R52) via R53 series resistor
VMON9		2, (7), 9	12 V switched input supply to 12 V Hot Swap circuit via R65 (part of resistor divider). Connected to SW1 in Board Power circuit. See the 12 V Hot Swap (Not Populated) section for more details.
HVMON (HIMONN_HVMON)		2, 7	12 V rail supply from either main FPGA board or Hot Swap output. See the 12 V Hot Swap (Not Populated) section for more details.

1. Not required for customer designs; this is only needed to support demonstrations on the breakout board.

The two potentiometers (R50 and R52) are tied to VMON7 and VMON8 these can be used to simulate a fault or trip a comparator (see Figure 4). The slide potentiometers provide a voltage in the range of 0 V to 3.3 V depending on their position. R51 and R53 are 1 kΩ series resistors which allow for the connection of an off-board source directly to the VMON7 and VMON8 test points. The voltage on either potentiometer can be read out from the A/D converter using the I^2C port.

Figure 4. Voltage Monitor Potentiometer Circuits

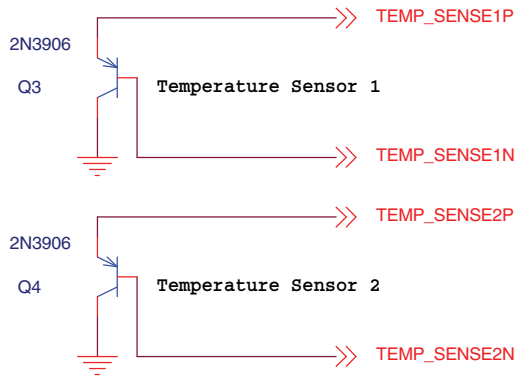


Temperature Monitoring

The board has PNP transistors mounted in the two corners opposite the main D-SUB connector. The PNP transistors are connected in the beta-compensated PNP temperature monitor configuration (preferred configuration for temperature monitors), as shown in Figure 5.

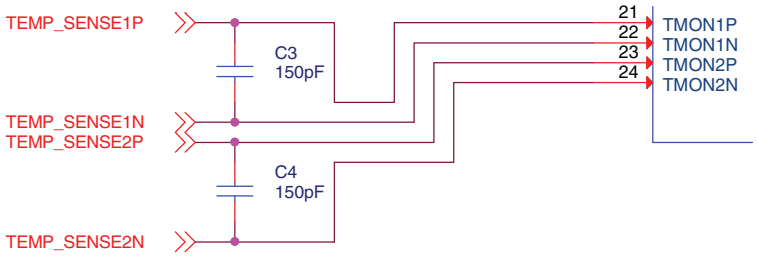
Provided the temperature monitors are enabled in the design, the temperature of each sensor can be read out using I^2C. The sensors can also be used to simulate over or under-temperature faults.

Figure 5. Temperature Monitor Circuits



The temperature sensors have 150 pF filter capacitors (C3 and C4) connected across the differential signals to improve noise-immunity that are located close to the ASC device, as shown in Figure 6.

Figure 6. Temperature Monitor Connections



The temperature monitor components and signals are summarized in Table 2 below.

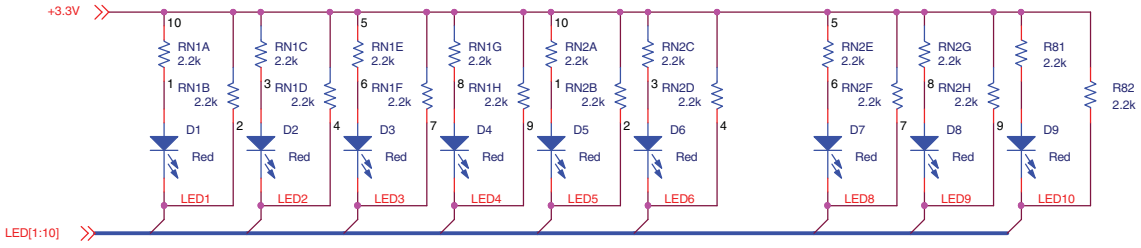
Table 2. Temperature Monitor Components and Signals

Component / Signals	Ref. Des.	Schematic Sheet	Description
Components Populated on Breakout Board			
Temperature Sensor	Q3, Q4	5	2N3906 PNP Transistor connected in Beta-Compensated PNP configuration.
Series Resistors	C3, C4	2	150 pF input filter capacitors for temperature monitoring signals to reject noise.
Signals			
TEMP_SENSE1P / TEMP_SENSE1N		2, 5	Input from temperature sensor to TMON1 (temperature monitor input) of L-ASC10
TEMP_SENSE2P / TEMP_SENSE2N		2, 5	Input from temperature sensor to TMON2 (temperature monitor input) of L-ASC10

LED Outputs

The ASC Breakout Board has 9 LEDs tied to the ASC open-drain outputs. The LEDs are pulled up to 3.3 V and are lit when GPIO1-GPIO10 are driven to a logic low (GPIO7 is not bonded out of the ASC). The LED circuit is shown in Figure 7 below (taken from Sheet 8 of the schematic).

Figure 7. ASC GPIO LEDs

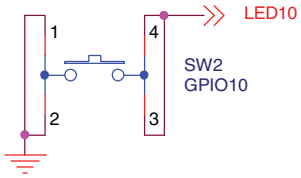


Push Button

The breakout board has one push-button (SW2), shown in Figure 8 (taken from Sheet 5 of the schematic). This signal is routed to GPIO10 of the ASC. This GPIO must be configured as an input in Platform Designer in order to use the push-button. When the button is pressed, GPIO10 is set to 0. When the button is released, GPIO10 is pulled to 1 by R82 (see the LED outputs section). The input signal can be used in the logic design of the main board FPGA.

GPIO10 is shared with LED10, pressing the push-button (SW2) will cause LED10 to illuminate.

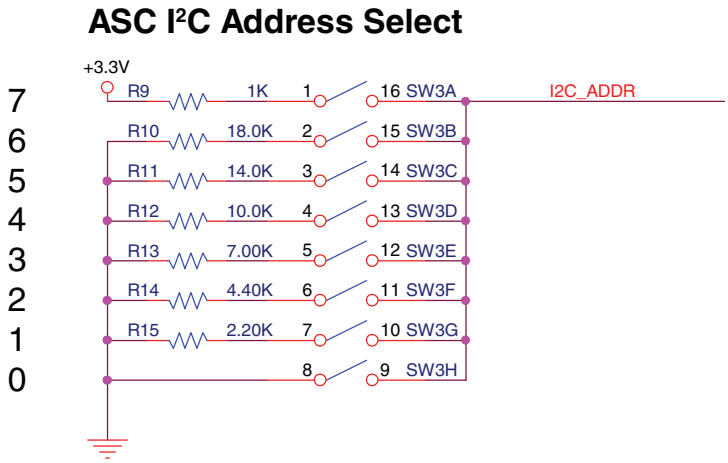
Figure 8. Push-Button Circuit



I²C Address Selection DIP Switch

The ASC Breakout Board provides an 8-position DIP switch for I²C address selection of the ASC device. The switch combines with a set of on-board resistors (R9 – R15) to connect to the I2C_ADDR pin of the device (shown in Figure 9, taken from Sheet 2 of the schematic). Each switch corresponds to a different resistor setting and address selection (see the ASC Datasheet for more details). The ASC device only checks the resistor setting at power-on-reset, updating the switches while the board is powered will have no effect. Only one switch should be closed at a time.

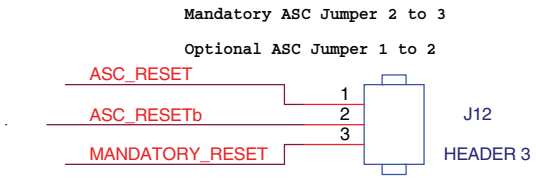
Figure 9. I²C Address Selection DIP Switch



Reset Configuration Jumper

The ASC on the breakout board can be configured as a Mandatory ASC or Optional ASC. This setting is configured in the Platform Designer software and described in the System Connections section of the ASC datasheet. The position of jumper J12 (shown in Figure 10, from Sheet 2 of the schematic) should match the setting in the software. This jumper routes the ASC RESETb signal to either the Mandatory Reset signal or to the Optional Reset signal on the ASC Interface Connector.

Figure 10. Reset Configuration Jumper



ASC Interface Connector

The ASC Interface Connector (shown in Figure 11 from Schematic Sheet 2) is used to connect the ASC Breakout Board to the main FPGA Board. The connector has been designed to pair with other available Lattice Evaluation Boards, including the Platform Manager 2 Evaluation Board (see the related literature section for more details).

The connector includes all the mandatory signals for connecting the ASC device to the hardware management controller as described in the system connections section of the ASC datasheet. This includes the ASC-Interface Signals, the I2C signals, and the Clock and Reset signals. The connector also includes a set of power rails as described in Table 3. Additionally, the connector provides the 5 V and 12 V Hot Swap signals.

Figure 11. ASC Interface Connector

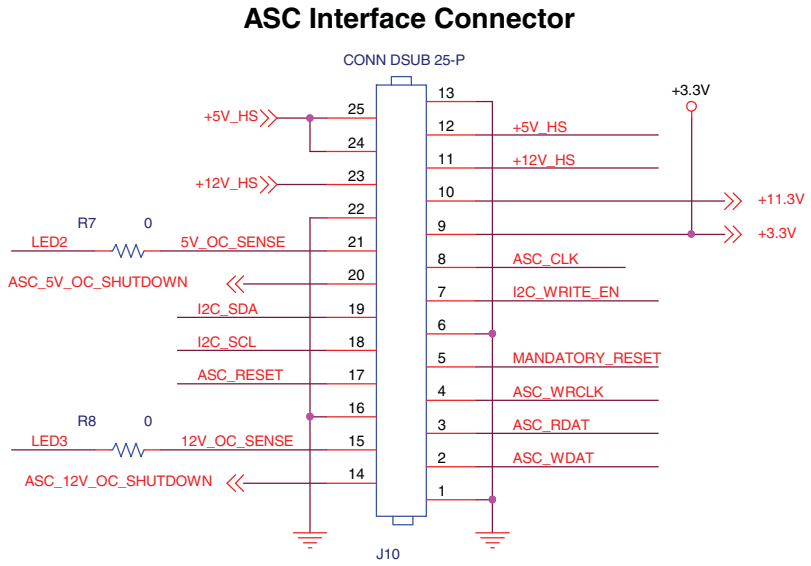


Table 3. ASC Interface Connector Pin Description

Pin #	Signal Name	Description
1	GND	Shared ground signal with main FPGA Board
2	ASC_WDAT	ASC-Interface Signal – must be connected to FPGA PIO and assigned in Diamond
3	ASC_RDAT	ASC-Interface Signal – must be connected to FPGA PIO and assigned in Diamond
4	ASC_WRCLK	ASC-Interface Signal – must be connected to FPGA PIO and assigned in Diamond
5	MANDATORY_RESET	RESETb signal if ASC device is declared as mandatory in Platform Designer. Must match J12 setting (Reset Configuration). Must be connected to FPGA PIO and assigned in Diamond.
6	GND	Shared ground signal with main FPGA Board
7	I2C_WRITE_EN	Connected to GPIO1 through R4. Used with optional ASC Write Protect feature. Connect to FPGA PIO and assign in Diamond if this feature is used.
8	ASC_CLK	8-MHz Clock Output by ASC0 in ASC hardware management controller systems. This signal is NC for all non-ASC0 ASC devices. ASC0 devices should connect to FPGA PCLK input and assign to ASCCLK signal in Diamond

Pin #	Signal Name	Description
9	+3.3V	ASC Supply Voltage. Provided by FPGA board or 12 V power supply (power supply not populated on Breakout Board).
10	+11.3V	Voltage rail generated from diode OR of +12V_SW and +5_SW input supplies. FPGA main board may use as input to 12 V DC-DC converters.
11	+12V_HS	12 V supply rail. Output from either 12 V Hot Swap circuit or main FPGA board. This rail is the input for DCDC1 and DCDC2.
12	+5V_HS	5 V supply rail. Output from either 5 V Hot Swap circuit or main FPGA board. This rail is the input for DCDC3 and DCDC4.
13	GND	Shared ground signal with main FPGA Board
14	ASC_12V_OC_SHUTDOWN	Output from main FPGA board, connected to fast shutoff transistor (Q12) of 12 V Hot Swap circuit. Assign to FPGA PIO in Platform Designer and Diamond when using 12 V Hot Swap.
15	12V_OC_SENSE	Output from ASC device (connected to GPIO3 through R8). Used as fast shutdown alarm to main FPGA board. Assign to FPGA PIO in Platform Designer and Diamond when using 12 V hot swap.
16	GND	Shared ground signal with main FPGA Board
17	ASC_RESET	RESETb signal if ASC device is declared as optional in Platform Designer. Must match J12 setting (Reset Configuration). Must be connected to FPGA PIO and assigned in Diamond.
18	I2C_SCL	I^2C Clock Signal. Should be connected to FPGA SCL pin. Main FPGA board should include pull-up resistors. Used for programming the ASC device.
19	I2C_SDA	I^2C Data Signal. Should be connected to FPGA SDA pin. Main FPGA board should include pull-up resistors. Used for programming the ASC device.
20	ASC_5V_OC_SHUTDOWN	Output from main FPGA board, connected to fast shutoff transistor (Q7) of 5 V Hot Swap circuit. Assign to FPGA PIO in Platform Designer and Diamond when using 5 V Hot Swap.
21	5V_OC_SENSE	Output from ASC device (connected to GPIO2 through R7). Used as fast shutdown alarm to main FPGA board. Assign to FPGA PIO in Platform Designer and Diamond when using 5 V Hot Swap.
22	GND	Shared ground signal with main FPGA Board
23	+12V_HS	12 V supply rail. Output from either 12 V Hot Swap circuit or main FPGA board. This rail is the input for DCDC1 and DCDC2.
24	+5V_HS	5 V supply rail. Output from either 5 V Hot Swap circuit or main FPGA board. This rail is the input for DCDC3 and DCDC4.
25	+5V_HS	5 V supply rail. Output from either 5 V Hot Swap circuit or main FPGA board. This rail is the input for DCDC3 and DCDC4.

Closed Loop Trimming (Not Populated)

The ASC provides four Closed Loop Trim (CLT) cells which are used to accurately trim and margin power supplies. The ASC Breakout Board provides four DC-DC converter and trimming circuit footprints on the breakout board. Table 4 lists the components and signal associated with CLT operation on the ASC Breakout Board.

Table 4. Closed Loop Trim Components & Signals

Component / Signals	Ref. Des.	Schematic-Sheet	Description
Components Not Populated on Breakout Board			
DC-DC Converter	DCDC1_A / DCDC1_B	3	Dual-footprint +12 V input adjustable output power supply. Trim circuit shown in schematic for DCDC1_A (NQR002A0X4Z) at 5 V output.
DC-DC Converter	DCDC2_A / DCDC2_B	3	Dual-footprint +12 V input adjustable output power supply. Trim circuit shown in schematic for DCDC2_A (NQR002A0X4Z) at 3.3 V output.
DC-DC Converter	DCDC3_A / DCDC3_B	4	Dual-footprint +5 V input adjustable output power supply. Trim circuit shown in schematic for DCDC3_A (NQR002A0X4Z) at 2.5 V output.
DC-DC Converter	DCDC4_A / DCDC4_B	4	Dual-footprint +5 V input adjustable output power supply. Trim circuit shown in schematic for DCDC4_A (NQR002A0X4Z) at 1.2 V output.
N-Channel MOSFET – SOT-23	Q1, Q2	3	FDV301N N-Channel MOSFET. Inverts the DC-DC enable signal from ASC GPIO8 / GPIO9 and shifts the level up to +12 V.
Green Indicator LED	D19, D20, D21, D22	3, 4	LED indicates output of DC-DC is active.
LED Bias Resistor	R86, R88, R90, R92	3, 4	470 Ω resistor limits the LED current.
NPN Transistor – SOT-23	Q13, Q14, Q15, Q16	3, 4	2N3904 NPN Transistor drives LED on when DC-DC output is active.
NPN Bias Resistor	R85, R87, R89, R91	3, 4	4.7 kΩ resistor limits the base current of NPN transistor.
Tantalum Cap	C5, C7, C9, C11	3, 4	6.8 µF, 20 V capacitor DC-DC input filter.
Tantalum Cap	C6, C8, C10, C12	3, 4	10 µF, 6.8 V capacitor DC-DC output filter.
DC-DC Output Load Resistor	R22,R31, R39, R47	3, 4	1k, 680, 470 and 330 Ω resistors pull DC-DC outputs down to zero when disabled.
DCDC1 Trim Resistors	R17 – R21	3	Resistor values based on Platform Designer Trim Calculator for DCDC1_A at 5 V.
DCDC2 Trim Resistors	R26 – R30	3	Resistor values based on Platform Designer Trim Calculator for DCDC2_A at 3.3 V.
DCDC3 Trim Resistors	R34 – R38	4	Resistor values based on Platform Designer Trim Calculator for DCDC3_A at 2.5 V.
DCDC4 Trim Resistors	R42 – R46	4	Resistor values based on Platform Designer Trim Calculator for DCDC4_A at 1.2 V.
Phoenix 4-Terminal Connector DCDC1-4	J4, J5, J7, J9	3, 4	Wire to board connectors to apply off-board loads to DC-DC with remote sensing.
Signals			
LED8		2, 3	DCDC1 control signal from GPIO8. Safe state is high. Inverted via Q1.
LED9		2, 3	DCDC2 control signal from GPIO9. Safe state is high. Inverted via Q1.
LED4		2, 4	DCDC3 control signal from GPIO4. Safe state is low.

Component / Signals	Ref. Des.	Schematic-Sheet	Description
LED5		2, 4	DCDC4 control signal from GPIO5. Safe state is low.
OUT_DCDC1		2, 3	DCDC1 Output connected to VMON1 via R23.
OUT_DCDC2		2, 3	DCDC2 Output connected to VMON2 via R32.
OUT_DCDC3		2, 4	DCDC3 Output connected to VMON3 via R40.
OUT_DCDC4		2, 4	DCDC4 Output connected to VMON4 via R48.
TRIM_DCDC1		2, 3	DCDC1 Trim signal from TRIM1.
TRIM_DCDC2		2, 3	DCDC2 Trim signal from TRIM2.
TRIM_DCDC3		2, 4	DCDC3 Trim signal from TRIM3.
TRIM_DCDC4		2, 4	DCDC4 Trim signal from TRIM4.

Overview of Trim and Margin

The board provides footprints for four DC-DC modules. Since all four are similarly designed and laid out, this section will provide an overview of the DC-DC circuit rather than provide a separate section for each DC-DC. Footprints are provided for both 5-pin SIP modules and DOSA power converters. The circuits shown in the schematic appendix support the NQR002A0X4 SIP from GE Industrial and the OKY-T/3-D12 DOSA converter from Murata. None of the components associated with the DC-DC operation (shown in Table 4) are populated on the breakout board.

The ASC Breakout board provides footprints and circuit connections for five trimming resistors for each DC-DC. These five resistors are shared by both the SIP and DOSA footprints because only one supply can be populated at a time. The resistors are organized in an “H” pattern both in the schematic and on the board layout. The resistors are named in the schematic to match the names used in the Platform Designer Trim-view calculator. The names are listed and described in Table 5 below. Typically only three resistors are suggested by the calculator; a pull-up, a pull-down, and a series resistor. The exact population of the “H” pattern depends on many factors that the calculator takes into account such as type of DC-DC, output voltage, and range of trim. The ASC Breakout board provides pads and connections to support any result from the Trim Calculator. However, with certain supplies and option settings, the calculator can produce a result that only uses two resistors: a pull-down and series resistor. The DC-DCs on the ASC Breakout board are populated with the two resistor solution. A key requirement for the calculator to produce a two-resistor solution is the Bi-Polar Zero (BPZ) voltage of the Trim Cell has to match the DC-DC internal reference voltage. Otherwise the calculator will add a pull-up or pull-down resistor in attempt to offset the imbalance between the BPZ voltage setting and DC-DC reference voltage. The values shown in the schematic have been calculated for the NQR002A0X4 SIP from GE Industrial. For more information on the Trim interface and Calculator please see AN6074, Interfacing the Trim Output of Power Manager II Devices to DC-DC Converters and the Platform Designer 3.1 User Guide.

Table 5. Trim Resistor "H-Network" Names.

Schematic Name	Calculator Name	Description
RpupS	RpupSupply	Pull Up Resistor at DC-DC Supply Trim input
RpdnS	RpdnSupply	Pull Down Resistor at DC-DC Supply Trim input
Rs	Rseries	Series Resistor between Trim DAC output and DC-DC Supply Trim input
RpupD	RpupDAC	Pull Up Resistor at Trim DAC output
RpdnD	RpupDAC	Pull Down Resistor at Trim DAC output

In order for the CLT circuits within the ASC to operate properly the output of the supply needs to be monitored by the correct VMON input. The ASC Breakout board illustrates the correct connections by using TRIM1 with VMON1 for DCDC1, TRIM2 with VMON2 for DCDC2, all the way to TRIM4 with VMON4 for DCDC4. As discussed in the Voltage Monitor Operation section, the DC-DC outputs are connected to the VMON inputs using a series resistor with a value of 270 Ω. The series resistor is not required in customer designs; its only function on the breakout board is to isolate the DC-DC outputs from the VMON test point. The VMON series resistor allows another voltage

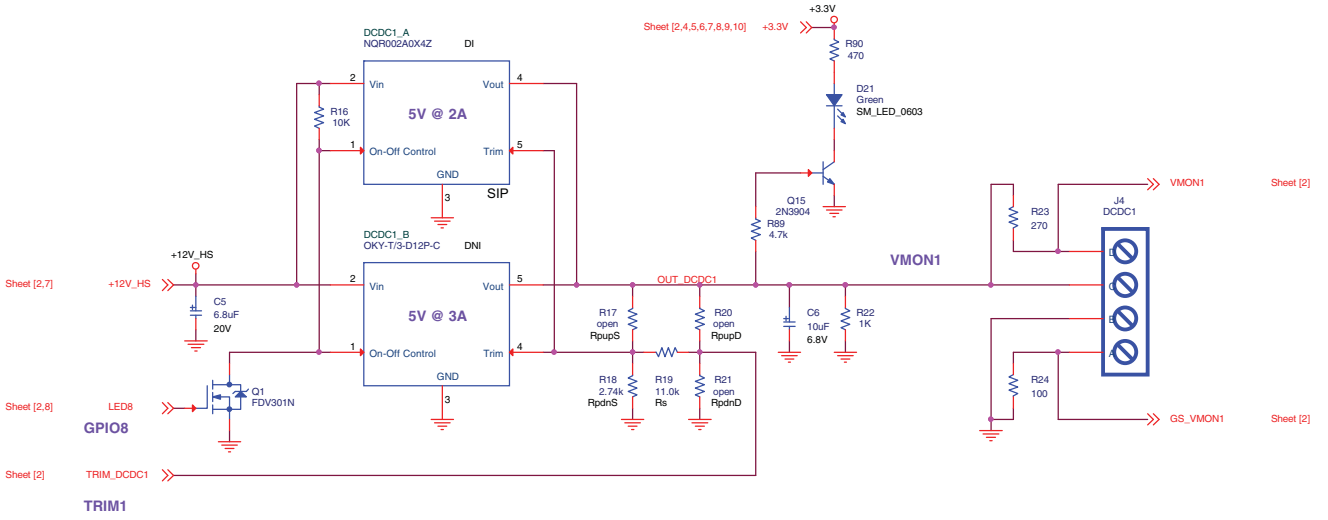
source to be applied to the VMON test point directly. If the voltage source is fairly weak, the VMON series resistor can be removed.

Each of the DC-DC supplies has a load resistor connected to the output. The load resistor is not required in customer designs as the supply is typically connected to a real load. The load resistor is only used on the breakout board to prevent the output of the supply from “creeping up” when the supply is disabled. Without the load resistor some disabled supplies may output around 1 Volt that can be read by either the VMON or a Digital Volt Meter (DVM). The load resistors are sized based on the target DC-DC supply output voltage; lower values for lower voltages and higher values for higher voltages. In all cases they are 1/10 watt packages so there is minimal heat generated.

DCDC1 – Enable and Trim

This section discusses the specific circuits that support DCDC1. In Figure 12 the control signal LED8, which comes from GPIO8, is inverted and level shifted by a small signal N-channel MOSFET (Q1 FDV301N). For +12 V supplies a buffer or inverter is needed because the ASC GPIOs can only be pulled up to +5.5 V. All GPIOs of the ASC have a “safe state” which defines the behavior independent of configuration during Power-On-Reset (POR) or during programming; the safe sate of GPIO8 is high. Both the DOSA and SIP supplies are enabled when the On-Off pin is high (positive enable logic). Since the enable signal is inverted by Q1, the supplies will be off during “safe state”. A 10 kΩ pull-up resistor (R16) to 12 V is used to insure a full logic swing at the enable input of the supplies. (Note that DCDC3 and DCDC4 do not require the MOSFET circuit, this is because there input supply is +5 V. See Table 6 for more details).

Figure 12. DCDC1 Trim and Control Circuit



The control signal LED8 is also used to turn on a red LED (D7) when it is low and pulled up to +3.3 V by a 2.2 kΩ resistor (RN2G – Sheet 8). Depending on the enable logic (positive or negative) of the installed supply, the illumination of LED D7 may not indicate that DCDC1 is enabled. (When the DC-DC converters from the schematic are used, DCDC1 and DCDC2 will be enabled when their control LED is illuminated. DCDC3 and DCDC4 will not be enabled when their control LED is illuminated. This is due to the inverting MOSFET used with DCDC1 and DCDC2). A separate green LED (D49) is used to indicate when the supply is enabled. An NPN transistor (Q15) is used to turn the green LED on when the supply has enough voltage to bias the emitter-base junction (slightly more than 0.7 V).

Supply filtering is provided by a 6.8 µF capacitor (C5) on the input and a 10 µF capacitor on the output (C6). These are located close to the DC-DC footprints to ensure their effectiveness. Note that these values may not be optimal for all supplies and loading conditions, specific filtering requirements should be followed from the DC-DC data sheet.

Table 6 shows a summary of the input voltage, output voltage, and control signal behavior for each of the four DC-DC converters. The +12V_HS and +5V_HS rails which are used to power the DC-DC converters can be provided by either the Hot Swap circuits or the ASC Interface Board connector. See the connector section for more details.

Table 6. Summary of DCDC Trim Circuits

DC-DC	Vin	Vout	VMON / Trim Channel	GPIO Enable Control	ON Logic Level	RpdnS	Rseries
1	+12V_HS	5 V	VMON1/TRIM1	GPIO8	0	2.74 kΩ	11.0 kΩ
2	+12V_HS	3.3 V	VMON2/TRIM2	GPIO9	0	4.42 kΩ	16.0 kΩ
3	+5V_HS	2.5 V	VMON3/TRIM3	GPIO4	1	6.34 kΩ	22.0 kΩ
4	+5V_HS	1.2 V	VMON4/TRIM4	GPIO5	1	20.0 kΩ	39.0 kΩ

Board Power Supplies (Not Populated)

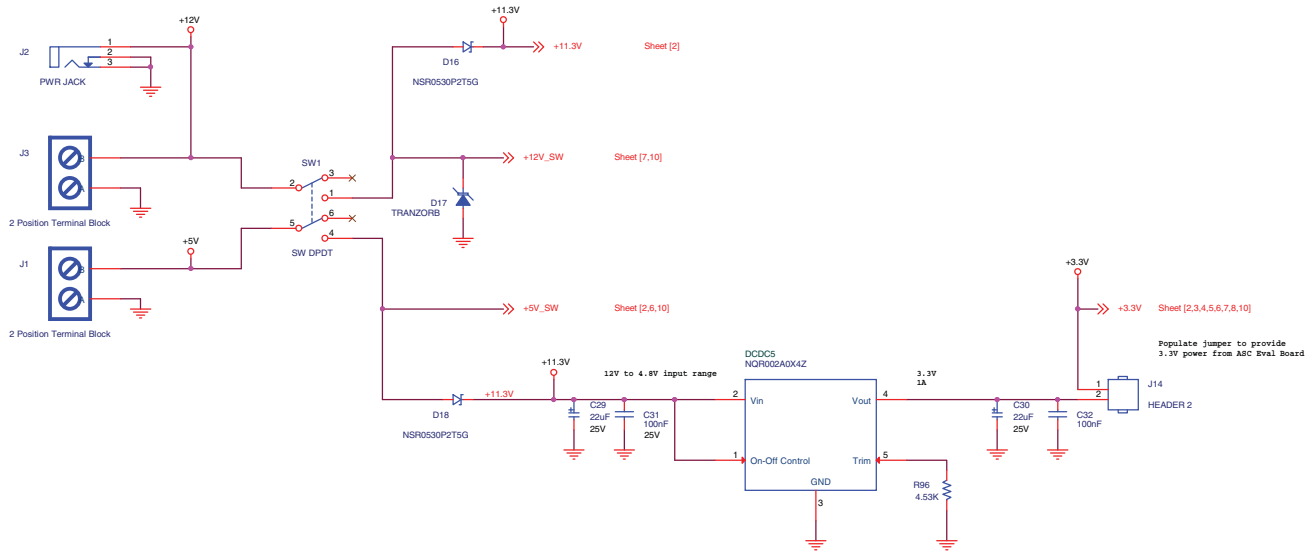
The breakout board is supplied by the +3.3 V rail from the ASC Interface connector. The breakout board also provides the footprint for the power supply circuit shown in Figure 13. Table 7 lists the power supply components on the ASC Breakout Board.

Table 7. Power Supply Components

Component	Ref. Des.	Schematic Sheet	Description
Components Not Populated on Breakout Board			
DC-DC Converter	DCDC5	9	SIP +12 V input power supply (NQR002A0X4Z) trimmed for 3.3 V output. Provides board power supply from +12 V or +5 V rails.
Power Jack	J2	9	+12 V AC Adapter connector.
Phoenix 2-Terminal Connector	J1, J3	9	Input terminal for +5 V supply voltage (J1) and +12 V supply voltage (J3)
Tranzorb TVS Diode	D17	9	Transient voltage suppressor diode – protects +12 V input from external voltage.
Schottky Diode	D16, D18	9	Schottky diodes for diode ORing for +11.3 V rail
Tantalum Capacitor	C29	9	22 µF, 25 V capacitor +12 V DC-DC input filter.
Ceramic Bypass Capacitors	C31, C32	9	100 nF 25 V capacitor +12 V DC-DC input and output filter.
Tantalum Capacitor	C30	9	22 µF, 25 V capacitor +12 V DC-DC output filter.
Trim Resistor	R96	9	4.53 kΩ trim resistor, sets DCDC5 output voltage at +3.3 V
2-pin Header	J14	9	Selects +3.3 V sources – populating with jumper sources +3.3 V from +11.3 V rail, unpopulated sources +3.3 V from ASC Interface Board connector

The terminal connector J1 connects the +5 V supply to the SW1 power switch. Either the J2 power supply jack or J3 terminal connect the +12 V supply to SW1. Switching SW1 to the on position will connect the terminals to the +12V_SW supply rail and the +5V_SW supply rail. The +12V_SW supply rail is connected to the D17 TRANZORB to protect the board from voltage transients. These voltage rails are the input supplies to the 12 V Hot Swap and 5 V Hot Swap circuits.

Figure 13. Board Power Supply Circuit



The +12 V connects through schottky diode D16 to the +11.3 V rail, while the +5 V connects through schottky diode D18 to the +11.3 V rail. Through this configuration, the +11.3 V rail will be sourced by either the +12V_SW rail (if present) or the +5V_SW rail (if present and +12V_SW rail not present). The +11.3 V rail is connected to the ASC Interface connector. This rail may be used as an input to a 12 V DC-DC converter on the main FPGA board.

The +11.3 V rail is also used as the input voltage to DCDC5. DCDC5 steps down the +11.3 V input to a +3.3 V output voltage. The +11.3 V is buffered and filtered by C29 and C31. The +3.3 V output is buffered and filtered by C30 and C32. The +3.3 V output voltage is set by the 4.53 kΩ resistor (R96) connected to the DCDC5 Trim pin.

The header J14 is used to connect the DCDC5 output to the +3.3 V rail using a 2-pin jumper. Placing a jumper on J14 will supply the ASC Breakout Board +3.3 V from DCDC5. It will also provide +3.3 V to the ASC Interface Connector – this will power the FPGA main board from only the +12V_SW input on the ASC Breakout Board. No other input supply is required.

5 V Hot Swap (Not Populated)

The ASC Breakout Board provides a set of footprints and connections for implementing a 5 V Hot Swap circuit using the ASC's built in hardware. Table 8 lists the components and signals associated with 5 V Hot Swap operation on the ASC Breakout Board.

Table 8. 5 V Hot Swap Components and Signals

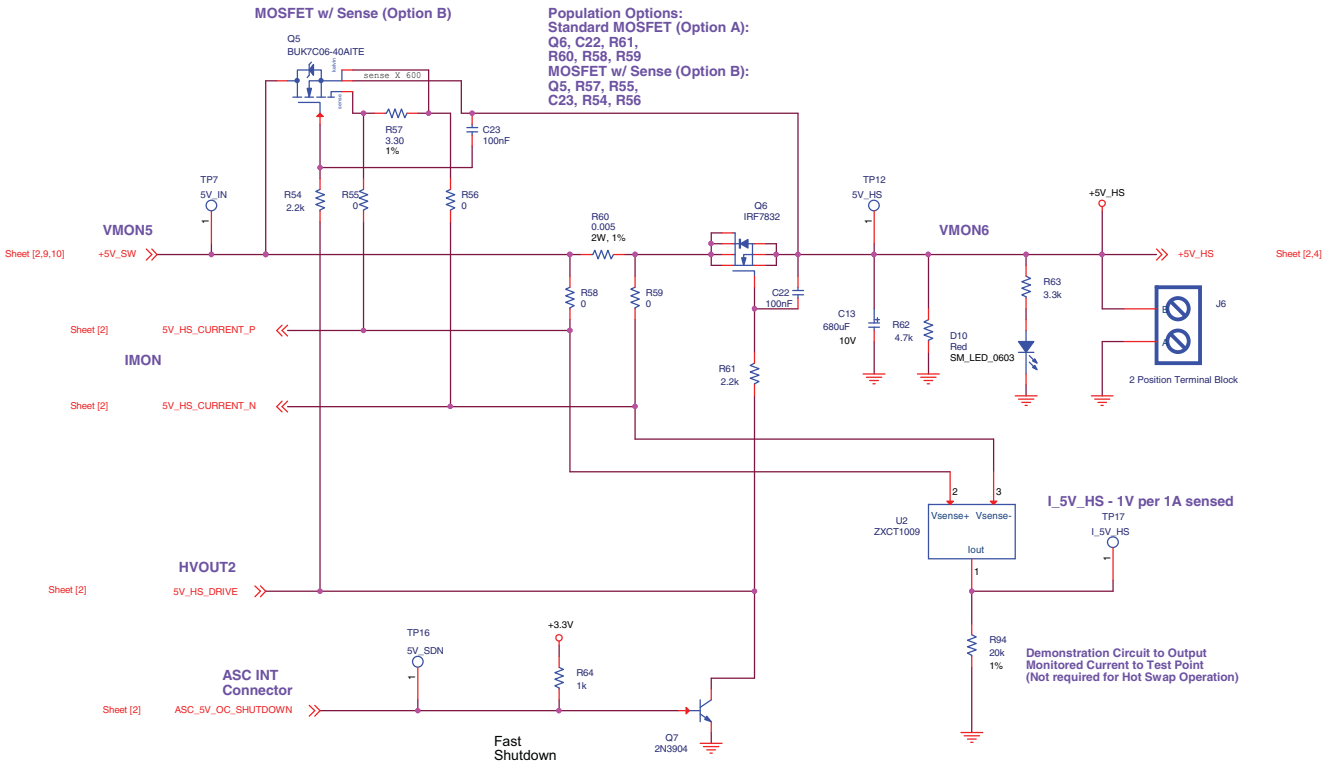
Component / Signals	Ref. Des.	Schematic Sheet	Description
Components Not Populated on Breakout Board			
Current sense resistor	R60[2]	6	5 mΩ 2 W resistor for supply side current monitoring with IMON1 input of ASC
IMON1 Isolation Resistor	R58[2], R59[2]	6	Zero Ω resistors – support population option for standard MOSFET versus MOSFET with Sense output
MOSFET Switch	Q6[2]	6	N-Channel MOSFET load-side Hot Swap switch supplies power to +5V_HS and load capacitor C13.
Gate Drive Resistor	R61[2]	6	2.2 kΩ resistor, located close to MOSFET Q6, limits parasitic oscillations at the gate of Q6. Works with C22 to slow switching at Q6, limiting current ripple during hysteretic switching.
Gate-Source Capacitor	C22[2]	6	100 nF capacitor, works with R61 to slow switching at Q6, limiting current ripple during hysteretic switching.

Component / Signals	Ref. Des.	Schematic Sheet	Description
MOSFET with Sense Output	Q5[3]	6	N-Channel MOSFET supply-side Hot Swap switch supplies power to +5V_HS and load capacitor C13. Sense output provides proportional current to drain current.
Gate Drive Resistor	R54[3]	6	2.2 kΩ resistor, located close to MOSFET Q5, limits parasitic oscillations at the gate of Q5. Works with C23 to slow switching at Q5, limiting current ripple during hysteretic switching.
Current sense resistor	R57[3]	6	3.30 Ω sense resistor for supply-side current monitoring with IMON1 input of ASC, connected to Sense output of MOSFET (Q5)
IMON1 Isolation Resistor	R55[3], R56[3]	6	Zero Ω resistors – support population option for MOSFET with Sense output versus standard MOSFET
Gate-Source Capacitor	C23[3]	6	100 nF capacitor, works with R54 to slow switching at Q5, limiting current ripple during hysteretic switching.
Load Capacitors	C13[1]	6	680 µF 10 V Bulk capacitance emulates a Hot Swap load.
Discharge Resistors	R62[1]	6	4.7 kΩ Resistor discharges load capacitor between Hot Swaps.
LED Bias Resistor	R63	6	3.3 kΩ resistor limits the LED current for D10.
Red Indicator LED	D10	6	LED to indicate Hot Swap has completed successfully.
Phoenix 2-Terminal Connector	J6	6	+5V_HS terminal block connector
Current Sense Amplifier	U2[1]	6	ZXCT1009 current sense amplifier – provides output current proportional to voltage across Vsense+ and Vsense-. Used for demonstration purpose only, not required in application.
Current Sense Output Resistor	R94[1]	6	20 kΩ resistor, sets output voltage at I_5V_HS test point to 1 V / 1A drain current of MOSFET.
NPN Fast Shutoff Transistor	Q7	6	NPN transistor, provides fast pull-down of Q5/Q6 gate voltage, enables fast shutdown from FPGA via ASC Interface connector during Hot Swap faults
Shutoff Transistor Pull-up Resistor	R64	6	1 kΩ pull-up resistor – biases Q7 ON by default (shutting off Q5/Q6).
Signals			
+5V_SW		2, 6	5 V input voltage, from Power Supply circuit and J1
5V_HS_DRIVE		2, 6	HVOUT2 signal from ASC
ASC_5V_OC_SHUTDOWN		2, 6	FPGA PIO signal, from ASC Interface Connector
5V_HS_CURRENT_P		2, 6	Connected to IMON1A_P, positive current monitor terminal
5V_HS_CURRENT_N		2, 6	Connected to IMON1A_N, negative current monitor terminal
+5V_HS		2, 4, 6	5 V Hot Swap output voltage, provided to J6 terminal block, ASC Interface Connector, and DCDC1 and 2 input voltage
Additional Test Points			
I_5V_HS			Current Sense Amplifier Output Voltage – 1 V per 1A

1.Not required for customer designs; this is only needed to support ASC device evaluation.
2.Only populate for 5 V Standard MOSFET Hot Swap. Populate only from either Note 2 or Note 3, never both.
3.Only populate for 5 V MOSFET with Sense output Hot Swap. Populate only from either Note 3 or Note 3, never both.

The 5 V Hot Swap circuit is designed to support two separate implementations. The Standard MOSFET implementation uses a standard power MOSFET (Q6) and a 5 mΩ sense resistor (R60). The MOSFET with Sense output implementation uses a power MOSFET with current sense output (Q5) and a 3.30 Ω sense resistor. The Standard MOSFET implementation is a Load-based Hot Swap implementation with the MOSFET connected between the current sensing resistor and the load capacitor. The MOSFET with Sense output implementation is a Supply-based Hot Swap implementation with the MOSFET connected between the supply and the current sensing resistor. The full 5 V Hot Swap circuit is shown in Figure 14 below.

Figure 14. 5 V Hot Swap Circuit



The Hot Swap circuit is designed to work with the Hot Swap component in the Platform Designer software. Platform Designer will automatically generate the Hot Swap algorithm and device configuration based on user defined settings for input voltage, MOSFET characteristics, load capacitance, and other parameters. For more detail on the Hot Swap algorithm and working with Hot Swap in Platform Designer, see the References section.

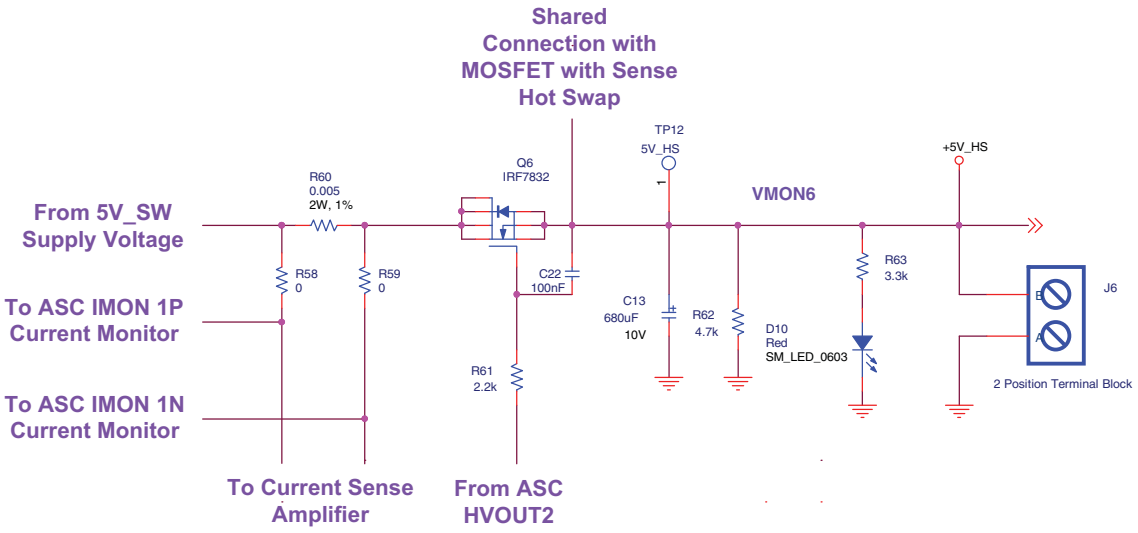
The Hot Swap circuit can be broken into three sections in order to understand the operation of the overall circuit:

- Hot Swap
  - Load-Based Using Standard MOSFET
  - Supply-Based Using MOSFET with Sense Output
- Fast Shutdown Circuit
- Current Sensing Test Circuit

Load-Based Hot Swap (Standard MOSFET)

The circuit in Figure 15 illustrates the Load-based Hot Swap using Standard MOSFET. The Load-based Hot Swap circuit has Q6 connected between the current sensing resistor R60 and the load capacitor. The N type MOSFET Q6 is controlled by the high voltage output (HVOUT2) from the ASC. The gate resistor (R61) and gate-source capacitor (C22) are used to maintain a soft turn on of Q6. The increased gate capacitance smooths out the current during the hysteretic control stage (see the References section for more details on the Hot Swap behavior).

Figure 15. 5 V Hot Swap - Load-Based, Standard MOSFET



The signals 5V_HS_CURRENT_P and 5V_HS_CURRENT_N are connected to the IMON1P and IMON1N signals of the ASC. The sensing resistor R60 is connected through the zero Ω isolation resistors (R58, 59) to the ASC using Kelvin connections and differential layout techniques to maximize the current sensing accuracy at the IMON1 inputs.

The +5V_HS signal is used by the Hot Swap function to monitor the load capacitor C13 voltage using VMON6 of the ASC. The Hot Swap function monitors the load capacitor C13 voltage for the following reasons:

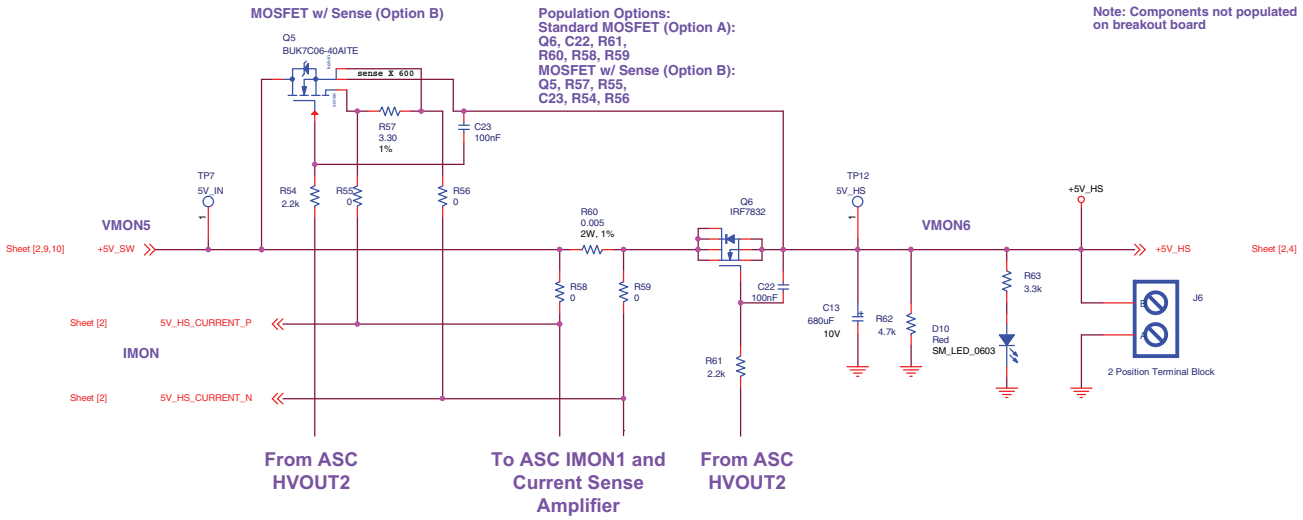
- to see that C13 is charging up and there is not a short or open in the circuit
- to see that C13 has reached a voltage where a higher current limit can be used
- to know when C13 is close to the 5 V supply voltage – Hot Swap is complete.

When Hot Swap is disabled R62 provides a discharge path for C13 to prepare the circuit for subsequent Hot Swaps. LED D10 and bias resistor R63 give a visual indication that the Hot Swap process is complete.

Supply-Based Hot Swap (MOSFET with Sense Output)

The circuit in Figure 16 illustrates the Supply-based Hot Swap using a MOSFET with Sense output. (Components from the Standard MOSFET Hot Swap are shown to illustrate the shared connections between the two circuits. Q6, R58, R59, R60, R61, C22 should not be populated when the MOSFET with Sense output is used.) The MOSFET with Sense output variation has Q5 connected to the supply side of R57. The SENSE output of Q5 provides a current proportional to the current flowing through the MOSFET drain (the BUK7C06 shown in the schematic has a typical drain current to sense current ratio of 615). The N type MOSFET Q5 is controlled by the HVOUT2 output from the ASC. The gate resistor (R54) and gate-source capacitor (C23) are used to maintain a soft turn on of Q5. The increased gate capacitance smooths out the current during the hysteretic control stage (see the References section for more details on the Hot Swap behavior).

Figure 16. 5 V Hot Swap - Supply Based, SENSEFET



The signals 5V_HS_CURRENT_P and 5V_HS_CURRENT_N are connected to the IMON1P and IMON1N signals of the ASC. In the MOSFET with Sense output variation, R57 is used as the sensing resistor. R57 is tied between the sense current output and the Kelvin source pin of MOSFET Q5. R57 is connected through the zero Ω isolation resistors (R55, 56) to the ASC using Kelvin connections and differential layout techniques to maximize the current sensing accuracy at the IMON1 inputs.

VMON6 is used by the Hot Swap function to monitor the load capacitor C13 voltage. The Hot Swap function monitors the load capacitor C13 voltage for the following reasons:

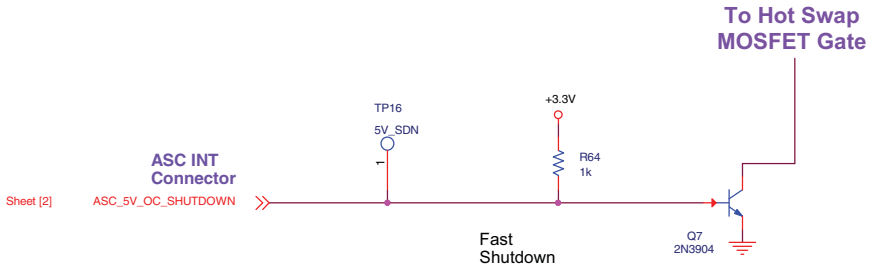
- to see that C13 is charging up and there is not a short or open in the circuit
- to see that C13 has reached a voltage where a higher current limit can be used
- to know when C13 is close to the 5 V supply voltage – Hot Swap is complete.

When Hot Swap is disabled R62 provides a discharge path for C13 to prepare the circuit for subsequent Hot Swaps. LED D10 and bias resistor R63 give a visual indication that the Hot Swap process is complete.

Fast Shutdown Circuit

The fast shutdown circuit for the 5 V Hot Swap is shown in Figure 17 below. The ASC_5V_OC_SHUTDOWN signal is output from the main FPGA board via the ASC Interface Connector. The ASC_5V_OC_SHUTDOWN signal is active high, and by default pulled up to 3.3 V by R64. When ASC_5V_OC_SHUTDOWN is high, Q7 is biased on. This will pull the MOSFET gate low, holding the MOSFET off (see the Hot Swap circuit description above for more details). When ASC_5V_OC_SHUTDOWN is driven low, Q7 will be biased off. When Q7 is turned off, the Hot Swap MOSFET will be controlled by the ASC HVOUT2 voltage. The fast shutdown feature can be implemented using the Hot Swap component in Platform Designer. Assign the FPGA PIO connected to ASC_5V_OC_SHUTDOWN on the main FPGA board to the Fast Shut Down feature in Platform Designer. See the Reference section for more details.

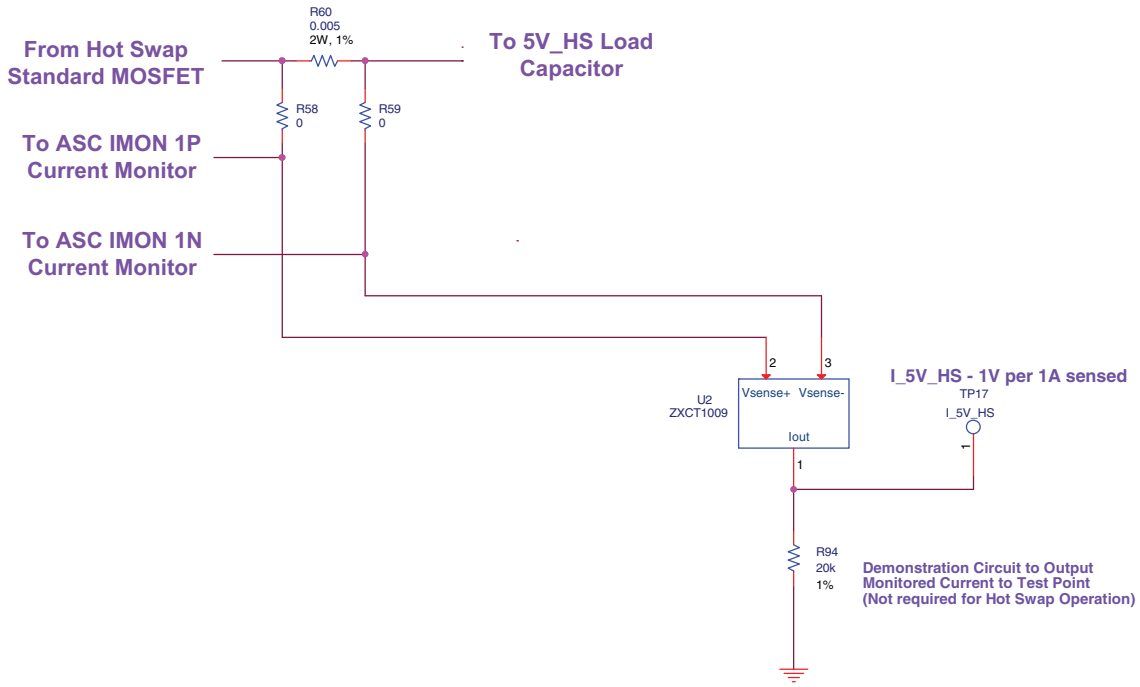
Figure 17. 5 V Hot Swap – Fast Shutdown Circuit



Current Sense Feedback Circuit

The 5 V Hot Swap circuit on the ASC Breakout board includes a current sense feedback circuit, shown in Figure 18. The purpose of this circuit is for demonstration and evaluation only, it does not need to be included on a customer application board. The current sense amplifier (U2 – ZXCT1009 from Diodes, Inc) provides an output current proportional to the voltage measured over R60. Based on the R60 resistance (5 mΩ) and the R94 resistance (20 kΩ), the ratio of output voltage at TP17 (I_5V_HS) to sensed current across R60 is about 1 V / 1A (this ratio is also maintained when Q5 and R57 are used instead of Q6 and R60). The test point I_5V_HS can be monitored on an oscilloscope to confirm the Hot Swap operation and evaluate the current behavior during Hot Swap. The internal current sense amplifier in the ASC is used in the Hot Swap algorithm, the circuit formed by U2 and R94 is only included to provide observable current feedback during the evaluation stage.

Figure 18. 5 V Hot Swap - Current Sense Feedback Circuit



12 V Hot Swap (Not Populated)

The ASC Breakout Board provides a set of footprints and connections for implementing a 12 V Hot Swap circuit using the ASC's built in hardware. Table 9 lists the key elements associated with 12 V Hot Swap operation on the ASC Breakout Board.

Table 9. 12 V Hot Swap Components and Signals

Component / Signals	Ref. Des.	Schematic Sheet	Description
Components Not Populated on Breakout Board			
Voltage Divider Resistor	R65, R66	7	3 kΩ (R65) and 1.02 kΩ (R66) to divide +12V_SW rail down to below 5.9 V limit for VMON input
Zener Diode	D11	7	Zener Diode for VMON input protection. Limits VMON9 input during transients and overvoltage.
MOSFET Switch	Q9[2], Q10	7	N-Channel MOSFET Supply-side Hot Swap switches supply power to +12V_HS and load capacitor C15.
Gate Drive Resistor	R71[2], R72	7	2.2 kΩ resistors, located close to MOSFETs Q9 & Q10, limits parasitic oscillations at the gates of Q9 & Q10. Works with C2, C21 to slow switching at Q9 & Q10, limiting current ripple during hysteretic switching.
Gate-Source Capacitor	C20[2], C21[2]	7	100nF capacitors, works with R71 & R72 to slow switching at Q9 & Q10, limiting inrush current during Hot Swap start and current ripple during hysteretic switching.
Current Sense Resistor	R73	7	10 mΩ 3 W resistor for load side current monitoring with HIMON input of ASC
HIMON Snubbing Resistor	R74[2], R75[2]	7	Snubber resistors (paired with C16, C17) protect HIMON input from momentary overvoltage, including inductive flyback voltages when Q9 and Q10 are turned off. Population option to support standard MOSFET Q9 versus MOSFET with Sense output Q11.
MOSFET with Sense Output	Q11[3]	7	N-Channel MOSFET supply-side Hot Swap switch supplies power to +12V_HS and load capacitor C15 with Q10. Sense output provides proportional current to drain current.
Gate Drive Resistor	R67[3]	7	2.2 kΩ resistor, located close to MOSFET Q11, limits parasitic oscillations at the gate of Q11. Works with C26 to slow switching at Q11, limiting current ripple during hysteretic switching.
Current sense resistor	R68[3]	7	6.20 Ω resistor for supply-side current monitoring with HIMON input of ASC using MOSFET with Sense output
HIMON Snubbing Resistor	R69[3], R70[3]	7	Snubber resistors (paired with C16, C17) protect HIMON input from momentary overvoltage, including inductive flyback voltages when Q10 and Q11 are turned off. Population option to support MOSFET with Sense output Q11 versus standard MOSFET Q9.
Gate-Source Capacitor	C26[3]	7	100 nF capacitor, works with R67 to slow switching at Q11, limiting inrush current during Hot Swap start and current ripple during hysteretic switching.
HIMON Snubbing Capacitor	C16, C17	7	Snubber capacitors (paired with snubbing resistors) protect HIMON input from momentary overvoltage, including inductive flyback voltages when MOSFETs are turned off.
Load Capacitors	C15[1]	7	1000 µF 25 V Bulk capacitance emulates a Hot Swap load.
Discharge Resistors	R76[1]	7	10 kΩ Resistor discharges load capacitor between Hot Swaps.
LED Bias Resistor	R77	7	10 kΩ resistor limits the current through LED D12
Red Indicator LED	D12	7	LED to indicate 12 V Hot Swap is complete
Phoenix 2-Terminal Connector	J8	7	+12V_HS terminal block connector

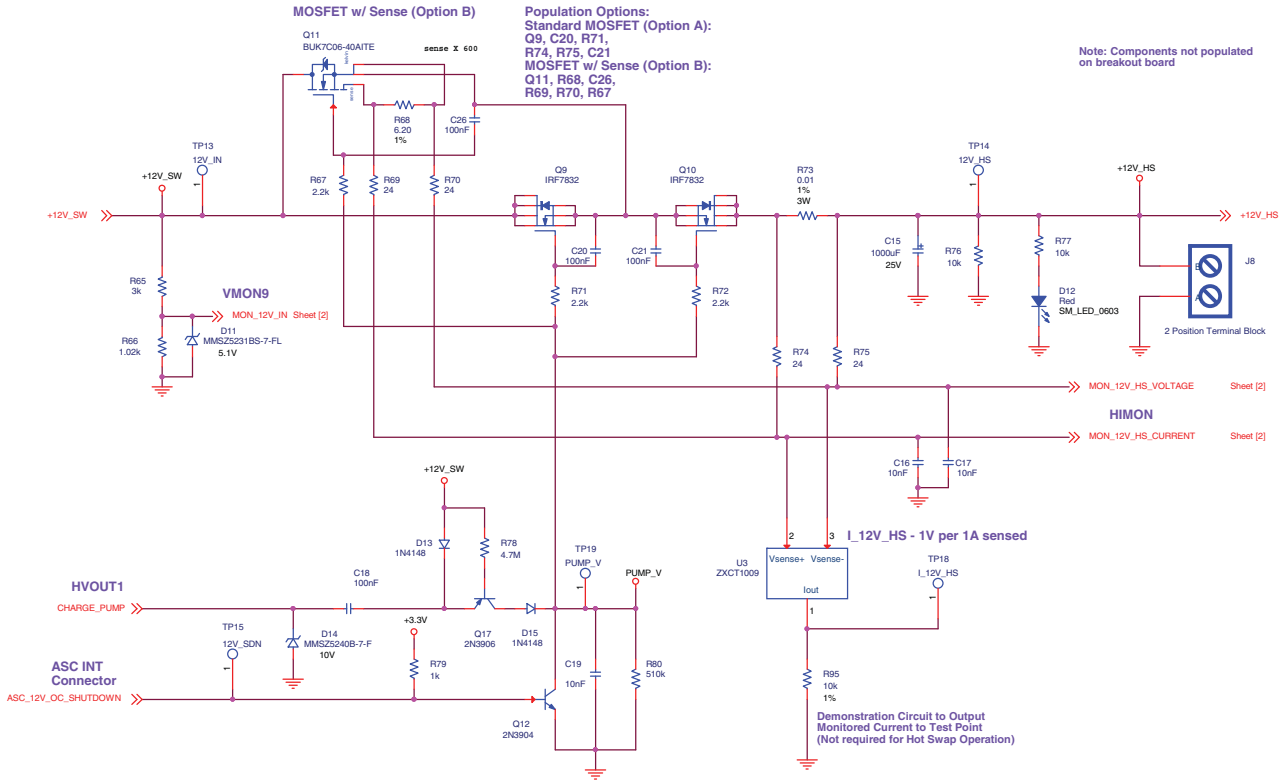
Component / Signals	Ref. Des.	Schematic Sheet	Description
Charge Pump Supply Diode	D13	7	Diode provides path for current from +12V_SW supply to charge C18 when HVOUT1 = 0 V
NPN Bias Resistor	R78	7	4.7 MΩ resistor limits the base current of NPN transistor, maintains NPN base voltage close to +12V_SW supply voltage
NPN Transistor – SOT-23	Q17	7	NPN transistor, only biased ON when C18 voltage rises above +12V_SW supply voltage. Transistor stays off when HVOUT1 and charge pump are disabled – protects Q12 from thermal stress
HVOUT Protection Zener Diode	D14	7	Zener Diode for HVOUT1 protection. Limits HVOUT1 voltage in case of transients on +12V_SW supply
Charge Pump Serial Capacitor	C18	7	100 nF capacitor, works with D13 to add +12V_SW voltage to HVOUT1 voltage
Charge Pump Diode	D15	7	Diode provides path for current from C18 (via Q17) to charge C19 to boosted voltage
Charge Pump Buffer Capacitor	C19	7	Stores boosted charge pump voltage. Boosted voltage drives MOSFET gate to fully conduct +12V_SW input supply to +12V_HS and C15 load capacitor (controlled by Hot Swap algorithm).
Charge Pump Discharge Resistor	R80	7	10 kΩ resistor, provides discharge path for C19 when Hot Swap is disabled
NPN Fast Shutoff Transistor	Q12	7	NPN transistor, provides fast pull-down of Q9/Q10/Q11 gate voltages, enables fast shutdown from FPGA via ASC Interface connector during Hot Swap faults
Shutoff Transistor Pull-up Resistor	R79	7	1 kΩ pull-up resistor – biases Q12 ON by default (shutting off Q9/Q10/Q11).
Current Sense Amplifier	U3[1]	7	ZXCT1009 current sense amplifier – provides output current proportional to voltage across Vsense+ and Vsense-. Used for demonstration purpose only, not required in application.
Current Sense Output Resistor	R95[1]	7	20 kΩ resistor, sets output voltage at I_12V_HS test point to 1 V / 1A drain current of MOSFET.
Signals			
+12V_SW		7, 9	12 V input voltage, from Power Supply circuit and J2/J3
MON_12V_IN		2, 7	12 V input voltage, divided down below 5.9 V, connected to VMON9
CHARGE_PUMP		2, 7	HVOUT1 signal from ASC, switched signal to charge pump circuit
ASC_12V_OC_SHUTDOWN		2, 7	FPGA PIO signal, from ASC Interface Connector
MON_12V_HS_VOLTAGE		5, 7	Connected to HIMONN_HVMON, negative current monitor terminal and high voltage monitor input
MON_12V_HS_CURRENT		2, 7	Connected to HIMONP, positive current monitor terminal
Separate Test Points			
I_12V_HS		7	Current Sense Amplifier Output Voltage – 1 V per 1A
PUMP_V		7	Charge Pump output voltage for Gate Drive

1.Not required for customer designs; this is only needed to support ASC device evaluation.
2.Only populate for 12 V standard MOSFET Hot Swap. Populate only from either Note 2 or Note 3, never both.
3.Only populate for 12 V MOSFET with Sense output Hot Swap. Populate only from either Note 3 or Note 3, never both.

The 12 V Hot Swap circuit is designed to support two separate implementations. The standard MOSFET implementation uses standard power MOSFETs (Q9 and Q10) and a 10 mΩ sense resistor (R73). The MOSFET with Sense output implementation uses a power MOSFET with current sense output (Q11) along with a standard power MOSFET (Q10) and a 6.20 Ω sense resistor (R68). Both circuits are Supply-based Hot Swap implementations with the MOSFETs connected between the supply and the current sensing resistors. The full 12 V Hot Swap circuit is

shown in Figure 19 below.

Figure 19. 12 V HS Circuit



The Hot Swap circuit is designed to work with the Hot Swap component in the Platform Designer software. Platform Designer will automatically generate the Hot Swap algorithm and device configuration based on user defined settings for input voltage, MOSFET characteristics, load capacitance, and other parameters. For more detail on the Hot Swap algorithm and working with Hot Swap in Platform Designer, see the References section.

The Hot Swap circuit can be broken into five sections in order to understand the operation of the overall circuit:

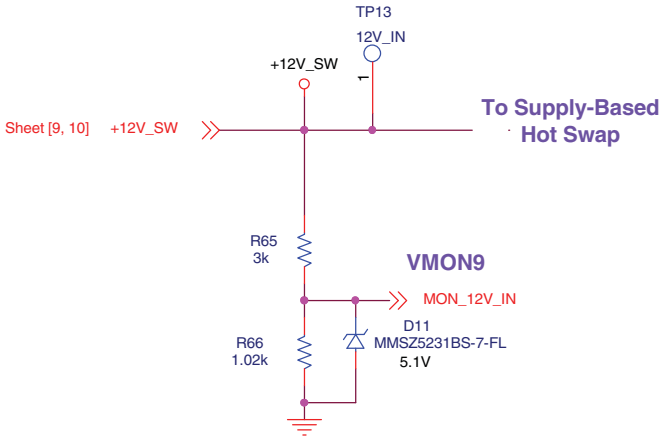
- Input Voltage Monitor
- Charge Pump
- Supply-Based Hot Swap
  - Using Standard MOSFET
  - Using MOSFET with Sense Output
- Fast Shutdown Circuit
- Current Sensing Test Circuit

Input Voltage Monitor

VMON9 is used to monitor the input voltage. The voltage monitors have a max input voltage of 5.9 V, so the circuit in Figure 20 below is required to monitor the 12 V input rail. R65 and R66 divide down the voltage within the operating range of the VMON. (The voltage at VMON9 will be approximately 25% of the voltage at +12V_SW). These resistors can be input into the Platform Designer tool in the Voltage view, and platform designer will automatically scale the trip points up to the input of the resistive divider.

D11 is included in the circuit to protect the voltage monitor input from transient voltages above the 5.9 V input voltage. The clamp voltage of 5.1 V is well below the 5.9 V max operating voltage for the VMON channel.

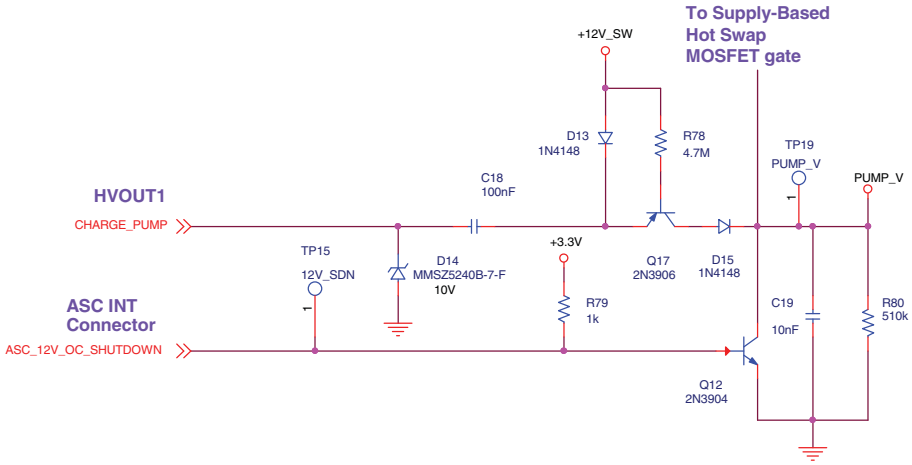
Figure 20. 12 V Hot Swap - Input Voltage Monitor Circuit



Charge Pump

The 12 V Hot Swap circuit requires a charge pump to boost the gate voltage to around 20 V to fully turn on the MOSFET to conduct 12 V. The circuit shown in Figure 21 is used to implement this external charge pump using diodes, capacitors, and a transistor.

Figure 21. 12 V Hot Swap - Charge Pump Circuit



The CHARGE_PUMP signal is output from HVOUT1. The Hot Swap component in Platform Designer will configure HVOUT1 in the switched mode output, so that the output will toggle between 12 V and 0 V with an 81.25% duty cycle at 31.25 kHz. D14 is connected to the CHARGE_PUMP signal to protect the HVOUT1 signal from transient voltages which may be present on the +12V_SW rail. D14 will clamp transient voltages above 10 V, keeping the HVOUT1 voltage below the 13.2 V maximum operating voltage.

When the CHARGE_PUMP signal is at 0 V, C18 will be charged to the +12V_SW voltage through diode D13. At this time, PNP transistor Q17 will be off, due to the emitter-base voltage being below the Q17 cutoff voltage (the emitter voltage will be around +12V_SW minus 0.7 V, while the base voltage is +12V_SW).

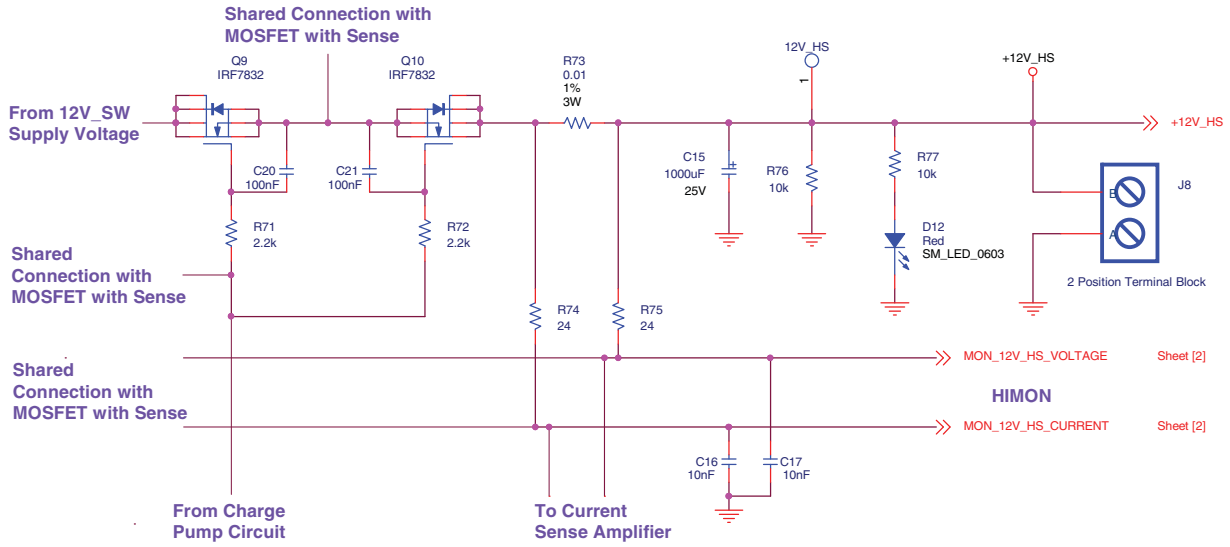
When the CHARGE_PUMP signal toggles up to 12 V, the voltage on C18 will be added to the CHARGE_PUMP output voltage, resulting in the generation of approximately 22 V at the junction of C18 and D13. This voltage will result in an emitter-base voltage that will bias on Q17 (the emitter voltage will be around 22 V, while the base voltage is +12V_SW). The 22 V will conduct through Q17 and D15 to charge up C19. C19 stores the voltage which is seen at the gate of the Hot Swap MOSFETs, and the MOSFETs will turn on as C19 is charged up. R80 provides a

discharge path for C19 when the charge pump is disabled. The PUMP_V test point can be used for monitoring the charge pump voltage level.

Supply-Based Hot Swap (Standard MOSFET)

The circuit in Figure 22 illustrates the Supply-Based Hot Swap using Standard MOSFETs. The Supply-Based Hot Swap circuit has Q9 and Q10 connected between the supply and the current sensing resistor R73. The N type MOSFETs Q9 and Q10 are controlled by the output of the charge pump circuit (the charge pump is controlled by HVOUT1). Q9 and Q10 have their sources tied together. Q9 is connected in such a way that it only conducts from the supply to the load when the gate is biased and the MOSFET is on. Q10 is connected in such a way that it only conducts from the load to the supply when the gate is biased and the MOSFET is on. Connecting the MOSFETs in this way ensures that the Hot Swap algorithm can fully control current flowing in to charge up the load capacitor C15 and the current flowing out from C15 to the input supply (in case of input supply brown out). The gate resistors (R71, R72) and gate-source capacitors (C20, C21) are used to maintain a soft turn on of Q9 and Q10. The increased gate capacitance limits inrush current during the initial Hot Swap turn on and smooths out the current during the hysteretic control stage (see the References section for more details on the Hot Swap behavior).

Figure 22. 12 V Hot Swap - Standard MOSFET Circuit



The signals MON_12V_HS_VOLTAGE and MON_12V_HS_CURRENT are connected to the HIMONN_HVMON and HIMONP signals of the ASC. These signals are protected from momentary over-voltage (including inductive flyback voltages when Q9 and Q10 are turned off) by the resistor (R74, R75) and capacitor (C16, C17) pair snubber circuit between the sensing resistor and the device inputs. The sensing resistor R73 is connected through the snubber circuit using Kelvin connections and differential layout techniques to maximize the current sensing accuracy at the HIMON inputs.

The MON_12V_HS_VOLTAGE signal is also used by the Hot Swap function to monitor the load capacitor C15 voltage using the HVMON of the ASC. The Hot Swap function monitors the load capacitor C15 voltage for the following reasons:

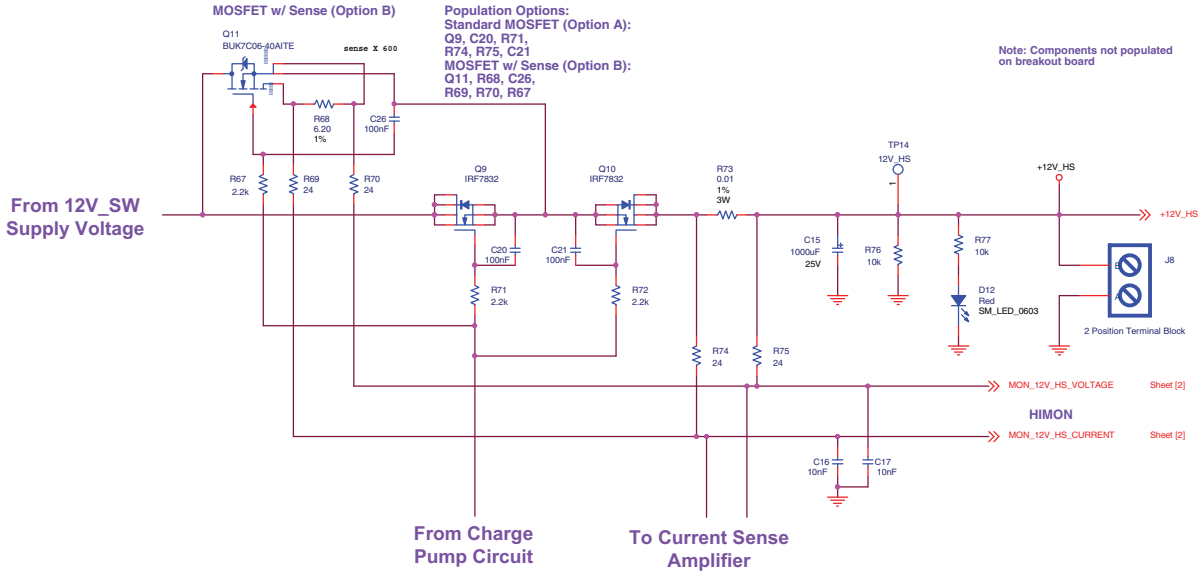
- to see that C15 is charging up and there is not a short or open in the circuit
- to see that C15 has reached a voltage where a higher current limit can be used
- to know when C15 is close to the 12 V supply voltage – Hot Swap is complete.

When Hot Swap is disabled R76 provides a discharge path for C15 to prepare the circuit for subsequent Hot Swaps. LED D12 and bias resistor R77 give a visual indication that the Hot Swap process is complete.

Supply-Based Hot Swap (MOSFET with Sense Output)

The circuit in Figure illustrates the Supply-based Hot Swap using a MOSFET with Sense output. (Components from the Standard MOSFET Hot Swap are shown also to illustrate the shared connections between the two circuits. Q9, R71, R74, R75, C20, and C21 are not used with the MOSFET with Sense output). The MOSFET with Sense output variation has Q11 and R68 connected with Q10 and R73, with Q11 on the supply side of R68. The SENSE output provides a current proportional to the current flowing through the MOSFET drain (the BUK7C06 shown in the schematic has a typical drain current to sense current ratio of 615). The MOSFET with Sense output (Q11) takes the place of Q9 in this variation. The N type MOSFETs Q10 and Q11 are controlled by the output of the charge pump circuit (the charge pump is controlled by HVOUT1). Q10 and Q11 have their sources tied together. Q11 is connected in such a way that it only conducts from the supply to the load when the gate is biased and the MOSFET is on. Q10 is connected in such a way that it only conducts from the load to the supply when the gate is biased and the MOSFET is on. Connecting the MOSFETs in this way ensures that the Hot Swap algorithm can fully control current flowing in to charge up the load capacitor C15 and the current flowing out from C15 to the input supply (in case of input supply brown out). The gate resistors (R67, R72) and gate-source capacitors (C26, C21) are used to maintain a soft turn on of Q11 and Q10. The increased gate capacitance limits inrush current during the initial Hot Swap turn on and smooths out the current during the hysteretic control stage (see the References section for more details on the Hot Swap behavior).

Figure 23. 12 V Hot Swap SENSEFET Circuit



The signals MON_12V_HS_VOLTAGE and MON_12V_HS_CURRENT are connected to the HIMONN_HVMON and HIMONP signals of the ASC. These signals are protected from momentary over-voltage (including inductive flyback voltages when Q11 and Q10 are turned off) by the resistor (R69, R70) and capacitor (C16, C17) pair snubber circuit between the sensing resistor and the device inputs. In the MOSFET with Sense output variation, R68 is used as the sensing resistor. R68 is tied between the sense current output and the Kelvin source pin of MOSFET Q11. R68 is connected through the snubber circuit using differential layout techniques to maximize the current sensing accuracy at the HIMON inputs. (Note that a resistor must be populated at R73, even in the MOSFET with Sense output variation. R74 and R75 are not populated. This allows the current to flow to the load capacitor without affecting the sense current measurement by the HIMON in ASC).

The MON_12V_HS_VOLTAGE signal is also used by the Hot Swap function to monitor the load capacitor C15 voltage using the HVMON of the ASC. The Hot Swap function monitors the load capacitor C15 voltage for the following reasons:

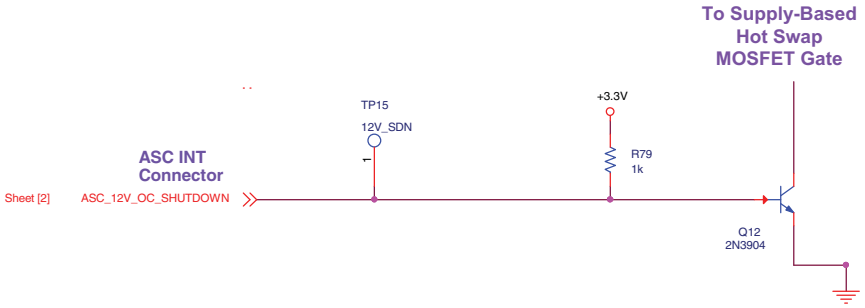
- to see that C15 is charging up and there is not a short or open in the circuit
- to see that C15 has reached a voltage where a higher current limit can be used
- to know when C15 is close to the 12 V supply voltage – Hot Swap is complete.

When Hot Swap is disabled R76 provides a discharge path for C15 to prepare the circuit for subsequent Hot Swaps. LED D12 and bias resistor R77 give a visual indication that the Hot Swap process is complete.

Fast Shutdown Circuit

The fast shutdown circuit for the 12 V Hot Swap is shown in Figure 24 below. The ASC_12V_OC_SHUTDOWN signal is output from the main FPGA board via the ASC Interface Connector. The ASC_12V_OC_SHUTDOWN signal is active high, and by default pulled up to 3.3 V by R79. When ASC_12V_OC_SHUTDOWN is high, Q12 is biased on. This will pull the MOSFET gate low, holding the MOSFET off. When ASC_12V_OC_SHUTDOWN is driven low, Q12 will be turned off. When Q12 is turned off, the Hot Swap MOSFET(s) will be controlled by the charge pump voltage. The fast shutdown feature can be implemented using the Hot Swap component in Platform Designer. Assign the FPGA PIO connected to ASC_12V_OC_SHUTDOWN on the main FPGA board to the Fast Shut Down feature in Platform Designer. See the References section for more details.

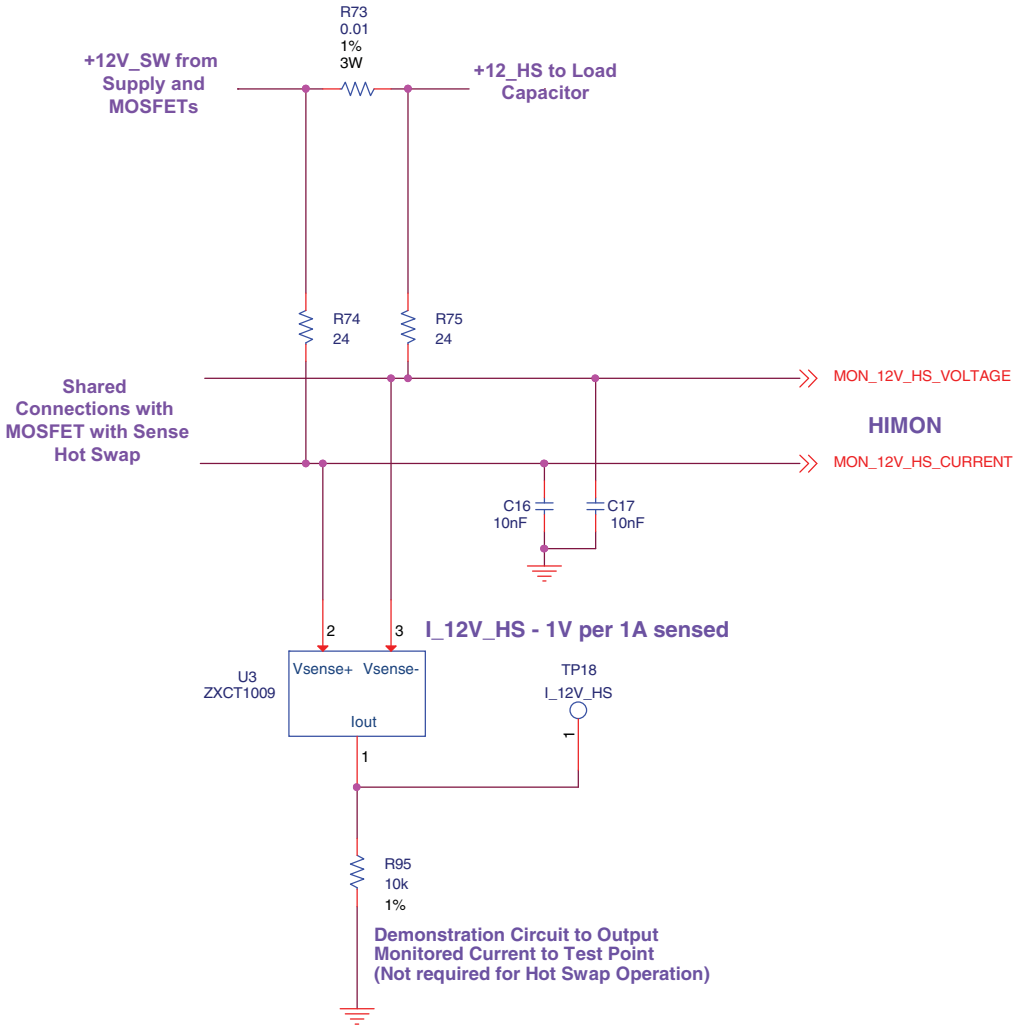
Figure 24. 12 V Hot Swap - Fast Shutdown Circuit



Current Sense Feedback Circuit

The 12 V Hot Swap circuit on the ASC Breakout board includes a current sense feedback circuit, shown in Figure 25. The purpose of this circuit is for demonstration and evaluation only, it does not need to be included on a customer application board. The current sense amplifier (U3 – ZXCT1009 from Diodes, Inc) provides an output current proportional to the voltage measured over R73. Based on the R73 resistance (10 mΩ) and the R95 resistance (10 kΩ), the ratio of output voltage to sensed current across R73 is about 1 V / 1A (this ratio is also maintained when Q11 and R68 are used instead of Q9 and R73). The test point I_12V_HS can be monitored on an oscilloscope to confirm the Hot Swap operation and evaluate the current behavior during Hot Swap. The internal current sense amplifier in the ASC is used in the Hot Swap algorithm, the circuit formed by U3 and R95 is only included to provide observable current feedback during the evaluation stage.

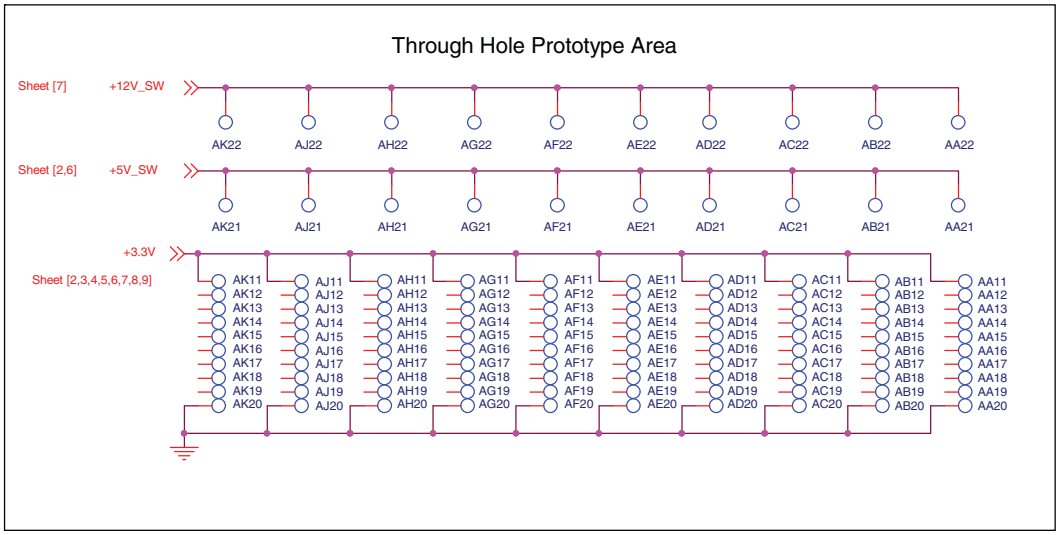
Figure 25. 12 V Hot Swap - Current Sense Feedback Circuit



Prototype Area

The ASC Breakout Board provides multiple areas for prototyping circuits with the ASC. The Through Hole Prototype Area (see Sheet 10 of the schematic) is accessible from both the top and bottom side of the board. As shown in Figure 26, the Through Hole Prototype Area is arranged as a grid on the breakout board. The top three rows provide ten connections each to the +12V_SW, +5V_SW and +3.3 V voltage rails. The next eight rows provide ten open connections each – these can be used for mounting and connecting through hole components. The bottom row provides ten connections to the ground plane of the breakout board.

Figure 26. Through Hole Prototype Area



The ASC Breakout Board also provides a surface-mount prototyping area on the bottom side of the board. The surface mount area is near the through hole prototyping area and provides a set of common footprints for resistors, capacitors, diodes, transistors and other integrated circuits as shown in Table 10. The schematic (Sheet 10) includes placeholder parts used to generate the footprints for the prototype area as shown in Figure 27. These surface mount footprints are unconnected – the user will need to connect any components placed on these footprints.

Figure 27. Surface Mount Prototype Area

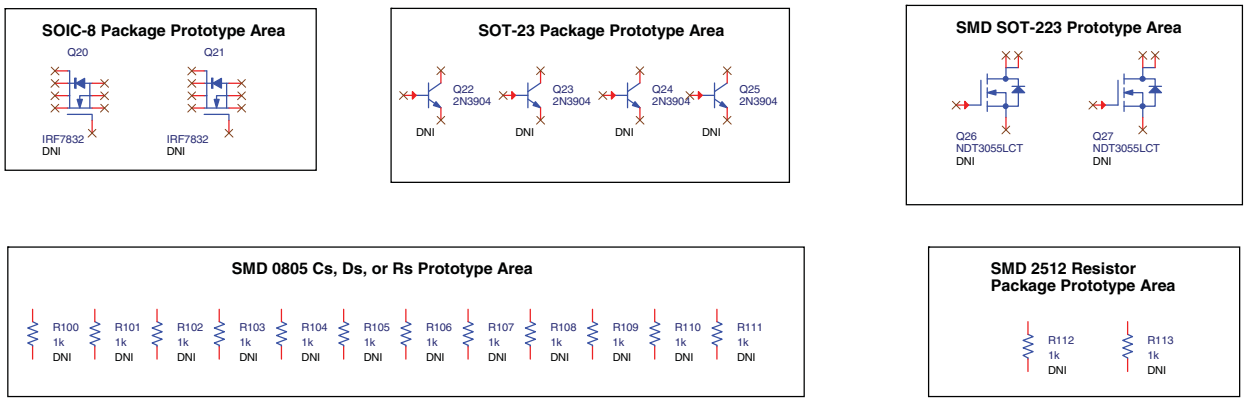


Table 10. SMD Prototype Area - Footprint Summary

Footprint Type	Quantity	Reference Designators	Common Use
SOIC-8	2	Q20, Q21	Power MOSFETs, other ICs
SOT-23	4	Q22, Q23, Q24, Q25	NPN, PNP, MOSFET Transistors, and other ICs
SOT-223	2	Q26, Q27	Power MOSFETs
SMD-0805	12	R100, R101, R102, R103, R104, R105, R106, R107, R108, R109, R110, R111	Resistors, Inductors, Capacitors, and Diodes
SMD-2512	2	R112, R113	Current Sense Resistors (Shunts)

Mechanical Specifications

Dimensions: 6 in. [L] x 3.5 in. [W] x 1 in. [H]

Environmental Specifications

The breakout board must be stored between -40°C and 100°C. The recommended operating temperature is between 0°C and 55°C.

Electrical Specifications

- 12 V Input +/- 15% (Input current requirement depending on Hot Swap settings and DC-DC Load Resistance)
- 5 V Input +/- 10% (Input current requirement depending on Hot Swap settings and DC-DC Load Resistance)
- 3.3 V Input +/- 5% (Breakout board current draw 100 mA typical)

References

- EB93, Platform Manager 2 Evaluation Board User Guide
- FPGA-DS-02038, L-ASC10 Data Sheet
- TN1225, Platform Manager 2 Hardware Checklist
- Platform Designer 3.1 User Guide
- AN6041, Extending the VMON Input Range of Power/Platform Management Devices
- AN6074, Interfacing the Trim Output of Power Manager II Devices to DC-DC Converters

Ordering Information

Description	Ordering Part Number	China RoHS Environment-Friendly Use Period
ASC Breakout Board	LPTM-ASC-B-EVN	

Technical Support Assistance

Submit a technical support case through www.latticesemi.com/techsupport.

Revision History

Date	Version	Change Summary
September 2018	1.1	Updated document number from EB92 to FPGA-EB-02023. Updated L-ASC10 Data Sheet number to FPGA-DS-02038.
		Updated ASC Breakout Board Photos (Figure 1 and Figure 2).
		Added Ordering Information section.
July 2015	1.0	Initial release.

Appendix A. Schematics

Figure 28. ASC System Block Diagram

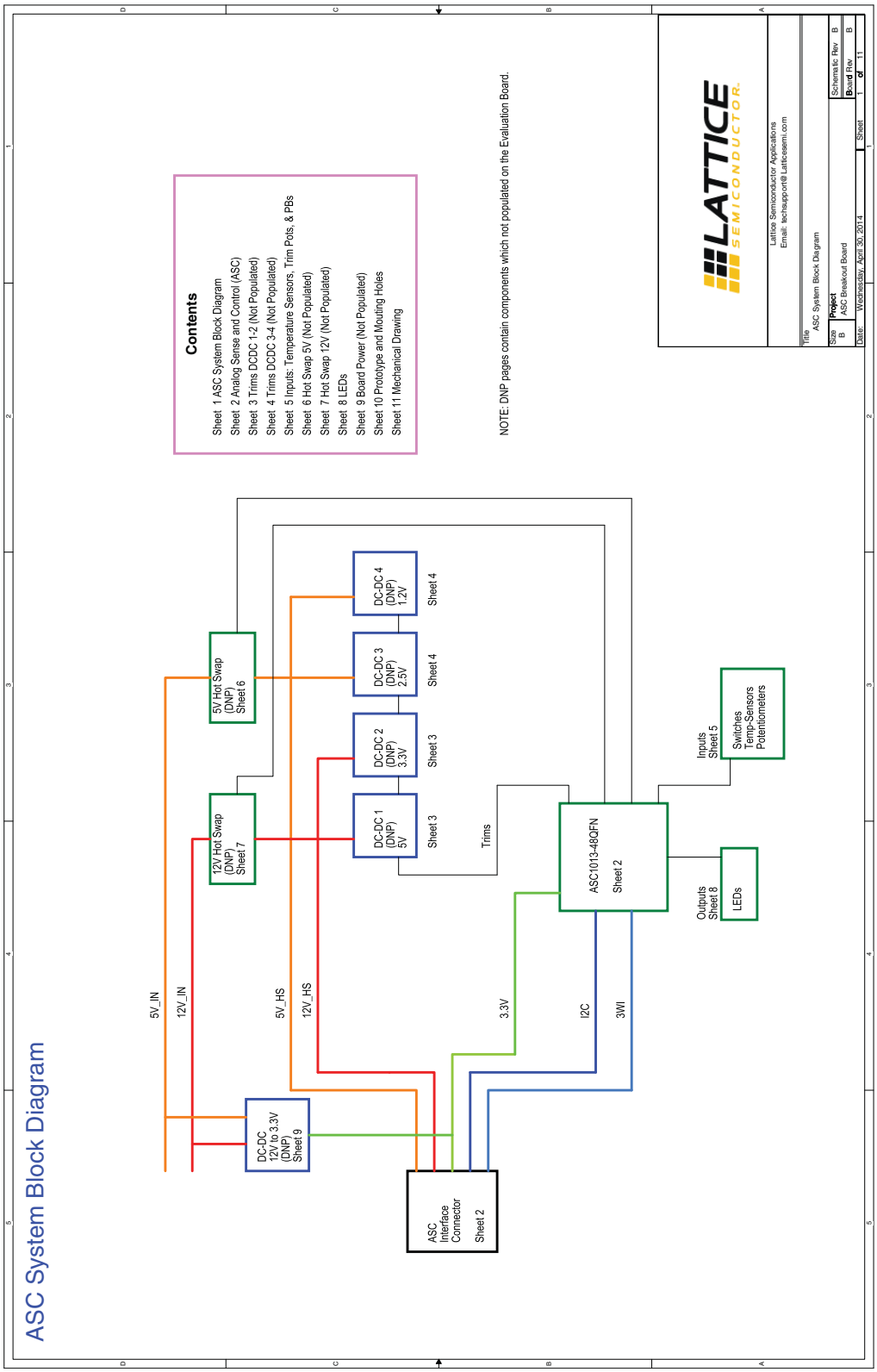


Figure 29. Analog Sense and Control

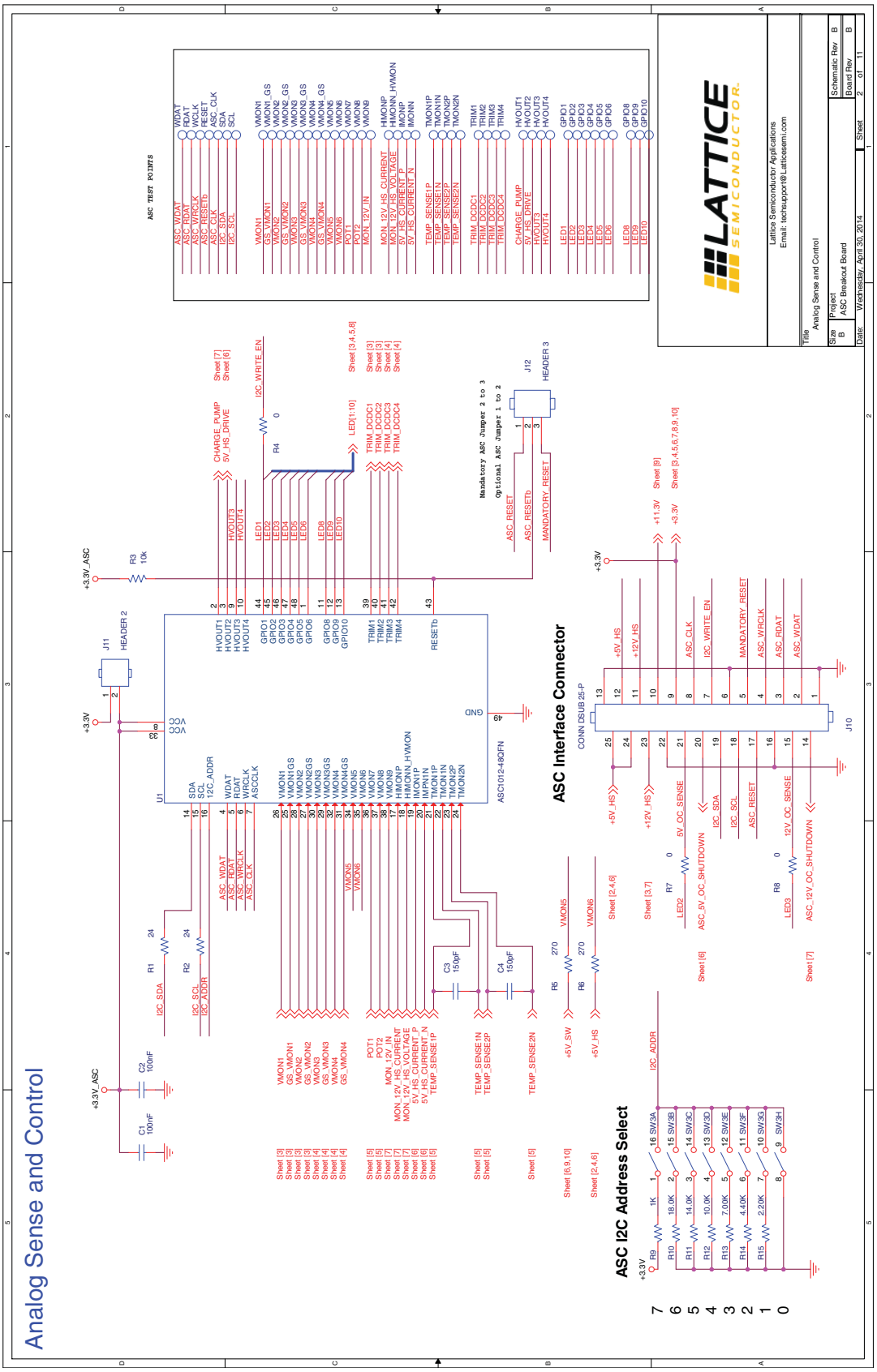


Figure 30. Trims DCDC 1-2 (Not Populated on Breakout Board)

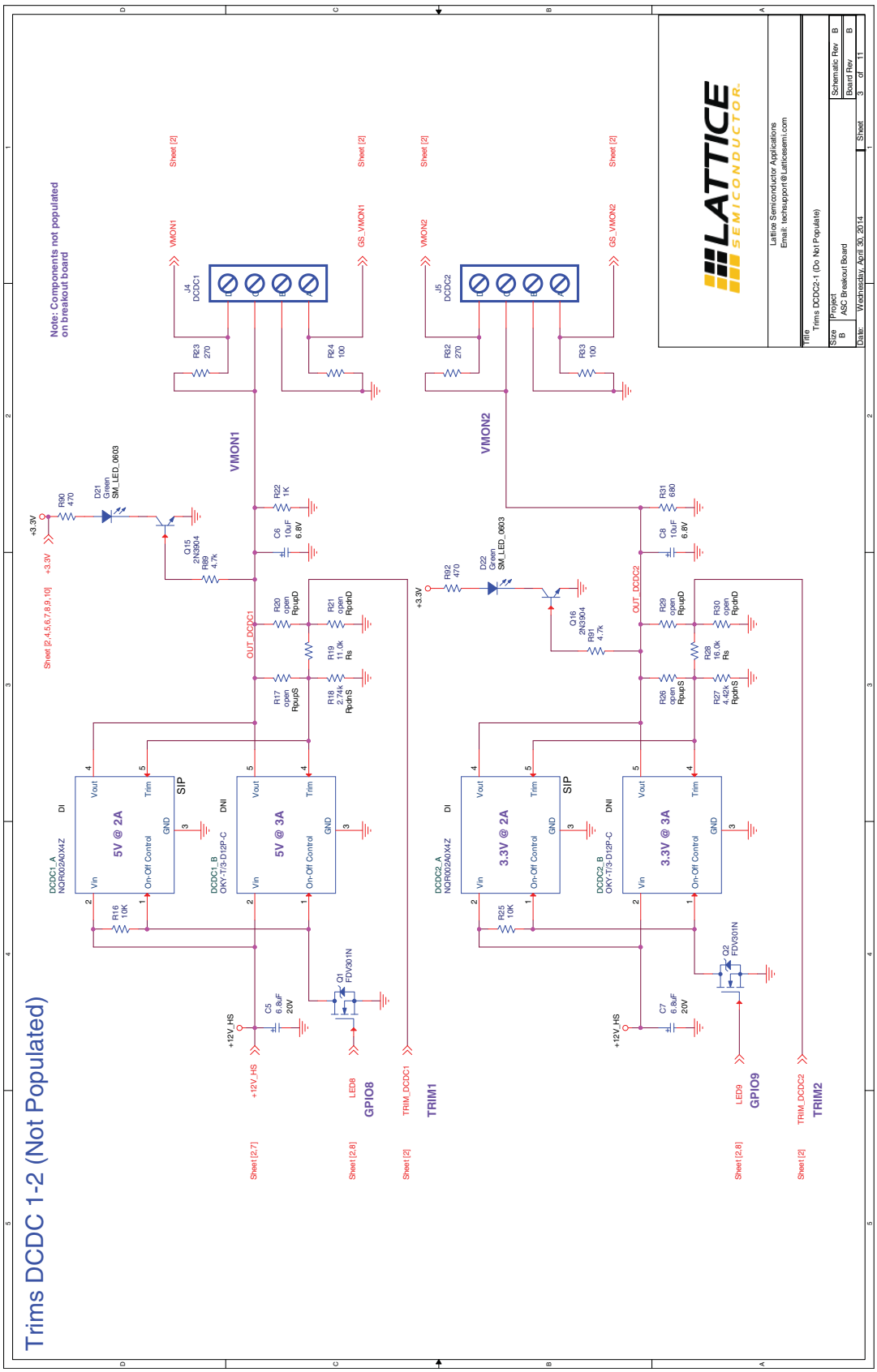


Figure 31. Trims DCDC 3-4 (Not Populated on Breakout Board)

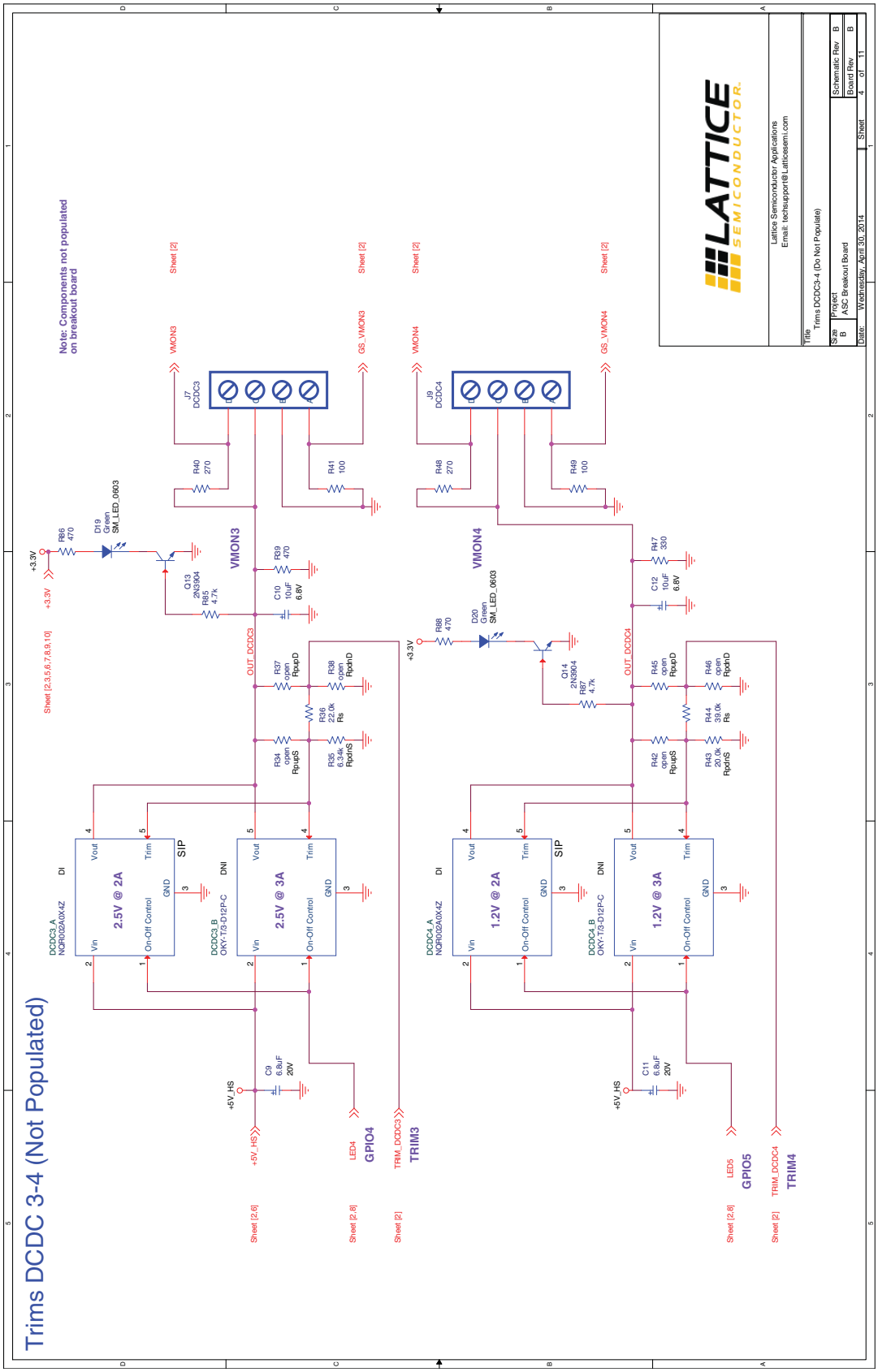


Figure 32. Inputs: Temperature Sensors, Trim Pots & Switches

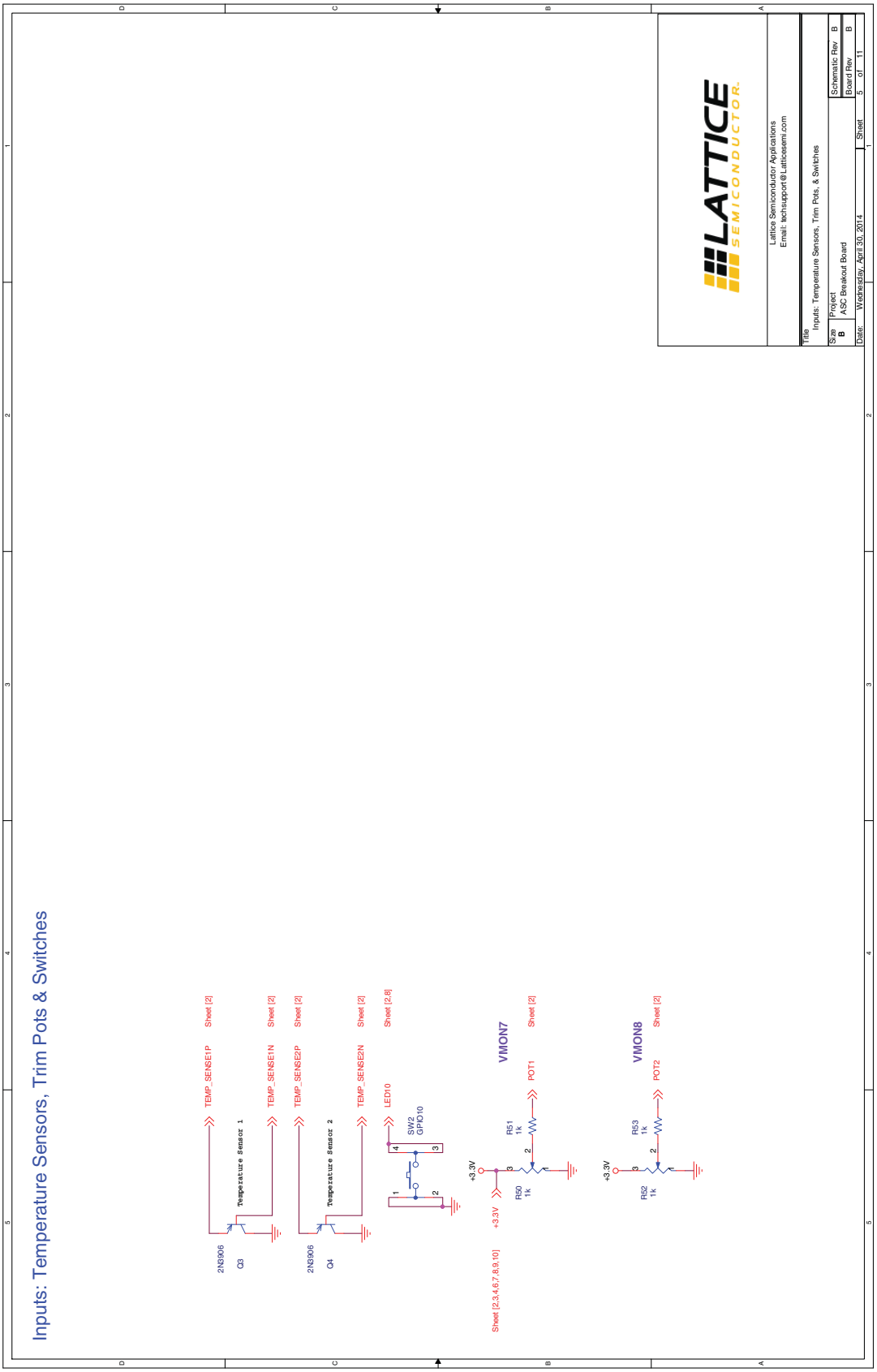


Figure 33. Hot Swap, 5 V (Not Populated on Breakout Board)

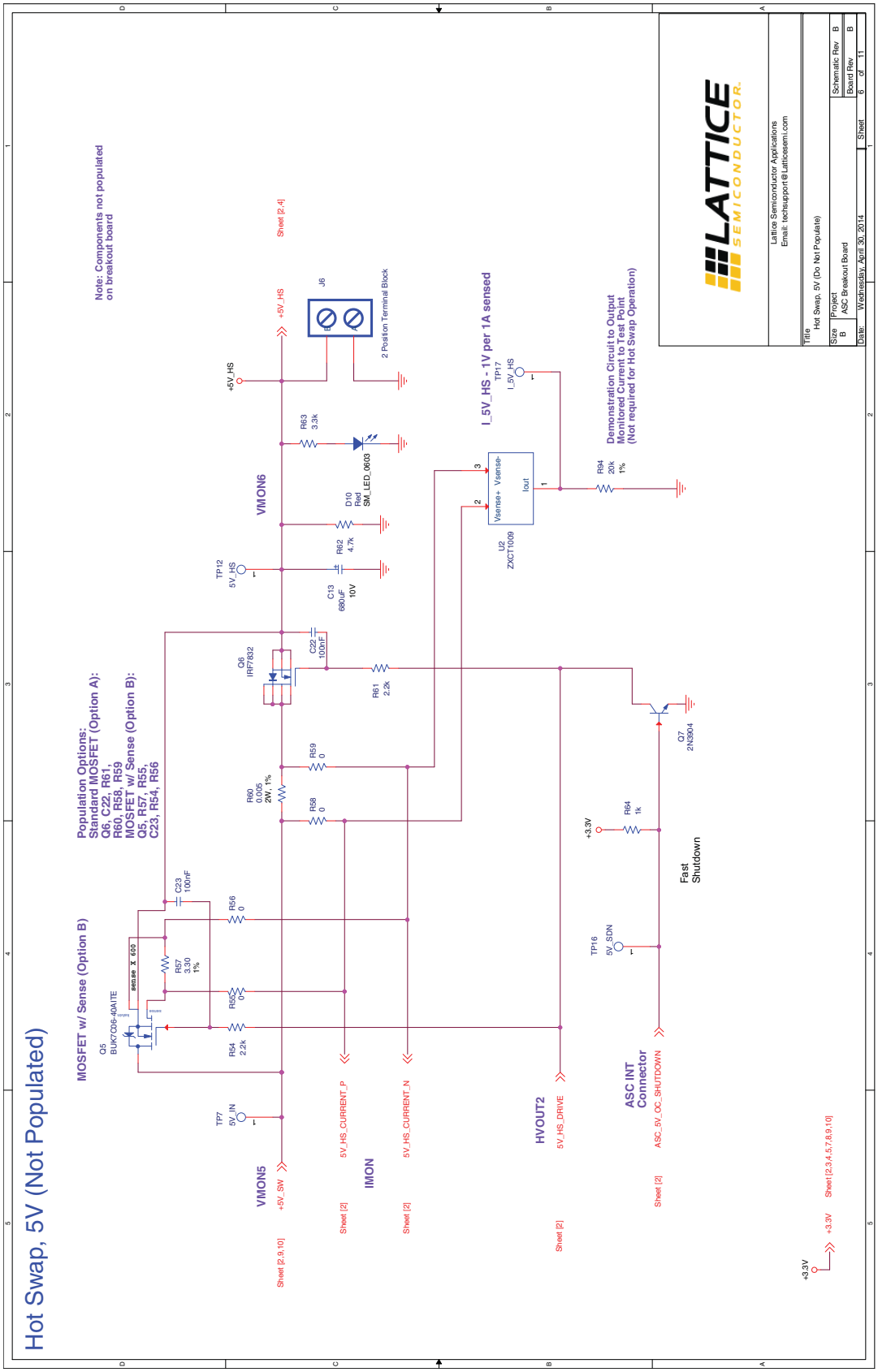


Figure 34. Hot Swap, 12 V (Not Populated on Breakout Board)

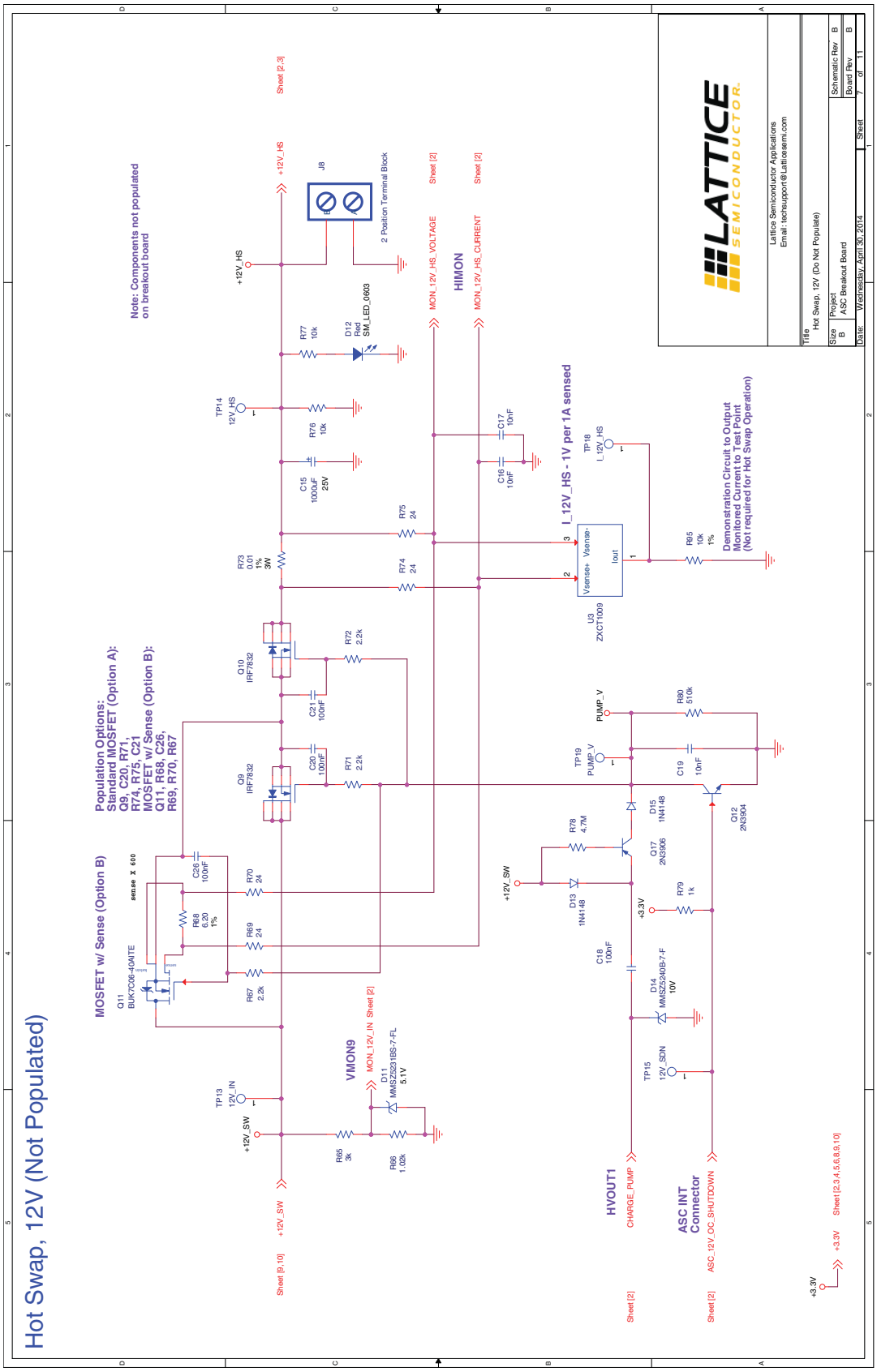


Figure 35. LEDs

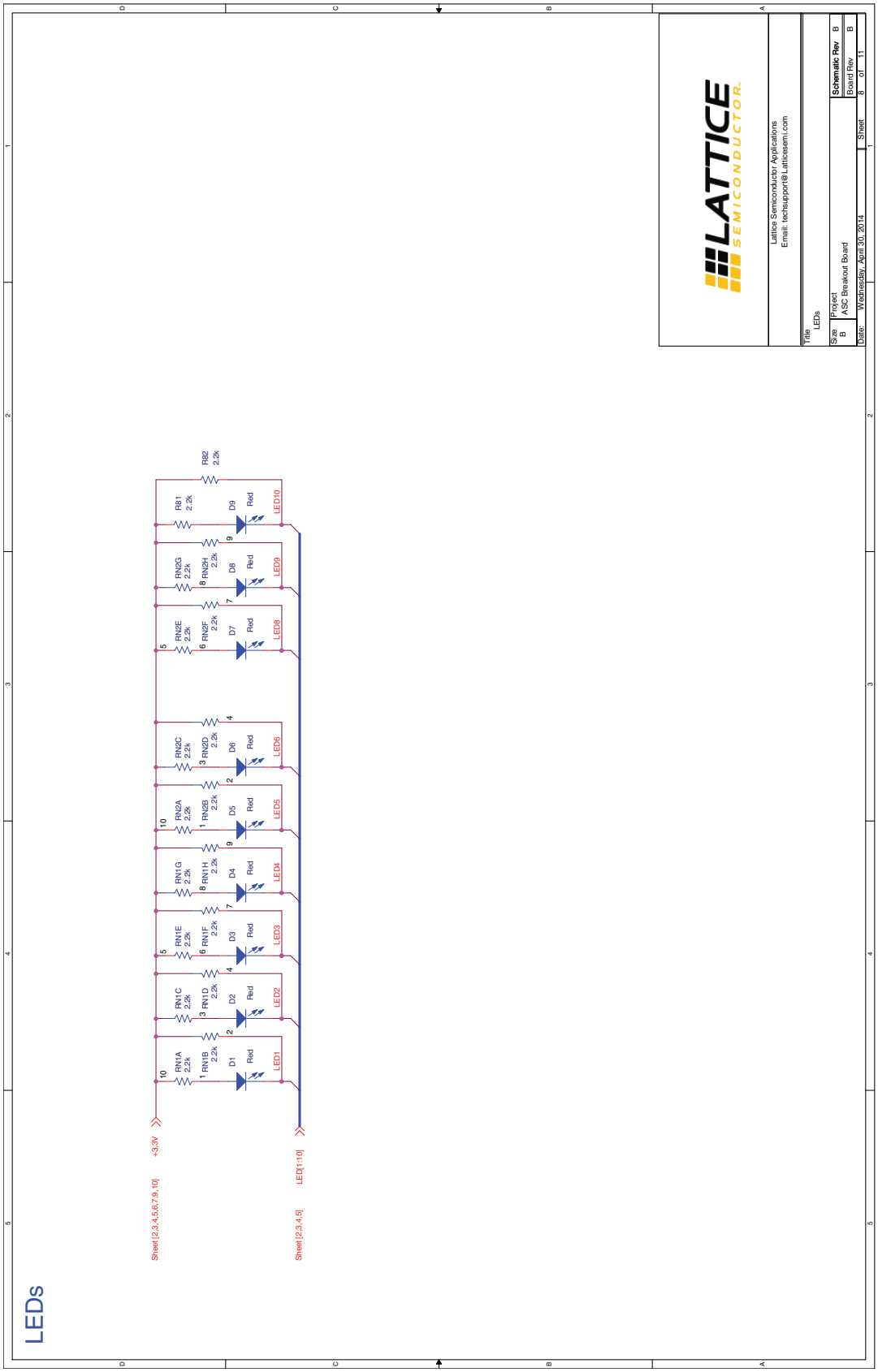


Figure 36. Board Power (Not Populated on Breakout Board)

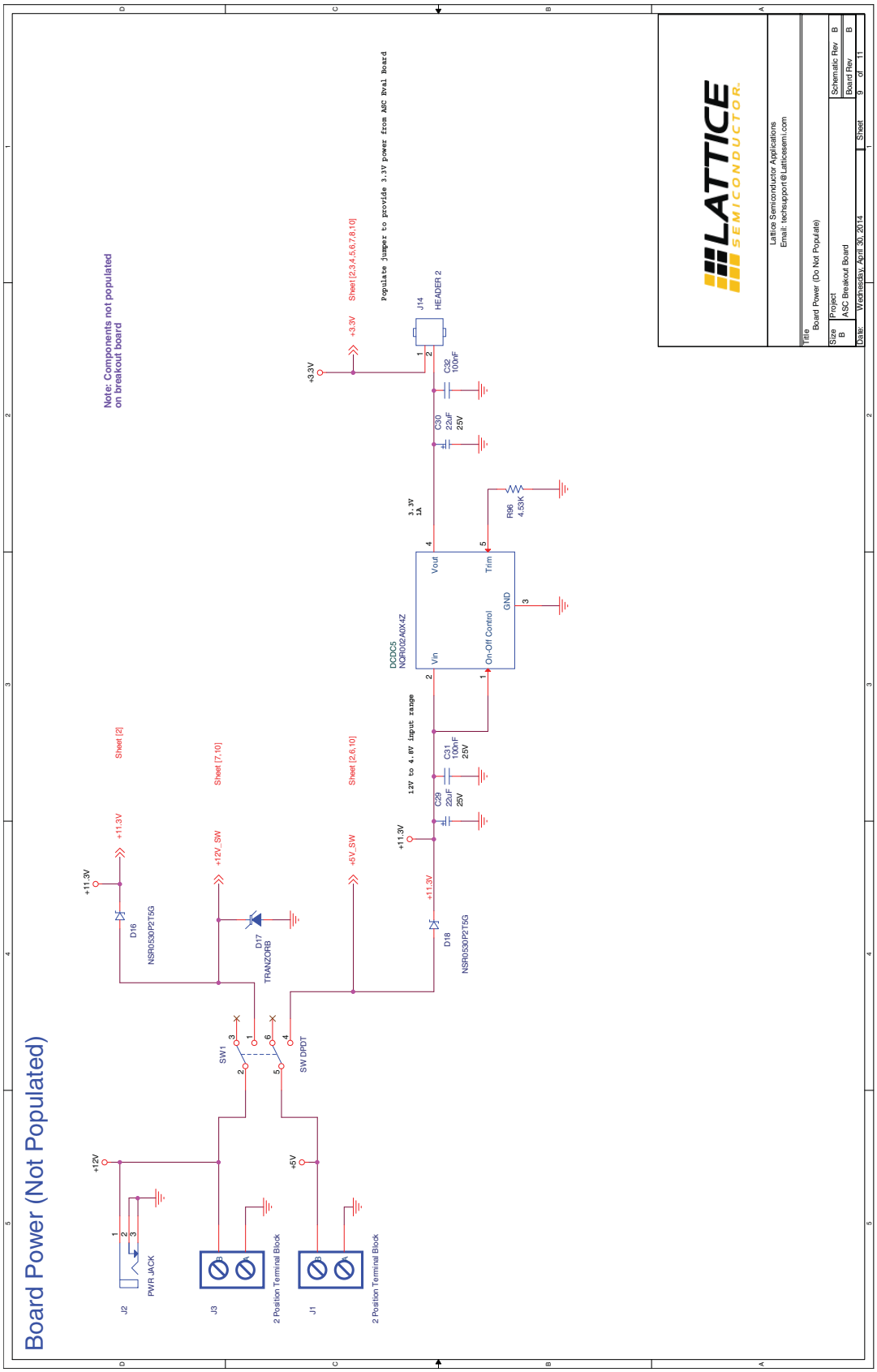


Figure 37. Prototype and Mounting Holes

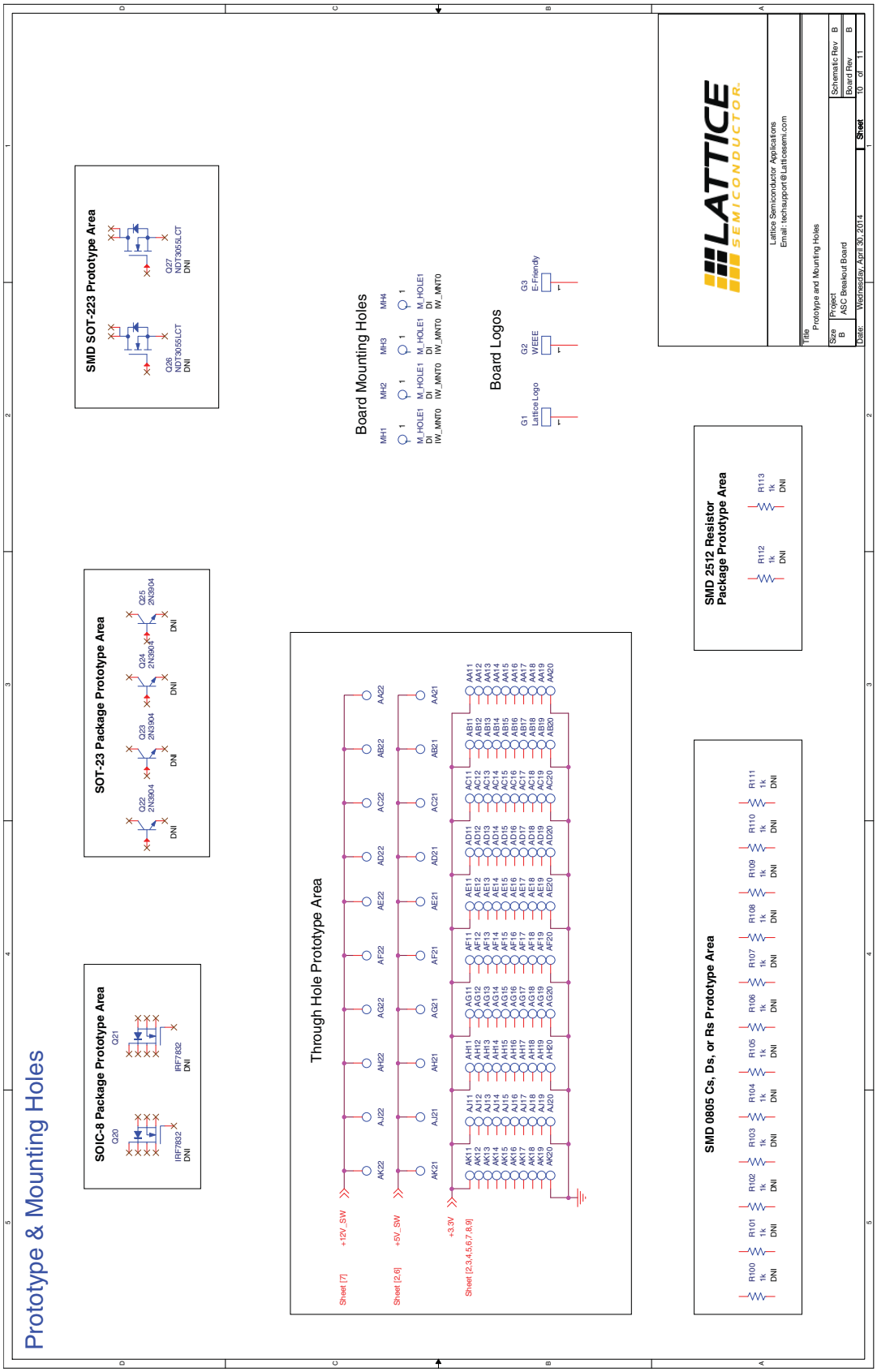
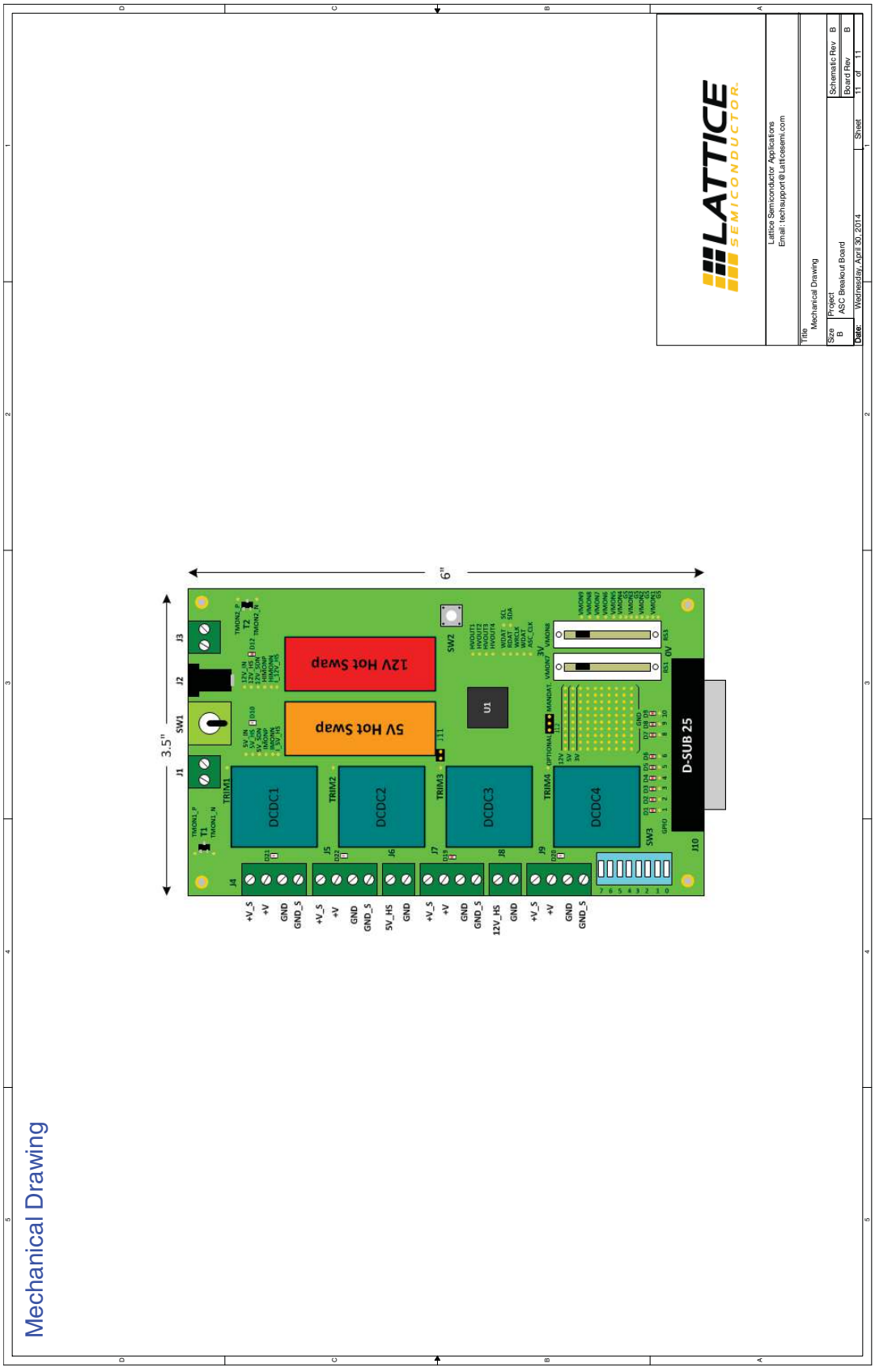


Figure 38. Mechanical Drawing



Mechanical Drawing

Appendix B. Bill of Materials – Populated on Breakout Board

Quantity	Reference Designator	Description	Package	Manufacturer	Part Number
ICs					
1	U1	ASC Device	TQFN_48	Lattice Semiconductor	L-ASC10-1SG48I
Capacitors					
2	C1, C2	0.1uF 16 V 10% Ceramic X7R	SMD 0603	Murata	GRM188R71C104KA01D
2	C3, C4	150pF 50 V 5% Ceramic NP0	SMD 0603	Murata	GRM1885C1H151JA01D
Diodes					
9	D1, D2, D3, D4, D5, D6, D7, D8, D9	Red LED	SMD 0603	Lite-On Inc	LTST-C190KRKT
Jumpers					
1	J10	25-pin DSUB Connector		TE Connectivity	5745783-4
1	J11	2 Pin Header	Header_1x2	Molex Inc	22-28-4364
1	J12	3 Pin Header	Header_1x3	Molex Inc	22-28-4364
Transistors					
2	Q3,Q4	2N3906 PNP	SOT23	Fairchild	MMBT3906
Resistors					
2	RN1, RN2	2.2 kΩ Resistor Network	SMD 2512	CTS Resistor	745C101222JP
2	R1, R2	24 Ω Resistor	SMD 0603	Panasonic	ERJ-3GEYJ240V
1	R3	10 kΩ Resistor	SMD 0603	Panasonic	ERJ-3GEYJ103V
1	R4	0 Ω Resistor	SMD 0603	Panasonic	ERJ-3GEY0R00V
2	R5, R6	270 Ω Resistor	SMD 0603	Panasonic	ERJ-3GEYJ271V
3	R9, R51, R53	1 kΩ Resistor	SMD 0603	Panasonic	ERJ-3GEYJ102V
1	R10	18.0 kΩ Resistor 1%	SMD 0603	Panasonic	ERJ-3EKF1802V
1	R11	14.0 kΩ Resistor 1%	SMD 0603	Panasonic	ERJ-3EKF1402V
1	R12	10.0 kΩ Resistor 1%	SMD 0603	Panasonic	ERJ-3EKF1002V
1	R13	7.00 kΩ Resistor 1%	SMD 0603	Panasonic	ERJ-3EKF7001V
1	R14	4.40 kΩ Resistor 1%	SMD 0603	Panasonic	ERJ-3EKF4401V
1	R15	2.20 kΩ Resistor 1%	SMD 0603	Panasonic	ERJ-3EKF2201V
2	R50, R52	1 kΩ Potentiometer	TH_SLIDEPOT_4_25mm	Alpha	RA2043F-20-10EB1-B1K
2	R81, R82	2.2 kΩ Resistor	SMD 0603	Panasonic	ERJ-3GEYJ222V
Switches					
1	SW2	Push Button Switch	SMT_SW	Panasonic	EVQ-Q2K03W
1	SW3	8 Position Dip Switch	195_8MST	CTS Electrocomponents	195-8MST

Appendix C. Bill of Materials – Not Populated on Breakout Board

Quantity	Reference Designator	Description	Package	Manufacturer	Part Number
ICs					
2	U2, U3	Current Sense Amplifier	SOT23	Diodes Inc	ZXCT1009FTA
Capacitors					
8	C18, C20[1], C21[1], C22[3], C23[4], C26[2], C31, C32	0.1 uF 16 V 10% Ceramic X7R	SMD 0603	Murata	GRM188R71C104KA01D
4	C5, C7, C9, C11	6.8 uF 16 V 10% Tantalum	SMD 1206	Kemet	T491A685K016AT
4	C6, C8, C10, C12	10 uF 10 V 10% Tantalum	SMD 1206	Kemet	T491A106K010AT
1	C13	680 uF 10 V 20% Aluminum	Radial	Panasonic	EEU-FM1A681L
1	C15	1000 uF 25 V 20% Aluminum	Radial	Panasonic	EEU-FM1E102
3	C16, C17, C19	10 nF 50 V 10% Ceramic X7R	SMD 0603	Kemet	C0603C103K5RACTU
2	C29, C30	22 uF 25 V 20% Aluminum	Radial	Panasonic	EEA-GA1E220H
DCDCs					
5	DCDC1_A, DCDC2_A, DCDC3_A, DCDC4_A, DCDC5	DC/DC Converter 0.6V-5.5 V 2A	5pin_SIP	GE Critical Power	NQR002A0X4Z
2	DCDC1_B, DCDC2_B	DC/DC Converter 15W 12VIN 3AOUT	DOSA-SMT	Murata Power	OKY-T/3-D12P-C
2	DCDC3_B, DCDC4_B	DC/DC Converter 10.9W 5VIN 3AOUT	DOSA-SMT	Murata Power	OKY-T/3-W5P-C
Diodes					
2	D10, D12	Red LED	SMD 0603	Lite-On Inc	LTST-C190KRKT
1	D11	Zener Diode 5.1 V	SM_SOD_323_12	Diodes Inc	MMSZ5231BS-7-F
2	D13, D15	Diode 100 V 0.15 A	SOD-123_12	Micro Commercial Co	1N4148W-TP
1	D14	Zener Diode 10 V	SM_SOD_123	Diodes Inc	MMSZ5240B-7-F
2	D16, D18	Schottky 30 V 500 mA	SM_SOD_923	ON Semiconductor	NSR0530P2T5G
1	D17	TVS Diode 22 V 600 W	SM_SOD_214AA_12	Littlefuse	SMBJ22CA
4	D19, D20, D21, D22	Green LED	SMD 0603	Lite-On Inc	LTST-C190KGKT
Jumpers					
4	J1, J3, J6, J8	2 Position Terminal Block	TERM_BLOCK_2POS	Phoenix	1727010
1	J2	Pwr Jack	PWR_JACK_PINS	CUI Inc	PJ-102AH
1	J4, J5, J7, J9	4 Position Terminal Block	TERM_BLOCK_4POS	Phoenix	1727036
1	J14	2 Pin Header	Header_1x2	Molex Inc	22-28-4364
Transistors					
2	Q1, Q2	N-Channel MOSFET 25 V	SOT23	Fairchild	FDV301N
2	Q5[4], Q11[2]	N-Channel TrenchPLUS FET with SENSE output	SOT427	NXP Semiconductor	BUK7C06-40AITE
3	Q6[3], Q9[1], Q10	N-Channel MOSFET 30 V	SOIC8	International Rectifier	IRF7832TRPBF
6	Q7, Q12, Q13, Q14, Q15, Q16	2N3904 NPN	SOT23	Fairchild	MMBT3904
1	Q17	2N3906 PNP	SOT23	Fairchild	MMBT3906
Resistors					
2	R74[1], R75[1]	24 Ω Resistor	SMD 0603	Panasonic	ERJ-3GEYJ240V
4	R16, R25, R76, R77	10 kΩ Resistor	SMD 0603	Panasonic	ERJ-3GEYJ103V
4	R7, R8, R58[3], R59[3]	0 Ω Resistor	SMD 0603	Panasonic	ERJ-3GEY0R00V
4	R23, R32, R40, R48	270 Ω Resistor	SMD 0603	Panasonic	ERJ-3GEYJ271V
3	R22, R64, R79	1 kΩ Resistor	SMD 0603	Panasonic	ERJ-3GEYJ102V
1	R27	4.42 kΩ Resistor	SMD 0603	Panasonic	ERJ-3EKF4421V
1	R28	16.0 kΩ Resistor	SMD 0603	Panasonic	ERJ-3EKF1602V
1	R31	680 Ω Resistor	SMD 0603	Panasonic	ERJ-3GEYJ681V
1	R35	6.34 kΩ Resistor	SMD 0603	Panasonic	ERJ-3EKF6341V
1	R36	22.0 kΩ Resistor	SMD 0603	Panasonic	ERJ-3EKF2202V

1	R39, R86, R88, R90, R92	470 Ω Resistor	SMD 0603	Panasonic	ERJ-3GEYJ471V
5	R43	20.0 kΩ Resistor	SMD 0603	Panasonic	ERJ-3EKF2002V
1	R44	39.0 kΩ Resistor	SMD 0603	Panasonic	ERJ-3EKF3902V
1	R47	330 Ω Resistor	SMD 0603	Panasonic	ERJ-3GEYJ331V
2	R54[4],R67[2]	2.2 k	SMD 0603	Panasonic	ERJ-3GEYJ222V
2	R55[4],R56[4]	0	SMD 0603	Panasonic	ERJ-3GEY0R00V
1	R57[4]	3.3	SMD 1206	Vishay-Dale	CRCW12063R30FKEA
1	R60[3]	0.005	SMD 2512	Rohm Semi	PMR100HZPFU5L00
1	R62	4.7 k	SMD 0603	Panasonic	ERJ-3GEYJ472V
1	R63	3.3 k	SMD 0603	Panasonic	ERJ-3GEYJ332V
1	R65	3 k	SMD 0603	Panasonic	ERJ-3GEYJ302V
1	R66	1.02 k	SMD 0603	Panasonic	ERJ-3EKF1021V
1	R68[2]	6.2	SMD 1206	Vishay-Dale	CRCW12066R20FKEA
2	R69[2], R70[2]	24	SMD 0603	Panasonic	ERJ-3GEYJ240V
3	R71[1], R72, R61[3]	2.2 k	SMD 0603	Panasonic	ERJ-3GEYJ222V
1	R73	0.01	SMD 2512	Bourns	CRA2512-FZ-R010ELF
1	R95	10 k	SMD 0603	Panasonic	ERJ-3EKF1002V
1	R78	4.7 M	SMD 0603	Panasonic	ERJ-3GEYJ475V
1	R80	510 k	SMD 0603	Panasonic	ERJ-3GEYJ514V
4	R85, R87, R89, R91	4.7 k	SMD 0603	Panasonic	ERJ-3GEYJ472V
1	R94	20 k	SMD 0603	Panasonic	ERJ-3EKF2002V
1	R96	4.53 k	SMD 0603	Panasonic	ERJ-3EKF4531V
Switches					
1	SW1	DPDT Power Switch	SW DPDT	NKK Switches	M2022SS1W03_RO

1. Only populate for 12 V Standard MOSFET Hot Swap. Populate only from either Note 1 or Note 2, never both.
2. Only populate for 12 V MOSFET with Sense Output Hot Swap. Populate only from either Note 1 or Note 2, never both.
3. Only populate for 5 V Standard MOSFET Hot Swap. Populate only from either Note 3 or Note 4, never both.
4. Only populate for 12 V MOSFET with Sense Output Hot Swap. Populate only from either Note 3 or Note 4, never both.

Appendix D. Known Issues

The populated components on the breakout board work as specified without issue. There is an issue related to the footprints and connections in the 12 V Hot Swap – Charge Pump section of the board.

The footprint for Q17 contains an error in the connection to the device pins. Figure 39 shows the footprint of Q17, with each of the device pin connections labeled. The footprint has the base and collector pin connections swapped. Q17 needs to be populated according to Figure 40, with the connections swapped, in order for the 12 V Hot Swap circuit to function properly.

Figure 39. 12 V Hot Swap - Charge Pump - Q17 Footprint Error

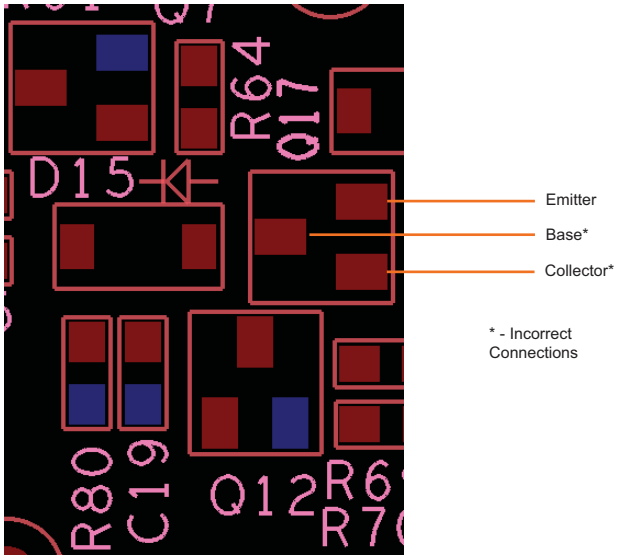
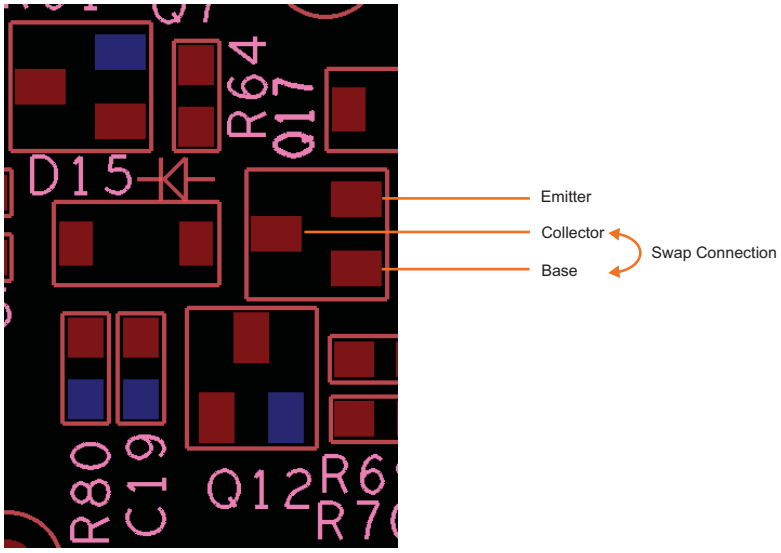


Figure 40. 12 V Hot Swap - Charge Pump - Q17 Correction



One method for fixing the connection on the board is to place Q17 (2N3906) in the configuration shown in Figure 41. In this configuration, Q17 is flipped upside down, and then rotated clockwise. This configuration results in the collector and base connections being swapped back to the correct pin connections.

Figure 41. Q17 - Orientation for Corrected Connection