To our customers,

Old Company Name in Catalogs and Other Documents

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Renesas Electronics website: http://www.renesas.com

April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (http://www.renesas.com)

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MOS FIELD EFFECT TRANSISTOR
2SJ687

SWITCHING
P-CHANNEL POWER MOSFET

DESCRIPTION

The 2SJ687 is P-channel MOSFET device and a excellent switch that can be driven by a low power-supply voltage.

FEATURES

- Low on-state resistance

  $R_{DS(on)1}$ = 7.0 mΩ MAX. (V_{GS} = –4.5 V, I_D = –10 A)

  $R_{DS(on)2}$ = 9.0 mΩ MAX. (V_{GS} = –3.0 V, I_D = –10 A)

  $R_{DS(on)3}$ = 20 mΩ MAX. (V_{GS} = –2.5 V, I_D = –10 A)

- 2.5 V drive available
- Avalanche capability ratings

ORDERING INFORMATION

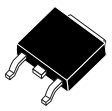
PART NUMBER	LEAD PLATING	PACKING	PACKAGE
2SJ687-ZK-E1-AY Note	Pure Sn (Tin)	Tape 2500 p/reel	TO-252 (MP-3ZK) 0.27 g TYP.
2SJ687-ZK-E2-AY Note			

Note Pb-free (This product does not contain Pb in external electrode.)

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C)

Drain to Source Voltage (V_{GS} = 0 V)	V_{DSS}	–20	V
Gate to Source Voltage (V_{DS} = 0 V)	V_{GSS}	∓12	V
Drain Current (DC) (T_C = 25°C)	$I_{D(DC)}$	∓20	A
Drain Current (pulse) Note1	$I_{D(pulse)}$	∓60	A
Total Power Dissipation (T_C = 25°C)	P_{T1}	36	W
Total Power Dissipation (T_A = 25°C)	P_{T2}	1.0	W
Channel Temperature	T_{ch}	150	°C
Storage Temperature	T_{stg}	–55 to +150	°C
Single Avalanche Current Note2	I_{AS}	–20	A
Single Avalanche Energy Note2	E_{AS}	40	mJ

(TO-252)



Notes 1. PW ≤ 10 μs, Duty Cycle ≤ 1%

2. Starting T_{ch} = 25°C, V_{DD} = –10 V, R_G = 25 Ω, V_{GS} = –12 → 0 V

Document No. D18719EJ2V0DS00 (2nd edition)
Date Published May 2007 NS
Printed in Japan

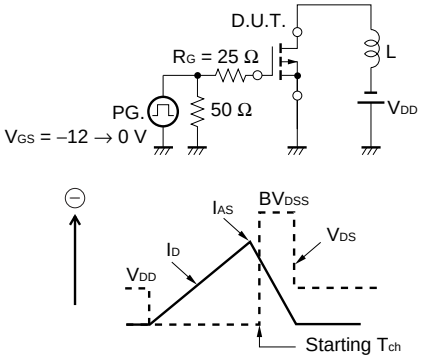
The mark <R> shows major revised points.
The revised points can be easily searched by copying an "<R>" in the PDF file and specifying it in the "Find what:" field.

ELECTRICAL CHARACTERISTICS (T_A = 25°C)

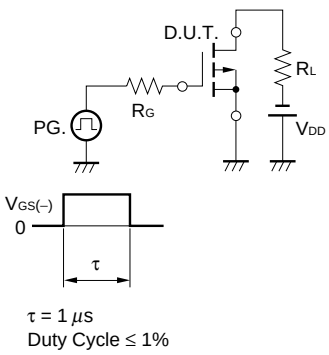
	CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
	Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = –20 V, V_{GS} = 0 V			–10	μA
<R>	Gate Leakage Current	I_{GSS}	V_{GS} = ∓12 V, V_{DS} = 0 V			∓100	nA
<R>	Gate to Source Cut-off Voltage	$V_{GS(off)}$	V_{DS} = –10 V, I_D = –1 mA	–0.6	–1.2	–1.45	V
	Forward Transfer Admittance **Note**	$\|y_{fs}\|$	V_{DS} = –10 V, I_D = –10 A	20			S
	Drain to Source On-state Resistance **Note**	$R_{DS(on)1}$	V_{GS} = –4.5 V, I_D = –10 A		5.4	7.0	mΩ
		$R_{DS(on)2}$	V_{GS} = –3.0 V, I_D = –10 A		7.1	9.0	mΩ
		$R_{DS(on)3}$	V_{GS} = –2.5 V, I_D = –10 A		10.8	20	mΩ
	Input Capacitance	C_{iss}	V_{DS} = –10 V,		4400		pF
	Output Capacitance	C_{oss}	V_{GS} = 0 V,		1070		pF
	Reverse Transfer Capacitance	C_{rss}	f = 1 MHz		760		pF
	Turn-on Delay Time	$t_{d(on)}$	V_{DD} = –10 V, I_D = –10 A,		36		ns
	Rise Time	t_r	V_{GS} = –4.5 V,		220		ns
	Turn-off Delay Time	$t_{d(off)}$	R_G = 3 Ω		270		ns
	Fall Time	t_f			310		ns
	Total Gate Charge	Q_G	V_{DD} = –16 V,		57		nC
	Gate to Source Charge	Q_{GS}	V_{GS} = –4.5 V,		12		nC
	Gate to Drain Charge	Q_{GD}	I_D = –20 A		28		nC
	Body Diode Forward Voltage **Note**	$V_{F(S-D)}$	I_F = –20 A, V_{GS} = 0 V		0.85	1.5	V
	Reverse Recovery Time	t_{rr}	I_F = –20 A, V_{GS} = 0 V,		200		ns
	Reverse Recovery Charge	Q_{rr}	di/dt = –100 A/μs		240		nC

Note Pulsed

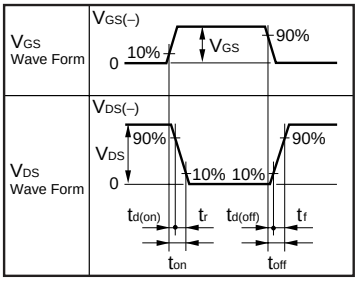
TEST CIRCUIT 1 AVALANCHE CAPABILITY



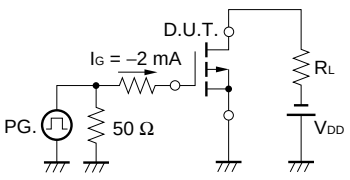
TEST CIRCUIT 2 SWITCHING TIME



τ = 1 μs
Duty Cycle ≤ 1%

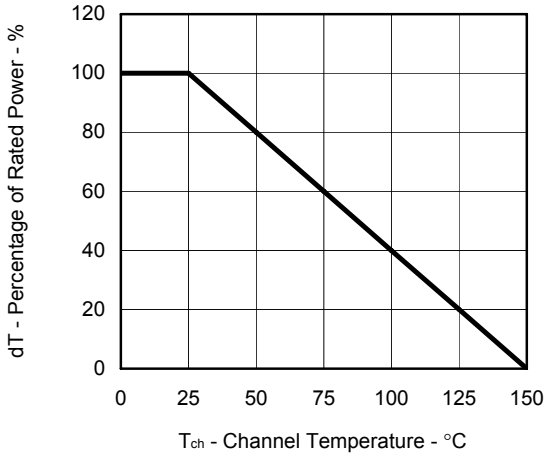


TEST CIRCUIT 3 GATE CHARGE

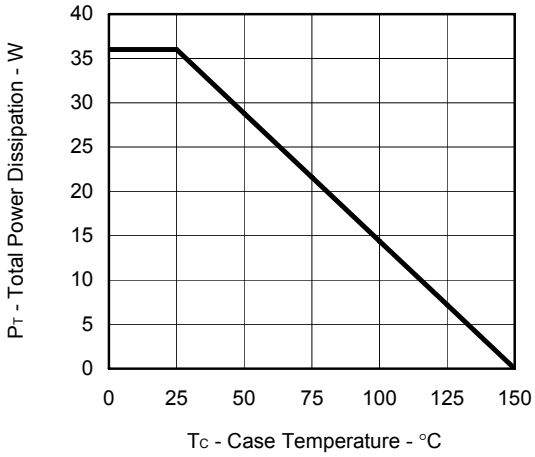


TYPICAL CHARACTERISTICS (T_A = 25°C)

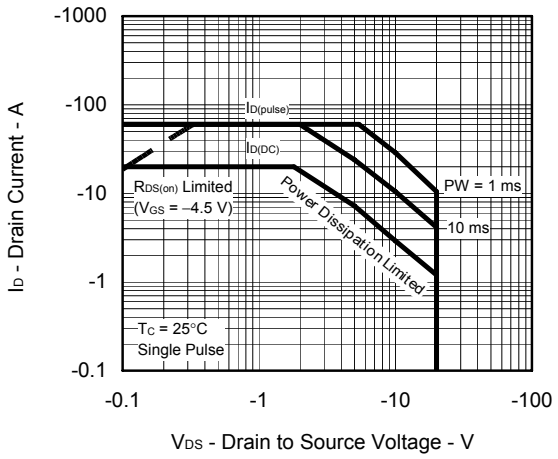
DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA



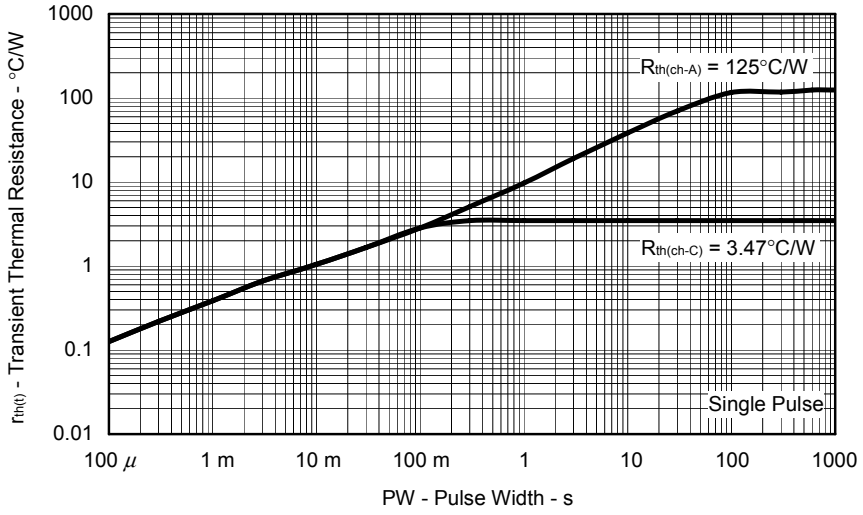
TOTAL POWER DISSIPATION vs. CASE TEMPERATURE



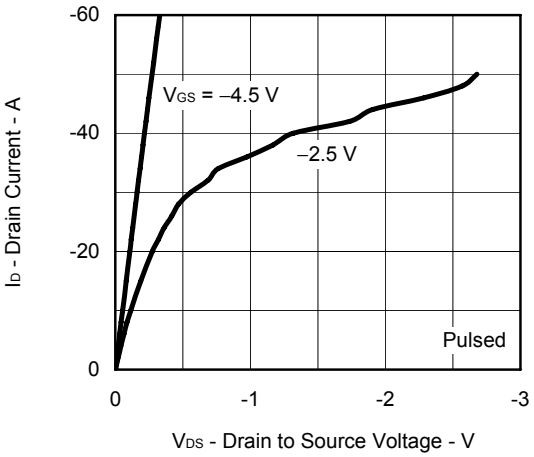
FORWARD BIAS SAFE OPERATING AREA



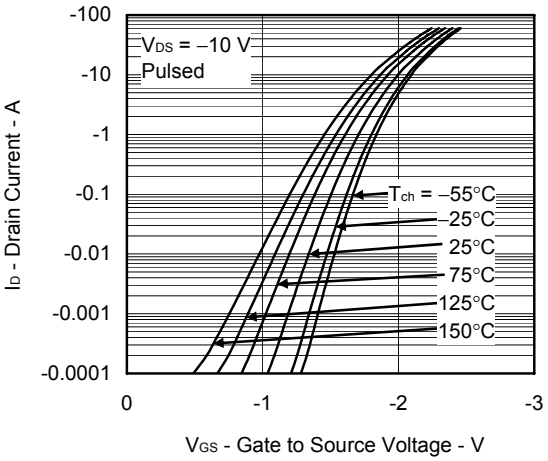
TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



DRAIN CURRENT vs.
DRAIN TO SOURCE VOLTAGE



FORWARD TRANSFER CHARACTERISTICS



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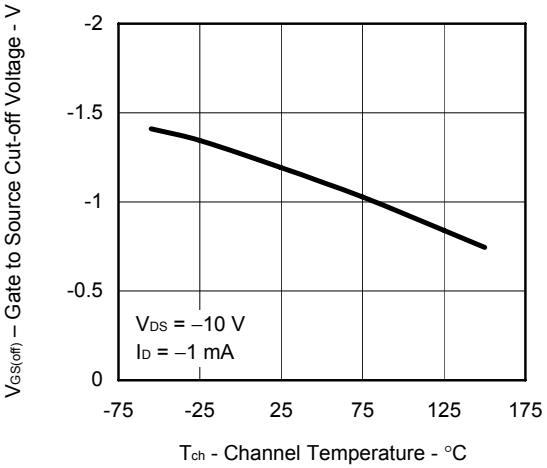
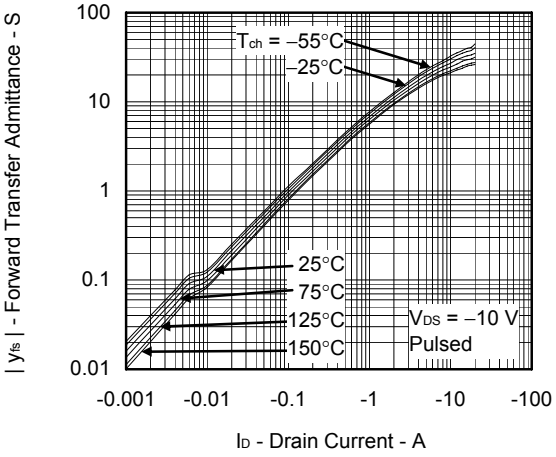
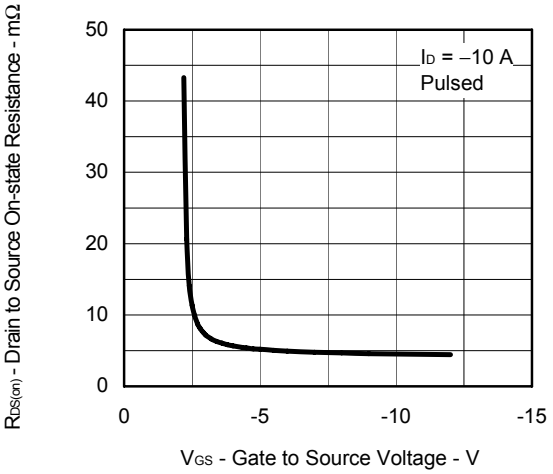
GATE TO SOURCE CUT-OFF VOLTAGE vs.
CHANNEL TEMPERATURE



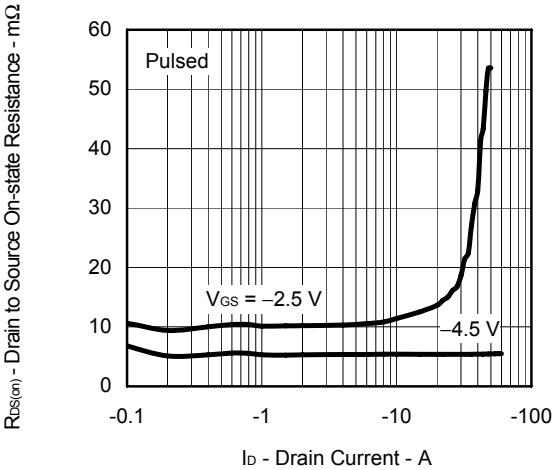
FORWARD TRANSFER ADMITTANCE vs.
DRAIN CURRENT



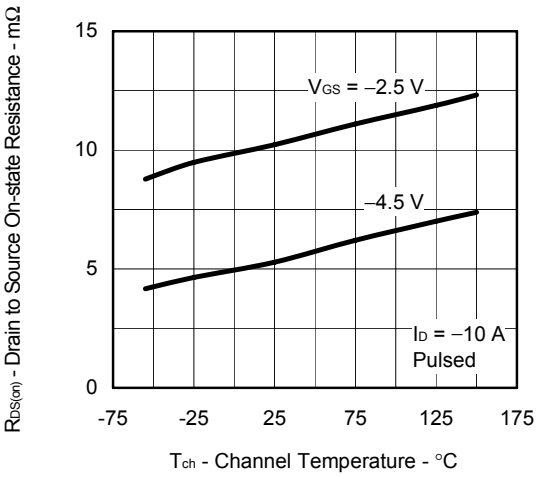
DRAIN TO SOURCE ON-STATE RESISTANCE vs.
DRAIN CURRENT



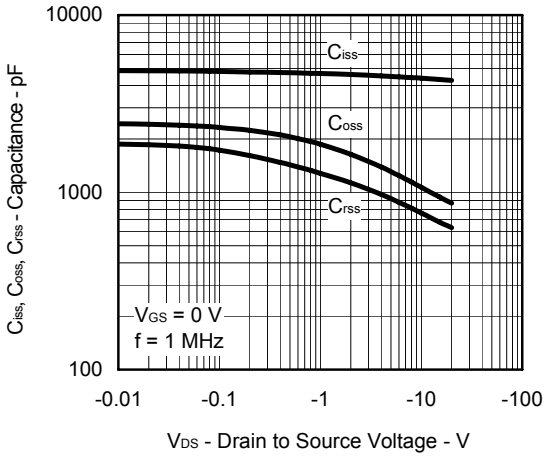
DRAIN TO SOURCE ON-STATE RESISTANCE vs.
GATE TO SOURCE VOLTAGE



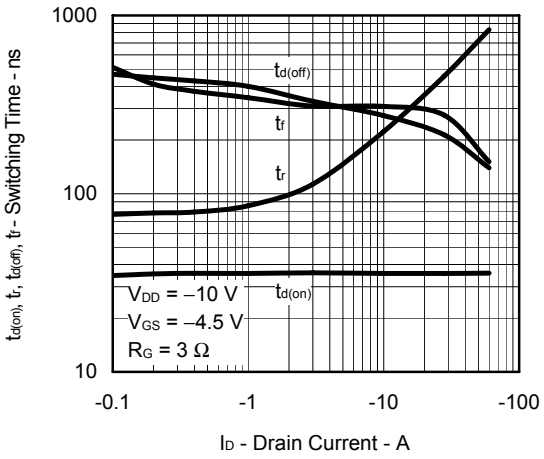
DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



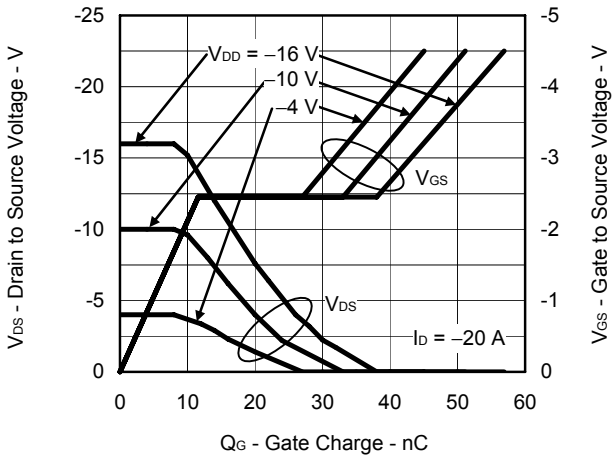
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



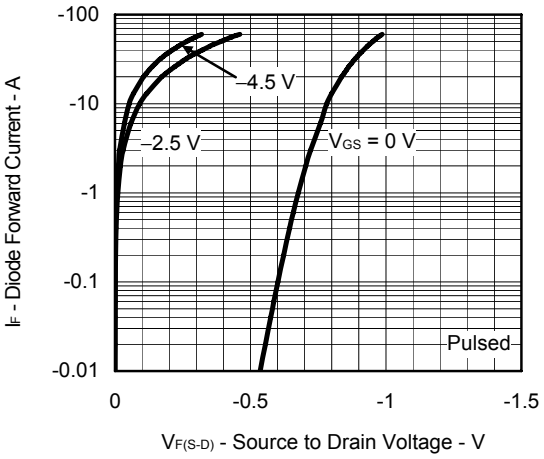
SWITCHING CHARACTERISTICS



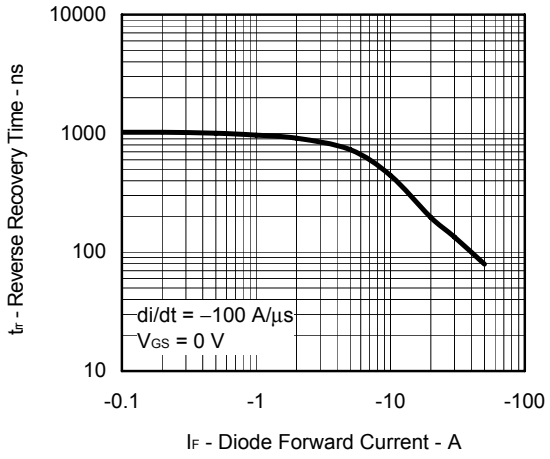
DYNAMIC INPUT/OUTPUT CHARACTERISTICS



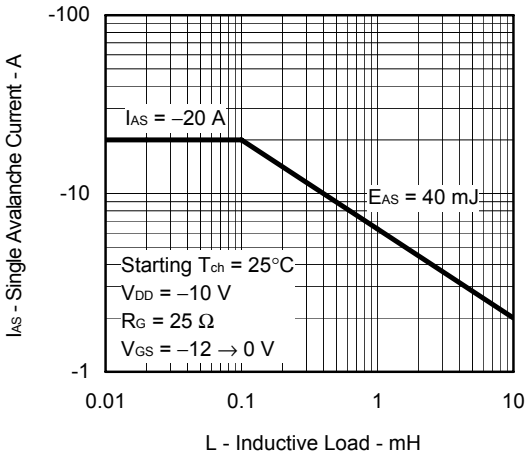
SOURCE TO DRAIN DIODE FORWARD VOLTAGE



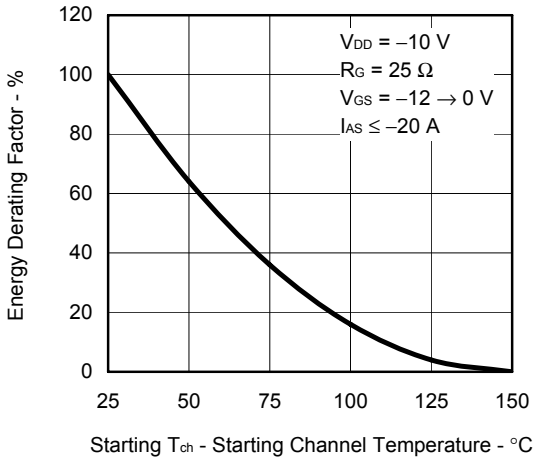
REVERSE RECOVERY TIME vs. DIODE FORWARD CURRENT



SINGLE AVALANCHE CURRENT vs.
INDUCTIVE LOAD

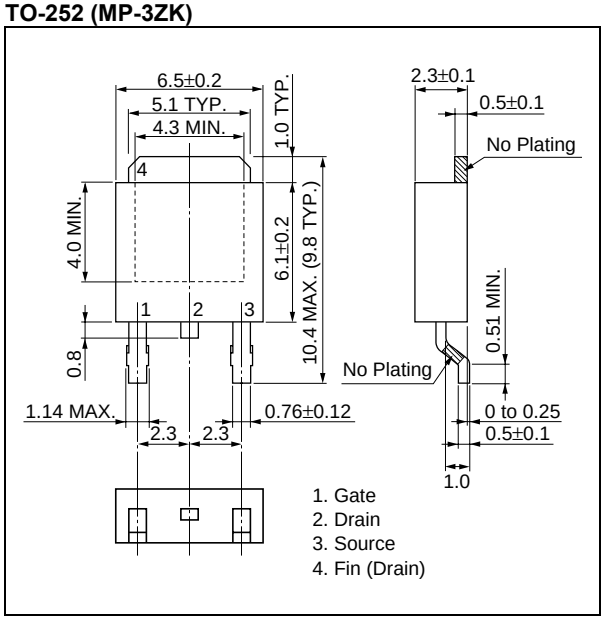


SINGLE AVALANCHE ENERGY
DERATING FACTOR

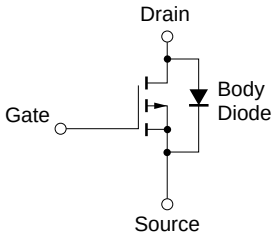


PACKAGE DRAWING (Unit: mm)

TO-252 (MP-3ZK)



EQUIVALENT CIRCUIT



Remark Strong electric field, when exposed to this device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred.

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