Low Power, 1 nV/√Hz, G ≥ 10 Stable, Rail-to-Rail Output Amplifier

Data Sheet

ADA4895-1/ADA4895-2

FEATURES

- Low wideband noise
  - 1 nV/√Hz
  - 1.6 pA/√Hz
- Low 1/f noise: 2 nV/√Hz at 10 Hz
- Low distortion (SFDR): −96 dBc at 100 kHz, V_{OUT} = 2 V p-p
- Low power: 3 mA per amplifier
- Low input offset voltage: 350 µV maximum
- High speed
  - 236 MHz, −3 dB bandwidth (G = +10)
  - 943 V/µs slew rate
  - 22 ns settling time to 0.1%
- Rail-to-rail output
- Wide supply range: 3 V to 10 V
- Disable feature

APPLICATIONS

- Low noise preamplifier
- Ultrasound amplifiers
- PLL loop filters
- High performance analog-to-digital converter (ADC) drivers
- Digital-to-analog converter (DAC) buffers

GENERAL DESCRIPTION

The ADA4895-1 (single) and ADA4895-2 (dual) are high speed voltage feedback amplifiers that are gain ≥ 10 stable with low input noise, rail-to-rail output, and a quiescent current of 3 mA per amplifier. With a 1/f noise of 2 nV/√Hz at 10 Hz and a spurious-free dynamic range (SFDR) of −72 dBc at 2 MHz, the ADA4895-1/ADA4895-2 are an ideal solution in a variety of applications, including ultrasound, low noise preamplifiers, and drivers of high performance ADCs. The Analog Devices, Inc., proprietary next generation SiGe bipolar process and innovative architecture enables the high performance of these amplifiers.

The ADA4895-1/ADA4895-2 have a small signal bandwidth of 236 MHz at a gain of +10 with a slew rate of 943 V/µs, and settle to 0.1% in 22 ns. The wide supply voltage range (3 V to 10 V) of the ADA4895-1/ADA4895-2 make these amplifiers ideal candidates for systems that require large dynamic range, high gain, precision, and high speed.

The ADA4895-1 is available in 8-lead SOIC and 6-lead SOT-23 packages, and the ADA4895-2 is available in a 10-lead MSOP package. All packages operate over the extended industrial temperature range of −40°C to +125°C.

FUNCTIONAL BLOCK DIAGRAMS

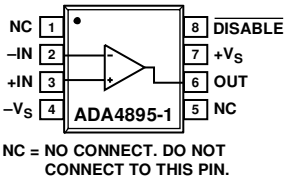

Figure 1. ADA4895-1 Single Amplifier (8-Lead SOIC)

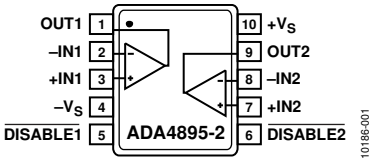

Figure 2. ADA4895-2 Dual Amplifier (10-Lead MSOP)

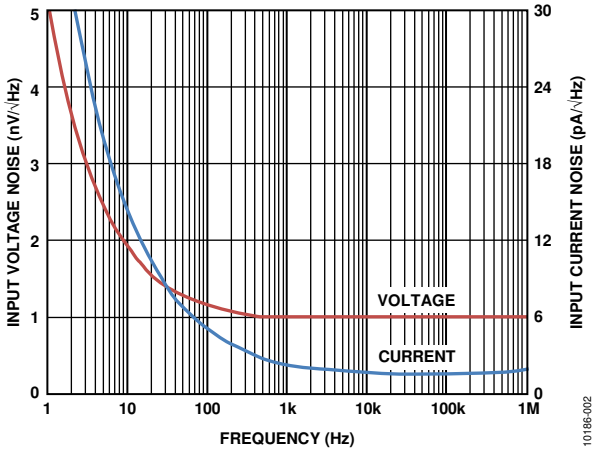

Figure 3. Input Voltage and Current Noise vs. Frequency

Table 1. Other Low Noise Amplifiers[1]

Part Number(s)	$\overline{e_{ven}}$ at 100 kHz (nV/√Hz)	Bandwidth (MHz)	Supply Voltage (V)
AD8021	2.1	490	5 to 24
AD8045	3	1000	3.3 to 12
AD8099	0.95	510	5 to 12
ADA4841-1/ADA4841-2	2.1	80	2.7 to 12
ADA4896-2	1	230	3 to 10
ADA4897-1/ADA4897-2	1	230	3 to 10
ADA4898-1/ADA4898-2	0.9	65	10 to 32
ADA4899-1	1	600	5 to 12

[1] See www.analog.com for the latest selection of low noise amplifiers.

COMPANION PRODUCTS

ADCs: AD7944 (14-bit), AD7985 (16-bit), AD7986 (18-bit)
Additional companion products on the ADA4895-1/ADA4895-2 product page

Rev. B
Document Feedback

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9/12—Revision 0: Initial Version

SPECIFICATIONS

±5 V (OR +10 V) SUPPLY

T_A = 25°C, G = +10, R_F = 249 Ω, R_L = 1 kΩ to midsupply, unless otherwise noted.

Table 2.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE					
−3 dB Bandwidth	V_{OUT} = 0.2 V p-p		236		MHz
	V_{OUT} = 2 V p-p		146		MHz
	V_{OUT} = 0.2 V p-p, G = +20, R_F = 1 kΩ		115		MHz
Bandwidth for 0.1 dB Flatness	V_{OUT} = 2 V p-p, R_L = 100 Ω		8.9		MHz
Slew Rate	V_{OUT} = 6 V step		943		V/µs
Settling Time to 0.1%	V_{OUT} = 2 V step		22		ns
NOISE/HARMONIC PERFORMANCE					
Harmonic Distortion (SFDR)	f_C = 100 kHz, V_{OUT} = 2 V p-p		−96		dBc
	f_C = 1 MHz, V_{OUT} = 2 V p-p		−78		dBc
	f_C = 2 MHz, V_{OUT} = 2 V p-p		−72		dBc
	f_C = 5 MHz, V_{OUT} = 2 V p-p		−64		dBc
Input Voltage Noise	f = 10 Hz, G = +25.9		2		nV/√Hz
	f = 100 kHz, G = +25.9		1		nV/√Hz
Input Current Noise	f = 10 Hz, R_F = 10 kΩ, R_G = 1.1 kΩ, R_S = 1 kΩ		14		pA/√Hz
	f = 100 kHz, R_F = 10 kΩ, R_G = 1.1 kΩ, R_S = 1 kΩ		1.6		pA/√Hz
0.1 Hz to 10 Hz Noise	G = +101, R_F = 1 kΩ, R_G = 10 Ω		99		nV p-p
DC PERFORMANCE					
Input Offset Voltage		−350	+53	+350	µV
Input Offset Voltage Drift			0.15		µV/°C
Input Bias Current		−16	−11	−6	µA
Input Bias Current Drift			1.2		nA/°C
Input Bias Offset Current		−0.6	−0.02	+0.6	µA
Open-Loop Gain	V_{OUT} = −4 V to +4 V	100	110		dB
INPUT CHARACTERISTICS					
Input Resistance	Common mode/differential mode		10 M/10 k		Ω
Input Capacitance	Common mode/differential mode		3/11		pF
Input Common-Mode Voltage Range			−4.9 to +4.1		V
Common-Mode Rejection	V_{CM} = −2 V to +2 V	−100	−109		dB
OUTPUT CHARACTERISTICS					
Output Overdrive Recovery Time	V_{IN} = −0.55 V to +0.55 V		80		ns
Positive Output Voltage Swing	R_L = 1 kΩ	4.85	4.96		V
	R_L = 100 Ω	4.5	4.77		V
Negative Output Voltage Swing	R_L = 1 kΩ	−4.85	−4.97		V
	R_L = 100 Ω	−4.5	−4.85		V
Linear Output Current	SFDR = −45 dBc		80		mA rms
Short-Circuit Current	Sinking/sourcing		116/111		mA
Capacitive Load Drive	30% overshoot		6		pF
POWER SUPPLY					
Operating Range			3 to 10		V
Quiescent Current per Amplifier		2.8	3	3.2	mA
	$\overline{\text{DISABLEx}}$ = −5 V		0.1		mA
Positive Power Supply Rejection	$+V_S$ = 4 V to 6 V, $-V_S$ = −5 V	−98	−136		dB
Negative Power Supply Rejection	$+V_S$ = 5 V, $-V_S$ = −4 V to −6 V	−98	−135		dB

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
$\overline{\text{DISABLE}}$x PIN					
$\overline{\text{DISABLE}}$x Voltage	Device enabled		>+V_S − 0.5		V
	Device disabled		<+V_S − 2		V
Input Current per Amplifier					
Device Enabled	$\overline{\text{DISABLE}}$x = +5 V		−1.1		µA
Device Disabled	$\overline{\text{DISABLE}}$x = −5 V		−40		µA
Switching Speed					
Device Enabled			0.25		µs
Device Disabled			6		µs

±2.5 V (OR +5 V) SUPPLY

T_A = 25°C, G = +10, R_F = 249 Ω, R_L = 1 kΩ to midsupply, unless otherwise noted.

Table 3.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE					
−3 dB Bandwidth	V_{OUT} = 0.2 V p-p		216		MHz
	V_{OUT} = 2 V p-p		131		MHz
	V_{OUT} = 0.2 V p-p, G = +20, R_F = 1 kΩ		113		MHz
Bandwidth for 0.1 dB Flatness	V_{OUT} = 2 V p-p, R_L = 100 Ω		7.9		MHz
Slew Rate	V_{OUT} = 3 V step		706		V/µs
Settling Time to 0.1%	V_{OUT} = 2 V step		21		ns
NOISE/HARMONIC PERFORMANCE					
Harmonic Distortion (SFDR)	f_C = 100 kHz, V_{OUT} = 2 V p-p		−94		dBc
	f_C = 1 MHz, V_{OUT} = 2 V p-p		−75		dBc
	f_C = 2 MHz, V_{OUT} = 2 V p-p		−69		dBc
	f_C = 5 MHz, V_{OUT} = 2 V p-p		−61		dBc
Input Voltage Noise	f = 10 Hz, G = +25.9		1.8		nV/√Hz
	f = 100 kHz, G = +25.9		1		nV/√Hz
Input Current Noise	f = 10 Hz, R_F = 10 kΩ, R_G = 1.1 kΩ, R_S = 1 kΩ		14		pA/√Hz
	f = 100 kHz, R_F = 10 kΩ, R_G = 1.1 kΩ, R_S = 1 kΩ		1.7		pA/√Hz
0.1 Hz to 10 Hz Noise	G = +101, R_F = 1 kΩ, R_G = 10 Ω		99		nV p-p
DC PERFORMANCE					
Input Offset Voltage		−350	+53	+350	µV
Input Offset Voltage Drift			0.15		µV/°C
Input Bias Current		−16	−11	−6	µA
Input Bias Current Drift			1.2		nA/°C
Input Bias Offset Current		−0.6	−0.02	+0.6	µA
Open-Loop Gain	V_{OUT} = −2 V to +2 V	97	108		dB
INPUT CHARACTERISTICS					
Input Resistance	Common mode/differential mode		10 M/10 k		Ω
Input Capacitance	Common mode/differential mode		3/11		pF
Input Common-Mode Voltage Range			−2.4 to +1.6		V
Common-Mode Rejection	V_{CM} = −1.5 V to +1.5 V	−98	−110		dB
OUTPUT CHARACTERISTICS					
Output Overdrive Recovery Time	V_{IN} = −0.275 V to +0.275 V		90		ns
Positive Output Voltage Swing	R_L = 1 kΩ	2.35	2.48		V
	R_L = 100 Ω	2.3	2.38		V
Negative Output Voltage Swing	R_L = 1 kΩ	−2.35	−2.48		V
	R_L = 100 Ω	−2.3	−2.38		V
Linear Output Current	SFDR = −45 dBc		64		mA rms
Short-Circuit Current	Sinking/sourcing		111/98		mA
Capacitive Load Drive	30% overshoot		6		pF

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
POWER SUPPLY					
Operating Range			3 to 10		V
Quiescent Current per Amplifier		2.6	2.8	3	mA
	$\overline{\text{DISABLEx}}$ = −2.5 V		0.05		mA
Positive Power Supply Rejection	$+V_S$ = 2 V to 3 V, $-V_S$ = −2.5 V	−98	−137		dB
Negative Power Supply Rejection	$+V_S$ = 2.5 V, $-V_S$ = −3 V to −2 V	−98	−141		dB
$\overline{\text{DISABLEx}}$ PIN					
$\overline{\text{DISABLEx}}$ Voltage	Device enabled		>$+V_S$ − 0.5		V
	Device disabled		<$+V_S$ − 2		V
Input Current per Amplifier					
Device Enabled	$\overline{\text{DISABLEx}}$ = +2.5 V		−1.1		µA
Device Disabled	$\overline{\text{DISABLEx}}$ = −2.5 V		−20		µA
Switching Speed					
Device Enabled			0.25		µs
Device Disabled			6		µs

±1.5 V (OR +3 V) SUPPLY

T_A = 25°C, G = +10, R_F = 249 Ω, R_L = 1 kΩ to midsupply, unless otherwise noted.

Table 4.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE					
−3 dB Bandwidth	V_{OUT} = 0.2 V p-p		205		MHz
	V_{OUT} = 1 V p-p		131		MHz
	V_{OUT} = 0.2 V p-p, G = +20, R_F = 1 kΩ		111		MHz
Bandwidth for 0.1 dB Flatness	V_{OUT} = 2 V p-p, R_L = 100 Ω		7.5		MHz
Slew Rate	V_{OUT} = 1 V step		384		V/µs
Settling Time to 0.1%	V_{OUT} = 2 V step		20		ns
NOISE/HARMONIC PERFORMANCE					
Harmonic Distortion (SFDR)	f_C = 100 kHz, V_{OUT} = 2 V p-p		−92		dBc
	f_C = 1 MHz, V_{OUT} = 2 V p-p		−73		dBc
	f_C = 2 MHz, V_{OUT} = 2 V p-p		−67		dBc
	f_C = 5 MHz, V_{OUT} = 2 V p-p		−59		dBc
Input Voltage Noise	f = 10 Hz, G = +25.9		1.9		nV/√Hz
	f = 100 kHz, G = +25.9		1		nV/√Hz
Input Current Noise	f = 10 Hz, R_F = 10 kΩ, R_G = 1.1 kΩ, R_S = 1 kΩ		14		pA/√Hz
	f = 100 kHz, R_F = 10 kΩ, R_G = 1.1 kΩ, R_S = 1 kΩ		1.7		pA/√Hz
0.1 Hz to 10 Hz Noise	G = +101, R_F = 1 kΩ, R_G = 10 Ω		99		nV p-p
DC PERFORMANCE					
Input Offset Voltage		−350	+55	+350	µV
Input Offset Voltage Drift			0.15		µV/°C
Input Bias Current		−16	−11	−6	µA
Input Bias Current Drift			1.2		nA/°C
Input Bias Offset Current		−0.6	−0.02	+0.6	µA
Open-Loop Gain	V_{OUT} = −1 V to +1 V	95	106		dB
INPUT CHARACTERISTICS					
Input Resistance	Common mode/differential mode		10 M/10 k		Ω
Input Capacitance	Common mode/differential mode		3/11		pF
Input Common-Mode Voltage Range			−1.4 to +0.6		V
Common-Mode Rejection	V_{CM} = −0.4 V to +0.4 V	−93	−110		dB

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
OUTPUT CHARACTERISTICS					
Output Overdrive Recovery Time	V_{IN} = −0.165 V to +0.165 V		80		ns
Positive Output Voltage Swing	R_L = 1 kΩ	1.35	1.48		V
	R_L = 100 Ω	1.3	1.43		V
Negative Output Voltage Swing	R_L = 1 kΩ	−1.35	−1.49		V
	R_L = 100 Ω	−1.3	−1.45		V
Linear Output Current	SFDR = −45 dBc		46		mA rms
Short-Circuit Current	Sinking/sourcing		99/83		mA
Capacitive Load Drive	30% overshoot		6		pF
POWER SUPPLY					
Operating Range			3 to 10		V
Quiescent Current per Amplifier		2.5	2.7	2.9	mA
	$\overline{\text{DISABLEx}}$ = −1.5 V		0.03		mA
Positive Power Supply Rejection	$+V_S$ = 1.2 V to 2.2 V, $-V_S$ = −1.5 V	−98	−133		dB
Negative Power Supply Rejection	$+V_S$ = 1.5 V, $-V_S$ = −2.2 V to −1.2 V	−98	−146		dB
$\overline{\text{DISABLEx}}$ PIN					
$\overline{\text{DISABLEx}}$ Voltage	Device enabled		> $+V_S$ − 0.5		V
	Device disabled		< $+V_S$ − 2		V
Input Current per Amplifier					
Device Enabled	$\overline{\text{DISABLEx}}$ = +1.5 V		−1.2		µA
Device Disabled	$\overline{\text{DISABLEx}}$ = −1.5 V		−10		µA
Switching Speed					
Device Enabled			0.25		µs
Device Disabled			6		µs

ABSOLUTE MAXIMUM RATINGS

Table 5.

Parameter	Rating
Supply Voltage	11 V
Power Dissipation	See Figure 4
Common-Mode Input Voltage	$-V_S - 0.7$ V to $+V_S + 0.7$ V
Differential Input Voltage	±0.7 V
Storage Temperature Range	−65°C to +125°C
Operating Temperature Range	−40°C to +125°C
Lead Temperature (Soldering 10 sec)	300°C
Junction Temperature	150°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, θ_{JA} is specified for a device soldered in a circuit board for surface-mount packages. Table 6 lists the θ_{JA} for the ADA4895-1/ADA4895-2.

Table 6. Thermal Resistance

Package Type	θ_{JA}	Unit
8-Lead Single SOIC	133	°C/W
6-Lead Single SOT-23	150	°C/W
10-Lead Dual MSOP	210	°C/W

MAXIMUM POWER DISSIPATION

The maximum safe power dissipation for the ADA4895-1/ADA4895-2 is limited by the associated rise in junction temperature (T_J) on the die. At approximately 150°C, which is the glass transition temperature, the properties of the plastic change. Even temporarily exceeding this temperature limit can change the stresses that the package exerts on the die, permanently shifting the parametric performance of the ADA4895-1/ADA4895-2. Exceeding a junction temperature of 175°C for an extended period of time can result in changes in silicon devices, potentially causing degradation or loss of functionality.

The power dissipated in the package (P_D) is the sum of the quiescent power dissipation and the power dissipated in the die due to the ADA4895-1/ADA4895-2 drive at the output.

$$P_D = \textit{Quiescent Power} + (\textit{Total Drive Power} - \textit{Load Power})$$

The quiescent power dissipation is the voltage between the supply pins ($\pm V_S$) multiplied by the quiescent current (I_S).

$$P_D = \left(V_S \times I_S\right) + \left(\frac{V_S}{2} \times \frac{V_{OUT}}{R_L}\right) - \frac{{V_{OUT}}^2}{R_L}$$

Consider rms output voltages. If R_L is referenced to $-V_S$, as in single-supply operation, the total drive power is $V_S \times I_{OUT}$. In single-supply operation with R_L referenced to $-V_S$, the worst case is $V_{OUT} = V_S/2$.

If the rms signal levels are indeterminate, consider the worst case, when $V_{OUT} = V_S/4$ with R_L referenced to midsupply.

$$P_D = \left(V_S \times I_S\right) + \frac{\left(V_S/4\right)^2}{R_L}$$

Airflow increases heat dissipation, effectively reducing θ_{JA}. Also, more metal directly in contact with the package leads reduces θ_{JA}.

Figure 4 shows the maximum safe power dissipation in the package vs. the ambient temperature on a JEDEC standard, 4-layer board. θ_{JA} values are approximations.

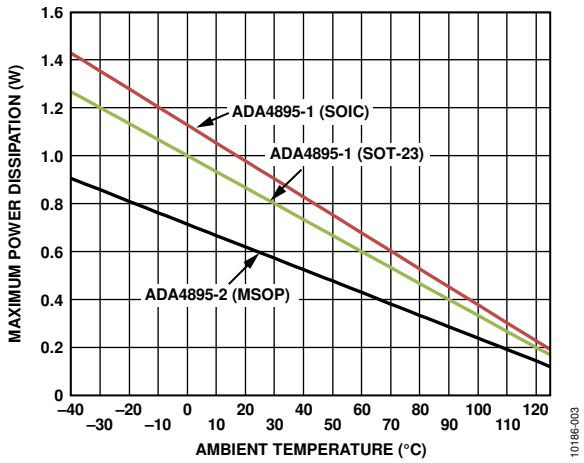


Figure 4. Maximum Power Dissipation vs. Temperature for a 4-Layer Board

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

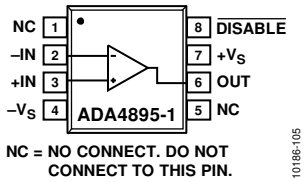


Figure 5. 8-Lead SOIC Pin Configuration for the ADA4895-1

Table 7. 8-Lead SOIC Pin Function Descriptions for the ADA4895-1

Pin No.	Mnemonic	Description
1, 5	NC	No Connect. Do not connect to these pins.
2	–IN	Inverting Input.
3	+IN	Noninverting Input.
4	$-V_S$	Negative Supply.
6	OUT	Output.
7	$+V_S$	Positive Supply.
8	$\overline{\text{DISABLE}}$	Disable.

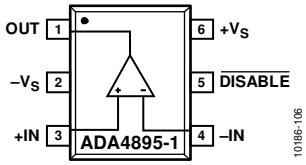


Figure 6. 6-Lead SOT-23 Pin Configuration for the ADA4895-1

Table 8. 6-Lead SOT-23Pin Function Descriptions for the ADA4895-1

Pin No.	Mnemonic	Description
1	OUT	Output
2	$-V_S$	Negative Supply
3	+IN	Noninverting Input
4	–IN	Inverting Input
5	$\overline{\text{DISABLE}}$	Disable
6	$+V_S$	Positive Supply

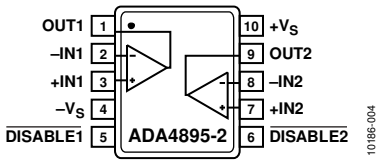


Figure 7. 10-Lead MSOP Pin Configuration for the ADA4895-2

Table 9. 10-Lead MSOP Pin Function Descriptions for the ADA4895-2

Pin Number	Mnemonic	Description
1	OUT1	Output 1
2	–IN1	Inverting Input 1
3	+IN1	Noninverting Input 1
4	$-V_S$	Negative Supply
5	$\overline{\text{DISABLE1}}$	Disable 1
6	$\overline{\text{DISABLE2}}$	Disable 2
7	+IN2	Noninverting Input 2
8	–IN2	Inverting Input 2
9	OUT2	Output 2
10	$+V_S$	Positive Supply

TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, V_S = ±2.5 V, G = +10, R_F = 249 Ω, R_L = 1 kΩ to midsupply, unless otherwise noted.

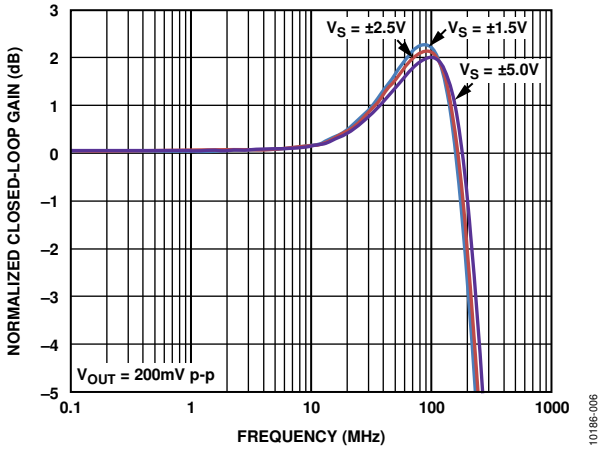


Figure 8. Small Signal Frequency Response vs. Supply Voltage

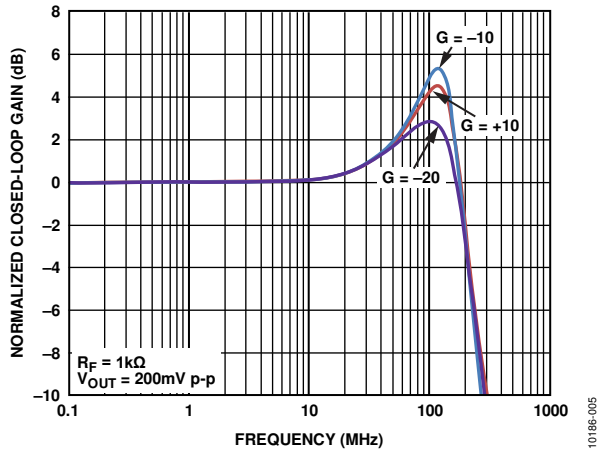


Figure 9. Small Signal Frequency Response vs. Gain

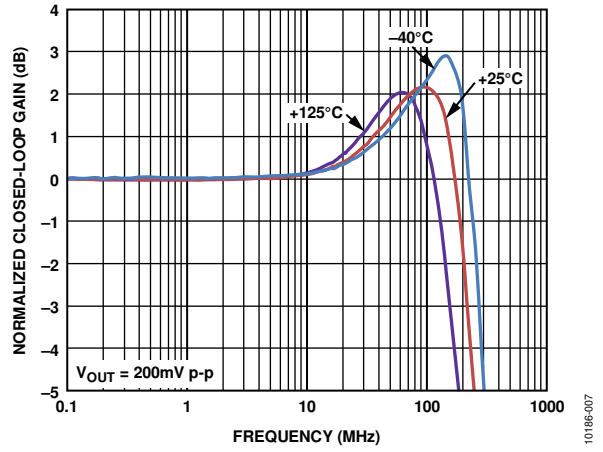


Figure 10. Small Signal Frequency Response vs. Temperature

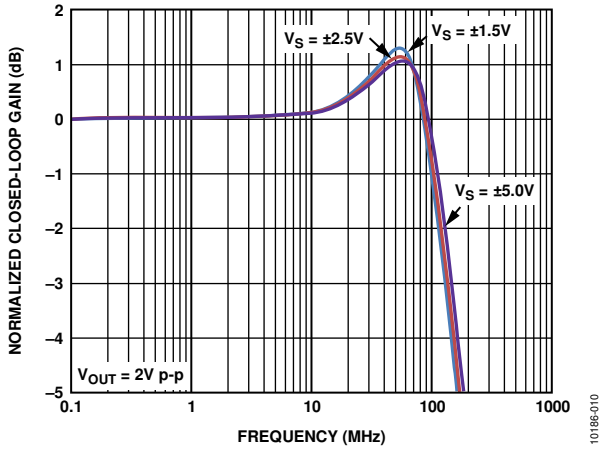


Figure 11. Large Signal Frequency Response vs. Supply Voltage

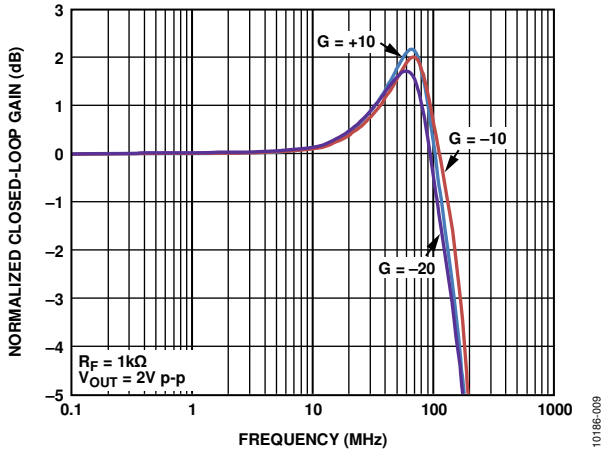


Figure 12. Large Signal Frequency Response vs. Gain

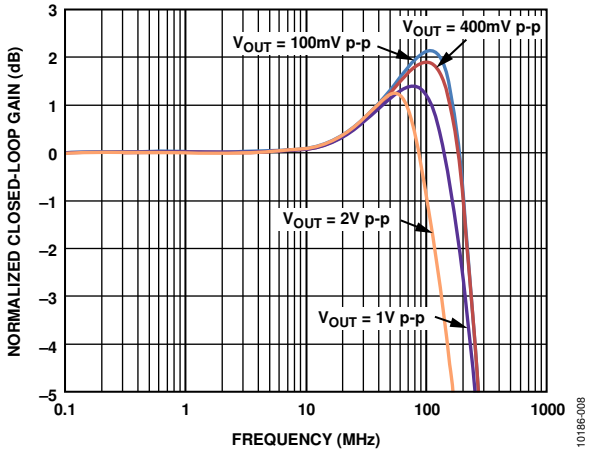


Figure 13. Frequency Response for Various Output Voltages

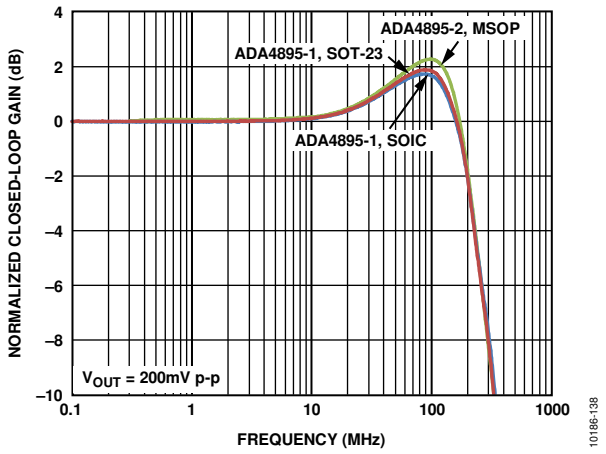


Figure 14. Small Signal Frequency Response vs. Package

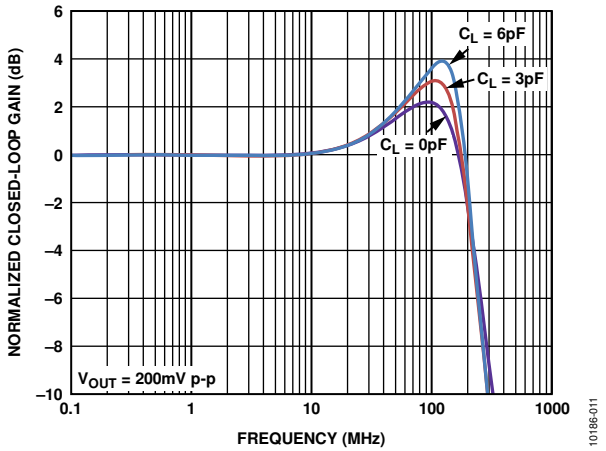


Figure 15. Small Signal Frequency Response vs. Capacitive Load

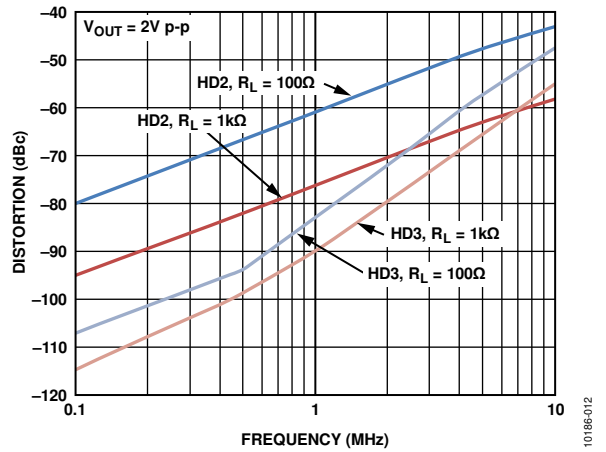


Figure 16. Harmonic Distortion vs. Frequency for Various Loads

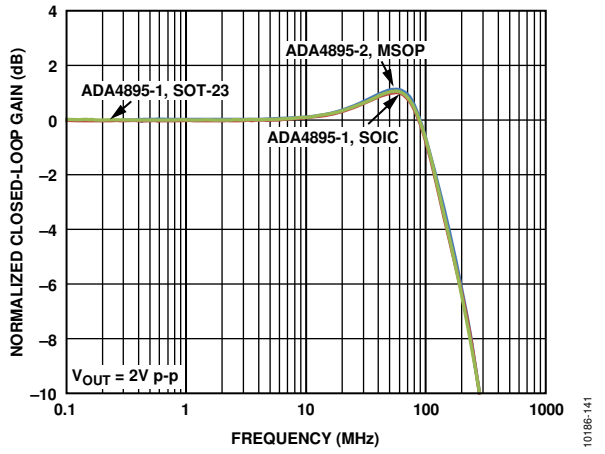


Figure 17. Large Signal Frequency Response vs. Package

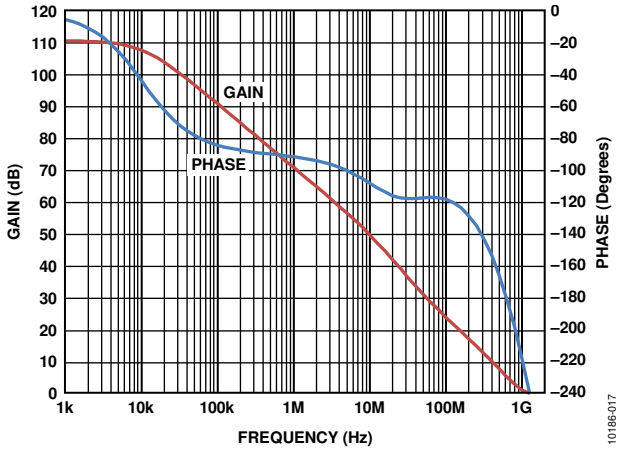


Figure 18. Open-Loop Gain and Phase vs. Frequency

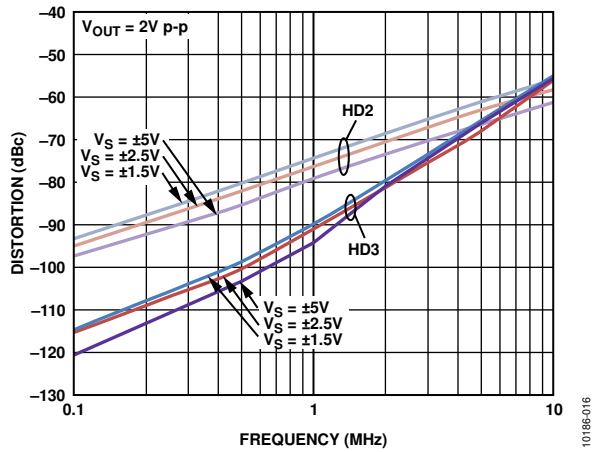


Figure 19. Harmonic Distortion vs. Frequency for Various Supplies

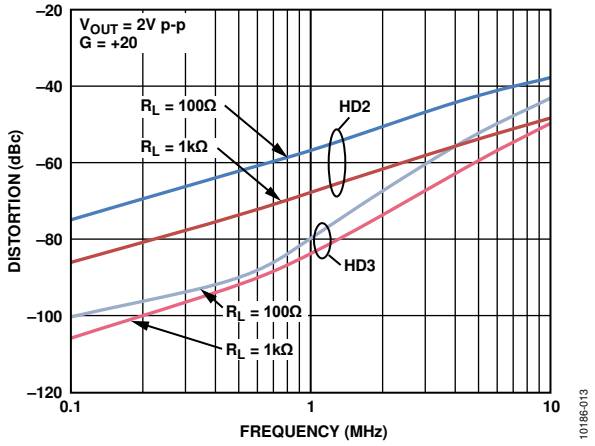


Figure 20. Harmonic Distortion vs. Frequency, G = +20

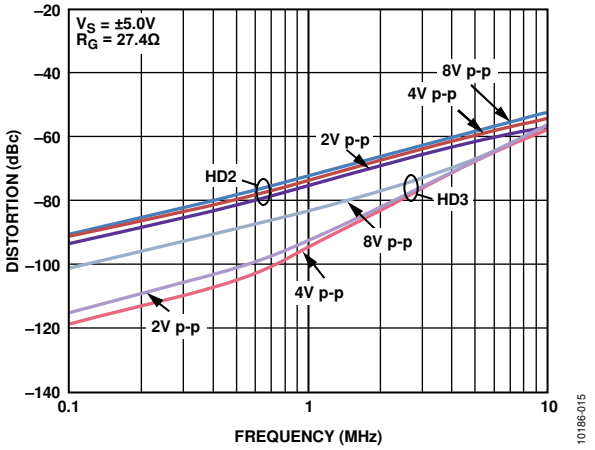


Figure 23. Harmonic Distortion vs. Frequency for Various Output Voltages

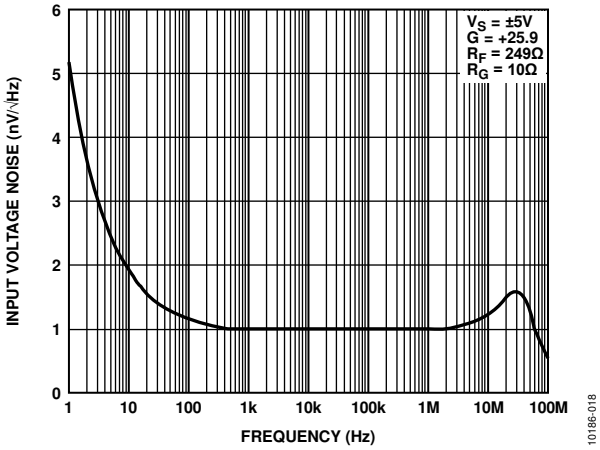


Figure 21. Input Voltage Noise vs. Frequency

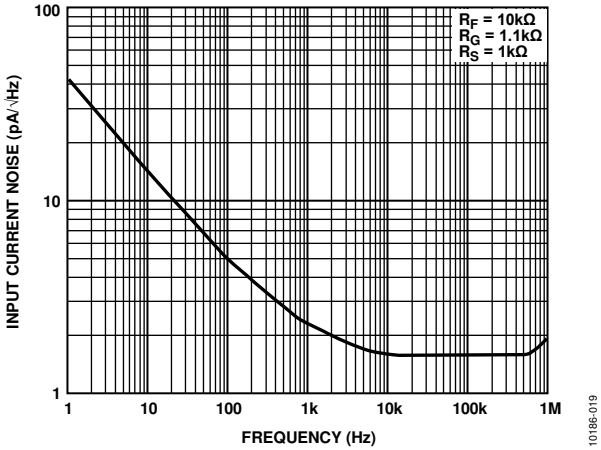


Figure 24. Input Current Noise vs. Frequency

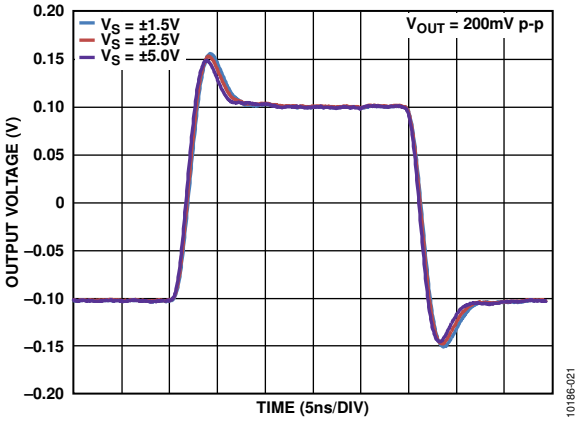


Figure 22. Small Signal Transient Response for Various Supplies

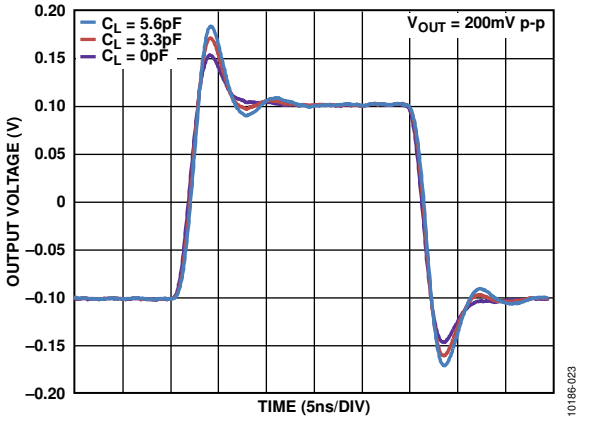


Figure 25. Small Signal Transient Response for Various Capacitive Loads

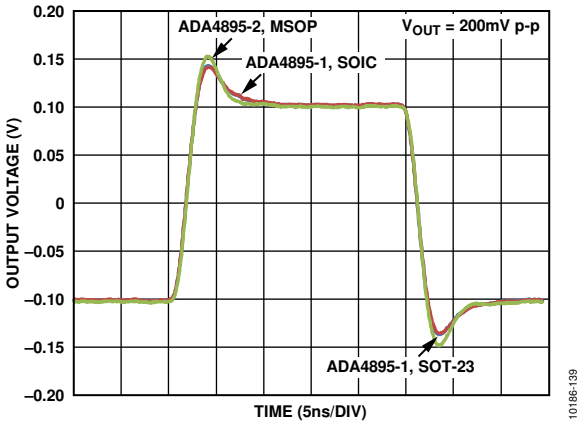


Figure 26. Small Signal Transient Response vs. Package

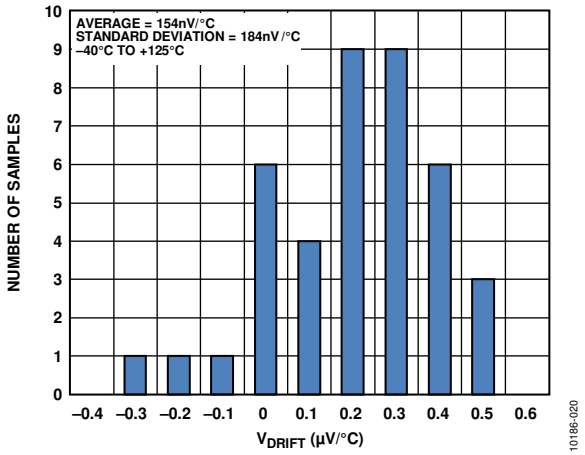


Figure 27. Input Offset Voltage Drift Distribution

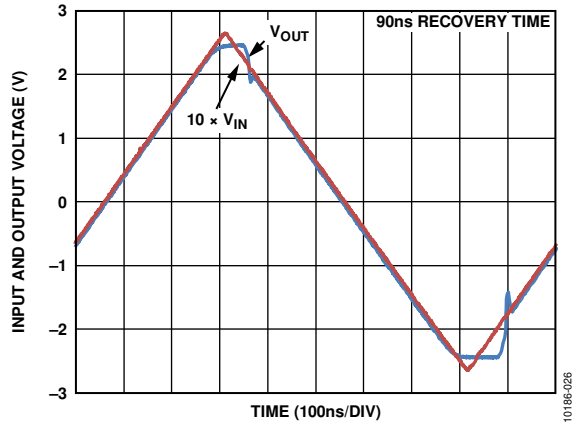


Figure 28. Output Overdrive Recovery Time

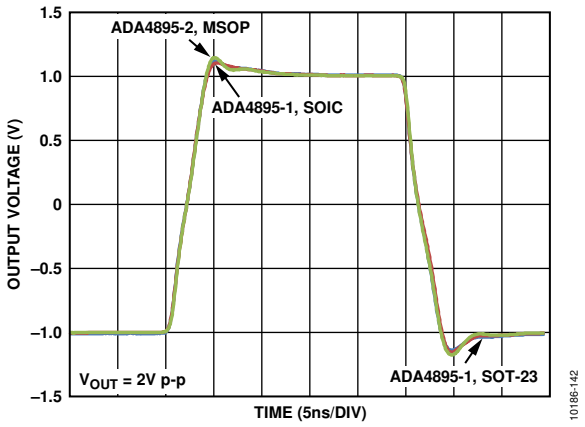


Figure 29. Large Signal Transient Response vs. Package

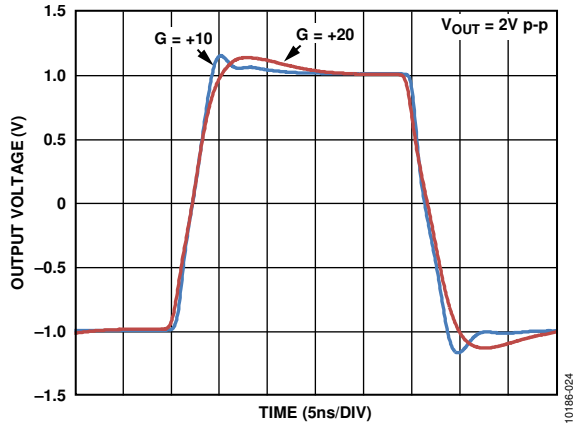


Figure 30. Large Signal Transient Response for Various Gains

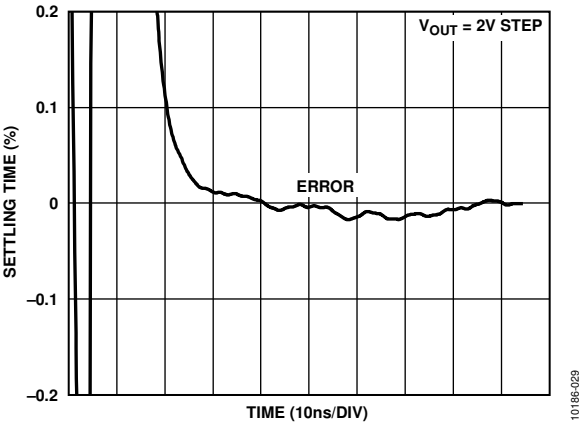


Figure 31. Settling Time to 0.1%

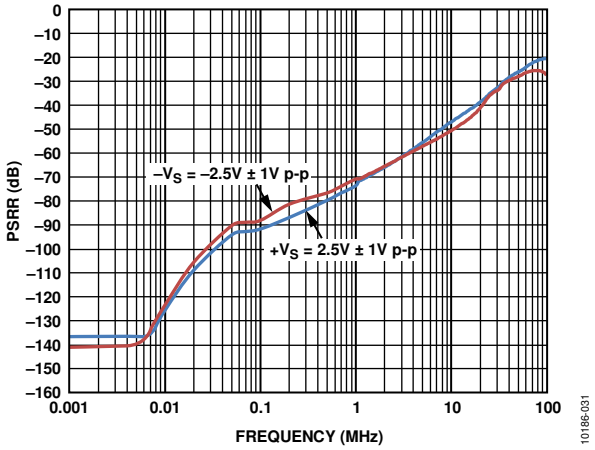


Figure 32. PSRR vs. Frequency

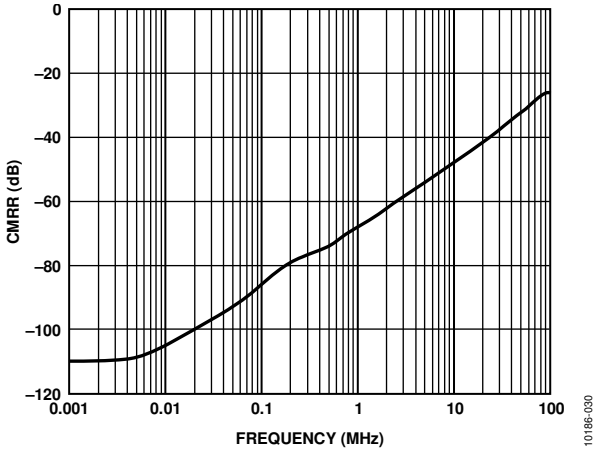


Figure 35. CMRR vs. Frequency

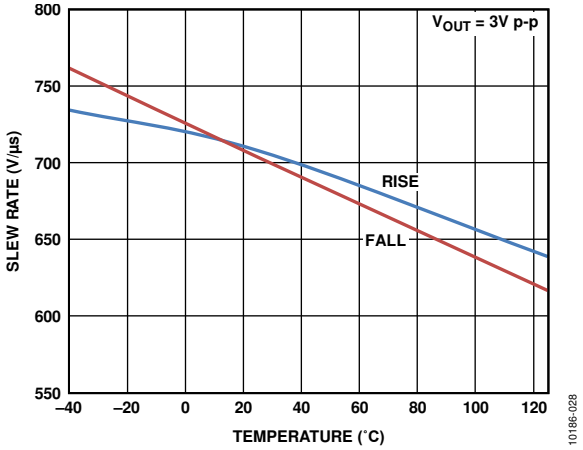


Figure 33. Slew Rate vs. Temperature

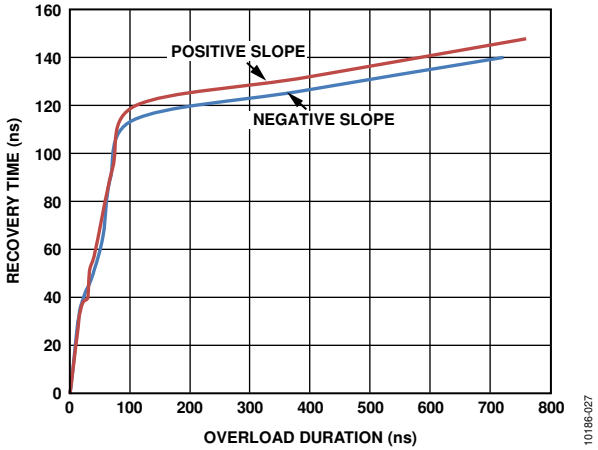


Figure 36. Output Overload Recovery Time vs. Overload Duration

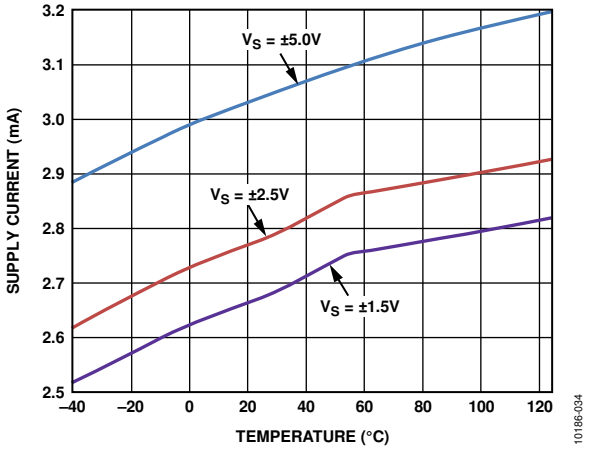


Figure 34. Supply Current vs. Temperature for Various Supplies

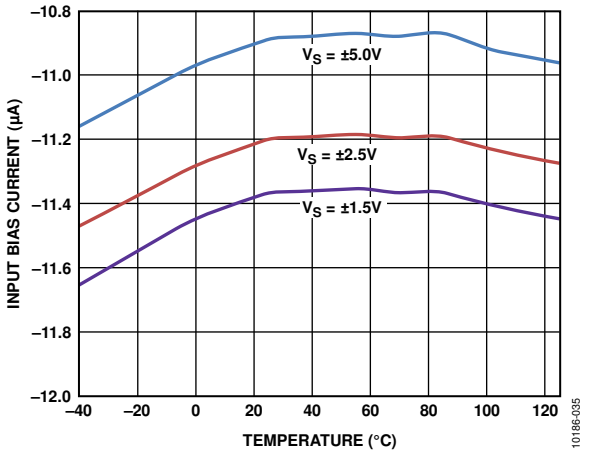


Figure 37. Input Bias Current vs. Temperature for Various Supplies

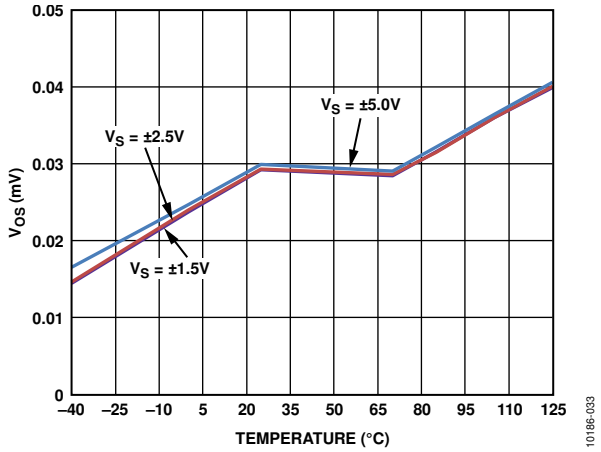


Figure 38. Input Offset Voltage vs. Temperature for Various Supplies

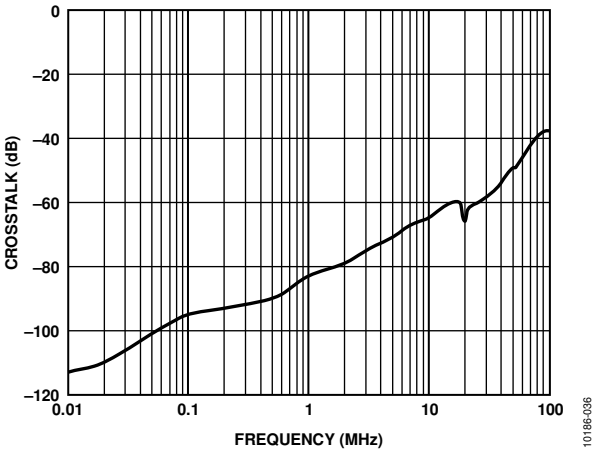


Figure 41. Crosstalk, OUT1 to OUT2

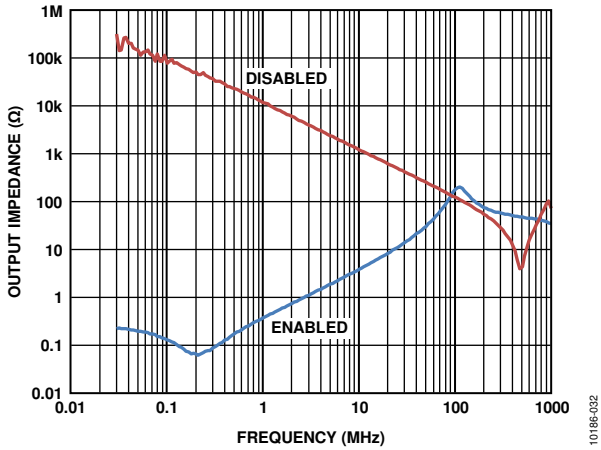


Figure 39. Output Impedance vs. Frequency

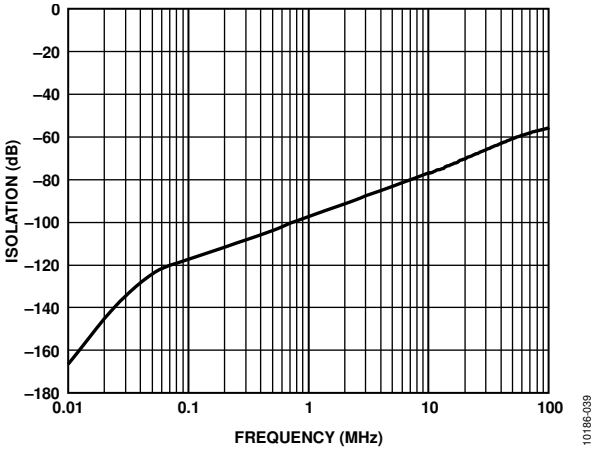


Figure 42. Forward Isolation vs. Frequency

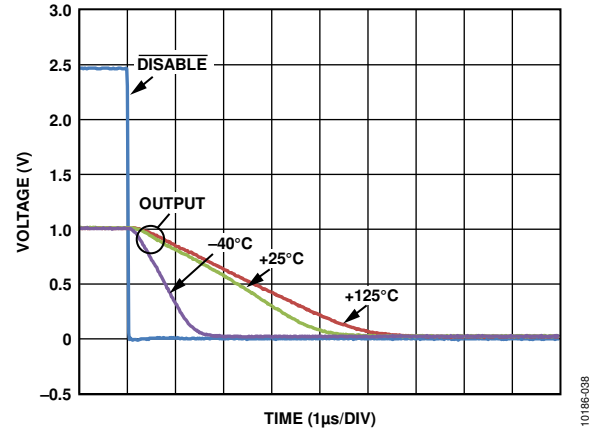


Figure 40. Output Turn-Off Time vs. Temperature

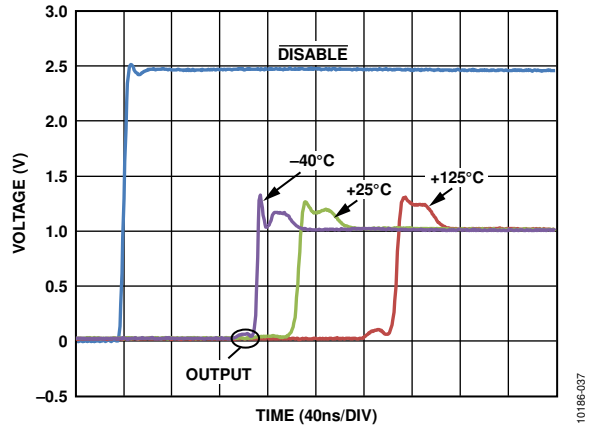


Figure 43. Output Turn-On Time vs. Temperature

THEORY OF OPERATION

AMPLIFIER DESCRIPTION

The ADA4895-1/ADA4895-2 amplifiers have an input noise of 1 nV/√Hz and consume 3 mA per amplifier from supply voltages of 3 V to 10 V. Using the Analog Devices XFCB3 process, the ADA4895-1/ADA4895-2 have a gain bandwidth product in excess of 1.5 GHz and are gain ≥ 10 stable, with an input structure that results in an extremely low input 1/f noise for a relatively high speed amplifier.

The rail-to-rail output stage is designed to drive the heavy feedback load required to achieve an overall low output referred noise. The low input noise and high bandwidth of the ADA4895-1/ADA4895-2 are achieved with minimal power penalty. For this reason, the maximum offset voltage of 350 µV and voltage drift of 0.15 µV/°C make the ADA4895-1/ADA4895-2 an excellent choice, even when the low noise performance of the amplifier is not needed.

For any gain greater than 10, the closed-loop frequency response of a basic noninverting configuration can be approximated by

$$Closed\text{-}Loop\ -3\ dB\ Frequency = (GBP) \times \frac{R_G}{(R_F + R_G)}$$

For inverting gain configurations, the source impedance must be considered when sizing R_G to maintain the minimum stable gain. For gains lower than 10, see the Using the ADA4895-1/ADA4895-2 at a Gain < +10 section, or use the ADA4897-1/ADA4897-2, which is a unity-gain stable amplifier with 230 MHz bandwidth.

INPUT PROTECTION

The ADA4895-1/ADA4895-2 are fully protected from ESD events and can withstand human body model ESD events of 2.5 kV and charged-device model events of 1 kV with no measured performance degradation. The precision input is protected with an ESD network between the power supplies and diode clamps across the input device pair, as shown in Figure 44.

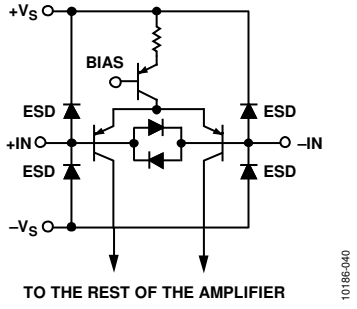


Figure 44. Input Stage and Protection Diodes

At differential voltages above approximately 0.7 V, the diode clamps begin to conduct. Too much current can cause damage due to excessive heating. If large differential voltages must be sustained across the input terminals, it is recommended that the current through the input clamps be limited to less than 10 mA. Series input resistors that are sized appropriately for the expected differential overvoltage provide the needed protection.

The ESD clamps begin to conduct at input voltages that are more than 0.7 V above the positive supply or more than 0.7 V below the negative supply. If an overvoltage condition is expected, it is recommended that the fault current be limited to less than 10 mA.

DISABLE OPERATION

Figure 45 shows the ADA4895-1/ADA4895-2 power-down circuitry. If the $\overline{\text{DISABLEx}}$ pin is left unconnected, the base of the input PNP transistor is pulled high through the internal pull-up resistor to the positive supply and the device is turned on. Pulling the $\overline{\text{DISABLEx}}$ pin more than 2 V below the positive supply turns the device off, reducing the supply current to approximately 50 µA for a 5 V voltage supply.

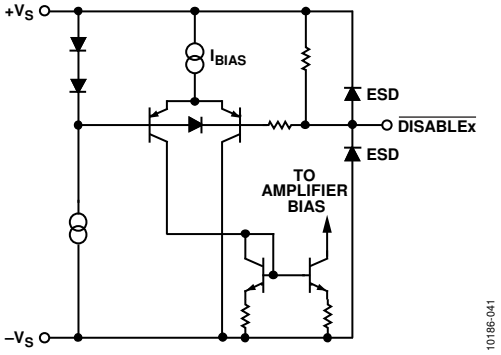


Figure 45. $\overline{\text{DISABLEx}}$ Circuit

The $\overline{\text{DISABLEx}}$ pin is protected by ESD clamps, as shown in Figure 45. Voltages beyond the power supplies cause these diodes to conduct. For protection of the $\overline{\text{DISABLEx}}$ pins, the voltage to these pins should not exceed 0.7 V beyond the supply voltage, or the input current should be restricted to less than 10 mA with a series resistor.

DC ERRORS

Figure 46 shows a typical connection diagram and the major dc error sources.

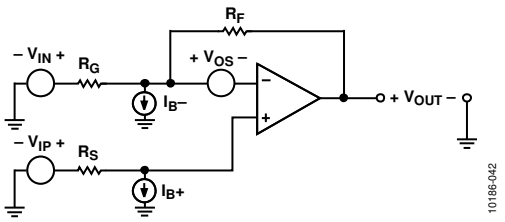


Figure 46. Typical Connection Diagram and DC Error Sources

The ideal transfer function (all error sources set to 0 and infinite dc gain) can be expressed as follows:

$$V_{OUT} = \left(1 + \frac{R_F}{R_G}\right) \times V_{IP} - \left(\frac{R_F}{R_G}\right) \times V_{IN} \quad (1)$$

This equation reduces to the familiar forms for noninverting and inverting op amp gain expressions, as follows:

For noninverting gain (V_{IN} = 0 V),

$$V_{OUT} = \left(1 + \frac{R_F}{R_G}\right) \times V_{IP} \quad (2)$$

For inverting gain (V_{IP} = 0 V),

$$V_{OUT} = \left(\frac{-R_F}{R_G}\right) \times V_{IN} \quad (3)$$

The total output voltage error is the sum of the errors due to the amplifier offset voltage and input currents. The output error due to the offset voltage can be estimated as follows:

$$V_{OUT_{ERROR}} = \left(V_{OFFSET_{NOM}} + \frac{V_{CM}}{CMRR} + \frac{V_P - V_{PNOM}}{PSRR} + \frac{V_{OUT}}{A}\right) \times \left(1 + \frac{R_F}{R_G}\right) \quad (4)$$

where:

$V_{OFFSET_{NOM}}$ is the offset voltage at the specified supply voltage, which is measured with the input and output at midsupply.
V_{CM} is the common-mode voltage.
CMRR is the common-mode rejection ratio.
V_P is the power supply voltage.
V_{PNOM} is the specified power supply voltage.
PSRR is the power supply rejection ratio.
A is the dc open-loop gain.

The output error due to the input currents can be estimated as follows:

$$V_{OUT_{ERROR}} = (R_F || R_G) \times \left(1 + \frac{R_F}{R_G}\right) \times I_{B-} - R_S \times \left(1 + \frac{R_F}{R_G}\right) \times I_{B+} \quad (5)$$

BIAS CURRENT CANCELLATION

To cancel the output voltage error due to unmatched bias currents at the inputs, Resistors R_{BP} and R_{BN} can be used (see Figure 47).

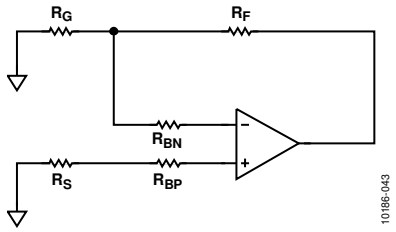


Figure 47. Using R_{BP} and R_{BN} to Cancel Bias Current Error

To compensate for the unmatched bias currents at the two inputs, set Resistors R_{BP} and R_{BN} as shown in Table 10.

Table 10. Setting R_{BP} and R_{BN} to Cancel Bias Current Error

Value of $R_F \| R_G$	Value of R_{BP} (Ω)	Value of R_{BN} (Ω)
Greater Than R_S	$R_F \| R_G - R_S$	0
Less Than R_S	0	$R_S - R_F \| R_G$

NOISE CONSIDERATIONS

Figure 48 illustrates the primary noise contributors for the typical gain configurations. The total rms output noise is the root mean square of all the contributions.

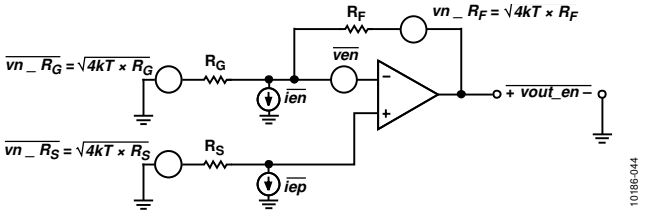


Figure 48. Noise Sources in Typical Gain Configurations

The output noise spectral density can be calculated as follows:

$$\overline{vout\_en} = \sqrt{4kTR_F + \left(1+\frac{R_F}{R_G}\right)^2\left[4kTR_S + \overline{iep}^2 R_S{}^2 + \overline{ven}^2\right] + \left(\frac{R_F}{R_G}\right)^2 4kTR_G + \overline{ien}^2 R_F{}^2} \quad (6)$$

where:
k is Boltzmann's constant.
T is the absolute temperature (degrees Kelvin).
R_F and R_G are the feedback network resistances, as shown in Figure 48.
R_S is the source resistance, as shown in Figure 48.
$\overline{iep}$ and $\overline{ien}$ represent the amplifier input current noise spectral density (pA/√Hz).
$\overline{ven}$ is the amplifier input voltage noise spectral density (nV/√Hz).

Source resistance noise, amplifier voltage noise ($\overline{ven}$), and the voltage noise from the amplifier current noise ($\overline{iep} \times R_S$) are all subject to the noise gain term ($1 + R_F/R_G$). Note that with a 1 nV/√Hz input voltage noise and a 1.7 pA/√Hz input current noise, the noise contributions of the amplifier are relatively small for source resistances from approximately 50 Ω to 700 Ω.

Figure 49 shows the total RTI noise due to the amplifier vs. the source resistance. In addition, the value of the feedback resistors affects the noise. It is recommended that the value of the feedback resistors be maintained between 250 Ω and 1 kΩ to keep the total noise low.

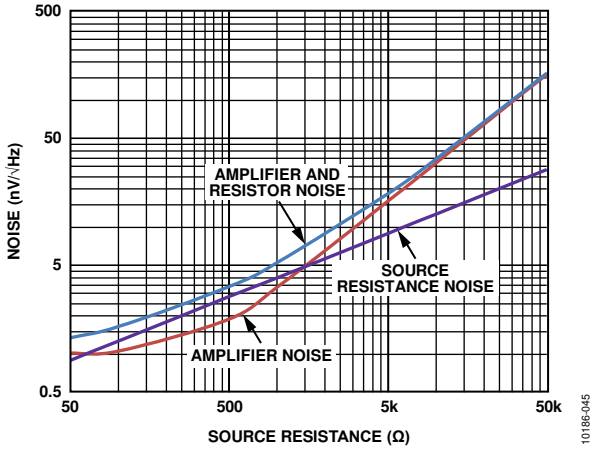


Figure 49. RTI Noise vs. Source Resistance

APPLICATIONS INFORMATION

USING THE ADA4895-1/ADA4895-2 AT A GAIN < +10

The ADA4895-1/ADA4895-2 are minimum gain 10 stable when used in normal gain configurations. However, the ADA4895-1/ADA4895-2 can be configured to work at lower gains down to a gain of +5. Figure 50 shows how to add a simple RC circuit (R1 = 49.9 Ω and C1 = 60 pF) to allow the ADA4895-1/ADA4895-2 to operate at a gain of +5.

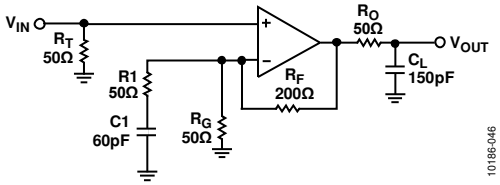


Figure 50. Configuring the ADA4895-1/ADA4895-2 for a Gain of +5 Stable

This circuit has a gain of +9 at high frequency and a gain of +5 at frequencies lower than the resonance frequency of 53 MHz (1/2πR1C1). With a noise gain of approximately +9 at high frequency, the total output noise increases unless an antialiasing filter is used to block the high frequency content.

Figure 51 shows the small and large signal frequency response of the circuit shown in Figure 50 into a 50 Ω analyzer (G = +5 V/V or 14 dB). As shown in Figure 51, the circuit is very stable, and the peaking is a little over 2 dB. This configuration is scalable to accommodate any gain from +5 to +10, as shown in Table 11.

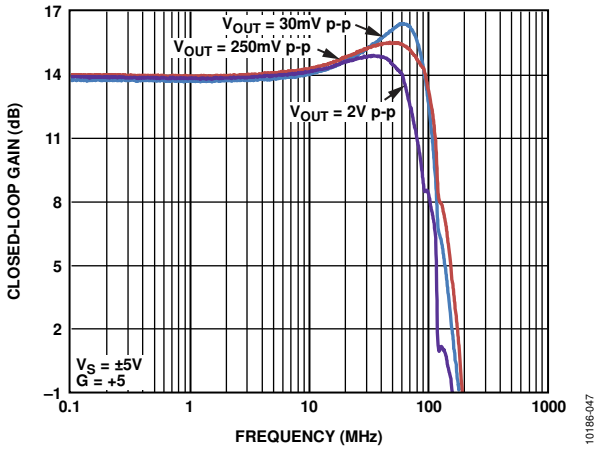


Figure 51. Frequency Response for G = +5

Table 11. Component Values Used with the ADA4895-1/ADA4895-2 for Gain < +10

Gain	R_T (Ω)	R1 (Ω)	C1 (pF)	R_G (Ω)	R_F (Ω)	R_O (Ω)	C_L (pF)
+5	49.9	49.9	60	49.9	200	49.9	150
+6	49.9	66.5	45	40.2	200	49.9	150
+7	49.9	110	27	37.4	226	49.9	150
+8	49.9	205	15	32.4	226	49.9	120
+9	49.9	Not applicable	Not applicable	30.9	249	49.9	100

HIGH GAIN BANDWIDTH APPLICATION

The circuit in Figure 52 shows cascaded dual amplifier stages using the ADA4895-1/ADA4895-2. Each stage has a gain of +10 (20 dB), making the output 100 times (40 dB) the input. The total gain bandwidth product is approximately 9 GHz with the device operating on 6 mA of quiescent current (3 mA per amplifier).

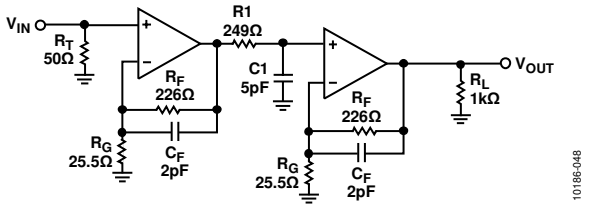


Figure 52. Cascaded Amplifier Stages for High Gain Applications (G = +100)

Figure 53 shows the large signal frequency response for two cases. The first case is with installed feedback capacitors (C_F = 2 pF), and the second case is without these capacitors. Removing the 2 pF feedback capacitors from this circuit increases the bandwidth, but adds about 0.5 dB of peaking.

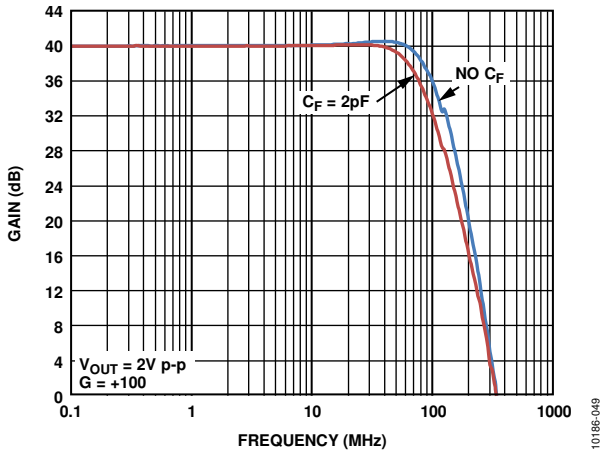


Figure 53. Large Signal Frequency Response, G = +100, V_S = ±5 V

To better balance the second stage and remove the current offset contribution, an R1C1 circuit can be sized to correct for any mis-match between the source impedance and the feedback network impedance on the input amplifier. (In the example shown in Figure 52, R1 = 249 Ω and C1 = 5 pF.) The offset of each amplifier is within the same statistical range. As configured, the offset of the output amplifier is not statistically significant to the overall offset of the system.

Figure 53 was captured using a ±5 V supply; however, this circuit also operates with supplies from ±1.5 V to ±5 V as long as the input and output headroom values are not violated.

FEEDBACK CAPACITOR APPLICATION

For applications where frequency response flatness is necessary, or a larger feedback resistor value is desired, a small feedback capacitor in parallel with the feedback resistor can be used to reduce peaking and increase flatness.

Figure 54 shows the small signal frequency response with and without a feedback capacitor.

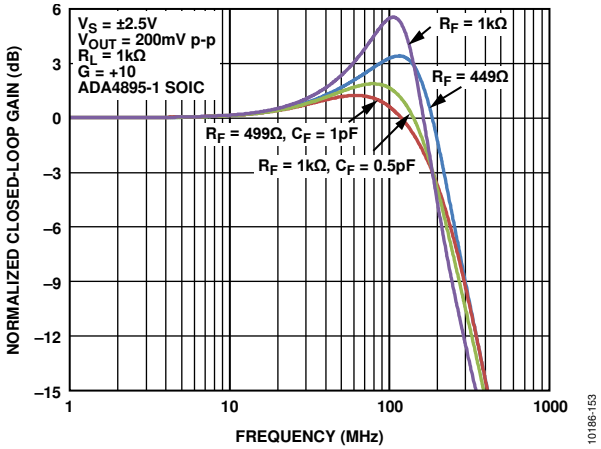


Figure 54. Small Signal Frequency Response With and Without a Feedback Capacitor

WIDEBAND PHOTOMULTIPLIER PREAMPLIFIER

A decompensated amplifier can provide significantly greater speed in transimpedance applications than a unity-gain stable amplifier. The speed increases by the square root of the ratio of the bandwidth of the two amplifiers; that is, a 1 GHz GBP amplifier is 10 times faster than a 10 MHz amplifier in the same transimpedance application if all other parameters are kept constant. Additionally, the input voltage noise normally dominates the total output rms noise because it is multiplied by the capacitive noise gain network.

$$\frac{(C_S + C_M + C_F + C_D)}{C_F}$$

In the case of the ADA4895-1/ADA4895-2, the input noise is low, but the capacitive noise gain network must be kept greater than 10 for stability reasons.

One disadvantage of using the ADA4895-1/ADA4895-2 in transimpedance applications is that the input current and input current noise can create large offsets and output voltage noise when coupled with an excessively high feedback resistance. Despite these two issues, the ADA4895-1/ADA4895-2 noise and gain bandwidth can provide a significant increase in performance within certain transimpedance ranges.

Figure 55 shows an I/V converter with an electrical model of a photomultiplier.

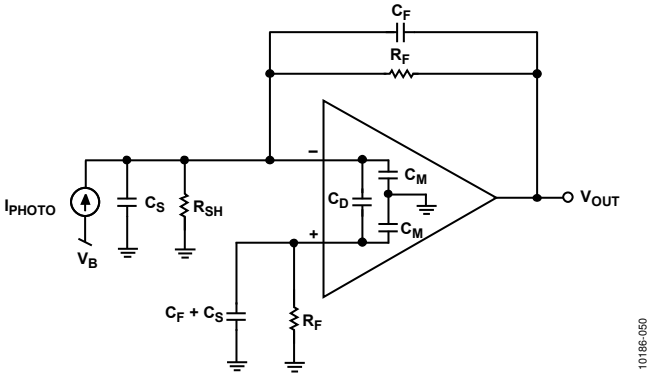


Figure 55. Wideband Photomultiplier Preamplifier

The basic transfer function is

$$V_{OUT} = \frac{I_{PHOTO} \times R_F}{1 + sC_F R_F}$$

where I_{PHOTO} is the output current of the photomultiplier, and the parallel combination of R_F and C_F sets the signal bandwidth.

The stable bandwidth attainable with this preamplifier is a function of R_F, the gain bandwidth product of the amplifier, and the total capacitance at the summing junction of the amplifier, including C_S and the amplifier input capacitance.

R_F and the total capacitance produce a pole in the loop transmission of the amplifier that can result in peaking and instability. Adding C_F creates a zero in the loop transmission that compensates for the pole effect and reduces the signal bandwidth. It can be shown that the signal bandwidth resulting in a 45° phase margin ($f_{(45)}$) is defined as follows:

$$f_{(45)} = \sqrt{\frac{GBP}{2\pi \times R_F \times C_S}}$$

where:
GBP is the gain bandwidth product.
R_F is the feedback resistance.
C_S is the total capacitance at the amplifier summing junction (amplifier + photomultiplier + board parasitics).

The value of C_F that produces $f_{(45)}$ is

$$C_F = \sqrt{\frac{C_S}{2\pi \times R_F \times GBP}}$$

The frequency response in this case shows approximately 2 dB of peaking and 15% overshoot. Doubling C_F and reducing the bandwidth by half results in a flat frequency response with approximately 5% transient overshoot.

The output noise over frequency for the preamplifier is shown in Figure 56.

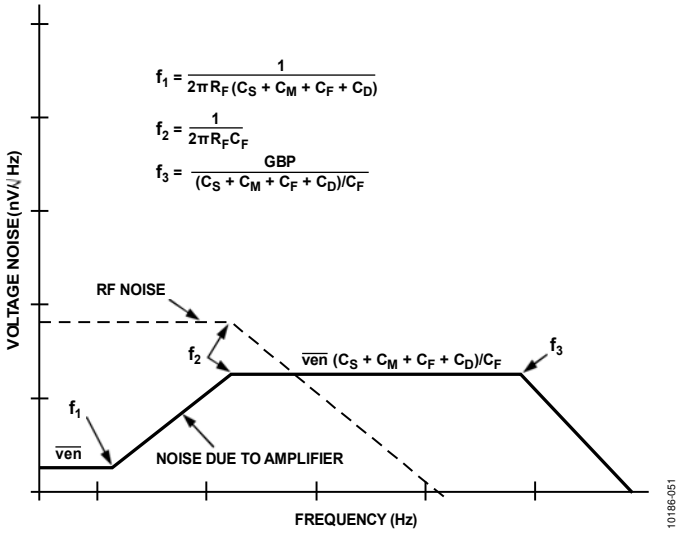


Figure 56. Photomultiplier Voltage Noise Contributions

Table 12. RMS Noise Contributions of Photomultiplier Preamplifier

Contributor	Expression
R_F	$\sqrt{4kT \times R_F \times f_2 \times 1.57}$
Amplifier $\overline{ven}$	$\overline{ven} \times \frac{(C_S + C_M + C_F + C_D)}{C_F} \times \sqrt{f_3 \times 1.57}$
Amplifier $\overline{ien}$	$\overline{ien} \times R_F \times \sqrt{f_2 \times 1.57}$

LAYOUT CONSIDERATIONS

To ensure optimal performance, careful and deliberate attention must be paid to the board layout, signal routing, power supply bypassing, and grounding.

Ground Plane

It is important to avoid ground in the areas under and around the input and output of the ADA4895-1/ADA4895-2. Stray capacitance created between the ground plane and the input and output pads of a device is detrimental to high speed amplifier performance. Stray capacitance at the inverting input, along with the amplifier input capacitance, lowers the phase margin and can cause instability. Stray capacitance at the output creates a pole in the feedback loop, which can reduce phase margin and can cause the circuit to become unstable.

Power Supply Bypassing

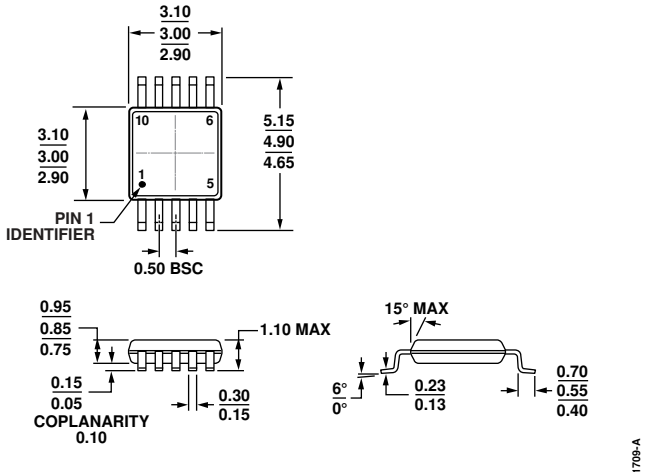
Power supply bypassing is a critical aspect in the performance of the ADA4895-1/ADA4895-2. A parallel connection of capacitors from each power supply pin to ground works best. Smaller value capacitor electrolytics offer better high frequency response, whereas larger value capacitor electrolytics offer better low frequency performance.

Paralleling different values and sizes of capacitors helps to ensure that the power supply pins are provided with low ac impedance across a wide band of frequencies. This is important for minimizing the coupling of noise into the amplifier—especially when the amplifier PSRR begins to roll off—because the bypass capacitors can help lessen the degradation in PSRR performance.

Place the smallest value capacitor on the same side of the board as the amplifier and as close as possible to the amplifier power supply pins. Connect the ground end of the capacitor directly to the ground plane.

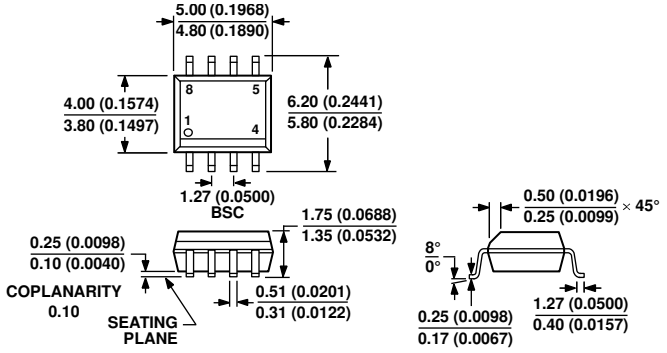
It is recommended that a 0.1 µF ceramic capacitor with a 0508 case size be used. The 0508 case size offers low series inductance and excellent high frequency performance. Place a 10 µF electrolytic capacitor in parallel with the 0.1 µF capacitor. Depending on the circuit parameters, some enhancement to performance can be realized by adding additional capacitors. Each circuit is different and should be analyzed individually for optimal performance.

OUTLINE DIMENSIONS



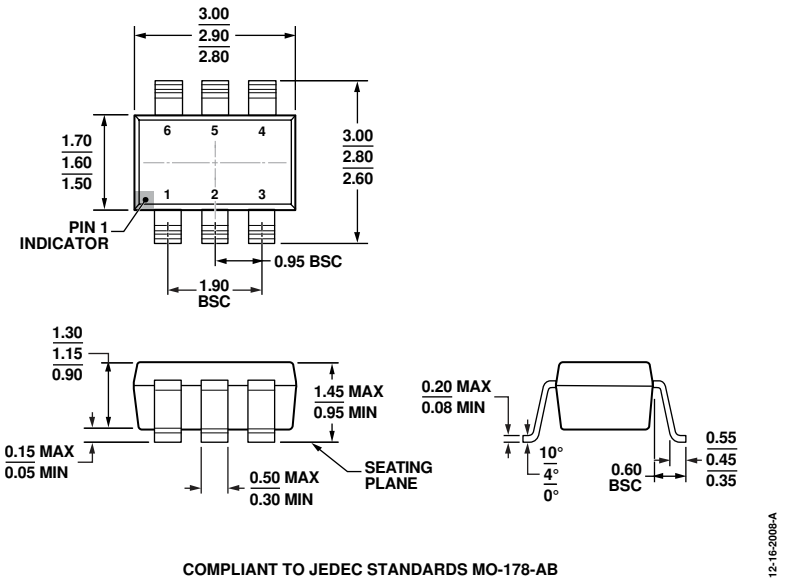
COMPLIANT TO JEDEC STANDARDS MO-187-BA

Figure 57. 10-Lead Mini Small Outline Package [MSOP]
(RM-10)
Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MS-012-AA
CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

Figure 58. 8-Lead Standard Small Outline Package [SOIC_N]
Narrow Body
(R-8)
Dimensions shown in millimeters and (inches)



COMPLIANT TO JEDEC STANDARDS MO-178-AB

Figure 59. 6-Lead Small Outline Transistor Package [SOT-23]
(RJ-6)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option	Ordering Quantity	Branding
ADA4895-1ARZ	−40°C to +125°C	8-Lead SOIC_N	R-8	98	
ADA4895-1ARZ-R7	−40°C to +125°C	8-Lead SOIC_N	R-8	1,000	
ADA4895-1ARZ-RL	−40°C to +125°C	8-Lead SOIC_N	R-8	2,500	
ADA4895-1ARJZ-R2	−40°C to +125°C	6-Lead SOT-23	RJ-6	250	H3D
ADA4895-1ARJZ-R7	−40°C to +125°C	6-Lead SOT-23	RJ-6	3,000	H3D
ADA4895-1AR-EBZ		Evaluation Board for the 8-Lead SOIC_N			
ADA4895-1ARJ-EBZ		Evaluation Board for the 6-Lead SOT-23			
ADA4895-2ARMZ	−40°C to +125°C	10-Lead Mini Small Outline Package [MSOP]	RM-10	50	H35
ADA4895-2ARMZ-R7	−40°C to +125°C	10-Lead Mini Small Outline Package [MSOP]	RM-10	1,000	H35
ADA4895-2ARMZ-RL	−40°C to +125°C	10-Lead Mini Small Outline Package [MSOP]	RM-10	3,000	H35
ADA4895-2ARM-EBZ		Evaluation Board			

[1] Z = RoHS Compliant Part.