14V, Low Noise, Low Power, Rail-to-Rail Input/Output, Operational Amplifier

FEATURES (V^+=5V, V^-=0V, Ta=25°C)

- ●Supply Voltage 1.8V to 14V
- ●Low Noise 10nV/√Hz at 1kHz
- ●Low Supply Current (All Amplifiers)
  - NJM8530 320µA typ.
  - NJM8532 580µA typ.
  - NJM8534 1200µA typ.
- ●Rail-to-Rail Input and Output
- ●GBW 1MHz
- ●Slew Rate 0.4V/µs
- ●Capacitive Load Drive 1000pF
- ●Unity Gain Stable
- ●Package
  - NJM8530 SOT-23-5
  - NJM8532 DMP8, SSOP8, MSOP8 (TVSP8)
  - NJM8534 SSOP14

APPLICATIONS

- ●Battery-powered instruments
  Audio, Sensor applications, Medical, Security
- ●High-side/Low-side Current sensing amplifiers
- ●Active Filters
- ●Analog-to-digital / Digital-to-analog Buffers
- ●Handheld Test Equipment

DESCRIPTION

The NJM8530/NJM8532/NJM8534 are single/dual/quad rail to rail input and output single supply operational amplifier featuring 14V supply voltage, low noise and low power.

A wide supply voltage range from 1.8V to 14V with a rail to rail input and output allows the device to be used in wide variety of applications, such as audio amplifier, hi-side current sensing, buffering and others. Furthermore, low supply current of 580µA typical at NJM8532 combined with a wide bandwidth of 1MHz and low very low noise of 10nV/√Hz at 1kHz make NJM8530/NJM8532/NJM8534 very suitable for a variety of battery-powered applications that require a good balance between low power, low noise and wide bandwidth.

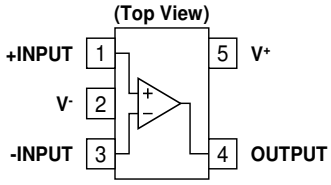
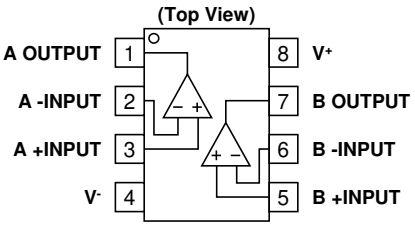
NJM8530/NJM8532/NJM8534 can drive up to approximately 1000pF, and is unity-gain stable. Operating temperature range is -40°C to 125°C.

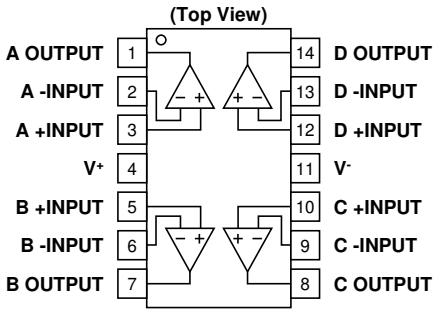
The NJM8530(single) is available in 5-pin SOT-23 package. NJM8532(dual) is available in 8-pin DMP, SSOP and MSOP(TVSP): meet JEDEC MO-187-DA / thin type package. NJM8534(quad) is available in 14-pin SSOP package.

Rail-to-Rail Input/Output Op-Amp (Bipolar)

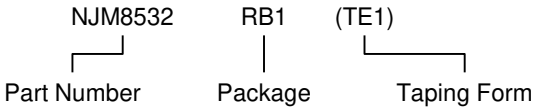
Supply Voltage	6V	14V
Single	NJM2730	NJM8530
Dual	NJM2732	NJM8532
Quad	NJM2734	NJM8534

■ PIN CONFIGURATIONS

PRODUCT NAME	NJM8530F	NJM8532M	NJM8532V	NJM8532RB1
Package	SOT-23-5	DMP8	SSOP8	MSOP8(TVSP8)
Pin Functions				

PRODUCT NAME	NJM8534V	
Package	SSOP14	
Pin Functions		

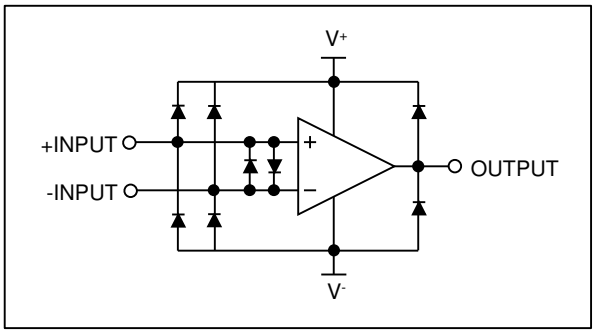
■ PRODUCT NAME INFORMATION



■ ORDERING INFORMATION

PRODUCT NAME	PACKAGE	RoHS	HALOGEN-FREE	TERMINAL FINISH	MARKING	WEIGHT (mg)	MOQ (pcs)
NJM8530F	SOT-23-5	○	-	Sn2Bi	A6L	15	3000
NJM8532M	DMP8	○	-	Sn2Bi	8532	95	2000
NJM8532V	SSOP8	○	-	Sn2Bi	8532	42	2000
NJM8532RB1	MSOP8 (TVSP8)	○	-	Sn2Bi	8532	18	2000
NJM8534V	SSOP14	○	○	Sn2Bi	8534	65	2000

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS

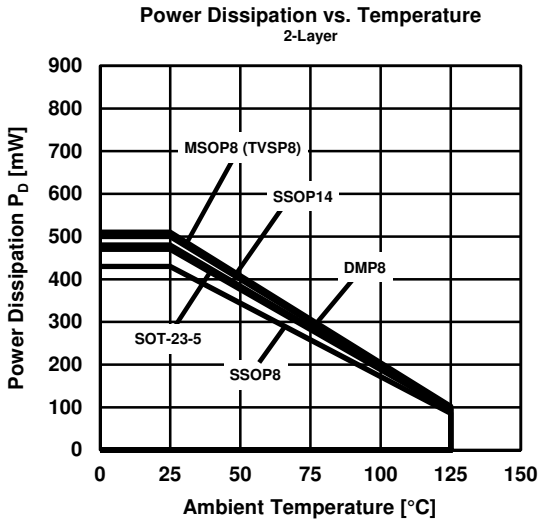
PARAMETER	SYMBOL	RATING	UNIT
Supply Voltage	$V^+ - V^-$	15	V
Input Voltage	V_{IN}	V^--0.3 to V^++0.3 (2)	V
Differential Input Voltage	V_{ID}	±1.0 (1)(2)	V
Input Current	I_{IN}	2 (2)	mA
Power Dissipation (Ta=25°C)	P_D	2-Layer / 4-Layer (3)	mW
SOT-23-5		480 / 650	
DMP8		470 / 600	
SSOP8		430 / 540	
TVSP8		510 / 680	
SSOP14		500 / 620	
Storage Temperature Range	T_{stg}	-40 to 150	°C
Maximum Junction Temperature	T_{jmax}	150	°C

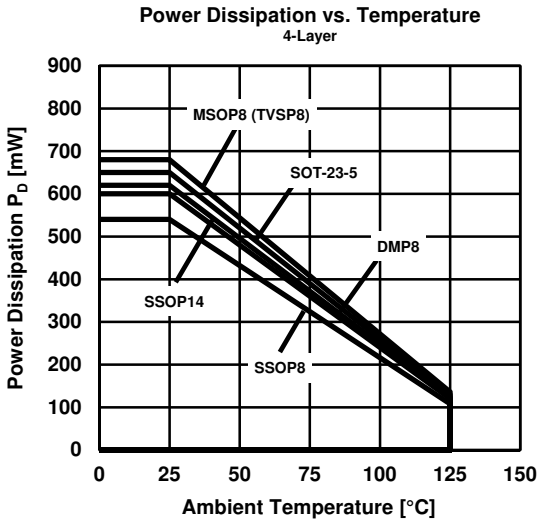
■ THERMAL CHARACTERISTICS

PACKAGE	SYMBOL	VALUE	UNIT
Junction-to-Ambient Thermal Resistance	Θja	2-Layer / 4-Layer (3)	°C/W
SOT-23-5		260 / 192	
DMP8		266 / 208	
SSOP8		291 / 231	
TVSP8		245 / 184	
SSOP14		250 / 202	
Junction-to-Top of Package Characterization Parameter	Ψjt	2-Layer / 4-Layer (3)	°C/W
SOT-23-5		67 / 58	
DMP8		72 / 65	
SSOP8		46 / 45	
TVSP8		51 / 45	
SSOP14		53 / 52	

(1) Differential voltage is the voltage difference between +INPUT and -INPUT.
(2) The inputs are protected by diodes. If the differential input voltage exceeds 1.0V, the input current must be limited 2 mA or less by using a restriction resistance.
(3) 2-Layer: Mounted on glass epoxy board. (76.2×114.3×1.6mm: based on EIA/JDEC standard, 2-Layer FR-4)
4-Layer: Mounted on glass epoxy board. (76.2×114.3×1.6mm: based on EIA/JDEC standard, 4-Layer FR-4), internal Cu area: 74.2×74.2mm

■ POWER DISSIPATION vs. AMBIENT TEMPERATURE





■ RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	CONDITIONS	VALUE	UNIT
Supply Voltage	$V^+ - V^-$		1.8 to 14	V
Operating Temperature Range	T_{opr}		-40 to 125	°C

■ **ELECTRICAL CHARACTERISTICS** (V^+=5V, V^-=0V, V_{COM}=2.5V, Ta=25°C, unless otherwise noted.)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT CHARACTERISTICS						
Input Offset Voltage	V_{IO}		-	1	4	mV
Input Offset Voltage Drift	$\Delta V_{IO}/\Delta T$	Ta=-40°C to 125°C	-	1.5	-	µV/°C
Input Bias Current	I_B		-	50	250	nA
Input Offset Current	I_{IO}		-	5	100	nA
Open-Loop Voltage Gain	A_V	R_L=2kΩ to 2.5V	60	85	-	dB
Common-Mode Rejection Ratio	CMR	(5)	55	70	-	dB
Common-Mode Input Voltage Range	V_{ICM}	CMR≥55dB	0	-	5	V
OUTPUT CHARACTERISTICS						
High-level Output Voltage	V_{OH}	R_L=20kΩ to 2.5V	4.9	4.95	-	V
		R_L=2kΩ to 2.5V	4.75	4.85	-	V
Low-level Output Voltage	V_{OL}	R_L=20kΩ to 2.5V	-	0.05	0.1	V
		R_L=2kΩ to 2.5V	-	0.15	0.25	V
Output Short-Circuit Current	I_{SC}	Sourcing, Short to 2.5V	-	20	-	mA
		Sinking, Short to 2.5V	-	5	-	mA
POWER SUPPLY						
Supply Current (All Amplifiers)	I_{SUPPLY}	No Signal				
NJM8530			-	320	550	µA
NJM8532			-	580	900	µA
NJM8534			-	1200	1800	µA
Supply Voltage Rejection Ratio	SVR	V^+=4V to 6V	70	85	-	dB
AC CHARACTERISTICS						
Slew Rate	SR	R_L=2kΩ to 2.5V	-	0.4	-	V/µs
Gain Bandwidth Product	GBW	R_L=2kΩ to 2.5V	-	1	-	MHz
Phase Margin	Φ_M	R_L=2kΩ to 2.5V	-	75	-	Deg
Equivalent Input Noise Voltage	e_n	f=1kHz	-	10	-	nV/√Hz
Channel Separation NJM8532/NJM8534	CS	f=1kHz	-	-133	-	dB

(5) CMR specified is the lower of the CMR+ and CMR-.
CMR+ measured with $V^+/2 \le V_{CM} \le V^+$, and CMR- measured with $V^- \le V_{CM} \le V^+/2$.

■ **ELECTRICAL CHARACTERISTICS** (V^+=3V, V^-=0V, V_{COM}=1.5V, Ta=25°C, unless otherwise noted.)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT CHARACTERISTICS						
Input Offset Voltage	V_{IO}		-	1	4	mV
Input Offset Voltage Drift	$\Delta V_{IO}/\Delta T$	Ta=-40°C to 125°C	-	1.8	-	µV/°C
Input Bias Current	I_B		-	50	250	nA
Input Offset Current	I_{IO}		-	5	100	nA
Open-Loop Voltage Gain	A_V	R_L=2kΩ to 1.5V	60	84	-	dB
Common-Mode Rejection Ratio	CMR	(5)	48	63	-	dB
Common-Mode Input Voltage Range	V_{ICM}	CMR≥48dB	0	-	3	V
OUTPUT CHARACTERISTICS						
High-level Output Voltage	V_{OH}	R_L=20kΩ to 1.5V	2.9	2.95	-	V
		R_L=2kΩ to 1.5V	2.75	2.85	-	V
Low-level Output Voltage	V_{OL}	R_L=20kΩ to 1.5V	-	0.05	0.1	V
		R_L=2kΩ to 1.5V	-	0.15	0.25	V
Output Short-Circuit Current	I_{SC}	Sourcing, Short to 1.5V	-	18	-	mA
		Sinking, Short to 1.5V	-	4.8	-	mA
POWER SUPPLY						
Supply Current (All Amplifiers)	I_{SUPPLY}	No Signal				
NJM8530				270	460	µA
NJM8532			-	510	880	µA
NJM8534			-	1000	1800	µA
Supply Voltage Rejection Ratio	SVR	V^+=2.4V to 4V	68	83	-	dB
AC CHARACTERISTICS						
Slew Rate	SR	R_L=2kΩ to 1.5V	-	0.35	-	V/µs
Gain Bandwidth Product	GBW	R_L=2kΩ to 1.5V	-	1	-	MHz
Phase Margin	Φ_M	R_L=2kΩ to 1.5V	-	75	-	Deg
Equivalent Input Noise Voltage	e_n	f=1kHz	-	10	-	nV/√Hz
Channel Separation NJM8532/NJM8534	CS	f=1kHz	-	-130	-	dB

(5) CMR specified is the lower of the CMR+ and CMR-.
CMR+ measured with $V^+/2 \le V_{CM} \le V^+$, and CMR- measured with $V^- \le V_{CM} \le V^+/2$.

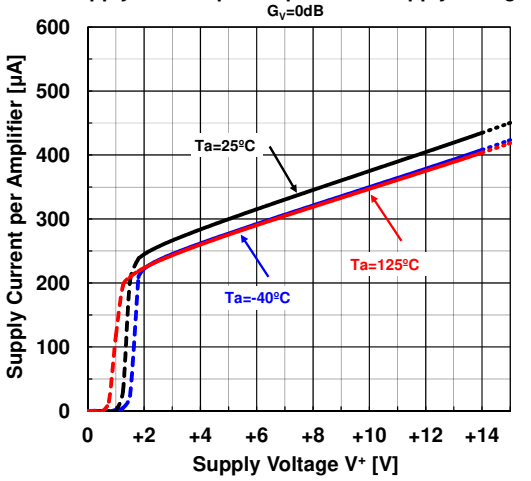
■ **ELECTRICAL CHARACTERISTICS** (V^+=1.8V, V^-=0V, V_{COM}=0.9V, Ta=25°C, unless otherwise noted.)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT CHARACTERISTICS						
Input Offset Voltage	V_{IO}		-	1	4	mV
Input Offset Voltage Drift	$\Delta V_{IO}/\Delta T$	Ta=-40°C to 125°C	-	2.4	-	µV/°C
Input Bias Current	I_B		-	50	250	nA
Input Offset Current	I_{IO}		-	5	100	nA
Open-Loop Voltage Gain	A_V	R_L=2kΩ to 0.9V	60	83	-	dB
Common-Mode Rejection Ratio	CMR	(5)	40	55	-	dB
Common-Mode Input Voltage Range	V_{ICM}	CMR≥40dB	0	-	1.8	V
OUTPUT CHARACTERISTICS						
High-level Output Voltage	V_{OH}	R_L=20kΩ to 0.9V	1.7	1.75	-	V
		R_L=2kΩ to 0.9V	1.55	1.65	-	V
Low-level Output Voltage	V_{OL}	R_L=20kΩ to 0.9V	-	0.05	0.1	V
		R_L=2kΩ to 0.9V	-	0.15	0.25	V
Output Short-Circuit Current	I_{SC}	Sourcing, Short to 0.9V	-	18	-	mA
		Sinking, Short to 0.9V	-	4.7	-	mA
POWER SUPPLY						
Supply Current (All Amplifiers)	I_{SUPPLY}	No Signal				
NJM8530				240	430	µA
NJM8532			-	460	800	µA
NJM8534			-	900	1600	µA
Supply Voltage Rejection Ratio	SVR	V^+=1.8V to 2.4V	65	80	-	dB
AC CHARACTERISTICS						
Slew Rate	SR	R_L=2kΩ to 0.9V	-	0.3	-	V/µs
Gain Bandwidth Product	GBW	R_L=2kΩ to 0.9V	-	1	-	MHz
Phase Margin	Φ_M	R_L=2kΩ to 0.9V	-	75	-	Deg
Equivalent Input Noise Voltage	e_n	f=1kHz	-	10	-	nV/√Hz
Channel Separation NJM8532/NJM8534	CS	f=1kHz	-	-125	-	dB

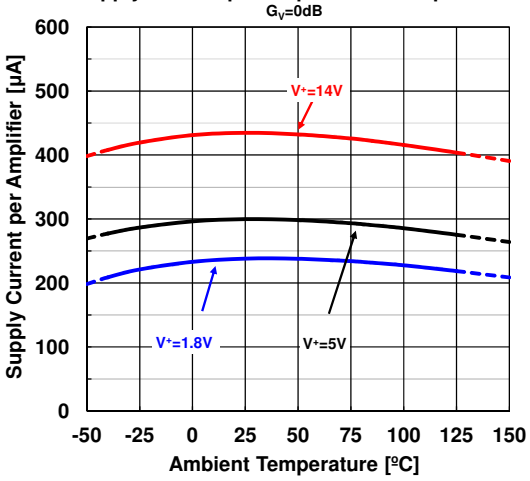
(5) CMR specified is the lower of the CMR+ and CMR-.
CMR+ measured with $V^+/2 \le V_{CM} \le V^+$, and CMR- measured with $V^- \le V_{CM} \le V^+/2$.

■ **TYPICAL CHARACTERISTICS** (V⁻=0V, Ta=25°C, unless otherwise noted.)

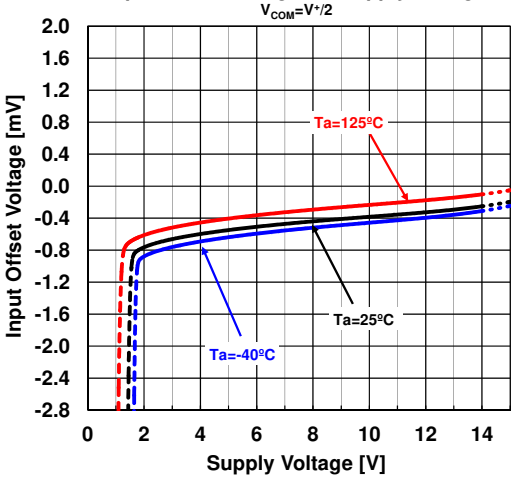
Supply Current per Amplifier vs. Supply Voltage



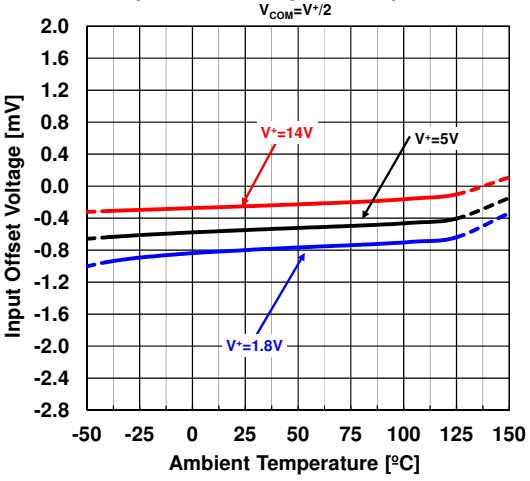
Supply Current per Amplifier vs. Temperature



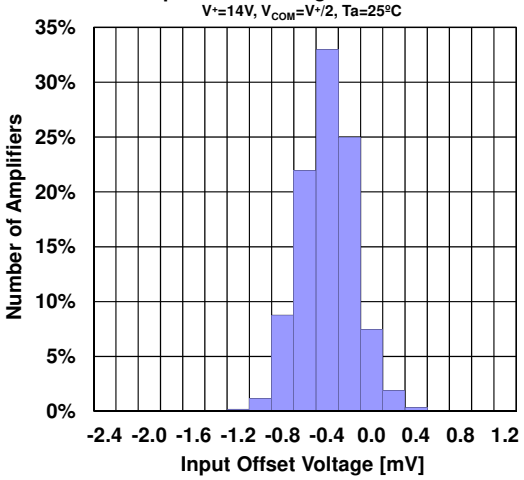
Input Offset Voltage vs. Supply Voltage



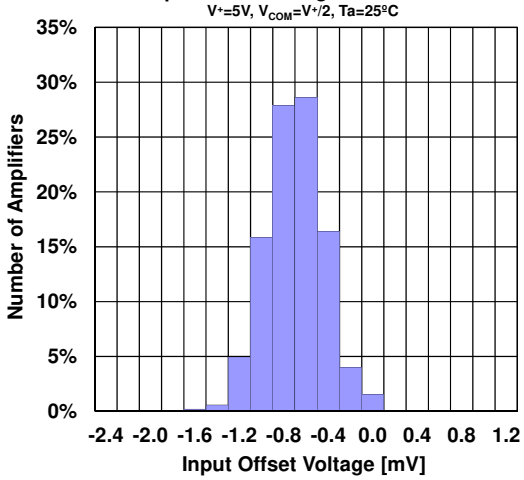
Input Offset Voltage vs. Temperature



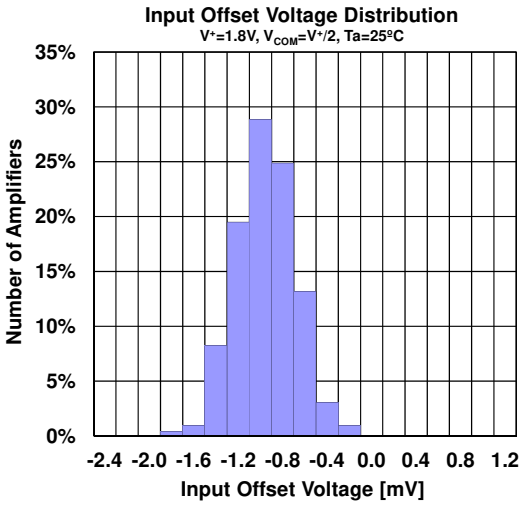
Input Offset Voltage Distribution

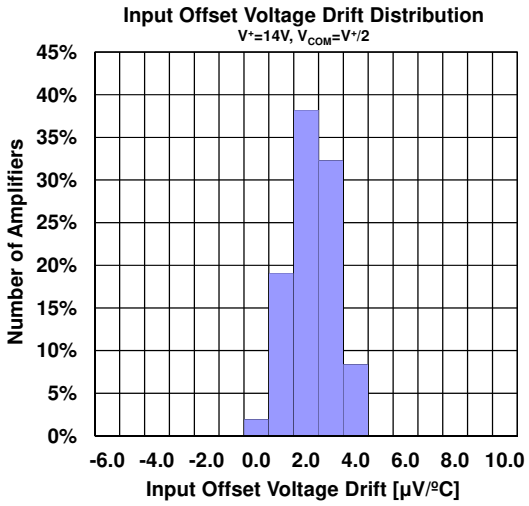


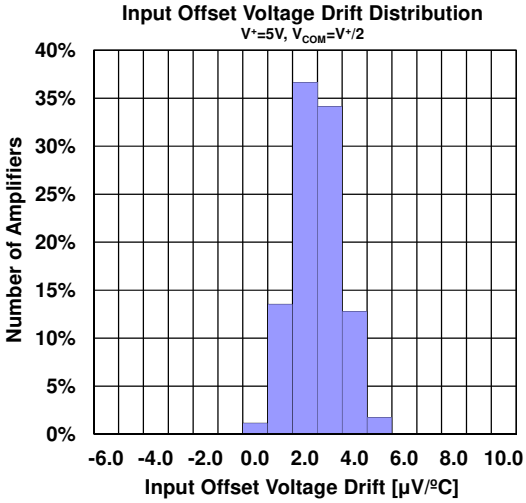
Input Offset Voltage Distribution

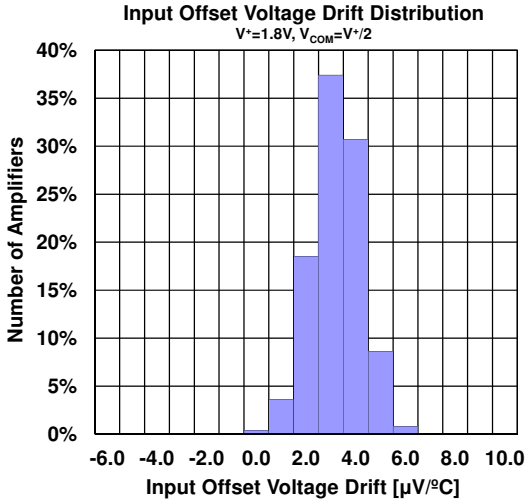


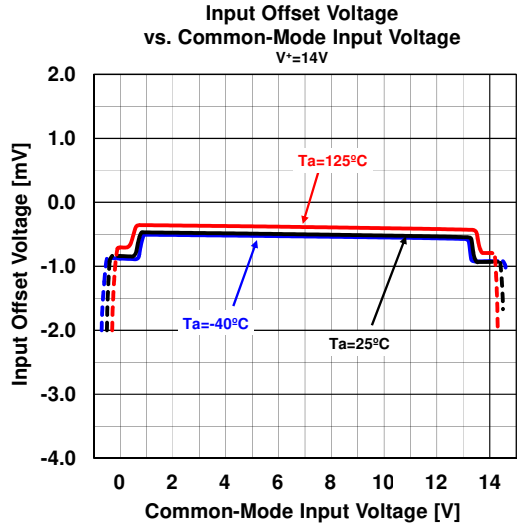
■ **TYPICAL CHARACTERISTICS** (V⁻=0V, Ta=25°C, unless otherwise noted.)

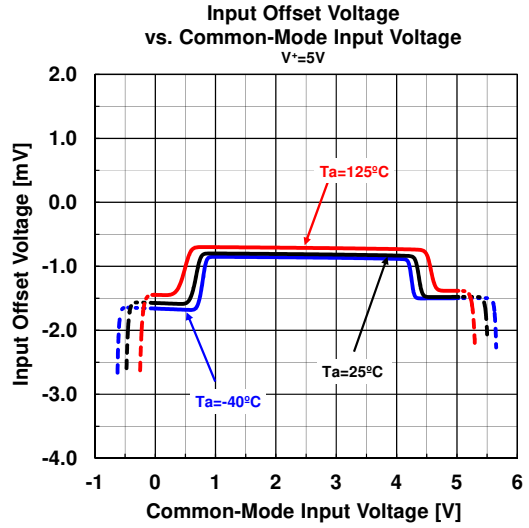






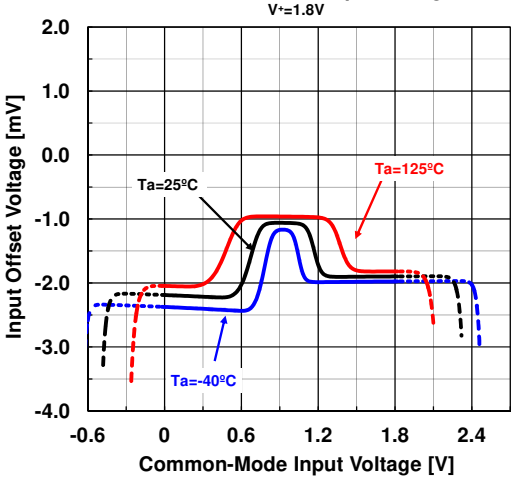




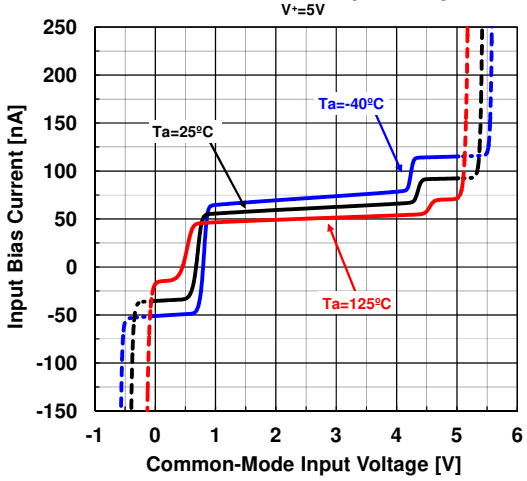


■ **TYPICAL CHARACTERISTICS** (V^-=0V, Ta=25°C, unless otherwise noted.)

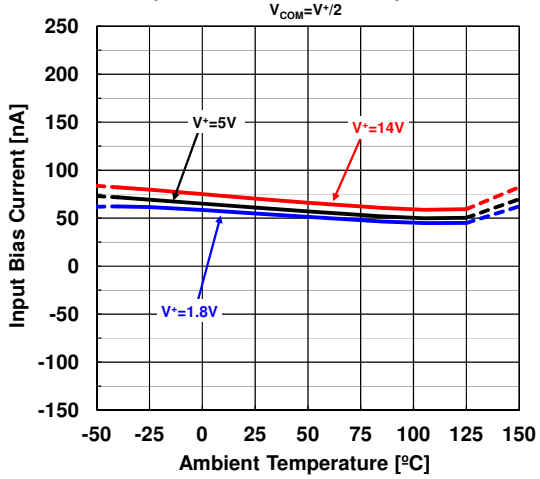
Input Offset Voltage vs. Common-Mode Input Voltage



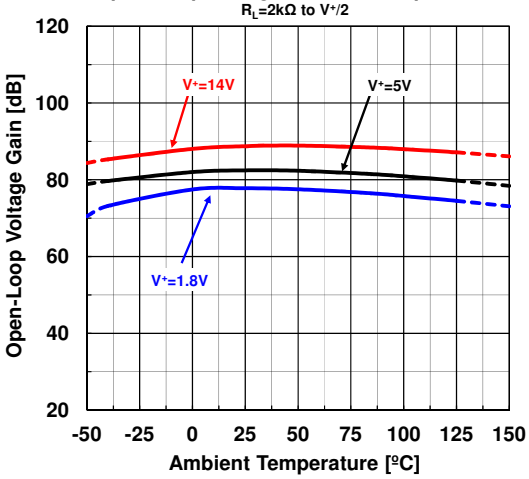
Input Bias Current vs. Common-Mode Input Voltage



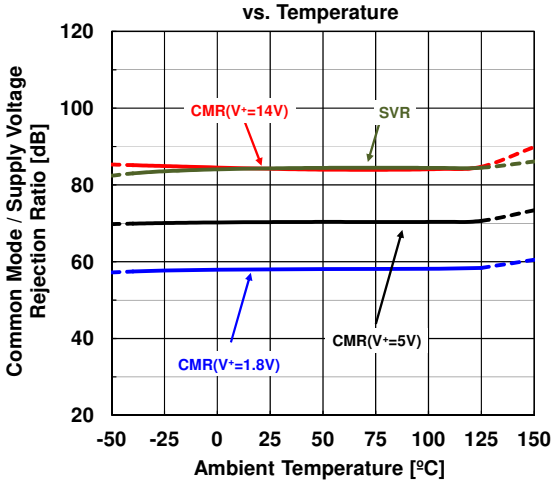
Input Bias Current vs. Temperature



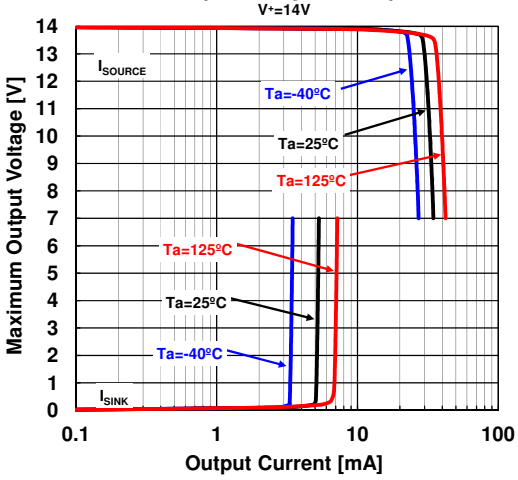
Open-Loop Voltage Gain vs. Temperature



Common Mode / Supply Voltage Rejection Ratio vs. Temperature

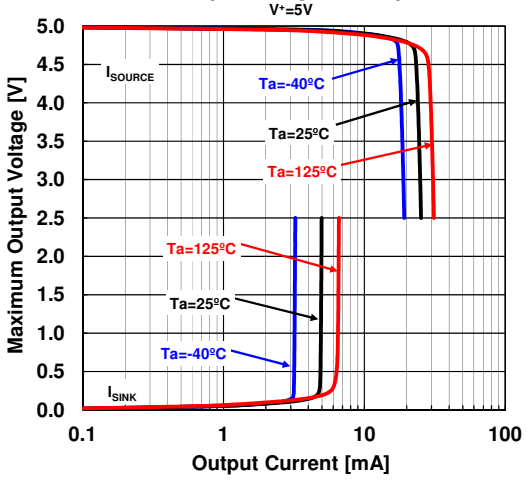


Maximum Output Voltage vs. Output Current

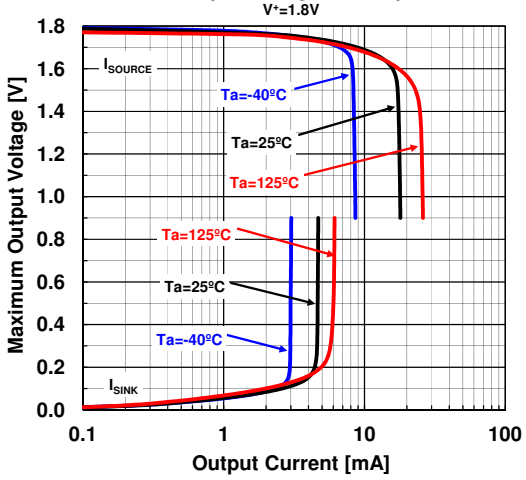


■ **TYPICAL CHARACTERISTICS** (V^-=0V, Ta=25°C, unless otherwise noted.)

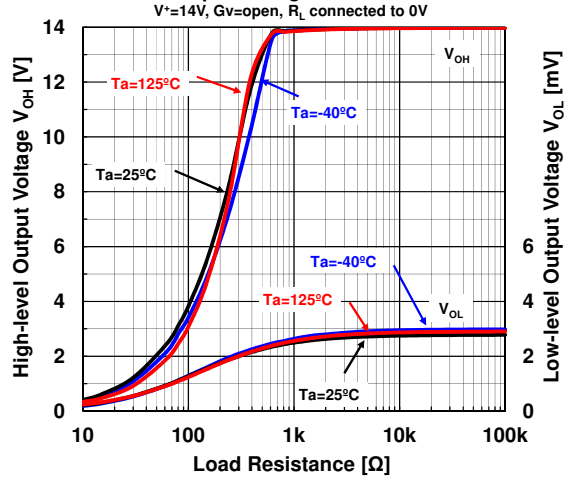
Maximum Output Voltage vs. Output Current



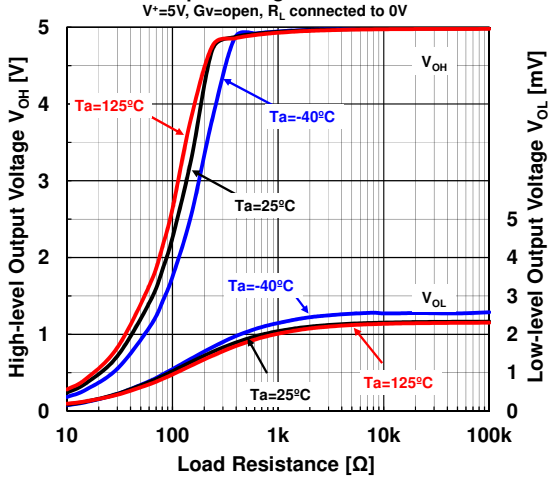
Maximum Output Voltage vs. Output Current



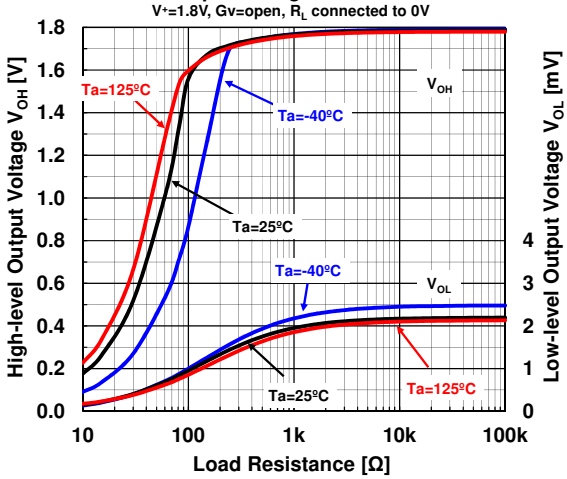
Maximum Output Voltage vs. Load Resistance



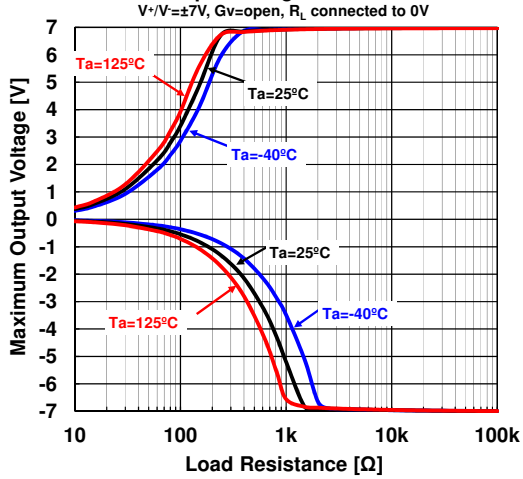
Maximum Output Voltage vs. Load Resistance



Maximum Output Voltage vs. Load Resistance

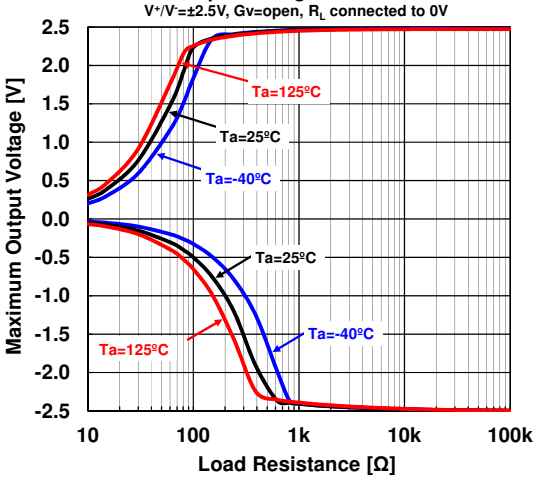


Maximum Output Voltage vs. Load Resistance

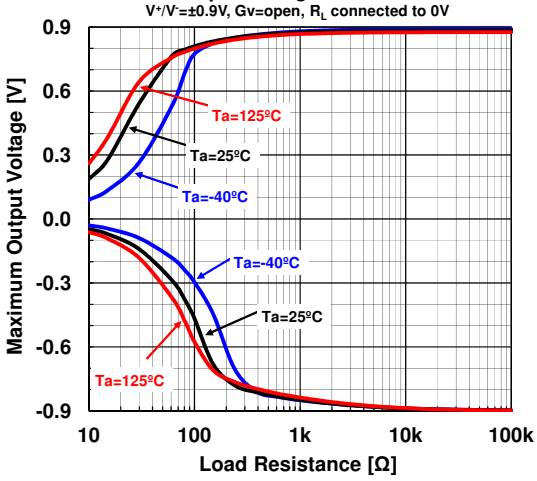


■ **TYPICAL CHARACTERISTICS** (V⁻=0V, Ta=25°C, unless otherwise noted.)

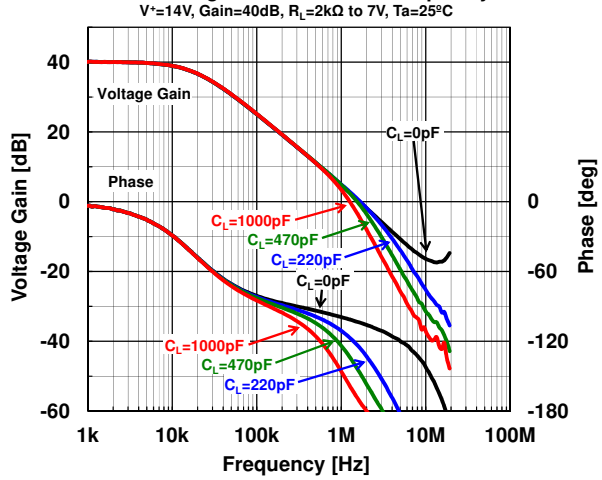
Maximum Output Voltage vs. Load Resistance
V⁺/V⁻=±2.5V, Gv=open, R_L connected to 0V



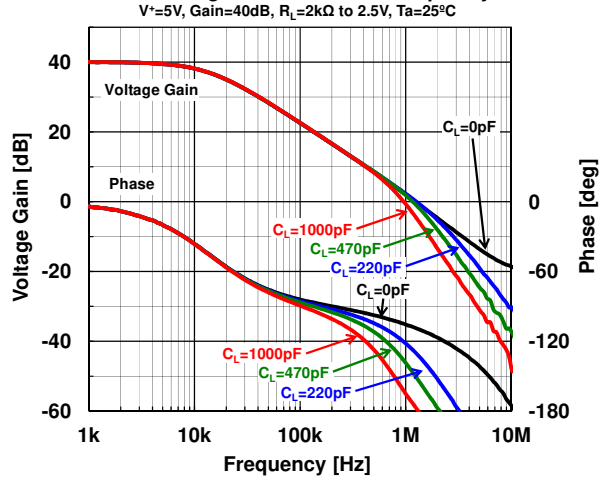
Maximum Output Voltage vs. Load Resistance
V⁺/V⁻=±0.9V, Gv=open, R_L connected to 0V



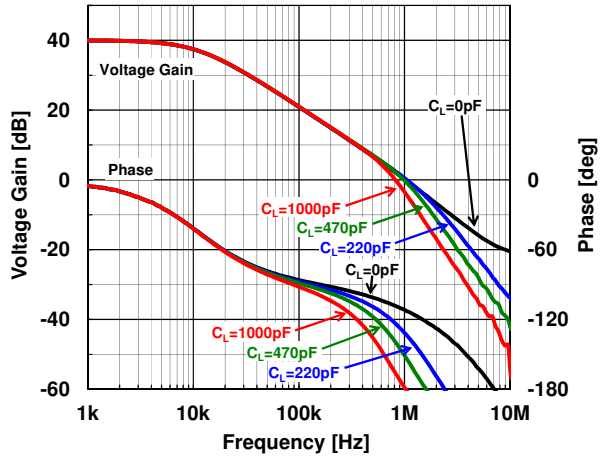
40dB Voltage Gain/Phase vs. Frequency
V⁺=14V, Gain=40dB, R_L=2kΩ to 7V, Ta=25ºC



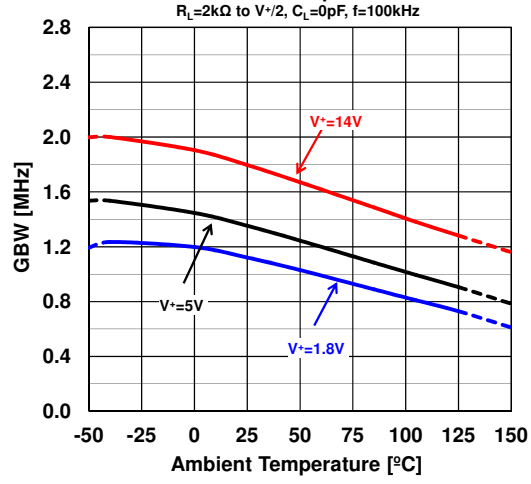
40dB Voltage Gain/Phase vs. Frequency
V⁺=5V, Gain=40dB, R_L=2kΩ to 2.5V, Ta=25ºC



40dB Voltage Gain/Phase vs. Frequency
V⁺=1.8V, Gain=40dB, R_L=2kΩ to 0.9V, Ta=25ºC

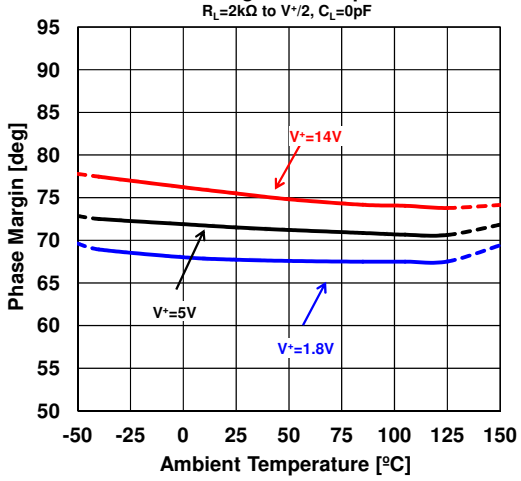


GBW vs. Temperature
R_L=2kΩ to V⁺/2, C_L=0pF, f=100kHz

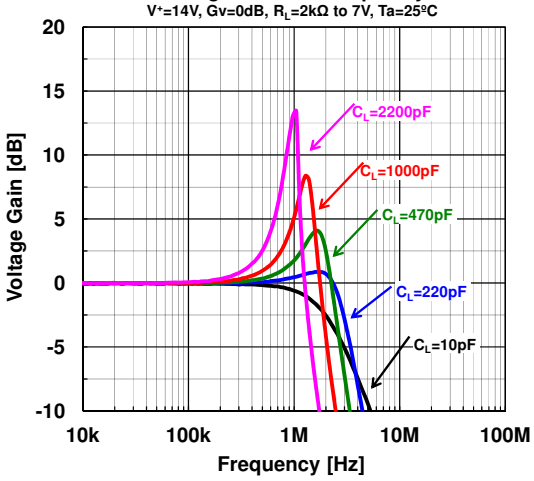


■ **TYPICAL CHARACTERISTICS** (V^-=0V, Ta=25°C, unless otherwise noted.)

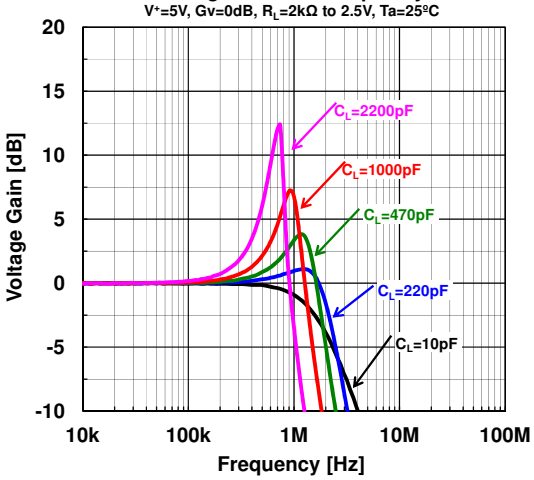
Phase Margin vs. Temperature
R_L=2kΩ to V^+/2, C_L=0pF



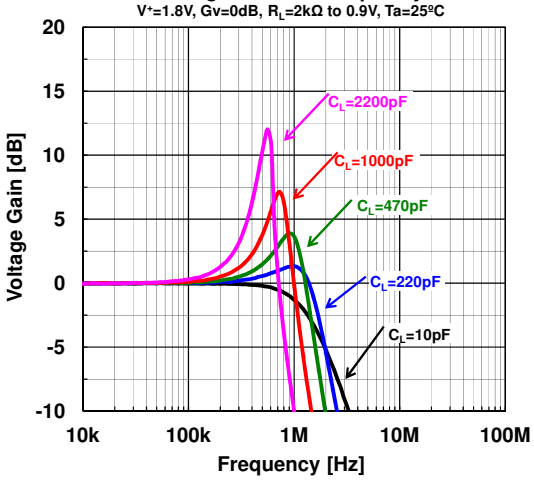
Voltage Gain vs. Frequency
V^+=14V, Gv=0dB, R_L=2kΩ to 7V, Ta=25ºC



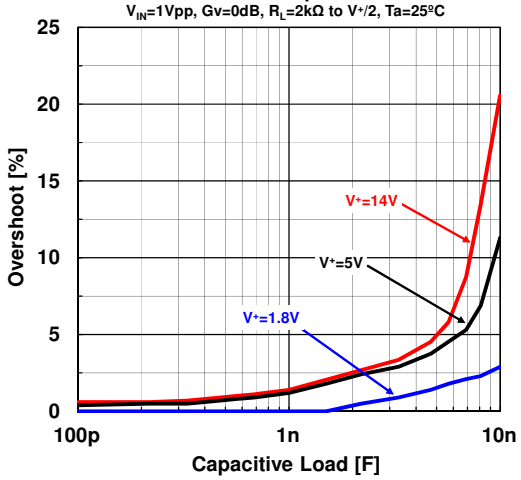
Voltage Gain vs. Frequency
V^+=5V, Gv=0dB, R_L=2kΩ to 2.5V, Ta=25ºC



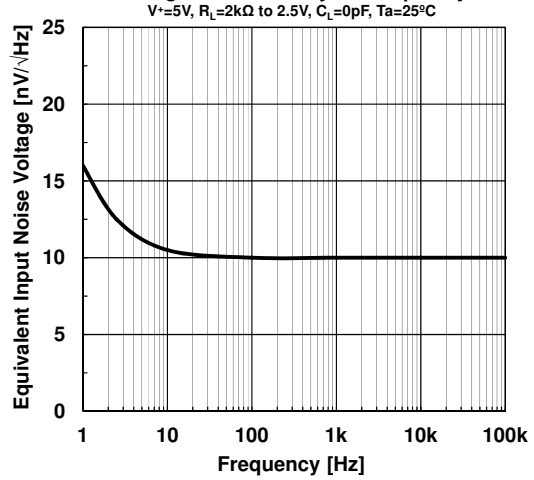
Voltage Gain vs. Frequency
V^+=1.8V, Gv=0dB, R_L=2kΩ to 0.9V, Ta=25ºC



Overshoot vs. Capacitive Load
V_{IN}=1Vpp, Gv=0dB, R_L=2kΩ to V^+/2, Ta=25ºC



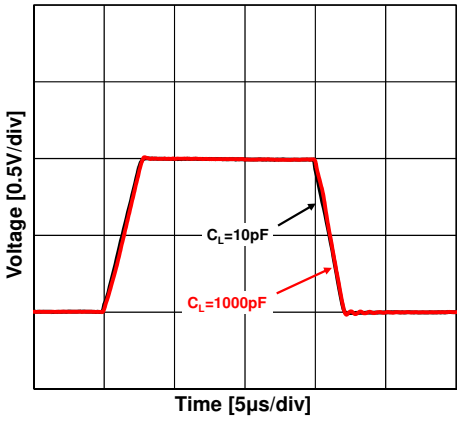
Voltage Noise Densityvs. Frequency
V^+=5V, R_L=2kΩ to 2.5V, C_L=0pF, Ta=25ºC



■ **TYPICAL CHARACTERISTICS** (V^-=0V, Ta=25°C, unless otherwise noted.)

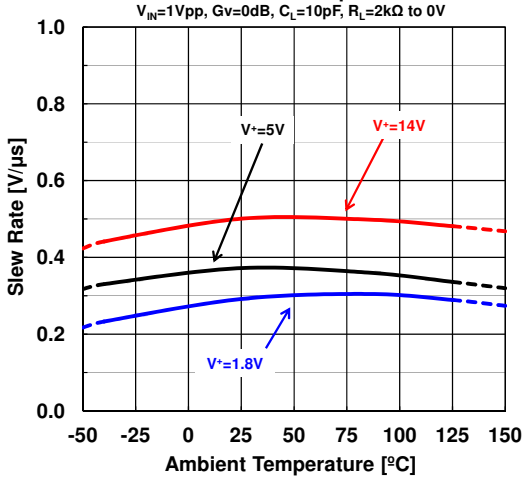
Pulse Response

V^+=5V, V_{IN}=1Vpp, Gv=0dB, R_L=2kΩ to GND, Ta=25ºC



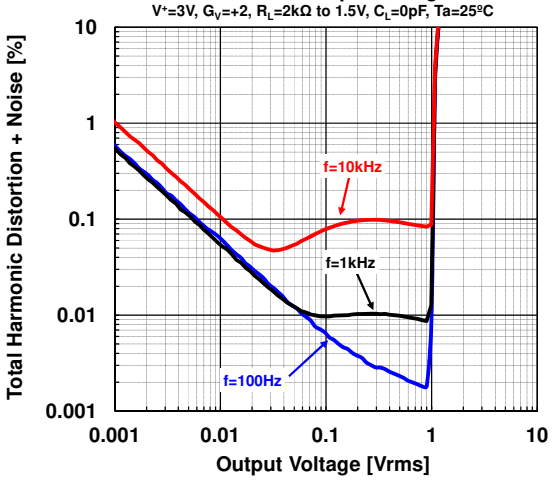
Slew Rate vs. Temperature

V_{IN}=1Vpp, Gv=0dB, C_L=10pF, R_L=2kΩ to 0V



THD+N vs. Output Voltage

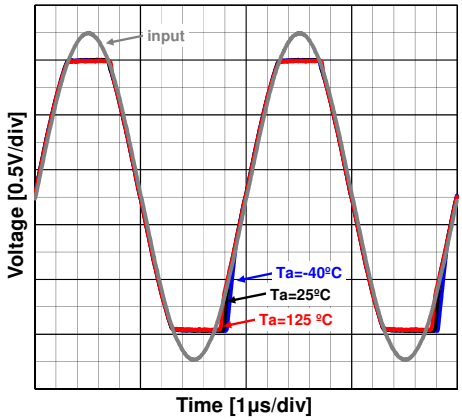
V^+=3V, G_V=+2, R_L=2kΩ to 1.5V, C_L=0pF, Ta=25ºC



No Phase Reversal

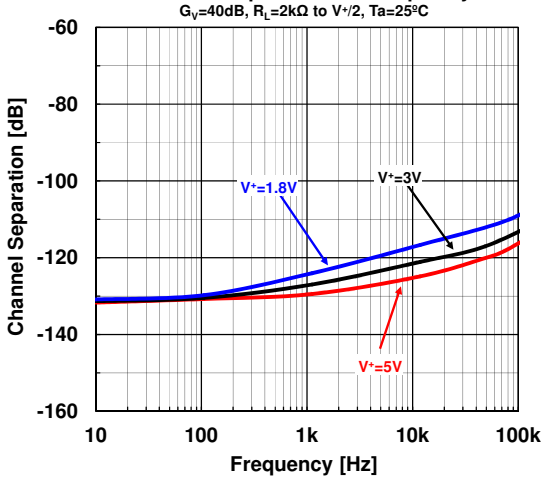
V^+=5V, f=10kHz, V_{IN}=6VP-P

Gv=0dB, R_L=2kΩ to V^+/2



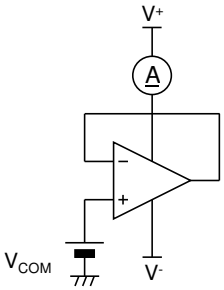
Channel Separation vs. Frequency

G_V=40dB, R_L=2kΩ to V^+/2, Ta=25ºC



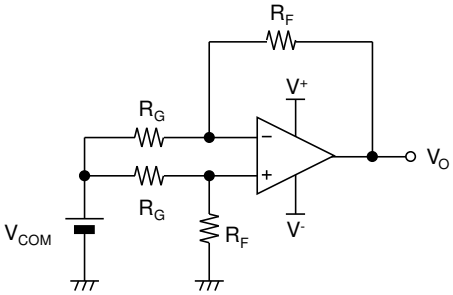
■ TEST CIRCUITS

● I_{SUPPLY}



● V_{IO}, CMR, SVR

R_G=50Ω, R_F=50kΩ



$$V_{IO}=\frac{R_G}{(R_G+R_F)}\times(V_O-V_{COM})$$

$$CMR=20\log\frac{\Delta V_{COM}\left(1+\frac{R_F}{R_G}\right)}{\Delta V_O}$$

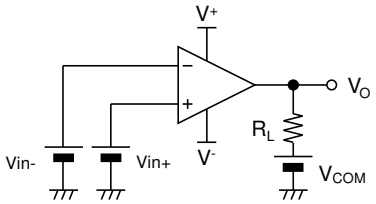
$$SVR=20\log\frac{\Delta V_S\left(1+\frac{R_F}{R_G}\right)}{\Delta V_O}$$

$V_S=V^+-V^-$

● V_{OH}, V_{OL}

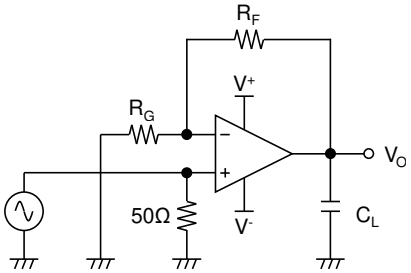
V_{OH}; Vin+ = 1V, Vin- = 0V, $V_{COM}=V^+/2$

V_{OL}; Vin+ = 0V, Vin- = 1V, $V_{COM}=V^+/2$



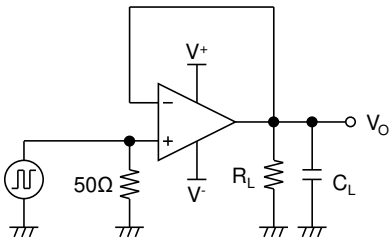
● GBW

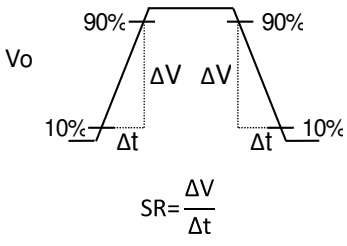
R_G=100Ω, R_F=10kΩ, C_L=0pF



● SR

R_L=2kΩ, C_L=10pF





$$SR=\frac{\Delta V}{\Delta t}$$

■ APPLICATION NOTE

Single and Dual Supply Voltage Operation

The NJM8530/NJM8532/NJM8534 works with both single supply and dual supply when the voltage supplied is between V^+ and V^-. These amplifiers operate from single 1.8 to 14V supply and dual ±0.9V to ±7V supply.

Common-Mode Input Voltage Range

When the supply voltage does not meet the condition of electrical characteristics, the range of common-mode input voltage is as follows:

V_{ICM} (typ.) = V^- to V^+ (Ta = 25°C)

Difference of V_{ICM} when Temperature change, refer to typical characteristic graph.

During designing, consider variations in characteristics for use with allowance.

Maximum Output Voltage Range

When the supply voltage does not meet the condition of electrical characteristics, the range of the typ. value of the maximum output voltage is as follows:

V_{OM} (typ.) = V^-+50mV to V^+-50mV (R_L=20kΩ, Ta=25°C)

During designing, consider variations in characteristics and temperature characteristics for use with allowance. In addition, also note that the output voltage range becomes narrow as shown in typical characteristics graph when an output current increases.

Rail-to-Rail Input

The input stage of NJM8530/NJM8532/NJM8534 has two input differential pairs, PNP-transistor and NPN-transistor (Figure1). When the common-mode input voltage is at the low end of the negative supply voltage, typically (V^-) to (V^-)+0.6V, the PNP-transistor input differential pair is active and amplifies the input signal. As the common-mode input voltage is increased above the typically (V^-)+0.6V, the NPN-transistor differential pair gradually turns on, thus both pairs are active. When the Common-Mode Input voltage continues increasing near the positive supply voltage, typically (V^+)-0.6V to positive supply voltage, the PNP-transistor differential pair gradually turns off and amplifies the input signal by NPN-transistor differential pair only. The transition occurs at approximately 0.6V away from both supply rails and results in a change in offset voltage due to the different offset voltage of the differential pairs as shown in figure2.

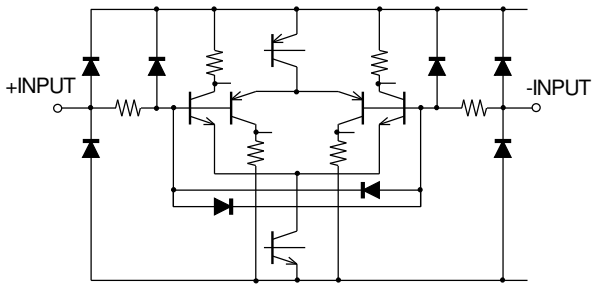


Figure1. Simplified Schematic of Input Stage

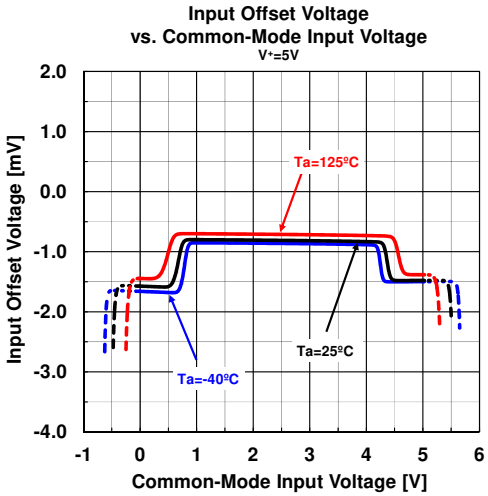


Figure2. Offset Voltage change with common-mode input voltage.

Input Voltage Exceeding the Supply Voltage

Inputs of the NJM8530/NJM8532/NJM8534 are protected by ESD diodes (shown in Figure1) that will conduct if the input voltages exceed the power supplies by more than approximately 300mV. Momentary voltages greater than 300mV beyond the power supply, inputs can be tolerated if the current is limited to 2mA. Figure3 is easily accomplished with an input resistor. If the input voltage exceeds the supply voltage, the input current must be limited 2mA or less by using a restriction resistance (R_{LIMIT}) as shown in figure3.

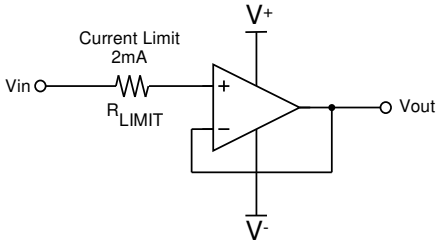


Figure3. Input Current Protection for Voltages Exceeding the Supply Voltage.

■ APPLICATION NOTE

Differential Input Voltage

The NJM8530/NJM8532/NJM8534 has internal protection circuitry that prevents damage to the input stage from large differential input voltages. This protection circuitry consists of two diodes and two resistors as shown in figure1. The diodes limit the differential voltage applied to the amplifiers' internal circuitry to no more than diodes' forward-voltage drop (V_F). Input bias current is specified typically 50nA for small differential input voltages. For large differential input voltage above the V_F, this protection circuitry increases the input current at +INPUT and -INPUT. The maximum differential input voltage is 1.0V, but if the differential input voltage exceeds 1.0V, the input current must be limited 2 mA or less by using a restriction resistance.

Capacitive load

The NJM8530/NJM8532/NJM8534 can use at unity gain follower, but the unity gain follower is the most sensitive configuration to capacitive loading. The combination of capacitive load placed directly on the output of an amplifier along with the output impedance of the amplifier creates a phase lag which in turn reduces the phase margin of the amplifier. If phase margin is significantly reduced, the response will cause overshoot and ringing in the step response.

The NJM8530/NJM8532/NJM8534 is unity gain stable for capacitive loads of 1000pF (see the overshoot vs. capacitive load graph). To drive heavier capacitive loads, an isolation resistor, R_{ISO} as shown Figure4, should be used. R_{ISO} improves the feedback loop's phase margin by making the output load resistive at higher frequencies. The larger the value of R_{ISO}, the more stable the output voltage will be. However, larger values of R_{ISO} result in reduced output swing, reduced output current drive and reduced frequency bandwidth.

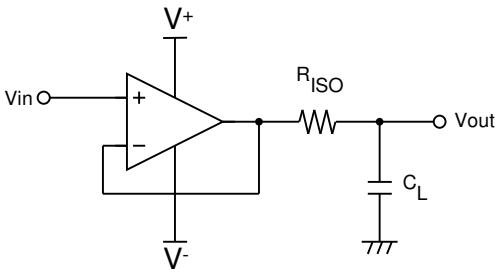
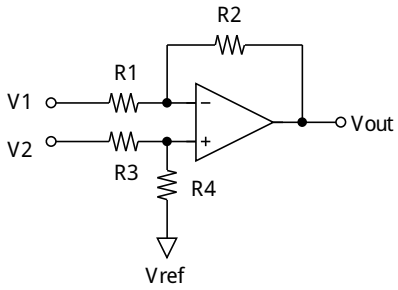


Figure4. Isolating capacitive load

Differential Amplifier

Figure5 shows a one op-amp differential amplifier that consists of the single op-amp and four external resistors. Differential amplifier amplifies the difference between its two input pins, and rejects the common- mode input voltage at both input pins. This is used in variety of applications including current sensing, differential to single-end converter, isolation amplifier to remove common-mode noise.



$$Vout = \left(\frac{R1+R2}{R3+R4}\right)\frac{R4}{R1}V2 - \frac{R2}{R1}V1 + \left(\frac{R1+R2}{R3+R4}\right)\frac{R3}{R1}Vref$$

R1=R3, R2=R4

$$Vout = \frac{R2}{R1}(V2-V1) + Vref$$

Figure5. Differential Amplifier

The differential amplifier's common-mode rejection ratio (CMR) is primarily determined by resistor mismatches, not by the op-amp's CMR. Ideally, the resistors are chosen such that R2/R1 = R4/R3. The CMR due to the resistors in differential amplifier can be calculated using the below formula:

$$CMR_{R_error} \approx 20\log\left(\frac{1+\frac{R2}{R1}}{4R_{error}}\right)$$

CMR_{R_error} = CMR due only to the resistors

R_{error} = Resistor's tolerance

Example:

R2/R1=1 and R_{error}=0.1%, then CMR=54dB

R2/R1=1 and R_{error}=1%, then CMR=34dB

If using resistors with 1% tolerance and gain=1, the CMR will only be 34dB.

■ APPLICATION NOTE

Current Sensing

Current sensing applications are one such application in a wide range of electronic applications and mostly used for feedback control systems, including power metering battery life indicators and chargers, over- current protection and supervising circuit, automotive, and medical equipment. In such applications, it is desirable to use a shunt with very low resistance to minimize the series voltage drop and minimizes wasted power, and allows the measurement of high current. The NJM8530/NJM8532/NJM8534 is ideal for these current sensing applications.

Figure6 shows a high-side current sensing circuit, and Figure7 shows a low-side current sensing circuit. The NJM8530/NJM8532/NJM8534 has rail-to-rail input and output characteristics, thus allows the both of high-side and low-side current sensing circuit. Futuremore, low supply current of 290µA/ch can save the power at battery applications.

The NJM8530/NJM8532/NJM8534 operates up to 14V, and rail-to-rail feature allows the output voltage close to 14V (almost reach the power supply of op-amp). For example, if using a typical shunt resistor of 0.1Ω, allows the current sensing up to approximately 1.4A of current. The differential amplifier's common-mode rejection ratio (CMR) is primarily determined by resistor mismatches. For details, refer to Differential Amplifiers in the Applications Information.

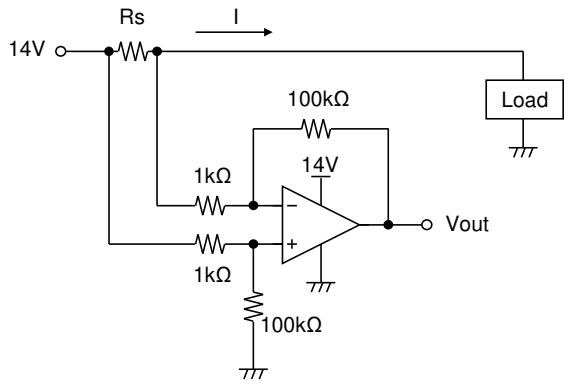


Figure6. High-Side Current Sensing

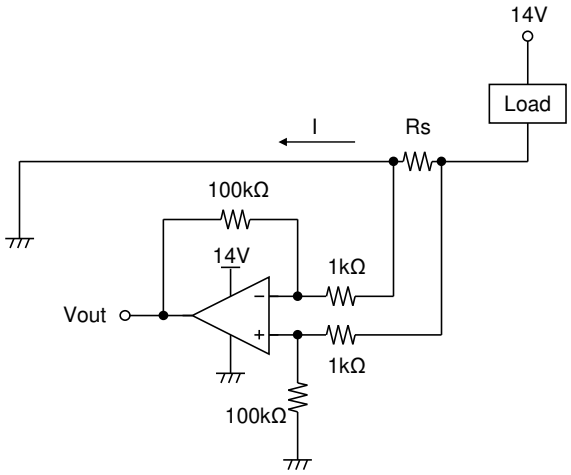
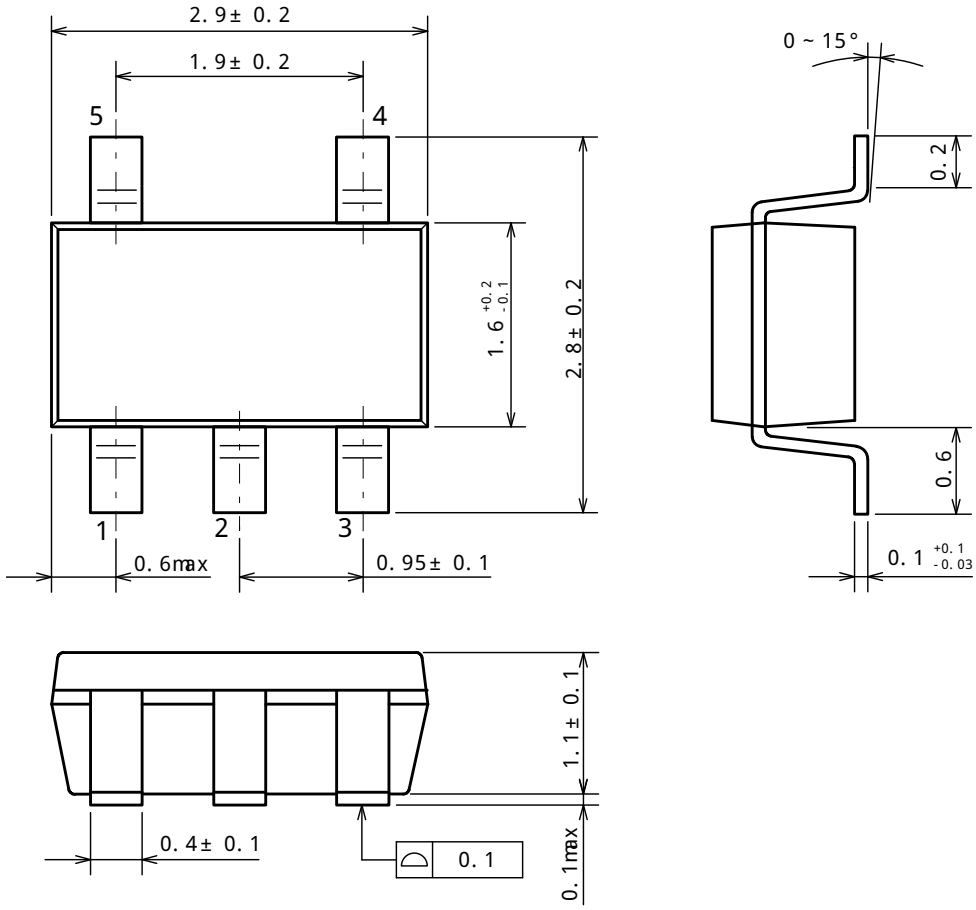


Figure7. Low-Side Current Sensing

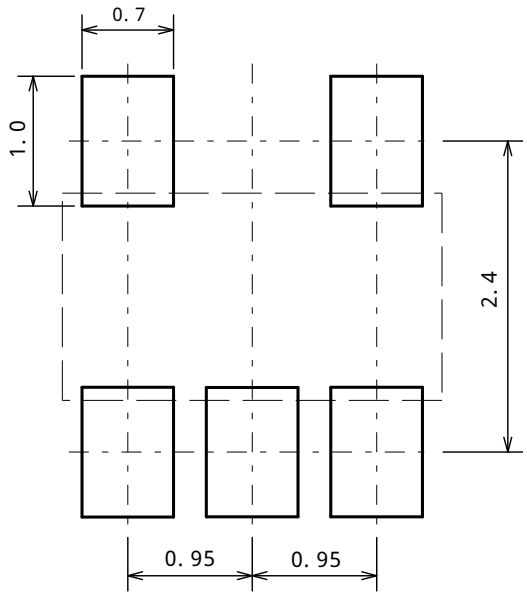
SOT-23-5

Unit: mm

■ PACKAGE DIMENSIONS



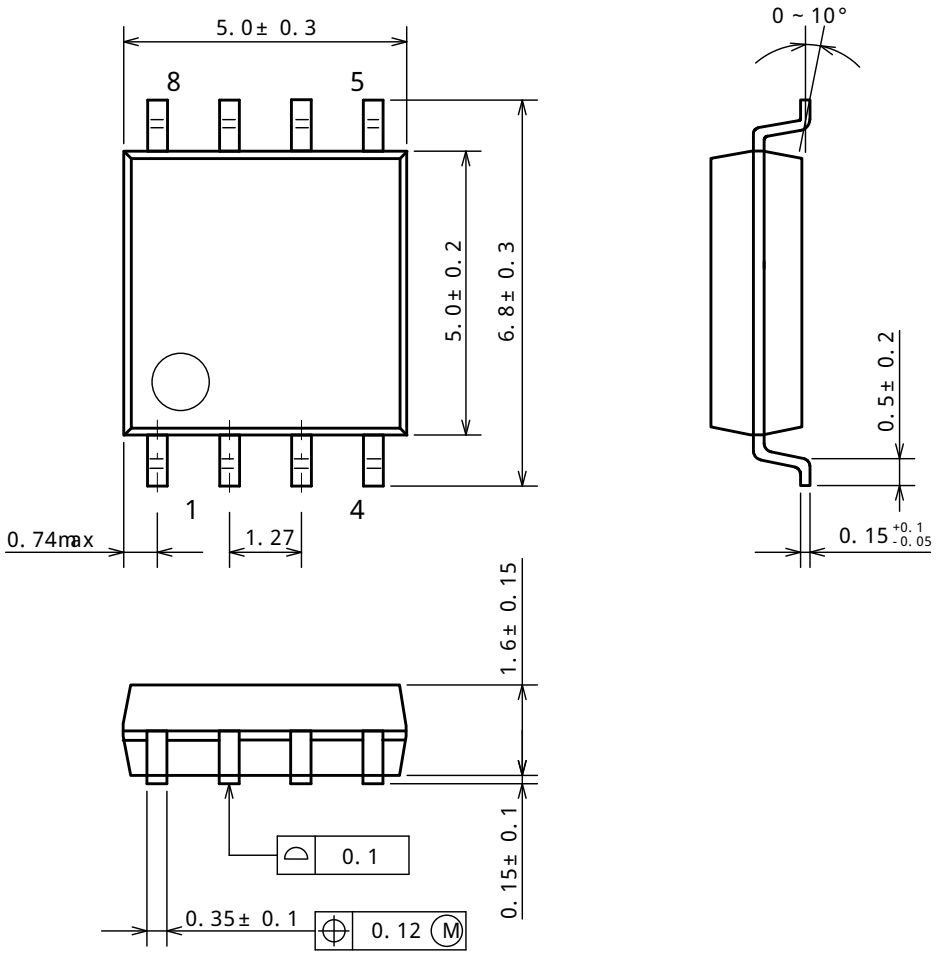
■ EXAMPLE OF SOLDER PADS DIMENSIONS



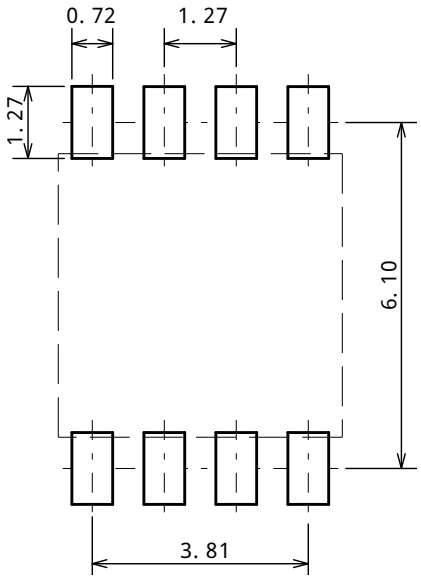
DMP8

Unit: mm

■ PACKAGE DIMENSIONS



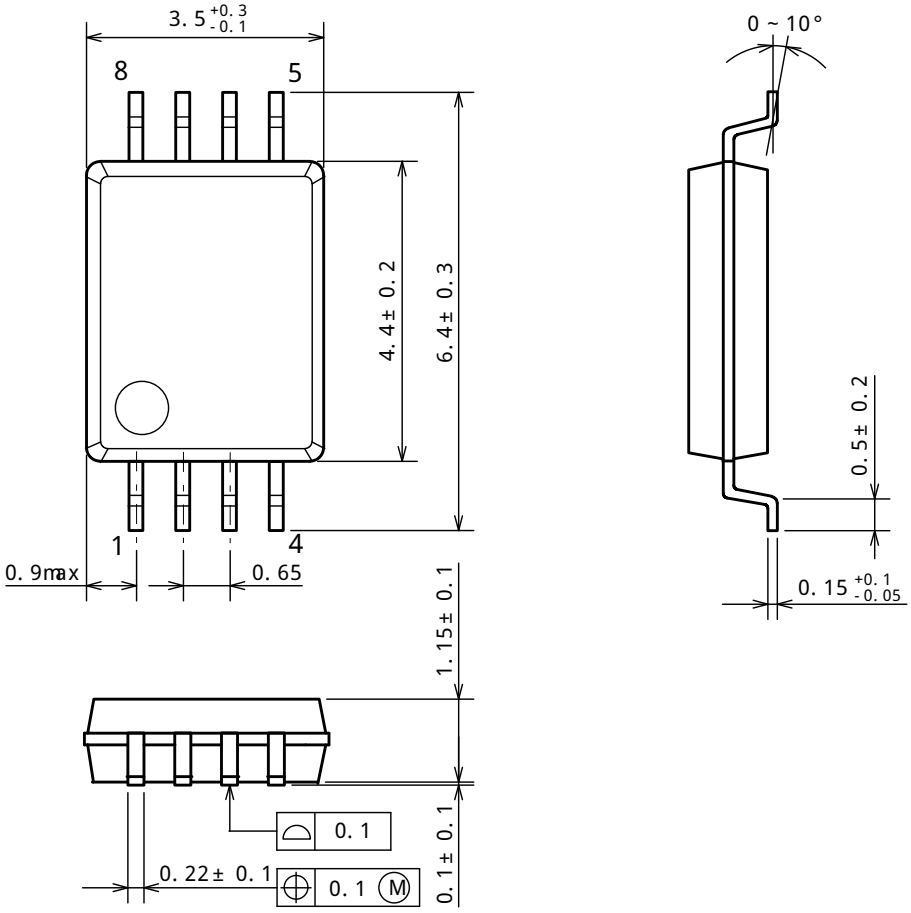
■ EXAMPLE OF SOLDER PADS DIMENSIONS



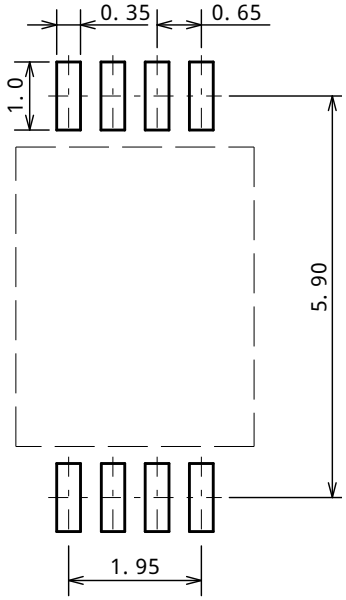
SSOP8

Unit: mm

■ PACKAGE DIMENSIONS



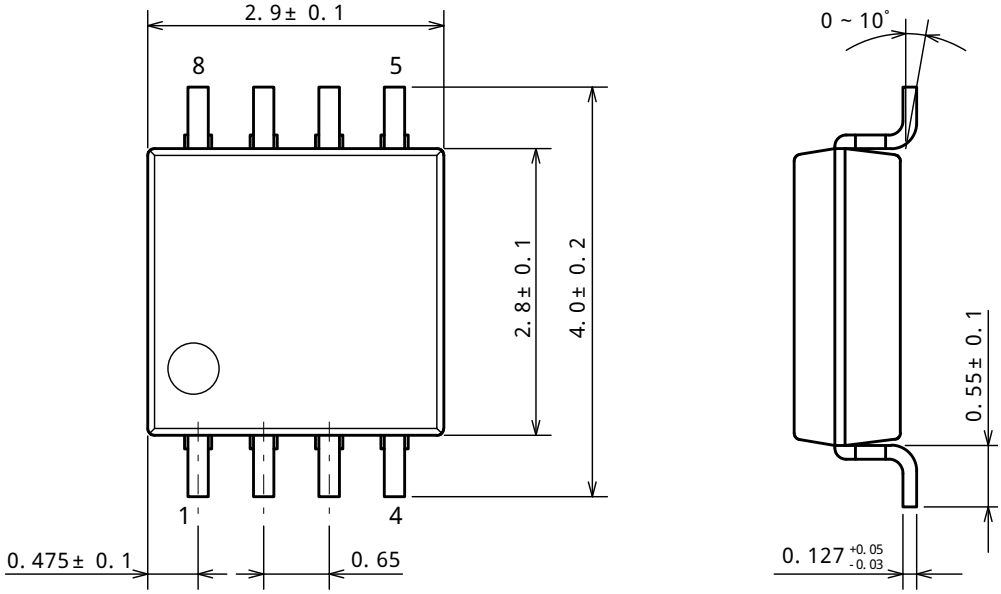
■ EXAMPLE OF SOLDER PADS DIMENSIONS

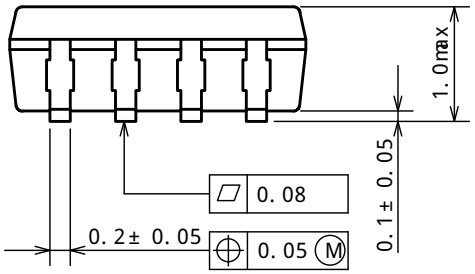


MSOP8 (TVSP8) JEDEC MO-187-DA/THIN TYPE

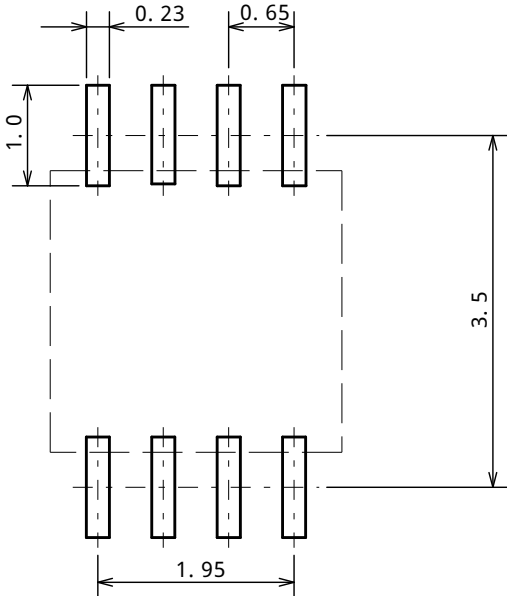
Unit: mm

■ PACKAGE DIMENSIONS





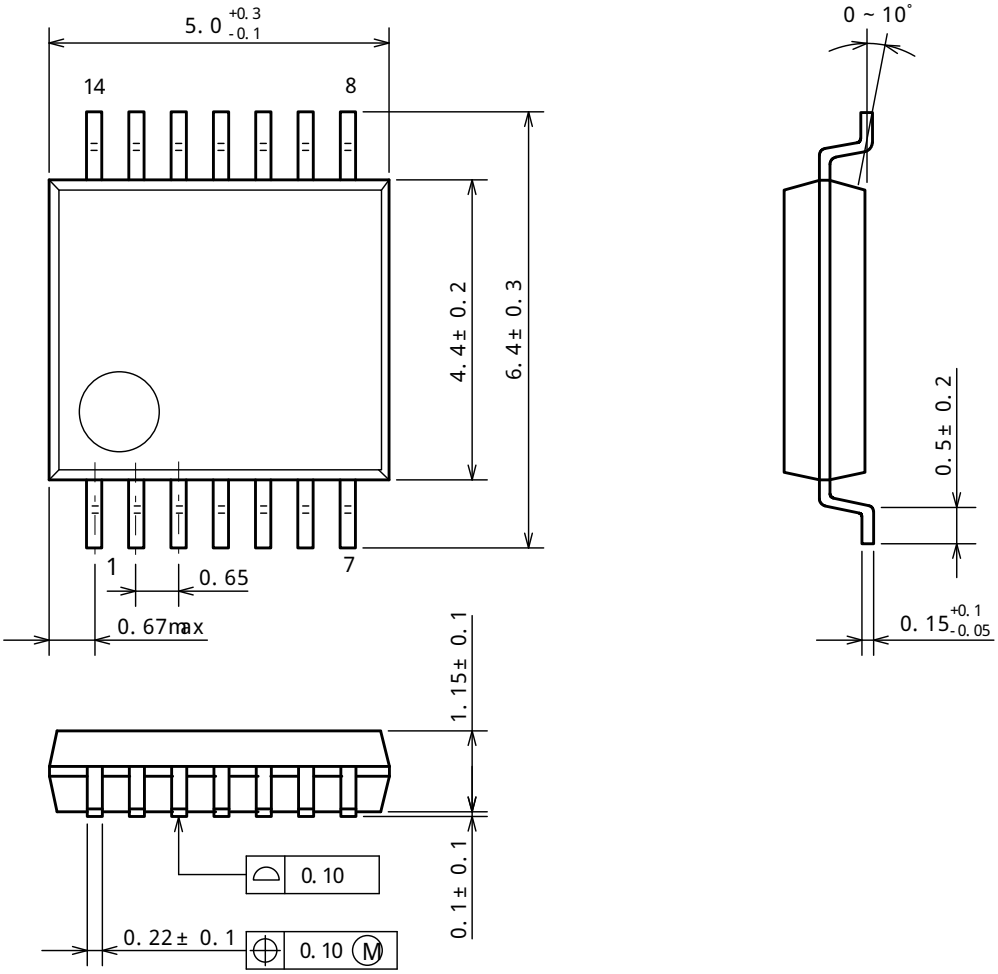
■ EXAMPLE OF SOLDER PADS DIMENSIONS



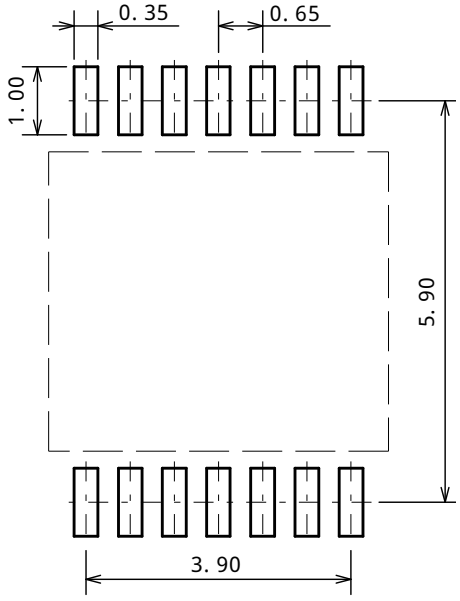
SSOP14

Unit: mm

■ PACKAGE DIMENSIONS



■ EXAMPLE OF SOLDER PADS DIMENSIONS

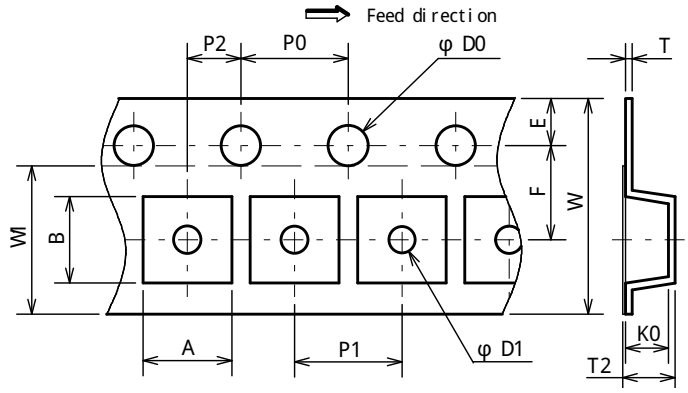


SOT-23-5

■ PACKING SPEC

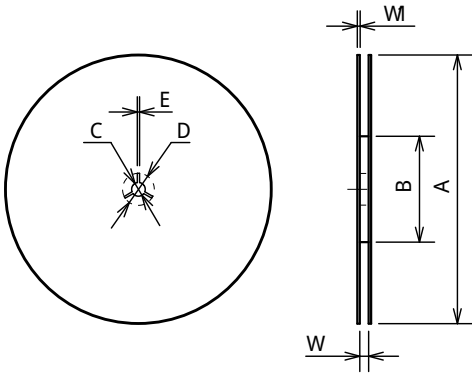
Unit: mm

TAPING DIMENSIONS



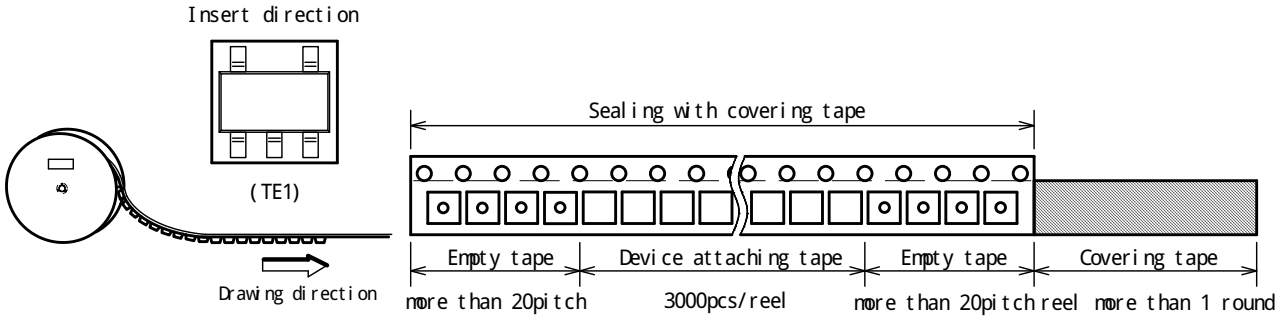
SYMBOL	DIMENSION	REMARKS
A	3.3± 0.1	BOTTOM DIMENSION
B	3.2± 0.1	BOTTOM DIMENSION
D0	1.55	
D1	1.05	
E	1.75± 0.1	
F	3.5± 0.05	
P0	4.0± 0.1	
P1	4.0± 0.1	
P2	2.0± 0.05	
T	0.25± 0.05	
T2	1.82	
K0	1.5± 0.1	
W	8.0± 0.3	
W1	5.5	THICKNESS 0.1MAX

REEL DIMENSIONS

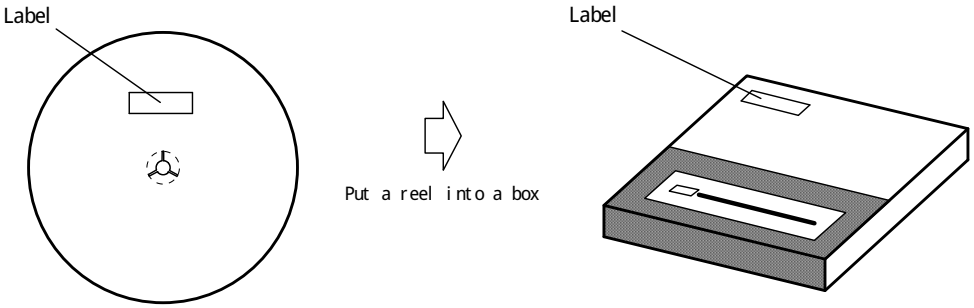


SYMBOL	DIMENSION
A	φ 180± 1
B	φ 60± 1
C	φ 13± 0.2
D	φ 21± 0.8
E	2± 0.5
W	9± 0.5
W1	1.2± 0.2

TAPING STATE



PACKING STATE

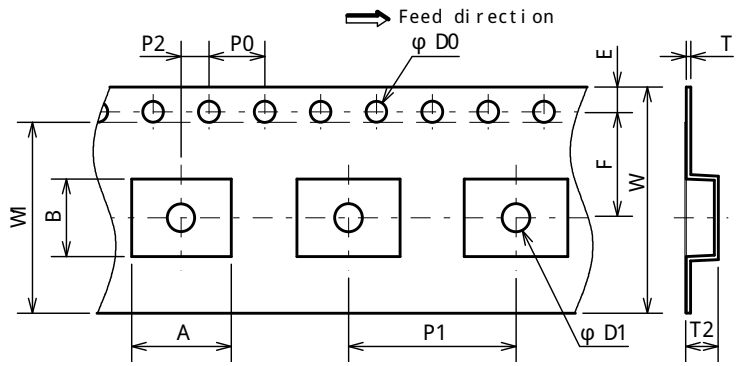


DMP8

■ PACKING SPEC

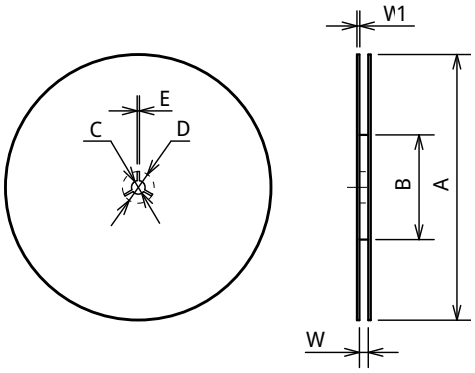
Unit: mm

TAPING DIMENSIONS



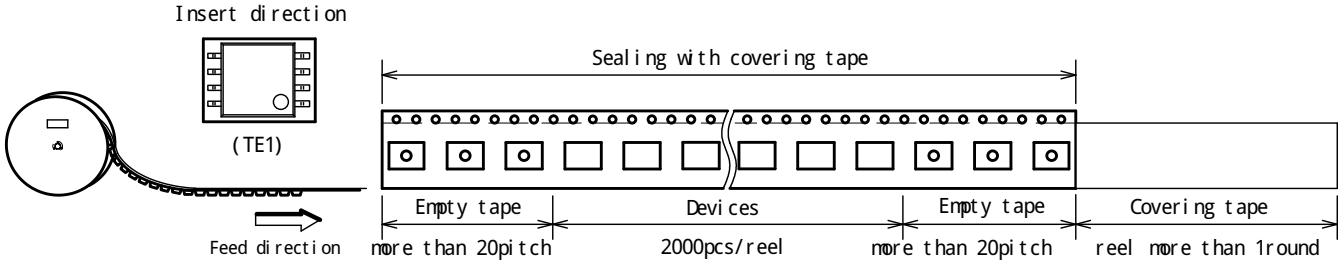
SYMBOL	DIMENSION	REMARKS
A	7.1	BOTTOM DIMENSION
B	5.4	BOTTOM DIMENSION
D0	1.55± 0.05	
D1	2.05± 0.1	
E	1.75± 0.1	
F	7.5± 0.1	
P0	4.0± 0.1	
P1	12.0± 0.1	
P2	2.0± 0.1	
T	0.3± 0.05	
T2	2.3	
W	16.0± 0.3	
W1	13.5	THICKNESS 0.1max

REEL DIMENSIONS

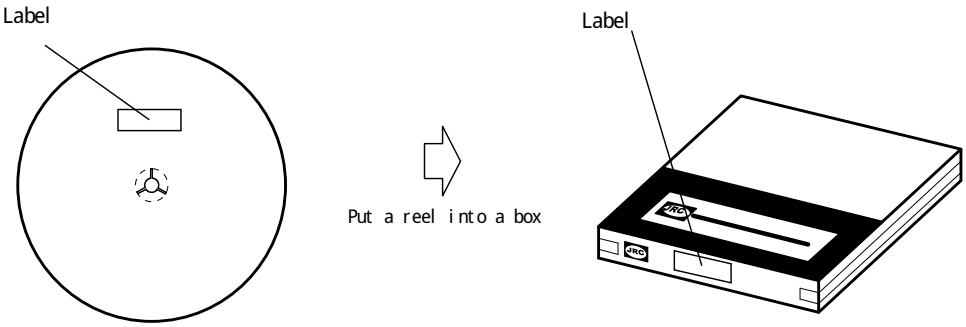


SYMBOL	DIMENSION
A	φ 330± 2
B	φ 80± 1
C	φ 13± 0.2
D	φ 21± 0.8
E	2± 0.5
W	17.5± 0.5
W1	2± 0.2

TAPING STATE



PACKING STATE

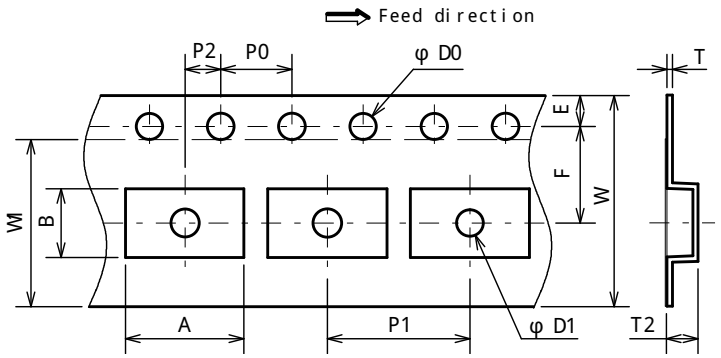


SSOP8

■ PACKING SPEC

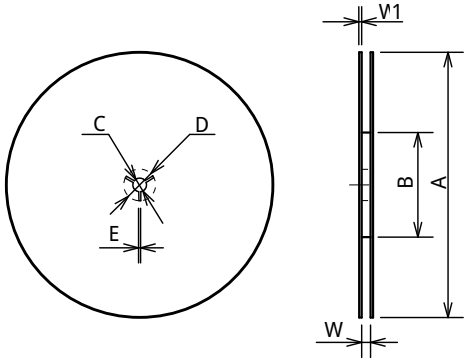
Unit: mm

TAPING DIMENSIONS



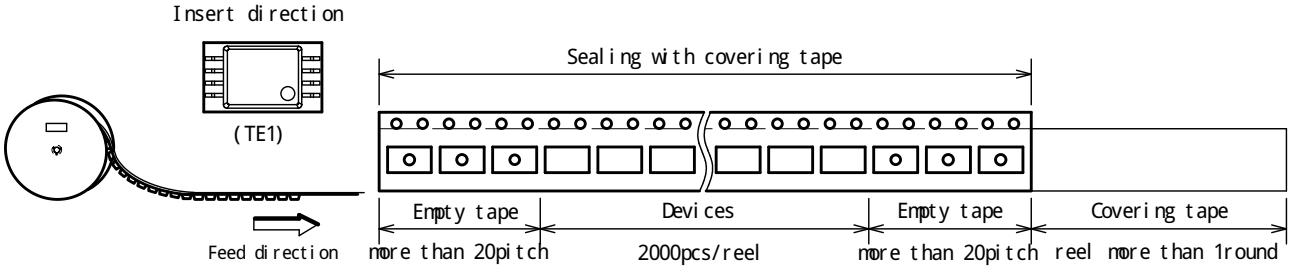
SYMBOL	DIMENSION	REMARKS
A	6.7	BOTTOM DIMENSION
B	3.9	BOTTOM DIMENSION
D0	1.55± 0.05	
D1	1.55± 0.1	
E	1.75± 0.1	
F	5.5± 0.05	
P0	4.0± 0.1	
P1	8.0± 0.1	
P2	2.0± 0.05	
T	0.3± 0.05	
T2	2.2	
W	12.0± 0.3	
W1	9.5	THICKNESS 0.1max

REEL DIMENSIONS

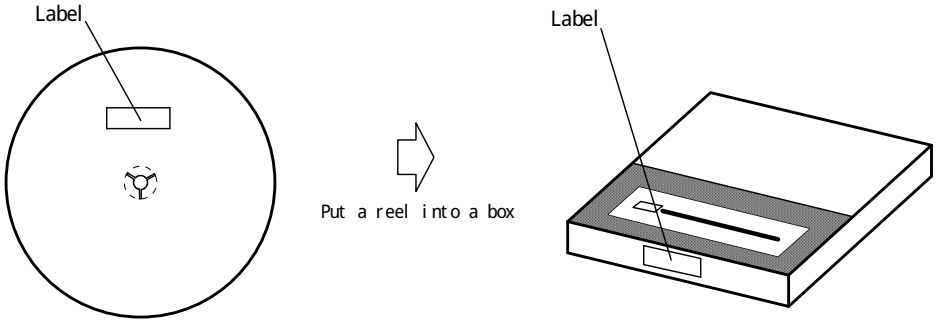


SYMBOL	DIMENSION
A	φ 254± 2
B	φ 100± 1
C	φ 13± 0.2
D	φ 21± 0.8
E	2± 0.5
W	13.5± 0.5
W1	2± 0.2

TAPING STATE



PACKING STATE

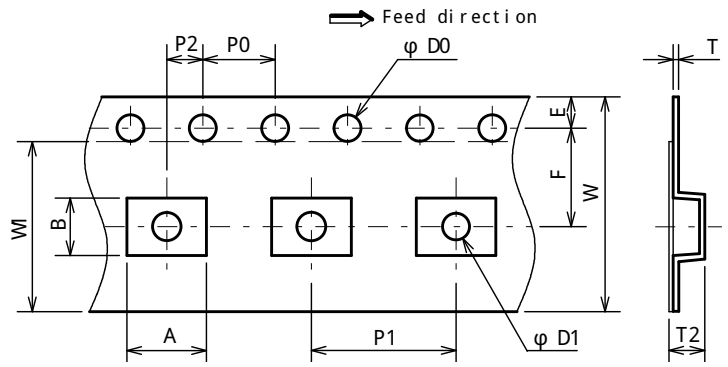


MSOP8 (TVSP8) MEET JEDEC MO-187-DA/THIN TYPE

Unit: mm

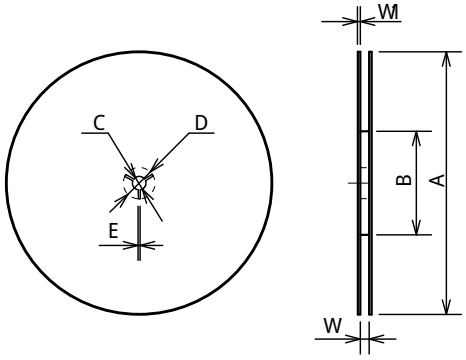
■ PACKING SPEC

TAPING DIMENSIONS



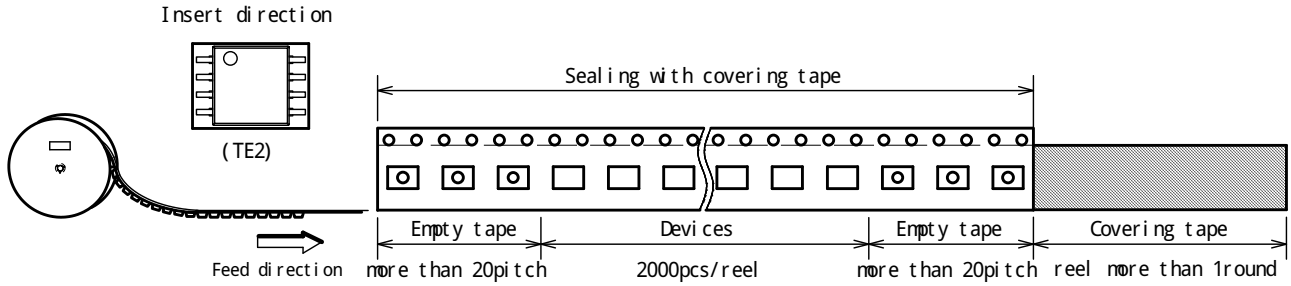
SYMBOL	DIMENSION	REMARKS
A	4.4	BOTTOM DIMENSION
B	3.2	BOTTOM DIMENSION
D0	$1.5^{+0.1}_{0}$	
D1	$1.5^{+0.1}_{0}$	
E	1.75± 0.1	
F	5.5± 0.05	
P0	4.0± 0.1	
P1	8.0± 0.1	
P2	2.0± 0.05	
T	0.30± 0.05	
T2	1.75 (MAX.)	
W	12.0± 0.3	
W1	9.5	THICKNESS 0.1max

REEL DIMENSIONS

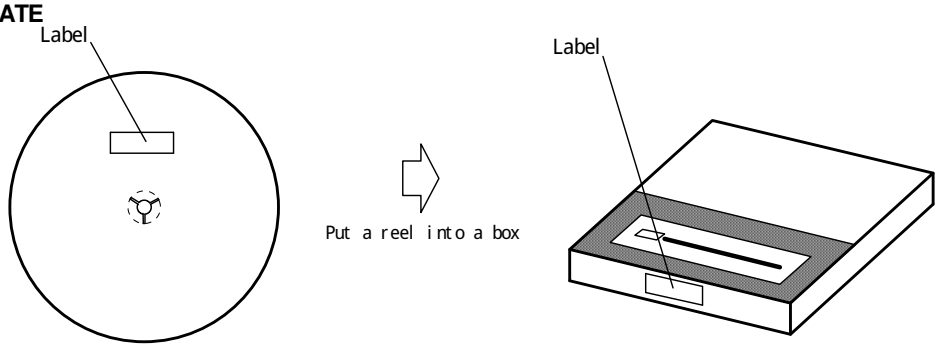


SYMBOL	DIMENSION
A	φ 254± 2
B	φ 100± 1
C	φ 13± 0.2
D	φ 21± 0.8
E	2± 0.5
W	13.5± 0.5
W1	2.0± 0.2

TAPING STATE



PACKING STATE

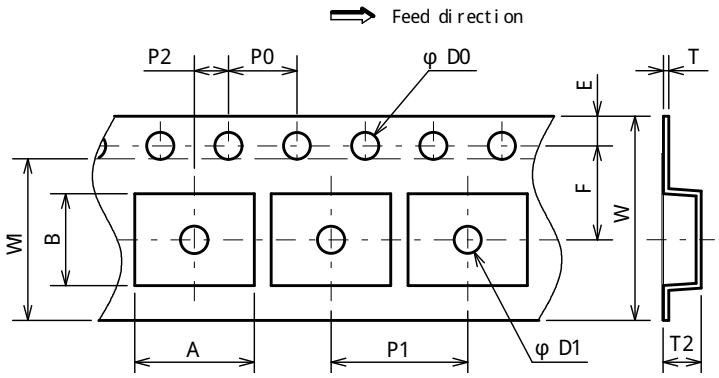


SSOP14

■ PACKING SPEC

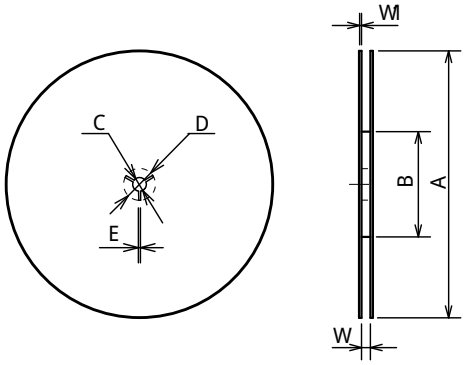
Unit: mm

TAPING DIMENSIONS



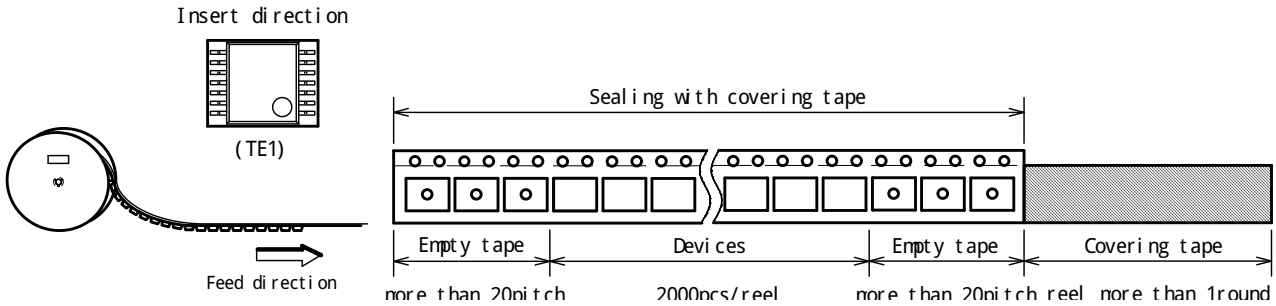
SYMBOL	DIMENSION	REMARKS
A	6.95	BOTTOM DIMENSION
B	5.4	BOTTOM DIMENSION
D0	1.55± 0.05	
D1	1.55± 0.1	
E	1.75± 0.1	
F	5.5± 0.05	
P0	4.0± 0.1	
P1	8.0± 0.1	
P2	2.0± 0.05	
T	0.3± 0.05	
T2	2.2	
W	12.0± 0.3	
W1	9.5	THICKNESS 0.1max

REEL DIMENSIONS



SYMBOL	DIMENSION
A	φ 254± 2
B	φ 100± 1
C	φ 13± 0.2
D	φ 21± 0.8
E	2± 0.5
W	13.5± 0.5
W1	2± 0.2

TAPING STATE



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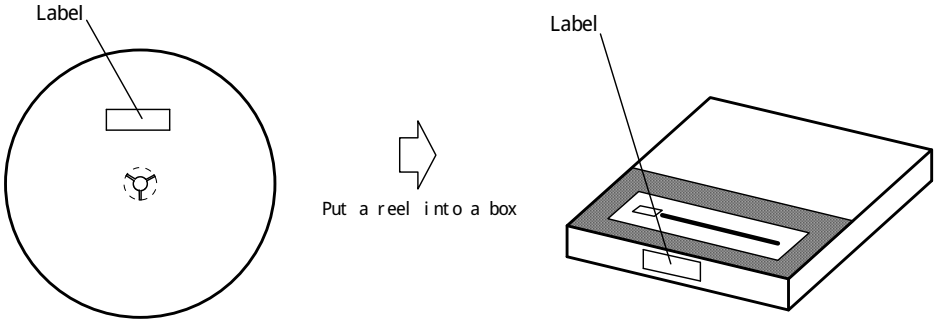
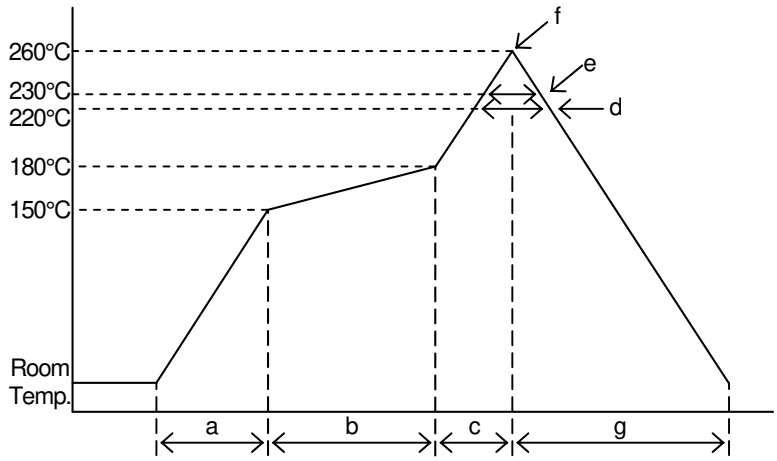


■ RECOMMENDED MOUNTING METHOD

INFRARED REFLOW SOLDERING PROFILE



a	Temperature ramping rate	1 to 4°C/s
b	Pre-heating temperature Pre-heating time	150 to 180°C 60 to 120s
c	Temperature ramp rate	1 to 4°C/s
d	220°C or higher time	shorter than 60s
e	230°C or higher time	shorter than 40s
f	Peak temperature	lower than 260°C
g	Temperature ramping rate	1 to 6°C/s

The temperature indicates at the surface of mold package.

■ REVISION HISTORY

DATE	REVISION	CHANGES
July 1, 2019	5	Changed design of datasheet format.

[CAUTION]

1. NJR strives to produce reliable and high quality semiconductors. NJR's semiconductors are intended for specific applications and require proper maintenance and handling. To enhance the performance and service of NJR's semiconductors, the devices, machinery or equipment into which they are integrated should undergo preventative maintenance and inspection at regularly scheduled intervals. Failure to properly maintain equipment and machinery incorporating these products can result in catastrophic system failures

2. The specifications on this datasheet are only given for information without any guarantee as regards either mistakes or omissions. The application circuits in this datasheet are described only to show representative usages of the product and not intended for the guarantee or permission of any right including the industrial property rights.
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3. To ensure the highest levels of reliability, NJR products must always be properly handled.
   The introduction of external contaminants (e.g. dust, oil or cosmetics) can result in failures of semiconductor products.

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5. Special care is required in designing devices, machinery or equipment which demand high levels of reliability. This is particularly important when designing critical components or systems whose failure can foreseeably result in situations that could adversely affect health or safety. In designing such critical devices, equipment or machinery, careful consideration should be given to amongst other things, their safety design, fail-safe design, back-up and redundancy systems, and diffusion design.

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   - Equipment Used in the Deep Sea
   - Power Generator Control Equipment (Nuclear, steam, hydraulic, etc.)
   - Life Maintenance Medical Equipment
   - Fire Alarms / Intruder Detectors
   - Vehicle Control Equipment (Airplane, railroad, ship, etc.)
   - Various Safety Devices

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9. The product specifications and descriptions listed in this datasheet are subject to change at any time, without notice.