Datasheet

Boundary Conduction Mode

Power Factor Correction Controller IC

BD7693FJ BD7694FJ

General Description

BD7693FJ and BD7694FJ are Power Factor Correction IC for AC/DC supplies the system which is suitable for all the products needing power factor improvement. The PFC adopts boundary conduction mode (BCM), and switching loss reduction and noise reduction are possible by Zero Current Detection (ZCD). This IC incorporates a circuit lowering total harmonics distortion (THD) and can support IEC61000-3-2 Class-C.

Features

- Boundary Conduction Mode PFC
- Low THD Circuit Incorporation
- Low Power Consumption
- VCC UVLO Function
- ZCD by Auxiliary Winding
- Static OVP by the VS Pin
- Error Amplifier Input Short Protection
- Stable MOSFET Gate Drive
- Soft Start

Applications

- Lighting Equipment, AC Adopter, TV, Refrigerator, etc.

Key Specifications

- Input VCC Voltage Range: 10 V to 38 V
- Operating Current: 0.58 mA (Typ)
- Operating Temperature Range: -40 °C to +105 °C

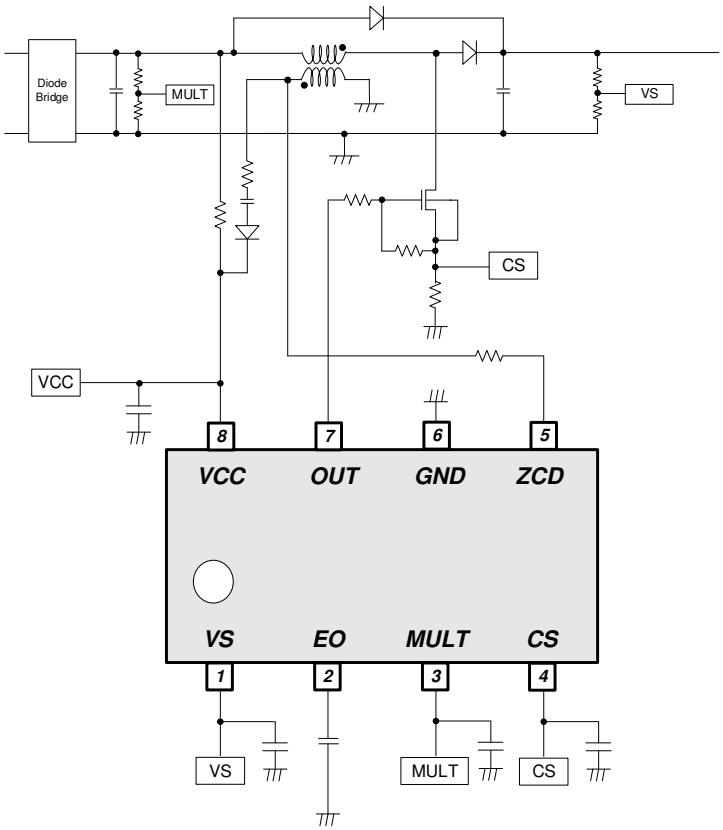
Package

	W (Typ) x D (Typ) x H (Max)
SOP-J8	4.9 mm x 6.0 mm x 1.65 mm

Lineup

Product name	Brown Out
BD7693FJ-E2	-
BD7694FJ-E2	○

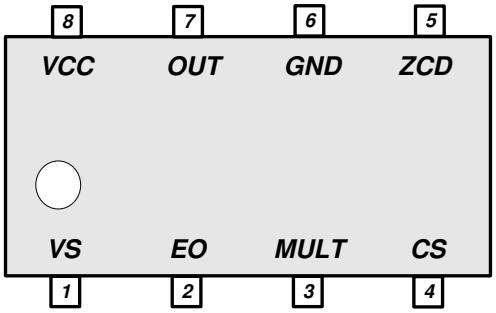
Typical Application Circuit



○Product structure : Silicon integrated circuit ○This product has no designed protection against radioactive rays.

Pin Configuration

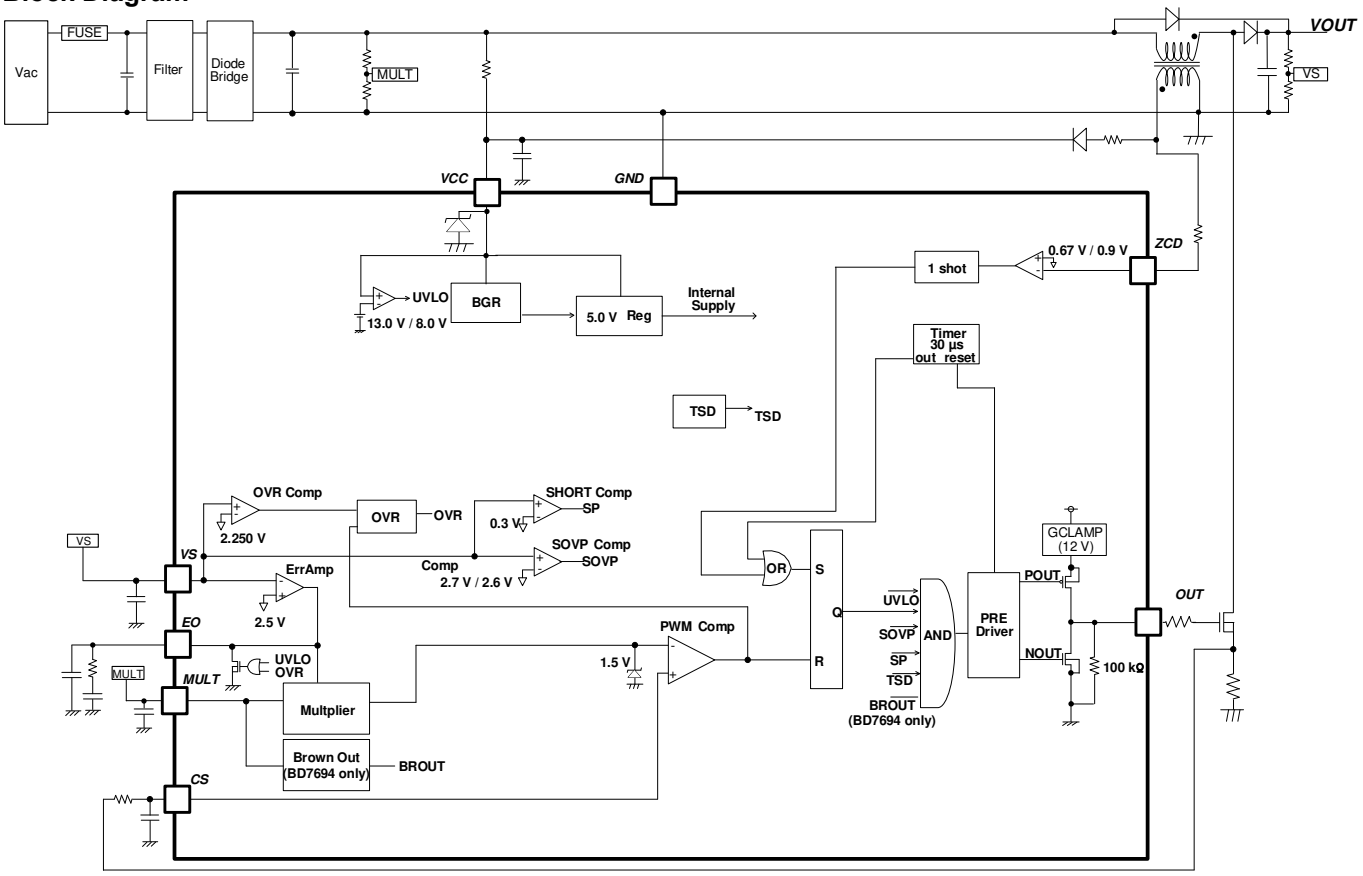
(TOP VIEW)



Pin Description

Pin No.	Pin Name	I/O	Function	ESD Diode	
				VCC	GND
1	VS	I	Feedback input pin	-	○
2	EO	O	Error amplifier output pin	-	○
3	MULT	I	Multiplier input pin	-	○
4	CS	I	Over current detection pin	-	○
5	ZCD	I	Zero current detection pin	-	○
6	GND	-	GND pin	○	-
7	OUT	O	External MOSFET driver pin	-	○
8	VCC	I	Power supply pin	-	○

Block Diagram



Description of Blocks

1 VCC Protection

This IC has VCC UVLO (Under Voltage Lock Out) of the VCC pin. Switching stops at the time of VCC voltage drop.
In addition, when the VCC voltage becomes higher than the V_{CC_DIS1} (38 V Typ) voltage, it increases operating current and suppresses the rise in VCC voltage. When the VCC voltage lowers than the V_{CC_DIS2} (34 V Typ) voltage, the operating current becomes usual. This function assumes the case that the VCC voltage rises by startup resistance.

2 PFC: Power Factor Correction

The power factor improvement circuit is a voltage control method of Boundary Conduction Mode.
The outline operation circuit diagram is shown in Figure 1. The switching operation is shown in Figure 2.

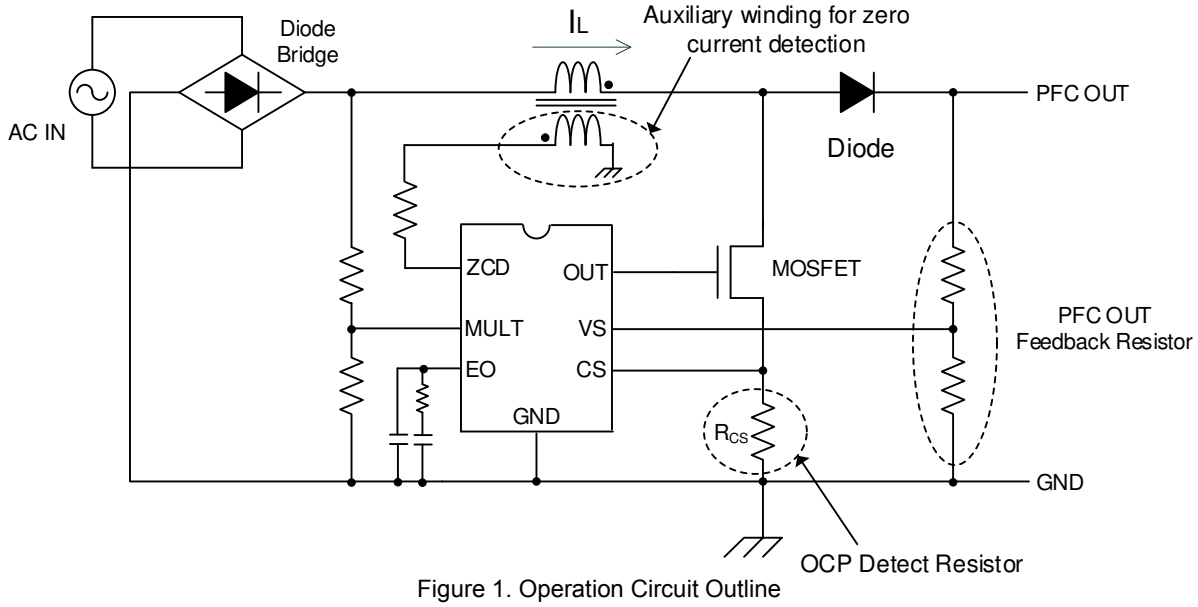


Figure 1. Operation Circuit Outline

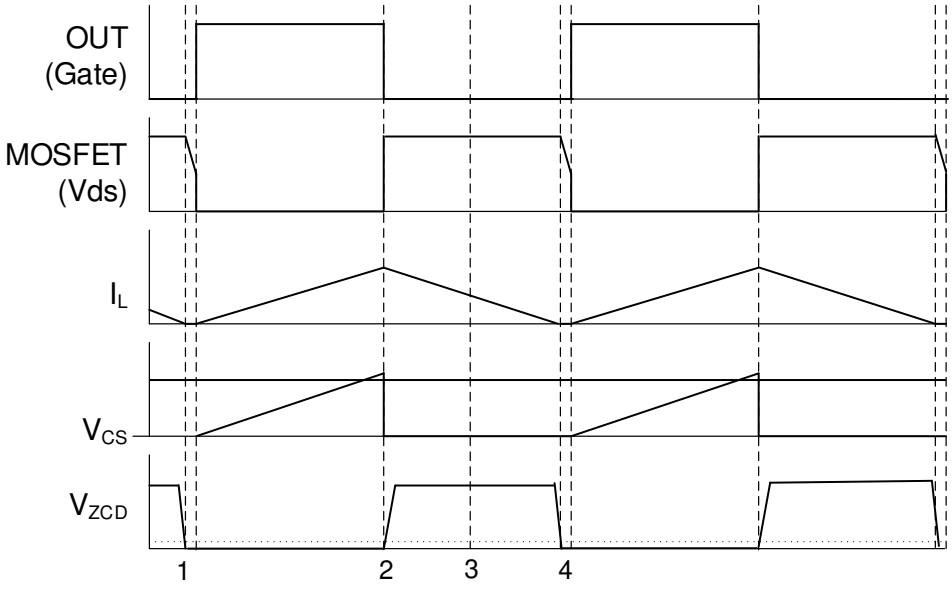


Figure 2. Switching Operation Timing Chart

Switching Operation

1. MOSFET is turned on, and I_L increases.
2. The IC compares Multiplier out with V_{CS} slope, and MOSFET is off when the V_{CS} voltage higher than Multiplier out.
3. MOSFET is off, and I_L decreases.
4. The ZCD pin detects a zero point of the I_L and turns on MOSFET.

Description of Blocks - continued

3 About ErrAMP

3.1 GmAMP

The VS pin monitors a divided point for resistance of the output voltage. The ripple voltage of AC frequency (50 Hz / 60 Hz) overlaps with the VS pin. GmAMP removes this ripple voltage. GmAMP compares V_{AMP1} (2.500 V Typ) with the removed voltage, GmAMP controls the EO voltage by this gap. When the EO pin voltage rises, ON width of the OUT pin becomes wide. When the EO voltage less than V_{BURST} (1.9 V Typ), the IC stops switching. Therefore, it can stop switching operation when the EO pin connects to the GND.
Also, you must set the error amplifier constant so that the AC frequency does not overlap on the EO pin. And, please confirm it by an actual board.

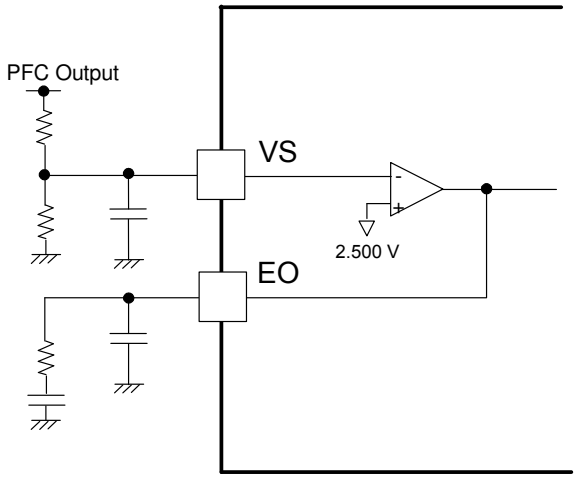


Figure 3. GmAMP Block Diagram

3.2 VS Short Protection

The VS pin has a short protection function.
A state of the VS pin voltage < V_{SHORT} (0.3 V Typ) continues t_{VS_SH} (150 µs Typ) or more, it stops switching.
Figure 4 shows the operation.

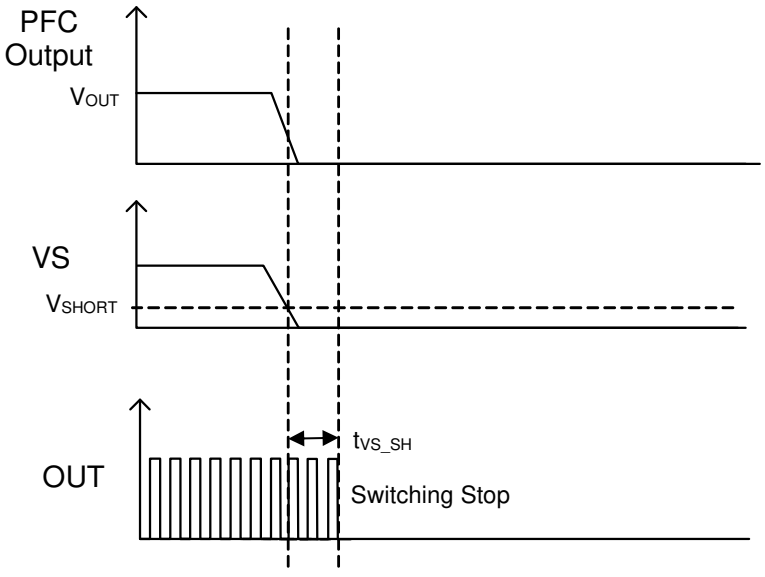


Figure 4. Operation of VS Short Protection

3 About ErrAMP - continued

3.3 VS Overvoltage Protection Function (SOVP)

The VS pin voltage rises from V_{OVP1} (2.7 V Typ), it stops switching immediately. The VS pin voltage less than V_{OVP2} (2.6 V Typ), it starts switching. Figure 5 shows the operation.

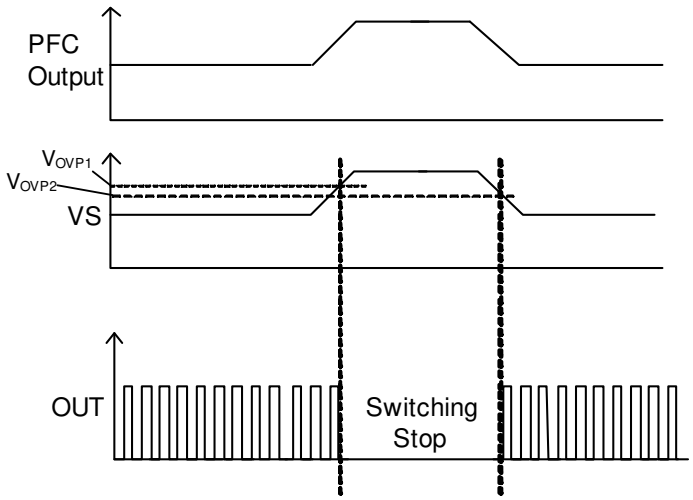


Figure 5. VS Overvoltage Protection Operation

3.4 Over Voltage Reduce Function at Start Up (OVR)

When the VS pin voltage performs a rise in startup to V_{OVR} (2.25 V Typ) (equivalent to -10 % of output voltage), it discharges the EO voltage to the V_{BURST} forcibly. OUT pulse width is narrows when the EO voltage falls, through rate of output voltage becomes slow and reduces over voltage in the startup.
This function is effective only once after VCC UVLO cancellation.

Description of Blocks - continued

4 ZCD pin

The zero current detection circuit is a function to detect a zero cross of the inductor current (I_L) (Figure 6, 7).
If the voltage at the ZCD pin becomes lower than V_{ZCD2} (0.67 V Typ) after becoming higher than V_{ZCD1} (0.9 V Typ), the OUT output becomes High after the ZCD output delay time (t_{ZCD} 260 ns Typ) has elapsed.
When the ZCD voltage does not reach V_{ZCD1} (0.9 V Typ), it becomes the restart timer operation. After the OUT output became Low, OUT becomes High after t_{REST} (30 µs Typ) progress (Figure 8).

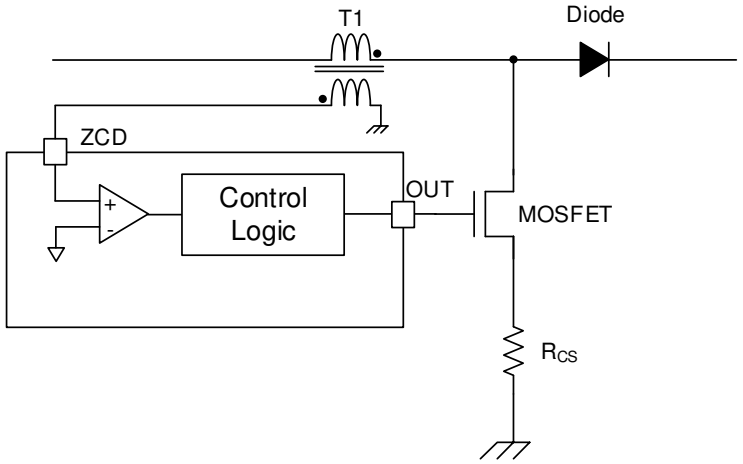


Figure 6. Zero Current Detection Circuit

Figure 7. Zero Current Detection

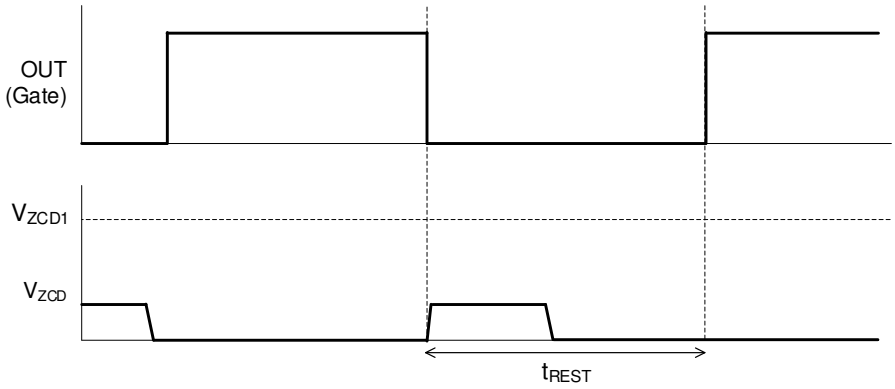


Figure 8. Restart Timer

Description of Blocks - continued

5 MULTIPLIER

The ON width of the OUT pin is fixed in Multiplier out and V_{CS} as it showed in Figure 2.
V_{CS} is expressed in the following formula.

$$V_{CS} = K \times V_{MULT}(V_{EO} - V_{BURST})$$

K: MULTIPLIER GAIN
V_{MULT}: MULT pin voltage
V_{EO}: EO pin voltage
V_{BURST}: Burst voltage

AC voltage information is input into V_{MULT}. The IC improves a power factor by controlling AC current with the AC voltage. In addition, V_{CS} in AC voltage 0 V (V_{MULT} = 0 V) is expressed in the following formula.

$$V_{CS} = K \times V_{MULT}(V_{EO} - V_{BURST}) + V_{OFFSET} = V_{OFFSET}$$

The ON width of the OUT pin at the age of AC voltage 0 V (V_{MULT} = 0 V) becomes long by adding V_{OFFSET} (25 mV Typ). Because ON width gets longer, diode bridge output voltage is discharged. As a result, an AC current distortion is improved without the current supply from a diode bridge stopping (Figure 9).

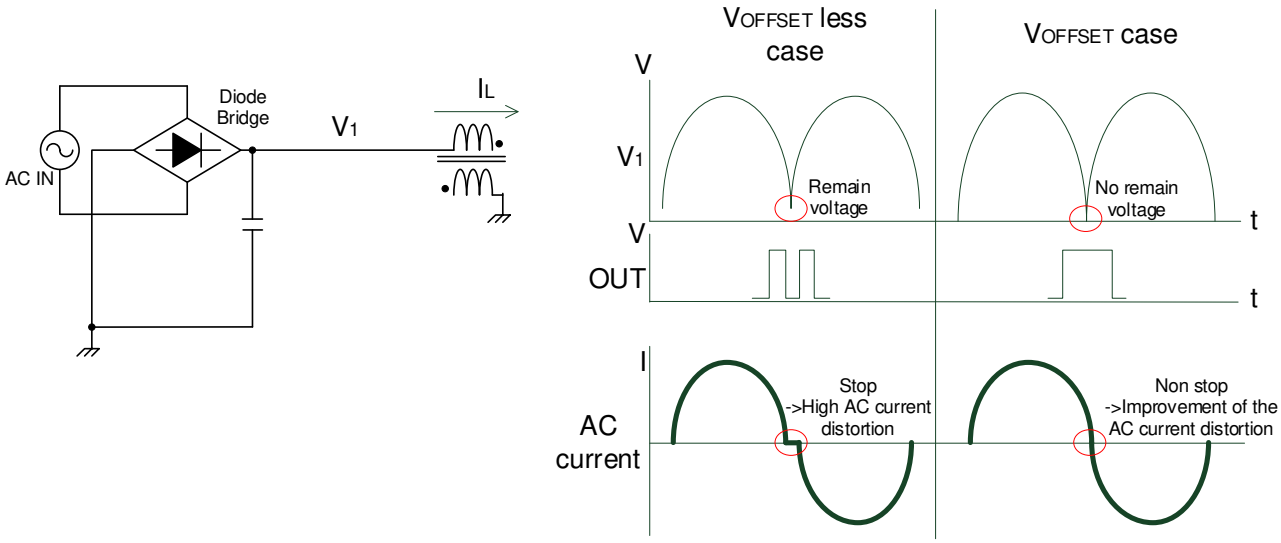


Figure 9. Improvement of the AC Current Distortion

Description of Blocks - continued

6 MULT pin

When the state that the MULT pin voltage is lower than V_{BROUT1} (0.8 V Typ) continues t_{BROUT} (160 ms Typ) or more, the IC stops switching by a brown out function (only in BD7694).
When the MULT pin voltage becomes higher than V_{BROUT2} (0.97 V Typ), the IC switches again.

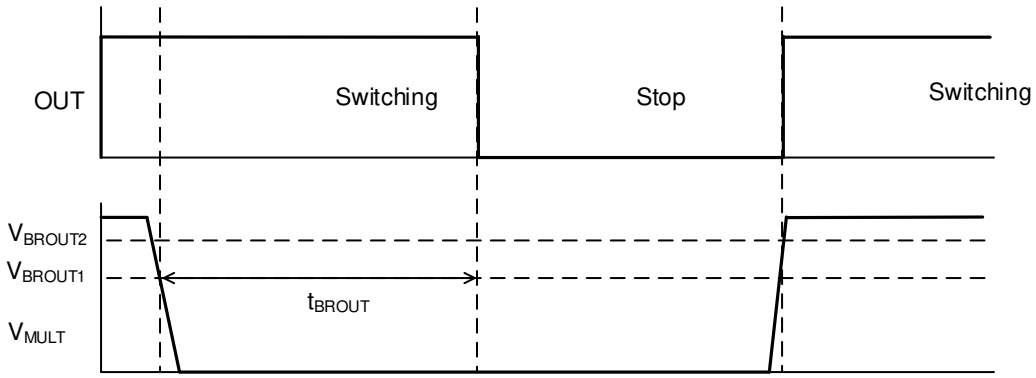


Figure 10. Brown Out

7 CS pin

In normal operation, turn OFF of the switching is usually decided by ON width by the EO pin and the MULT pin voltage. However, the IC is off in a pulse by pulse in overcurrent protection when the CS pin rises than V_{CS} (1.5 V Typ). By this protection, it prevents an overcurrent to MOSFET.
The overcurrent protection function limits ON width. When this protection becomes the working PFC load, PFC output voltage decreases. You must decide sense resistance of PFC so that this protection does not work in rated load with the minimum input voltage at the time of the application design.

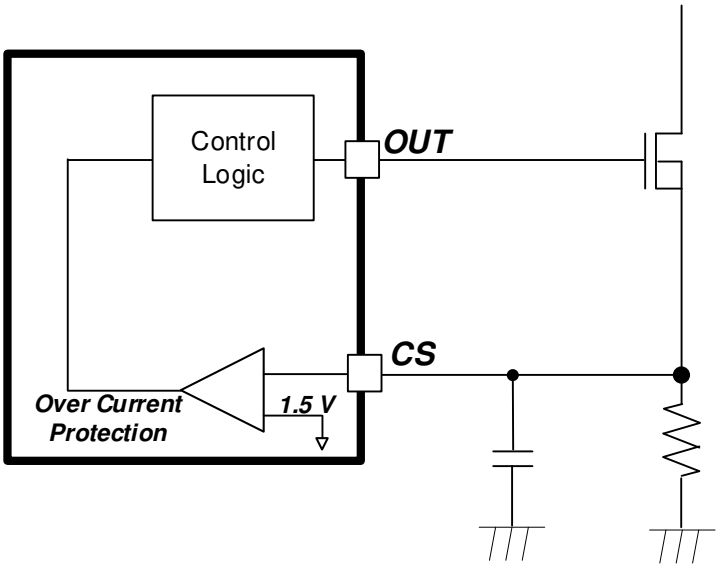


Figure 11. Current Limit

Operation Mode of Protection Circuit

Table 1 showed the operation mode of each protection function.

Table 1. Operation Mode of Each Protective Circuit

Parameter	Contents	Protection Mode			
		Detection Method	Detection Operation	Cancellation Method	Cancellation Operation
VCC UVLO	Under Voltage Lock Out on the VCC pin	VCC < 8 V (Typ) (VCC drop)	OUT OFF EO discharge	VCC > 13 V (Typ) (VCC rise)	Startup Operation
CS OCP	Over Current Protection on the CS pin	CS > 1.5 V (Typ) (CS rise)	OUT OFF	CS < 1.5 V (Typ) (CS drop)	Normal Operation
VS Short	Short Protection on the VS pin	VS < 0.3 V (Typ) (VS drop)	OUT OFF EO discharge	VS > 0.3 V (Typ) (VS rise)	Normal Operation
VS Static OVP	Over Voltage Protection on the VS pin	VS > 2.7 V (Typ) (VS rise)	OUT OFF	VS < 2.6 V (Typ) (VS drop)	Normal Operation
Brown Out (Only BD7694)	Low Voltage Protection on the MULT pin	MULT < 0.8 V (Typ) (MULT drop)	OUT OFF EO discharge	MULT > 0.97 V (Typ) (MULT rise)	Normal Operation

Absolute Maximum Ratings (Ta = 25 °C)

Parameter	Symbol	Rating	Unit	Condition
Maximum Voltage 1	V_{MAX1}	-0.3 to +40	V	VCC
Maximum Voltage 2	V_{MAX2}	-0.3 to +14	V	OUT
Maximum Voltage 3	V_{MAX3}	-0.3 to +6.5	V	CS, MULT, VS, EO
Maximum Current 1	I_{ZCD1}	-10 to +10	mA	ZCD current
OUT Pin Output Peak Current 1	I_{OUT1}	-0.5	A	Source current
OUT Pin Output Peak Current 2	I_{OUT2}	+1	A	Sink current
Maximum Junction Temperature	Tjmax	+150	°C	
Storage Temperature Range	Tstg	-55 to +150	°C	

Caution 1: *Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.*

Caution 2: *Should by any chance the maximum junction temperature rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. In case of exceeding this absolute maximum rating, design a PCB with thermal resistance taken into consideration by increasing board size and copper area so as not to exceed the maximum junction temperature rating.*

Thermal Resistance*(Note 1)*

Parameter	Symbol	Thermal Resistance (Typ)		Unit
		1s*(Note 3)*	2s2p*(Note 4)*	
SOP-J8				
Junction to Ambient	θ_{JA}	149.3	76.9	°C/W
Junction to Top Characterization Parameter*(Note 2)*	Ψ_{JT}	18	11	°C/W

(Note 1) Based on JESD51-2A(Still-Air)
(Note 2) The thermal characterization parameter to report the difference between junction temperature and the temperature at the top center of the outside surface of the component package.
(Note 3) Using a PCB board based on JESD51-3.
(Note 4) Using a PCB board based on JESD51-7.

Layer Number of Measurement Board	Material	Board Size
Single	FR-4	114.3 mm x 76.2 mm x 1.57 mmt

Top	
Copper Pattern	Thickness
Footprints and Traces	70 µm

Layer Number of Measurement Board	Material	Board Size
4 Layers	FR-4	114.3 mm x 76.2 mm x 1.6 mmt

Top		2 Internal Layers		Bottom	
Copper Pattern	Thickness	Copper Pattern	Thickness	Copper Pattern	Thickness
Footprints and Traces	70 µm	74.2 mm x 74.2 mm	35 µm	74.2 mm x 74.2 mm	70 µm

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit	Condition
Supply Voltage	VCC	10	15	38	V	VCC Voltage
Operating Temperature	Topr	-40	+25	+105	°C	

Recommended Range of the External Component (Ta = 25 °C)

Parameter	Symbol	Rating	Unit
VCC Pin Connection Capacity	C_{VCC}	22 or more	µF

Electrical Characteristics (Unless otherwise specified VCC = 15 V, Ta = -40 °C to +105 °C)

Parameter	Symbol	Min	Typ	Max	Unit	Condition
[Circuit Current]						
Circuit Current (ON) 1	I_{ON1}	-	0.58	1.20	mA	VS = 0 V
Circuit Current (ON) 2	I_{ON2}	-	0.95	2.00	mA	50 kHz switching
Circuit Current (ON) 3	I_{ON3}	4.5	9.0	13.5	mA	VCC discharge Switching stop
Start Up Current	I_{START}	-	100	200	µA	VCC = 12 V
[VCC Pin Protection]						
VCC UVLO Voltage1	V_{UVLO1}	12	13	14	V	VCC rise
VCC UVLO Voltage2	V_{UVLO2}	7	8	9	V	VCC drop
VCC UVLO Hysteresis	V_{UVLO3}	3.8	5.0	6.2	V	$V_{UVLO3} = V_{UVLO1} - V_{UVLO2}$
VCC Discharge Voltage1	V_{CC_DIS1}	-	38	-	V	VCC rise
VCC Discharge Voltage2	V_{CC_DIS2}	-	34	-	V	VCC drop
[Gm Amplifier Block]						
VS Pin Pull-up Current	I_{VS}	-	0.1	0.5	µA	VS = 0 V
Gm Amplifier Reference Voltage1	V_{AMP1}	2.465	2.500	2.535	V	Ta = 25 °C
Gm Amplifier Reference Voltage2	V_{AMP2}	2.44	-	2.54	V	Ta = -40 °C to +105 °C
Gm Amplifier Line Regulation	V_{AMP_LINE}	-	1	10	mV	VCC = 10 V to 38 V
Gm Amplifier Trans Conductance	T_{VS}	80	100	130	µA/V	EO = 2.5 V, Ta = 25 °C
Gm Amplifier Source Current	I_{EO_SOURCE}	5	10	20	µA	VS = 2.3 V
Gm Amplifier Sink Current	I_{EO_SINK}	5	10	20	µA	VS = 2.7 V
[EO Block]						
EO L Voltage	V_{EOL}	-	1.6	1.8	V	VS = 2.7 V
Burst Voltage	V_{BURST}	1.8	1.9	-	V	
EO Discharge Current	I_{EO}	0.8	1.8	3.0	mA	VCC = 12 V, EO = 1.0 V
[MULT Block]						
MULT Pin Pull-up Current	I_{MULT}	-	0.1	0.5	µA	MULT = 0 V
MULT Pin Dynamic Range	V_{MULT}	0 to 2.5	0 to 3.5	-	V	
EO Pin Dynamic Range	V_{EOD}	V_{BURST} to 2.9	V_{BURST} to 3.4	-	V	
MULTIPLIER Gain	K	0.43	0.65	0.87	1/V	MULT = 0.5 V, EO = 3.0 V
Brown Out Detect Voltage1	V_{BROUT1}	0.7	0.8	0.9	V	MULT drop BD7694FJ Only
Brown Out Detect Voltage2	V_{BROUT2}	0.87	0.97	1.07	V	MULT rise BD7694FJ Only
Brown Out Detect Timer	t_{BROUT}	80	160	320	ms	BD7694FJ Only
[ZCD Block]						
ZCD Threshold Voltage1	V_{ZCD1}	0.8	0.9	1.0	V	ZCD rise
ZCD Threshold Voltage2	V_{ZCD2}	0.55	0.67	0.79	V	ZCD drop
ZCD Output Delay	t_{ZCD}	-	260	520	ns	
Input H Clamp Voltage	V_{IH}	6.1	6.7	-	V	Isink = 3 mA
Input L Clamp Voltage	V_{IL}	-0.3	-0.1	-	V	Isource = -3 mA
Restart Timer	t_{REST}	15	30	45	µs	
[VS Protection Block]						
VS Short Protection Detection Voltage	V_{SHORT}	0.2	0.3	0.4	V	
VS Shortstop Protection Detection Time	t_{VS_SH}	50	150	300	µs	
Over Voltage Reduce Detection Voltage	V_{OVR}	-	0.9 x V_{AMP1}	-	V	
VS Overvoltage Protection Detection Voltage 1	V_{OVP1}	1.065 x V_{AMP1}	1.080 x V_{AMP1}	1.095 x V_{AMP1}	V	VS rise Ta = 25 °C
VS Overvoltage Protection Detection Voltage 2	V_{OVP2}	1.020 x V_{AMP1}	1.040 x V_{AMP1}	1.060 x V_{AMP1}	V	VS drop Ta = 25 °C

Electrical Characteristics (Unless otherwise specified VCC = 15 V, Ta = -40 °C to +105 °C) - continued

Parameter	Symbol	Min	Typ	Max	Unit	Condition
[CS Block]						
CS Threshold Voltage	V_{CS}	1.3	1.5	1.8	V	
Output Delay Time	t_{DELAY}	-	150	300	ns	
CS Pin Pull-up Current	I_{CS}	-	0.15	1.00	µA	CS = 0 V
CS Offset Voltage	V_{OFFSET}	-	25	-	mV	MULT = 0 V
[OUT Block]						
OUT H Voltage	V_{POUTH}	9.0	10.2	11.4	V	OUT = -20 mA
OUT L Voltage	V_{POUTL}	-	-	0.8	V	OUT = +20 mA
Rise Time	tr	-	50	-	ns	OUT load capacitor = 1000 pF OUT L Voltage to 5 V
Fall Time	tf	-	50	-	ns	OUT load capacitor = 1000 pF OUT H Voltage to 5 V
OUT Pull-down Resistance	R_{PDOUT}	50	100	150	kΩ	

Typical Performance Curves
(Reference data)

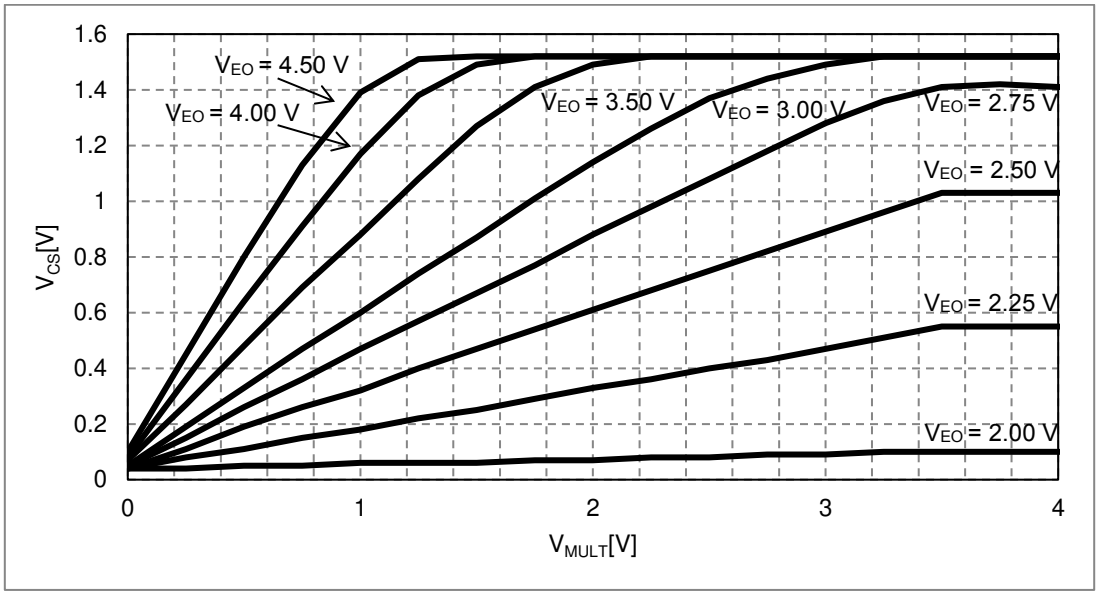


Figure 12. V_{CS} vs V_{MULT}

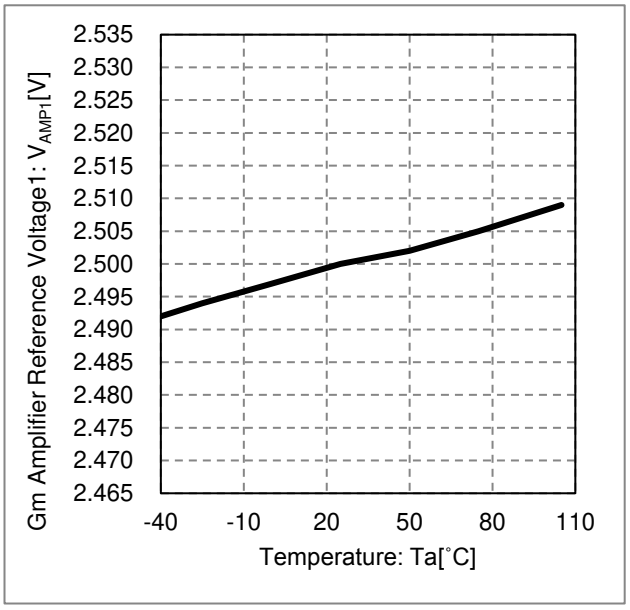


Figure 13. Gm Amplifier Reference Voltage1 vs Temperature

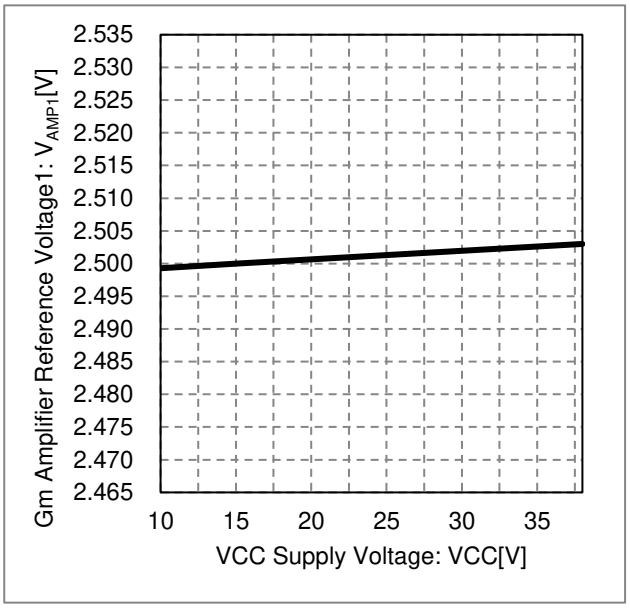


Figure 14. Gm Amplifier Reference Voltage1 vs VCC

Typical Performance Curves - continued

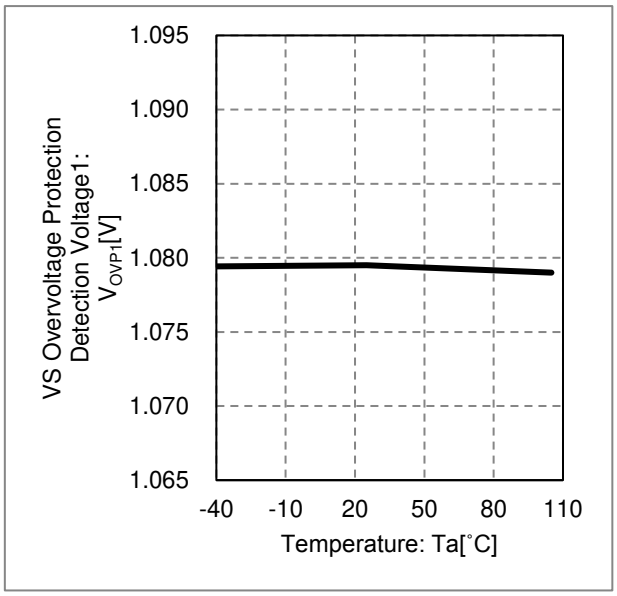


Figure 15. VS Overvoltage Protection Detection Voltage1 vs Temperature

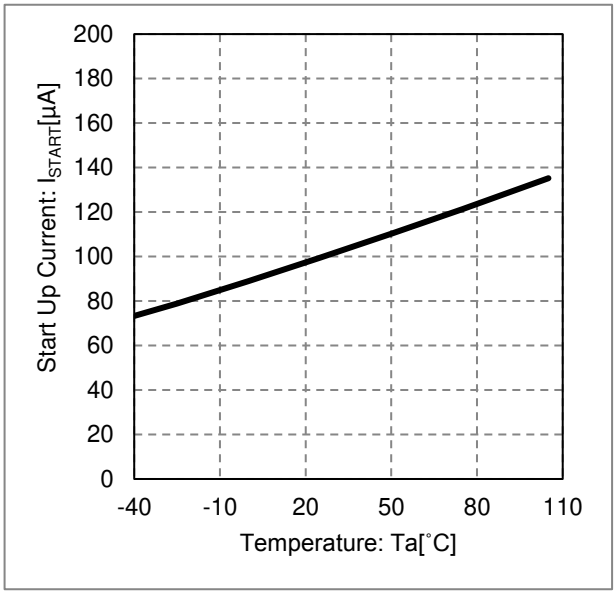


Figure 16. Start Up Current vs Temperature

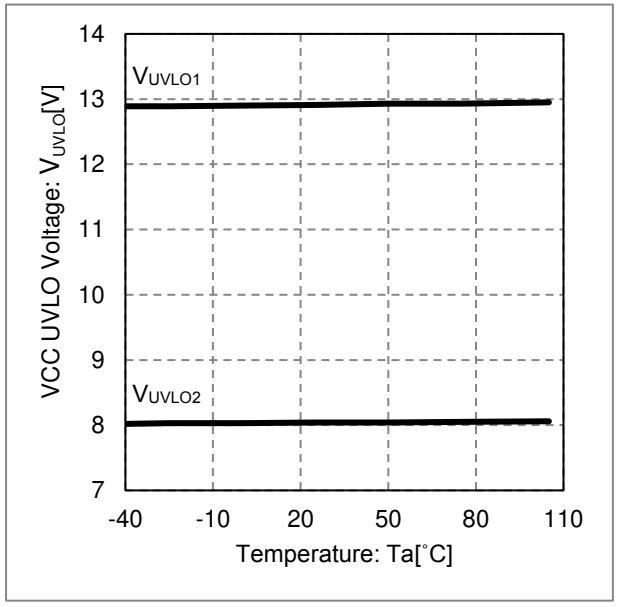


Figure 17. VCC UVLO Voltage vs Temperature

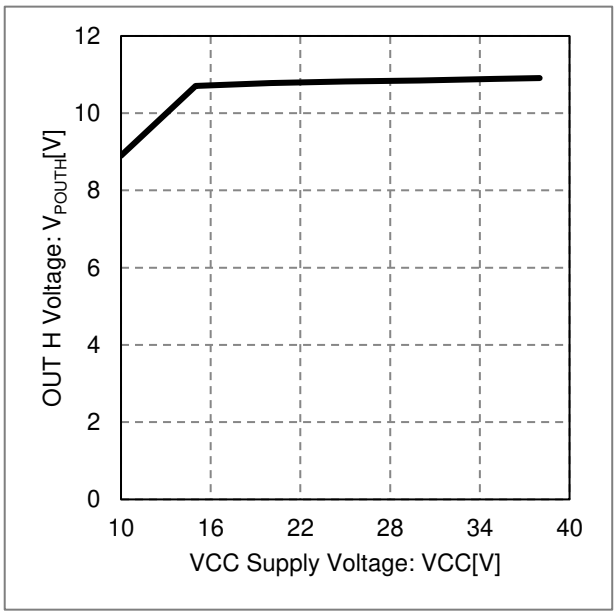


Figure 18. OUT H Voltage vs VCC

Application Example

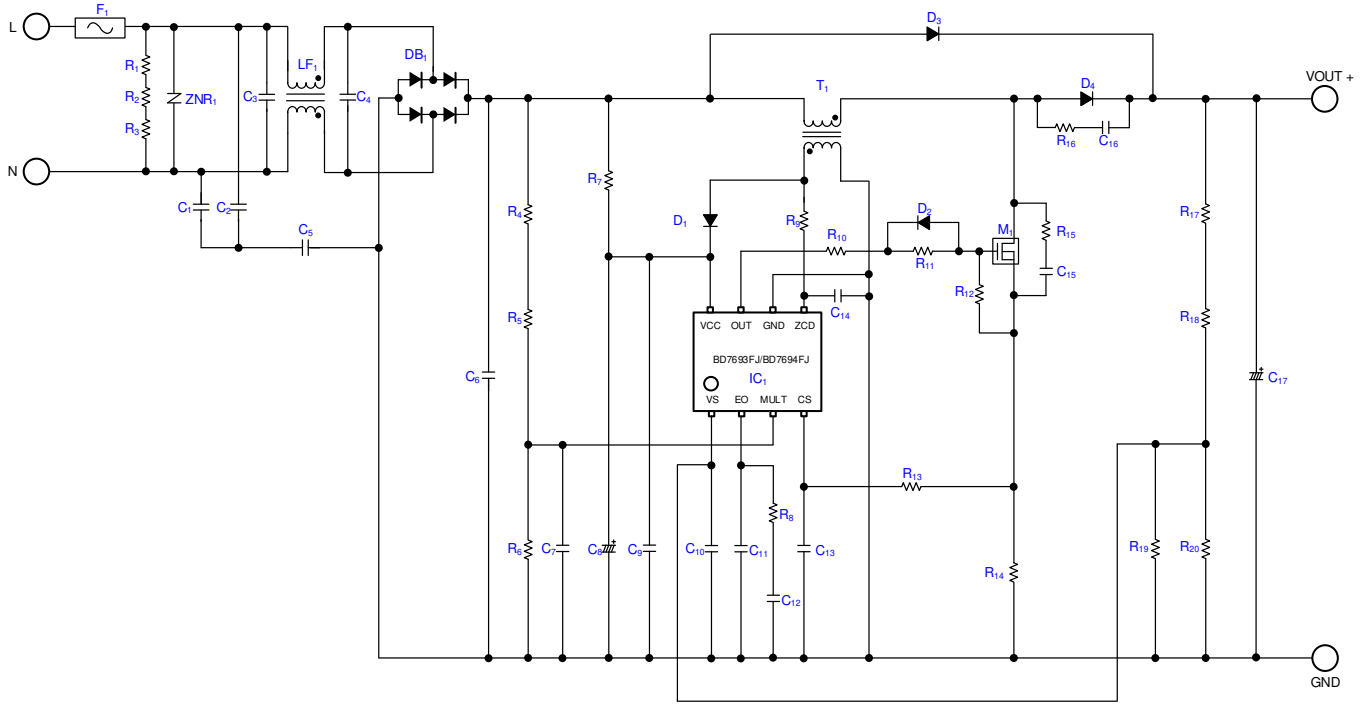


Figure 19. Application Example

1 Output Voltage Setting

The output voltage is decided on feedback resistance by the VS pin.

$$V_{OUT} = \left(1 + \frac{(R_{17}+R_{18})}{(R_{19}//R_{20})}\right) \times V_{AMP} = \left(1 + \frac{1582\ k\Omega}{10\ k\Omega}\right) \times 2.5\ V = 398\ \text{[V]}$$

$R_{17} + R_{18}$: Upper side resister of the output feedback
$R_{19}//R_{20}$: Bottom side resister of the output feedback
V_{AMP}: Gm amplifier reference voltage1

2 Calculation of the Inductance

Reference value in case of V_{OUT} = 400 V, Output power = 200 W

$$L = 250 \quad \text{[µH]}$$

Setting a large value of inductance will reduce the THD but increase the component size.

3 External Parts of VCC

The VCC pin can reduce VCC voltage change at the time of the switching by attaching capacitor.
This IC drives gate capacitor of the external MOSFET by the OUT pin. The VCC capacitor recommends electric field capacitor 22 µF or more withstand pressure 50 V or more.
In addition, you must confirm VCC voltage evaluation at the time of startup and the protection detection with an actual board when VCC is generated by startup resistance and the auxiliary winding of the transformer.
Because the consumption current of the IC decreases when an IC becomes the switching stop state after startup, the VCC voltage may rise by startup resistance. The overvoltage destruction of VCC is prevented by VCC voltage discharge function. The startup resistor value makes small by this function, boot-time becomes fast.

Attention in the Board Design

About parts placement

You must locate the parts in the Figure 20 inside dot line near the IC. In addition, please do parts placement to avoid the interference with switching lines and high current lines such as inductor, DRAIN.

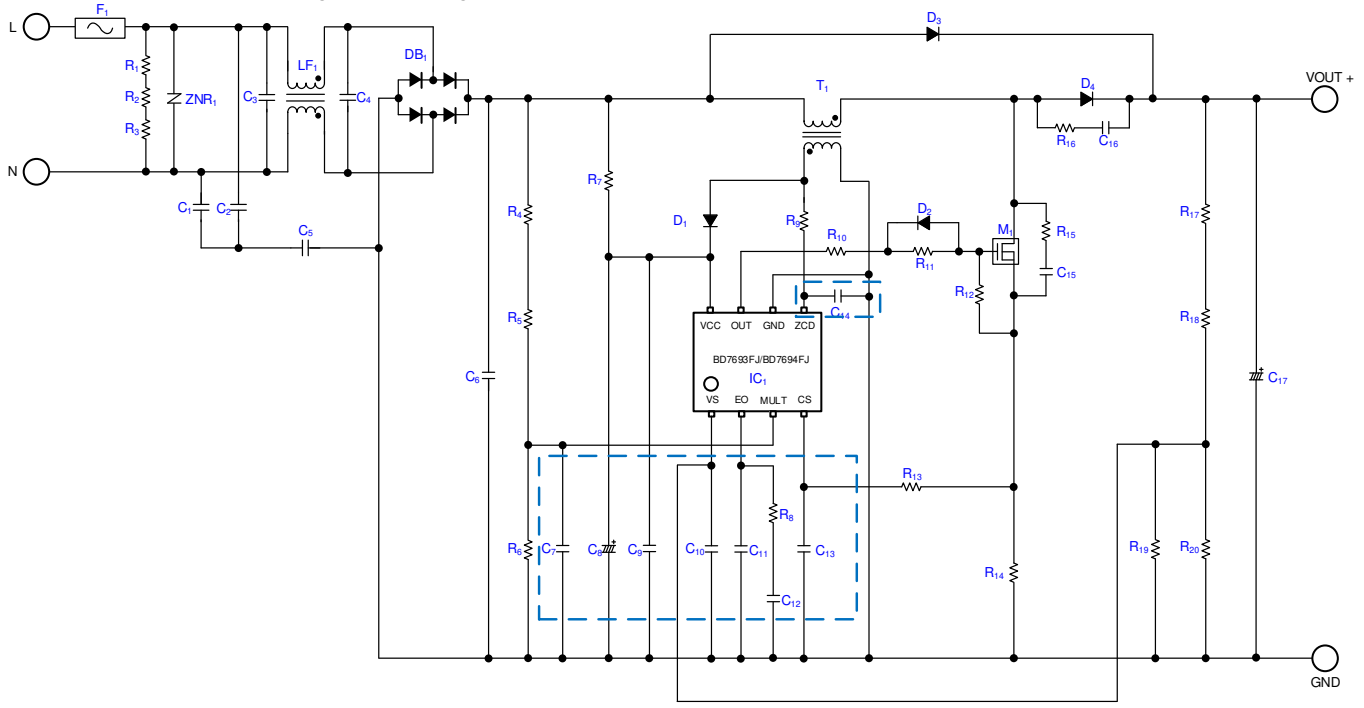


Figure 20. Parts Placement

About GND wiring guidance

The red line of Figure 21 is the GND lines which large current flows. Draw each line as an independent wire. In addition, pull the wiring thick and short. The blue line is the GND of the IC. Make the GND of the IC and the GND of the peripheral parts common.

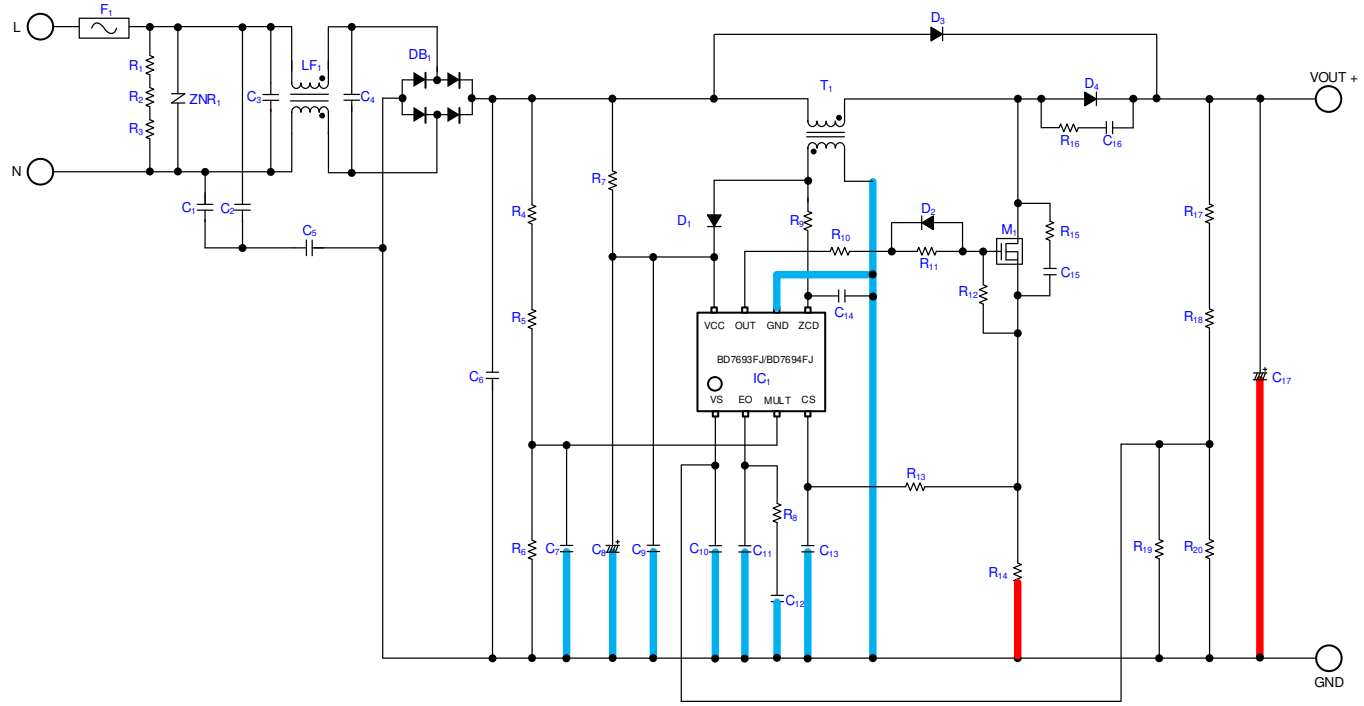


Figure 21. GND Line Layout

Attention in the Board – continued

About large current line
Large circuit current flows through the part of the red line of Figure 22. You must wire it short and thickly. Do not place IC and high impedance line near the red line because it has large noise.

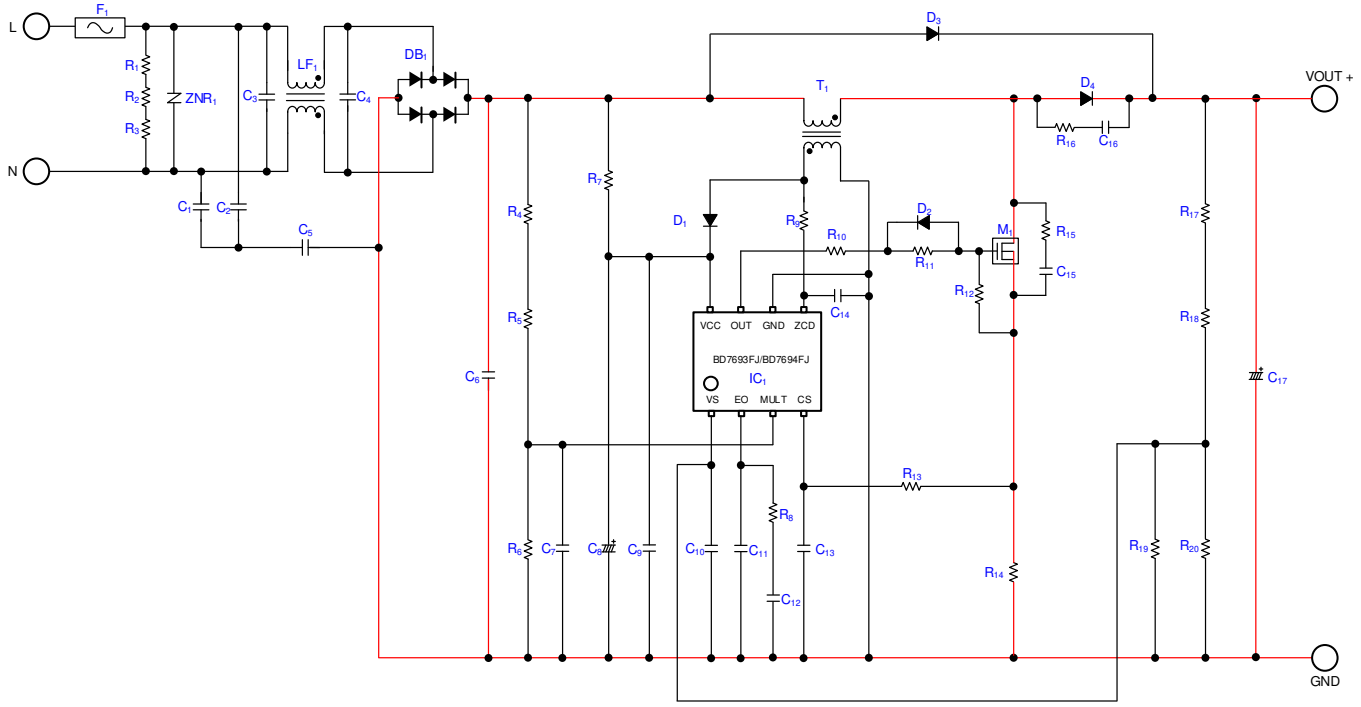
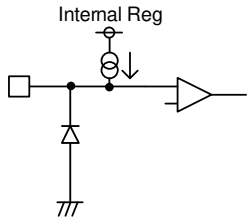
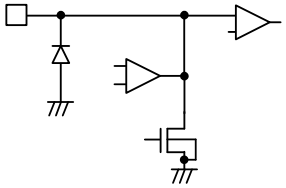
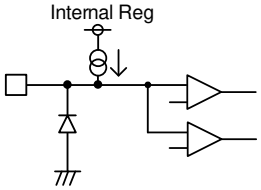
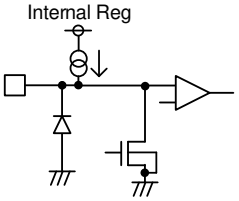
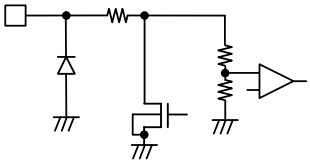
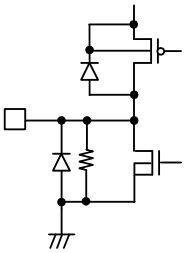
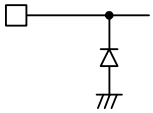


Figure 22. High Current Line Layout

I/O Equivalence Circuits

1 VS	2 EO	3 MULT	4 CS
			
5 ZCD	**6 GND**	**7 OUT**	**8 VCC**
			

Operational Notes

1. **Reverse Connection of Power Supply**
   Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

2. **Power Supply Lines**
   Design the PCB layout pattern to provide low impedance supply lines. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. **Ground Voltage**
   Except for pins the output and the input of which were designed to go below ground, ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

4. **Ground Wiring Pattern**
   When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. **Recommended Operating Conditions**
   The function and operation of the IC are guaranteed within the range specified by the recommended operating conditions. The characteristic values are guaranteed only under the conditions of each item specified by the electrical characteristics.

6. **Inrush Current**
   When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

7. **Testing on Application Boards**
   When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

8. **Inter-pin Short and Mounting Errors**
   Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

9. **Unused Input Pins**
   Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

Operational Notes – continued

10. Regarding the Input Pin of the IC

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode.
When GND > Pin B, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.

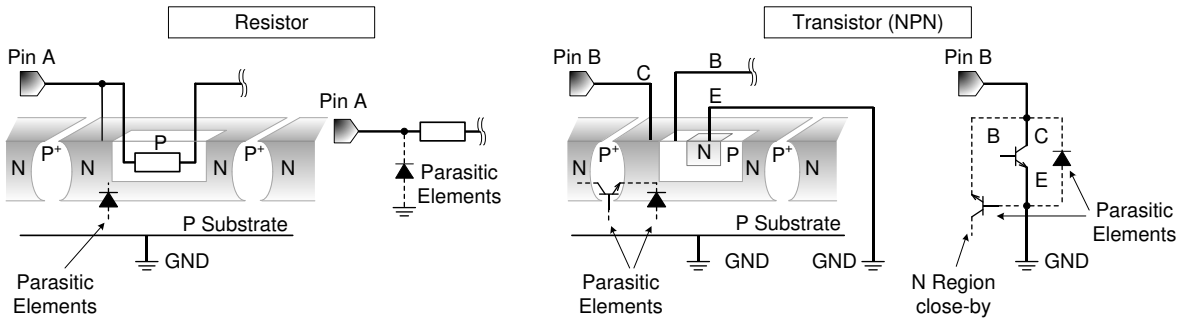


Figure 23. Example of Monolithic IC Structure

11. Ceramic Capacitor

When using a ceramic capacitor, determine a capacitance value considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

12. Thermal Shutdown Circuit (TSD)

This IC has a built-in thermal shutdown circuit that prevents heat damage to the IC. Normal operation should always be within the IC's maximum junction temperature rating. If however the rating is exceeded for a continued period, the junction temperature (Tj) will rise which will activate the TSD circuit that will turn OFF power output pins. When the Tj falls below the TSD threshold, the circuits are automatically restored to normal operation.
Note that the TSD circuit operates in a situation that exceeds the absolute maximum ratings and therefore, under no circumstances, should the TSD circuit be used in a set design or for any purpose other than protecting the IC from heat damage.

13. Over Current Protection Circuit (OCP)

This IC incorporates an integrated overcurrent protection circuit that is activated when the load is shorted. This protection circuit is effective in preventing damage due to sudden and unexpected incidents. However, the IC should not be used in applications characterized by continuous operation or transitioning of the protection circuit.

Ordering Information

B	D	7	6	9	x	F	J	-	E 2

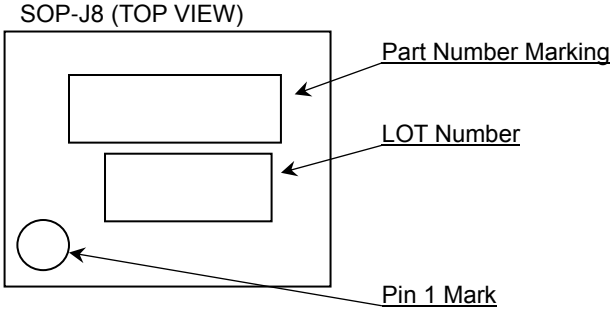
x: Brown Out / 3: None- / 4: With

Package: FJ: SOP-J8

Packaging and forming specification: E2: Embossed tape and reel

Marking Diagram

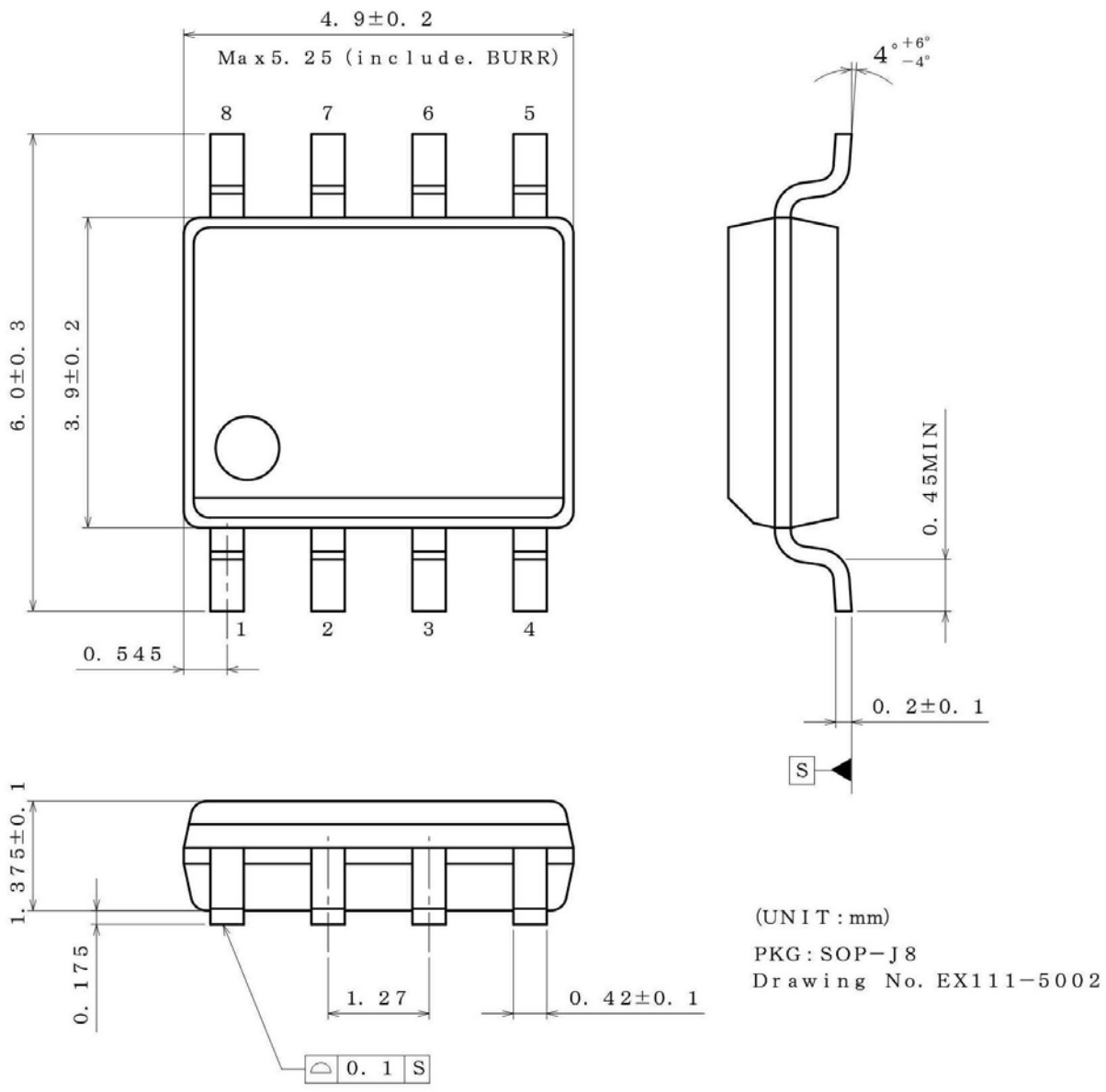
SOP-J8 (TOP VIEW)



Product name	Part Number Marking
BD7693FJ-E2	D7693
BD7694FJ-E2	D7694

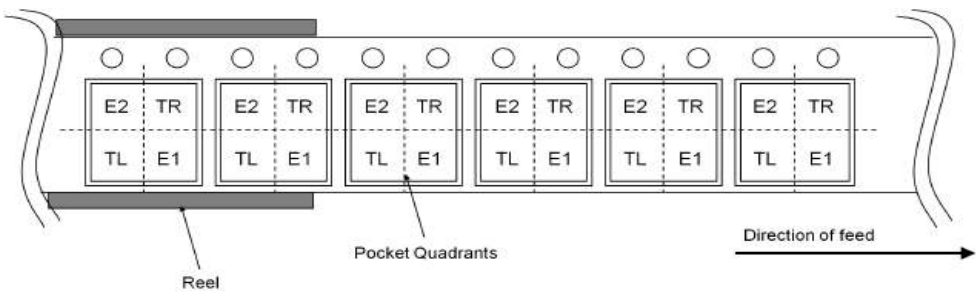
Physical Dimension and Packing Information

Package Name	SOP-J8



<Tape and Reel information>

Tape	Embossed carrier tape
Quantity	2500pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



Revision History

Date	Revision	Changes
25.Nov.2020	001	New Release

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(Note1) Medical Equipment Classification of the Specific Applications

JAPAN	USA	EU	CHINA
CLASSⅢ	CLASSⅢ	CLASSⅡb	CLASSⅢ
CLASSⅣ		CLASSⅢ	

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   [b] Use of our Products outdoors or in places where the Products are exposed to direct sunlight or dust
   [c] Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   [d] Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
   [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
   [f] Sealing or coating our Products with resin or other coating materials
   [g] Use of our Products without cleaning residue of flux (Exclude cases where no-clean type fluxes is used. However, recommend sufficiently about the residue.) ; or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
   [h] Use of the Products in places subject to dew condensation

4. The Products are not subject to radiation-proof design.

5. Please verify and confirm characteristics of the final or mounted products in using the Products.

6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse, is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.

7. De-rate Power Dissipation depending on ambient temperature. When used in sealed area, confirm that it is the use in the range that does not exceed the maximum junction temperature.

8. Confirm that operation temperature is within the specified range described in the product specification.

9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

Precaution for Mounting / Circuit board design

1. When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.

2. In principle, the reflow soldering method must be used on a surface-mount products, the flow soldering method must be used on a through hole mount products. If the flow soldering method is preferred on a surface-mount products, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

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This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of Ionizer, friction prevention and temperature / humidity control).

Precaution for Storage / Transportation

1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
   [a] the Products are exposed to sea winds or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   [b] the temperature or humidity exceeds those recommended by ROHM
   [c] the Products are exposed to direct sunshine or condensation
   [d] the Products are exposed to high Electrostatic

2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.

3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.

4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

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