

# FDD5N50U

## N-Channel UniFET™ Ultra FRFET™ MOSFET 500 V, 3 A, 2.0 Ω

### Features

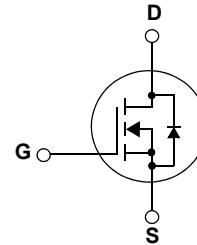
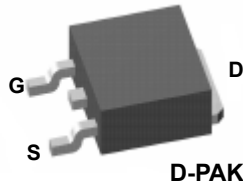
- $R_{DS(on)} = 1.65 \Omega$  (Typ.) @  $V_{GS} = 10 V$ ,  $I_D = 1.5 A$
- Low gate charge (Typ. 11 nC)
- Low  $C_{rss}$  (Typ. 5 pF)
- 100% avalanche tested
- RoHS compliant

### Applications

- LCD/LED/PDP TV
- Lighting
- Uninterruptible Power Supply

### Description

UniFET™ MOSFET is Fairchild Semiconductor®'s high voltage MOSFET family based on planar stripe and DMOS technology. This MOSFET is tailored to reduce on-state resistance, and to provide better switching performance and higher avalanche energy strength. UniFET™ Ultra FRFET™ MOSFET has much superior body diode reverse recovery performance. Its  $t_{rr}$  is less than 50nsec and the reverse  $dv/dt$  immunity is 20V/nsec while normal planar MOSFETs have over 200nsec and 4.5V/nsec respectively. Therefore UniFET Ultra FRFET MOSFET can remove additional component and improve system reliability in certain applications that require performance improvement of the MOSFET's body diode. This device family is suitable for switching power converter applications such as power factor correction (PFC), flat panel display (FPD) TV power, ATX and electronic lamp ballasts.



### MOSFET Maximum Ratings $T_C = 25^\circ C$ unless otherwise noted\*

Symbol	Parameter	FDD5N50U	Unit
$V_{DSS}$	Drain to Source Voltage	500	V
$V_{GSS}$	Gate to Source Voltage	±30	V
$I_D$	Drain Current	- Continuous ( $T_C = 25^\circ C$ )	3
		- Continuous ( $T_C = 100^\circ C$ )	1.8
$I_{DM}$	Drain Current	- Pulsed (Note 1)	12
$E_{AS}$	Single Pulsed Avalanche Energy	(Note 2)	275
$I_{AR}$	Avalanche Current	(Note 1)	3
$E_{AR}$	Repetitive Avalanche Energy	(Note 1)	4
$dv/dt$	Peak Diode Recovery $dv/dt$	(Note 3)	4.5
$P_D$	Power Dissipation	( $T_C = 25^\circ C$ )	40
		- Derate above $25^\circ C$	0.3
$T_J, T_{STG}$	Operating and Storage Temperature Range	-55 to +150	$^\circ C$
$T_L$	Maximum Lead Temperature for Soldering Purpose, 1/8" from Case for 5 Seconds	300	$^\circ C$

### Thermal Characteristics

Symbol	Parameter	FDD5N50U	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case, Max.	1.4	$^\circ C/W$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient, Max.	110	

## Package Marking and Ordering Information $T_C = 25^\circ\text{C}$ unless otherwise noted

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDD5N50U	FDD5N50UTM	D-PAK	380mm	16mm	2500
FDD5N50U	FDD5N50UTM_WS	D-PAK	380mm	16mm	2500
FDD5N50U	FDD5N50UTF	D-PAK	380mm	16mm	2000

## Electrical Characteristics

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
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### Off Characteristics

$BV_{DSS}$	Drain to Source Breakdown Voltage	$I_D = 250\mu\text{A}, V_{GS} = 0\text{V}, T_J = 25^\circ\text{C}$	500	-	-	V
$\Delta BV_{DSS} / \Delta T_J$	Breakdown Voltage Temperature Coefficient	$I_D = 250\mu\text{A}$ , Referenced to $25^\circ\text{C}$	-	0.6	-	$V/^\circ\text{C}$
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 500\text{V}, V_{GS} = 0\text{V}$ $V_{DS} = 400\text{V}, T_C = 125^\circ\text{C}$	-	-	25 250	$\mu\text{A}$
$I_{GSS}$	Gate to Body Leakage Current	$V_{GS} = \pm 30\text{V}, V_{DS} = 0\text{V}$	-	-	$\pm 100$	nA

### On Characteristics

$V_{GS(th)}$	Gate Threshold Voltage	$V_{GS} = V_{DS}, I_D = 250\mu\text{A}$	3	-	5	V
$R_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 10\text{V}, I_D = 1.5\text{A}$	-	1.65	2	$\Omega$
$g_{FS}$	Forward Transconductance	$V_{DS} = 20\text{V}, I_D = 1.5\text{A}$	-	4	-	S

### Dynamic Characteristics

$C_{iss}$	Input Capacitance	$V_{DS} = 25\text{V}, V_{GS} = 0\text{V}$ $f = 1\text{MHz}$	-	485	650	pF
$C_{oss}$	Output Capacitance		-	65	90	pF
$C_{rss}$	Reverse Transfer Capacitance		-	5	8	pF
$Q_{g(tot)}$	Total Gate Charge at 10V	$V_{DS} = 400\text{V}, I_D = 5\text{A}$ $V_{GS} = 10\text{V}$	-	11	15	nC
$Q_{gs}$	Gate to Source Gate Charge		-	3	-	nC
$Q_{gd}$	Gate to Drain "Miller" Charge		-	5	-	nC

(Note 4)

### Switching Characteristics

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 250\text{V}, I_D = 5\text{A}$ $R_G = 25\Omega$	-	14	38	ns
$t_r$	Turn-On Rise Time		-	21	52	ns
$t_{d(off)}$	Turn-Off Delay Time		-	27	64	ns
$t_f$	Turn-Off Fall Time		-	20	50	ns

(Note 4)

### Drain-Source Diode Characteristics

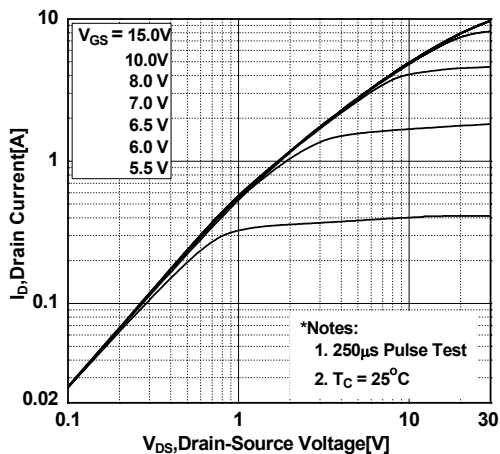
$I_S$	Maximum Continuous Drain to Source Diode Forward Current	-	-	3	A	
$I_{SM}$	Maximum Pulsed Drain to Source Diode Forward Current	-	-	12	A	
$V_{SD}$	Drain to Source Diode Forward Voltage	$V_{GS} = 0\text{V}, I_{SD} = 3\text{A}$	-	-	1.6	V
$t_{rr}$	Reverse Recovery Time	$V_{GS} = 0\text{V}, I_{SD} = 5\text{A}$	-	36	-	ns
$Q_{rr}$	Reverse Recovery Charge	$di_F/dt = 100\text{A}/\mu\text{s}$	-	33	-	nC

#### Notes:

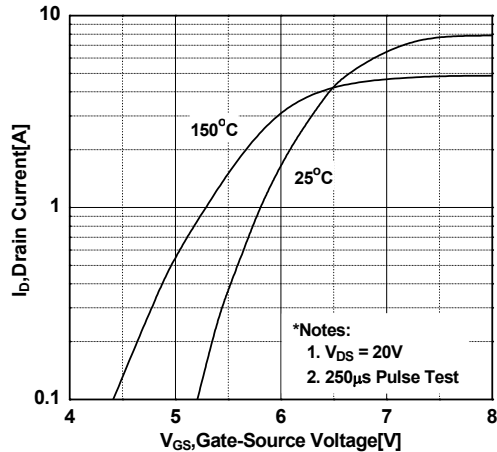
- 1: Repetitive Rating: Pulse width limited by maximum junction temperature
- 2:  $L = 61\text{mH}, I_{AS} = 3\text{A}, V_{DD} = 50\text{V}, R_G = 25\Omega$ , Starting  $T_J = 25^\circ\text{C}$
- 3:  $I_{SD} \leq 3\text{A}, di/dt \leq 200\text{A}/\mu\text{s}, V_{DD} \leq BV_{DSS}$ , Starting  $T_J = 25^\circ\text{C}$
- 4: Essentially Independent of Operating Temperature Typical Characteristics

## Typical Performance Characteristics

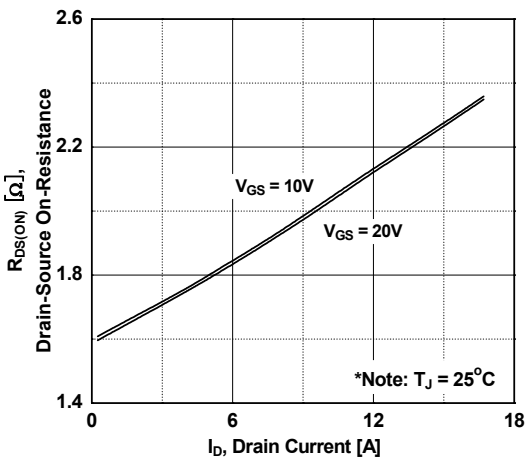
**Figure 1. On-Region Characteristics**



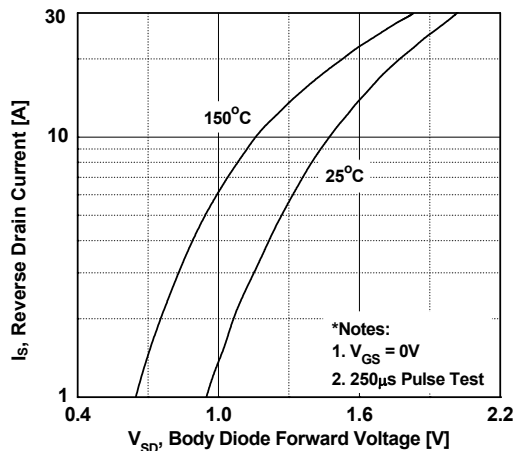
**Figure 2. Transfer Characteristics**



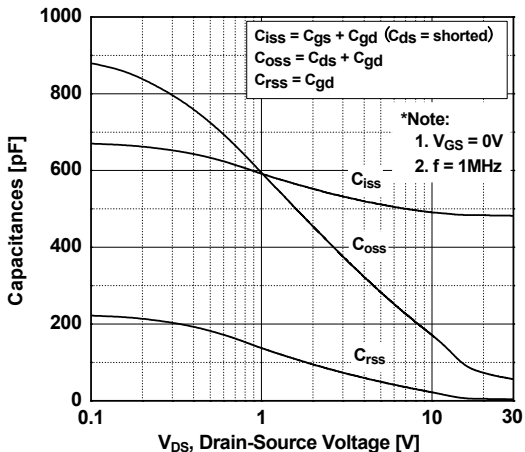
**Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage**



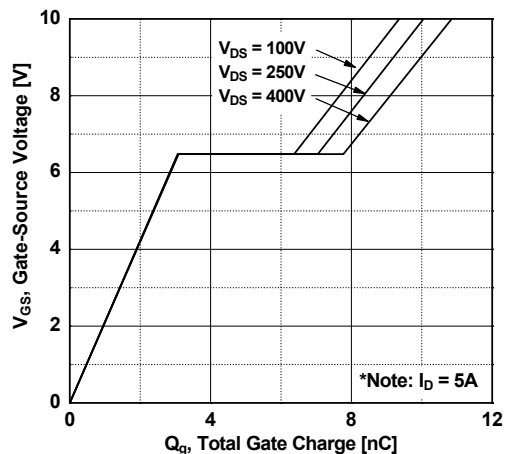
**Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature**



**Figure 5. Capacitance Characteristics**



**Figure 6. Gate Charge Characteristics**



Typical Performance Characteristics (Continued)

Figure 7. Breakdown Voltage Variation vs. Temperature

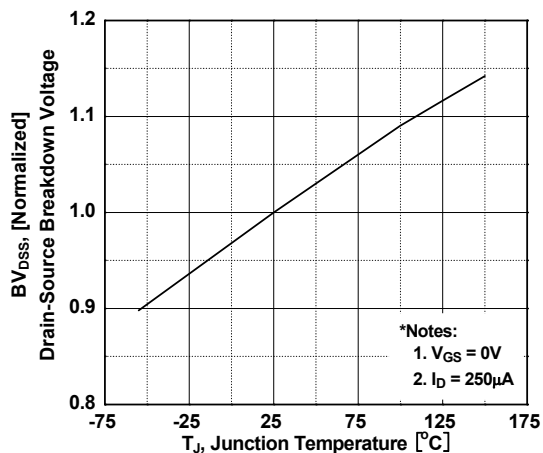


Figure 8. Maximum Safe Operating Area

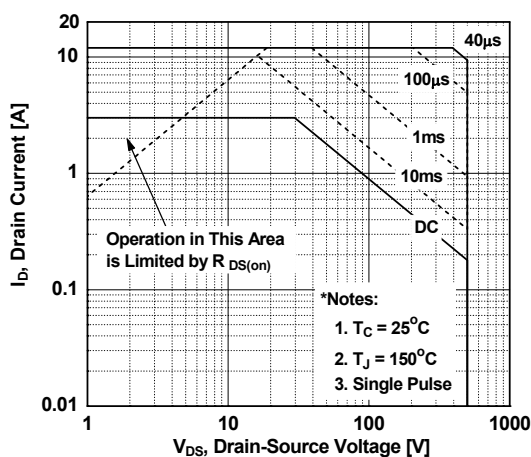


Figure 9. Maximum Drain Current vs. Case Temperature

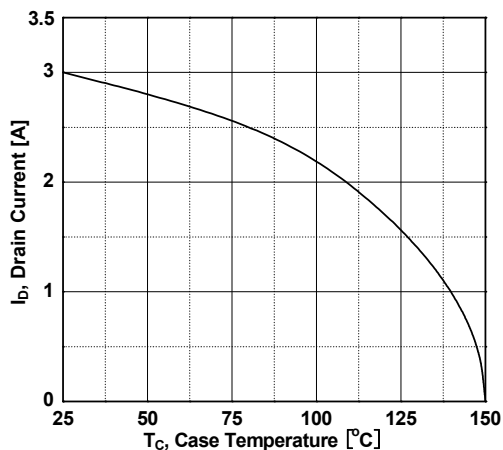
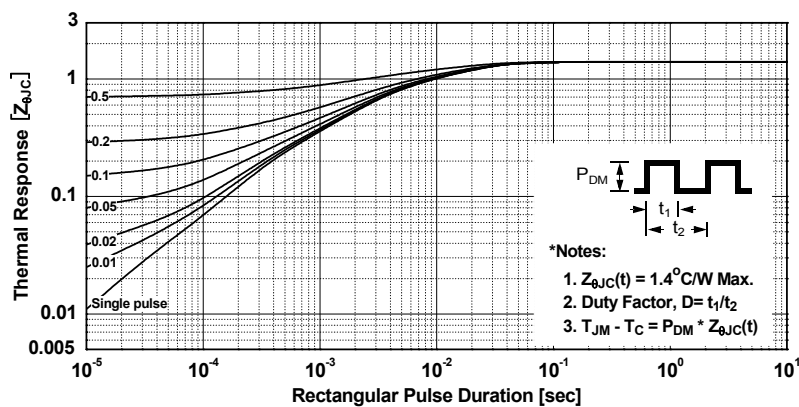


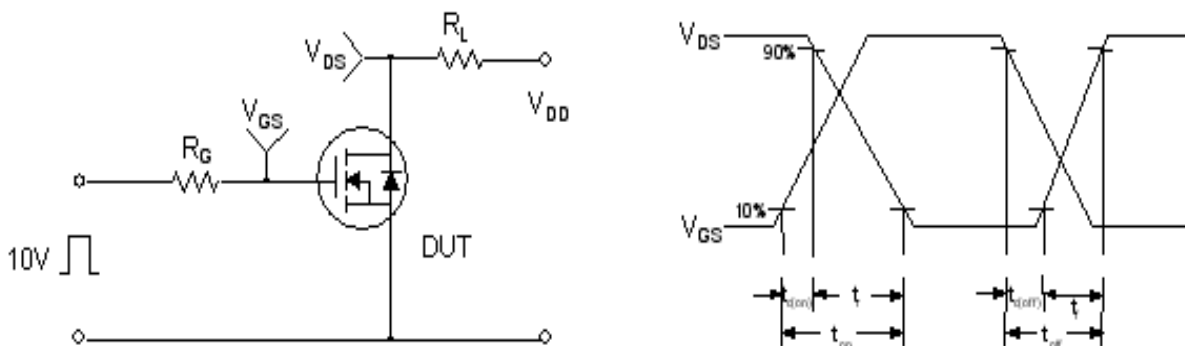
Figure 10. Transient Thermal Response Curve



**Gate Charge Test Circuit & Waveform**



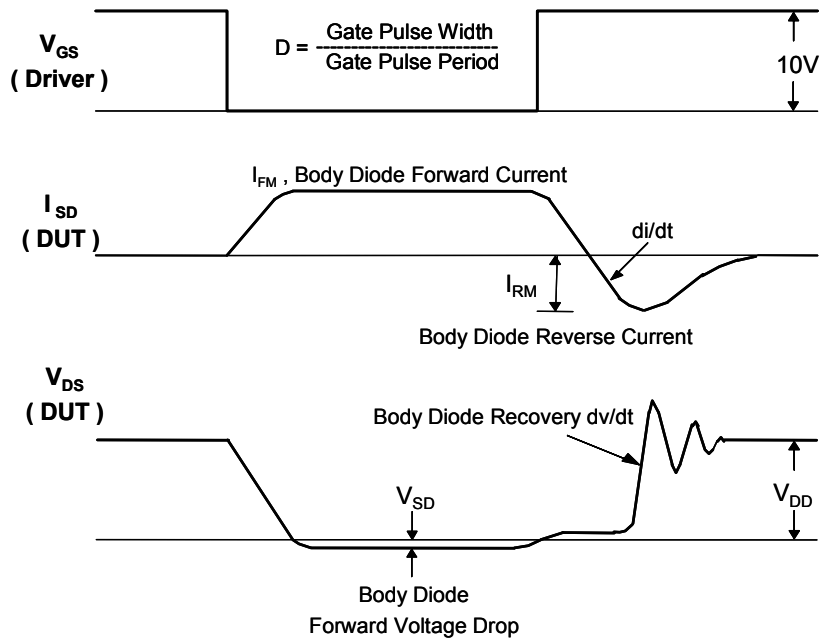
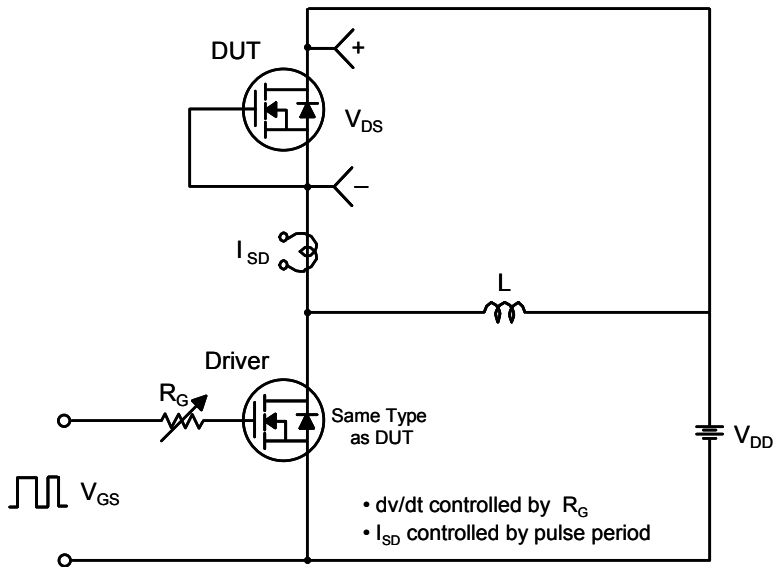
**Resistive Switching Test Circuit & Waveforms**



**Unclamped Inductive Switching Test Circuit & Waveforms**

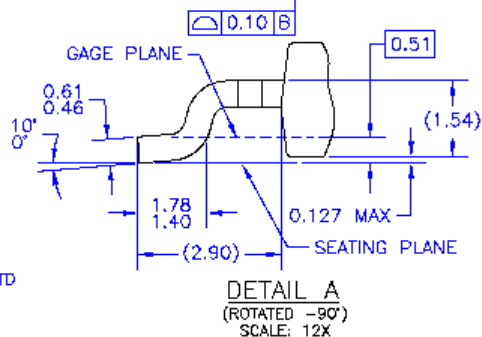
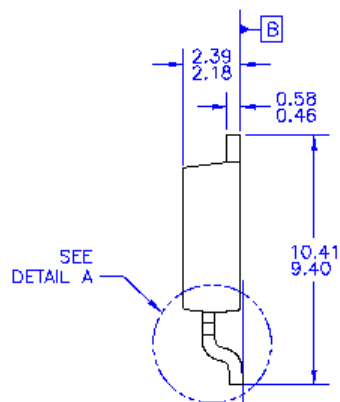
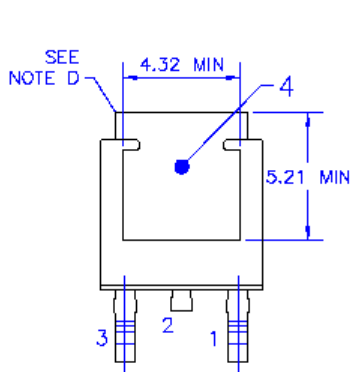
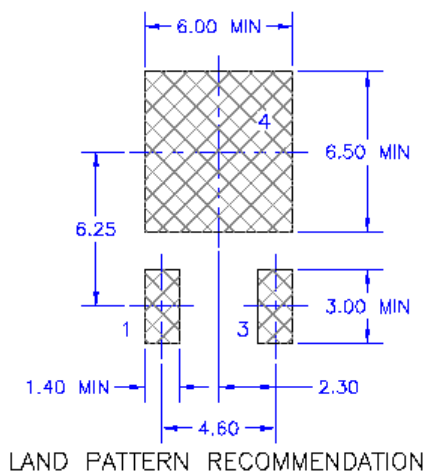
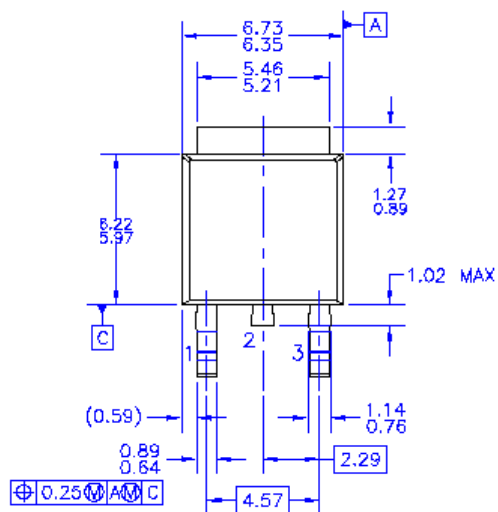


Peak Diode Recovery dv/dt Test Circuit & Waveforms



## Mechanical Dimensions

### D-PAK



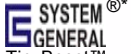




- NOTES: UNLESS OTHERWISE SPECIFIED
- A) THIS PACKAGE CONFORMS TO JEDEC, TO-252, ISSUE C, VARIATION AA.
  - B) ALL DIMENSIONS ARE IN MILLIMETERS.
  - C) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
  - D) HEAT SINK TOP EDGE COULD BE IN CHAMFERED CORNERS OR EDGE PROTRUSION.
  - E) PRESENCE OF TRIMMED CENTER LEAD IS OPTIONAL.
  - F) DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH AND TIE BAR EXTRUSIONS.
  - G) LAND PATTERN RECOMMENDATION IS BASED ON IPC7351A STD TO22DP1003X238-3N.
  - H) DRAWING NUMBER AND REVISION: MKT-TO252A03REV8

Dimensions in Millimeters



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