AFBR-7QERxxZ

40 Gigabit Ethernet & InfiniBand QDR
QSFP+ Pluggable, Parallel Active Optical Cable

Data Sheet

Description

The Avago Technologies AFBR-7QERxxZ is a Four-Channel, Pluggable, Parallel, Fiber-Optic QSFP+ Active Optical Cable (AOC) solution for 40 Gigabit Ethernet Applications. This AOC is a high performance cable for short-range multi-lane data communication and interconnect applications. It integrates four data lanes in each direction with 40 Gbps aggregate bandwidth. Each lane can operate at 10.3125 Gbps. These cables also support 4 × 10G InfiniBand QDR applications and are backwards compatible to the 4 × 5G IB DDR and 4 × 2.5G IB single IB SDR applications.

These Active Optical Cables operate over multimode fiber systems using a nominal wavelength of 850 nm. The electrical interface uses a 38 contact edge type connector. This AOC incorporates Avago Technologies proven integrated circuit and VCSEL technology to provide reliable long life, high performance, and consistent service.

Part Number

40 Gigabit Ethernet & InfiniBand QDR	AFBR-7QERxxZ
40GbE QSFP+ to 4× 10GbE SFP+ Breakout AOC	AFBR-7IERxxZ

Where xx = cable length in meters

For specifications pertaining to the SFP+ Active Cable-end see AV02-2948EN AFBR-7CERxxZ SFP+ Active Optical Cable (AOC) Datasheet

Evaluation Board	AFBR-79Q4EKZ*
Evaluation Kit	AFBR-79Q2EKZ**

* Includes GUI and User Guide
** Includes GUI, User Guide, i-Port and Power Supply

Note: Two evaluation boards are needed to run the bi-directional QSFP+ Active Cable Assembly

Features

- Compliant to the 40GBASE-SR4 and XLPPI Specification per IEEE 802.3ba-2010 and supporting 40G-IB-QDR/ 20G-IB-DDR/10G-IB-SDR applications
- Compliant to the industry standard SFF-8436 QSFP+ Specification
- Power Level 1: Max Power < 1.5 W
- High port density: 21 mm horizontal port pitch
- Operate at 10.3125 Gbps per channel with 64b/66b encoded data for 40GbE application and at 10 Gbps with 8b/10b compatible encoded data for 40G-IB-QDR application
- 0 to 70 °C case temperature operating range
- Proven High Reliability 850 nm technology: Avago VCSEL transmitter and Avago PIN receiver
- Hot pluggable for ease of servicing and installation
- Two Wire Serial (TWS) interface
- Utilizes optical fiber for high density and thin, lightweight cable management

Applications

- 40GbE and 40G-IB-QDR / 20G-IB-DDR / 10G-IB-SDR interconnects
- Datacom/Telecom switch and router connections
- Data aggregation and backplane applications
- Proprietary protocol and density applications

Part Number	Description
AFBR-7QER01Z	1 m QSFP+ Active Optical Cable
AFBR-7QER02Z	2 m QSFP+ Active Optical Cable
AFBR-7QER03Z	3 m QSFP+ Active Optical Cable
AFBR-7QER05Z	5 m QSFP+ Active Optical Cable
AFBR-7QER07Z	7 m QSFP+ Active Optical Cable
AFBR-7QER10Z	10 m QSFP+ Active Optical Cable
AFBR-7QER15Z	15 m QSFP+ Active Optical Cable
AFBR-7QER20Z	20 m QSFP+ Active Optical Cable

Transmitter

The optical transmitter portion of the AOC (see Figure 1) incorporates 4 VCSELs (Vertical Cavity Surface Emitting Laser), input buffer and laser drivers and control & bias blocks. The transmitter is designed for EN 60825 and CDRH eye safety compliance; Class 1M out of the module. The Tx Input Buffer provides CML compatible differential inputs presenting a nominal differential input impedance of 100 ohms. AC coupling capacitors are located inside the QSFP+ AOC and are not required on the host board. For AOC interrogation, the control interface (LVTTL compatible) incorporates a Two Wire Serial (TWS) interface of clock and data signals. Tx_Disable is available through the TWS interface.

Receiver

The optical receiver portion of the Active Cable-end (see Figure 1) incorporates 4 PIN photodiodes, TIAs, channel output buffer and control & bias blocks. The Rx Output Buffer provides CML compatible differential outputs for the high speed electrical interface presenting nominal single-ended output impedances of 50 ohms to AC ground and 100 ohms differentially that should be differentially terminated with 100 ohms. AC coupling capacitors are located inside the QSFP+ and are not required on the host board. For AOC interrogation and control, the control interface (LVTTL compatible) incorporates a Two Wire Serial (TWS) interface of clock and data signals. Rx_LOS and Rx Squelch are available through the TWS interface.

Flags are set and interrupts generated for Rx loss of optical input signal (LOS). Flags are latched and will remain set even if the condition initiating the flag clears and operation resumes. Interrupts can be masked and flags are reset upon reading the appropriate flag register. The electrical output will squelch for loss of input signal (unless squelch is disabled). To reduce the need for polling, the hardware interrupt signal is provided to inform hosts of an assertion of Rx LOS.

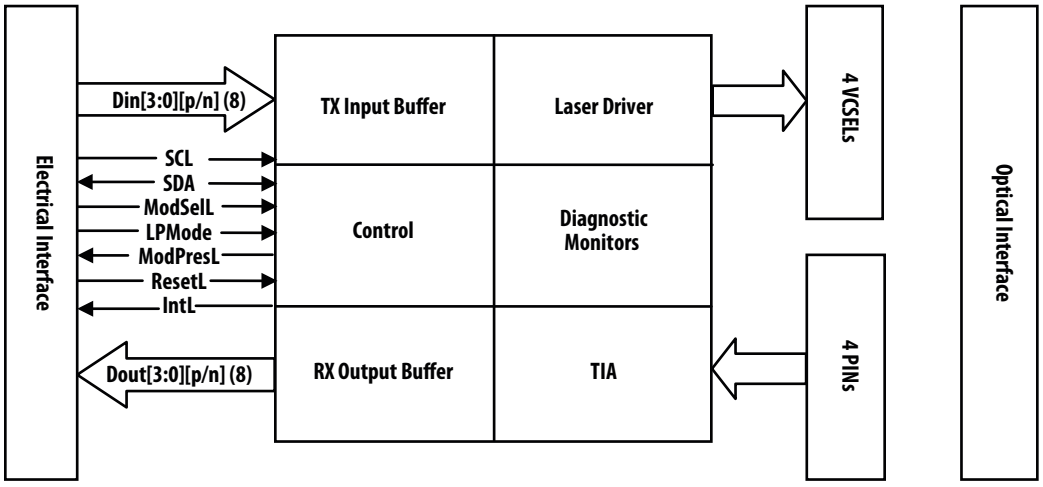


Figure 1. Active Optical Cable Diagram – Active components

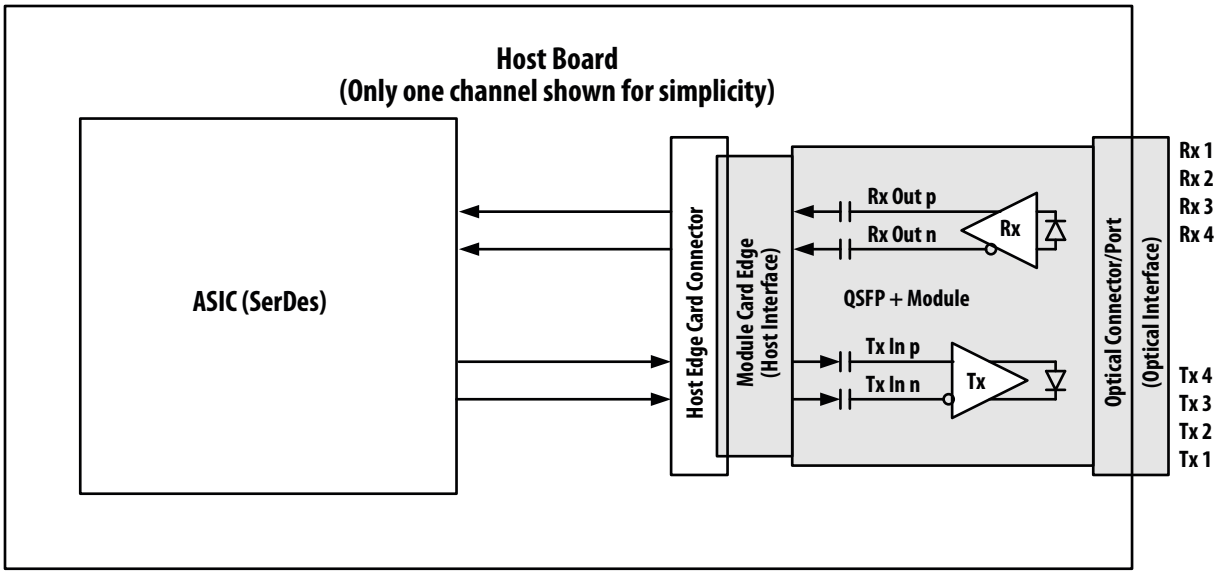


Figure 2. Application Reference Diagram

Control Signal Interface

The module has the following low speed signals for control and status: ModSelL, LPMode, ResetL, ModPrsL, IntL. In addition, there is an industry standard two wire serial interface scaled for 3.3 volt LVTTL. It is implemented as a slave device. Signals and timing characteristics are further defined in the Control Interface section. The registers of the serial interface memory are defined in the Memory Map section and corresponding Avago Technologies QSFP+ Memory Map document

High Speed Signal Interface

Figure 2 shows the interface between an ASIC/SerDes and the QSFP+ AOC. For simplicity, only one channel is shown. The high speed signal lines are AC-coupled 100 ohm differential lines. The AC coupling is inside the QSFP+ AOC and not required on the host board. The 100 ohm differential terminations are inside the QSFP+ AOC for the transmitter lines and at the host ASIC/SerDes for the receiver lines. All transmitter and receiver electrical channels are compliant to module XLPPI specifications per IEEE 802.3ba.

Regulatory & Compliance Issues

Various standards and regulations apply to the cables. These include eye-safety, EMC, ESD and RoHS. See the Regulatory Section for details, including component recognition. Please note the transmitter is a Class 1M laser product – In the event of fiber breakage, DO NOT VIEW RADIATION DIRECTLY WITH OPTICAL INSTRUMENTS. See Regulatory Compliance Table for details.

Package Outline

The module is designed to meet the package outline defined in the SFF-8436 Specification for QSFP+ Optical Modules. See the package outline and host board footprint figures (Figures 10 – 13) for details.

Handling and Cleaning

The Active Cable-end can be damaged by exposure to current surges and over voltage events. Care should be taken to restrict exposure to the conditions defined in the Absolute Maximum Ratings. Wave soldering, reflow soldering and/or aqueous wash process with the modules on board are not recommended. Normal handling precautions for electrostatic discharge sensitive devices should be observed.

Absolute Maximum Ratings

Stress in excess of any of the individual Absolute Maximum Ratings can cause immediate catastrophic damage to the AOC even if all other parameters are within Recommended Operation Conditions. It should not be assumed that limiting values of more than one parameter can be applied to the AOC concurrently. Exposure to any of the Absolute Maximum Ratings for extended periods can adversely affect reliability.

Parameter	Symbol	Min	Max	Units	Reference
Storage Temperature	Ts	-40	85	°C	
3.3 V Power Supply Voltage	Vcc	-0.5	3.6	V	
Data Input Voltage – Single Ended		-0.5	4	V	
Data Input Voltage – Differential	$\lvert V_{dip} - V_{din} \rvert$		1.0	V	1
Control Input Voltage	Vi	-0.5	Vcc+0.5, 3.6	V	
Control Output Current	Io	-20	20	mA	
Relative Humidity	RH	5	95	%	

Note:
1. This is the maximum voltage that can be applied across the differential inputs without damaging the input circuitry.

Recommended Operating Conditions

Recommended Operating Conditions specify parameters for which the electrical characteristics hold unless otherwise noted. Electrical characteristics are not defined for operation outside the Recommended Operating Conditions, reliability is not implied and damage to the module may occur for such operation over an extended period of time.

Parameter	Symbol	Min	Typ	Max	Units	Reference
Case Temperature	Tc	0	40	70	°C	1
3.3 V Power Supply Voltage	Vcc	3.135	3.3	3.465	V	
Signal Rate per Channel			10.3125		GBd	2
Control* Input Voltage High	Vih	2		Vcc+0.3	V	
Control* Input Voltage Low	Vil	-0.3		0.8	V	
Two Wire Serial (TWS) Interface Clock Rate				400	kHz	
Power Supply Noise				50	mVpp	3
Receiver Differential Data Output Load			100		ohms	

* Control signals, LVTTL (3.3 V) compatible

Notes:
1. The position of case temperature measurement is shown in Figure 7.
2. 64b/66b coding is assumed
3. Power Supply Noise is defined as the peak-to-peak noise amplitude over the frequency range at the host supply side of the recommended power supply filter with the module and recommended filter in place. Voltage levels including peak-to-peak noise are limited to the recommended operating range of the associated power supply. See Figure 8 for recommended power supply filter.

Active Cable-End Electrical Characteristics*

The following characteristics are defined over the Recommended Operating Conditions unless otherwise noted. Typical values are for Tc = 40° C, Vcc = 3.3 V

Parameter	Symbols	Min	Typ	Max	Units	Reference
10G Active Cable-End Power Consumption				1.5	W	
10G Active Cable-End Power Supply Current				475	mA	

* See Figure 6 for Test Point definitions.

Transmitter Electrical Characteristics

The following characteristics are defined over the Recommended Operating Conditions unless otherwise noted. Typical values are for Tc = 40° C, Vcc33 = 3.3 V

Parameter (From Table 86A-2 of IEEE 802.3ba)	Test Point	Min	Typ	Max	Units	Notes/Conditions
Single ended input voltage tolerance [1]	TP1a	-0.3		4	V	Referred to TP1 signal common
AC common mode input voltage tolerance	TP1a	15			mV	RMS
Differential input return loss	TP1	See IEEE 802.3ba 86A.4.1.1			dB	10 MHz to 11.1 GHz
Differential to common-mode input return loss	TP1	10			dB	10 MHz to 11.1 GHz
J2 Jitter tolerance	TP1a	0.17			UI	Defined in 802.3ba spec
J9 Jitter tolerance	TP1a	0.29			UI	Defined in 802.3ba spec
Data Dependent Pulse Width Shrinkage (DDPWS) tolerance	TP1a	0.07			UI	
Eye Mask Coordinates:	TP1a		SPECIFICATION VALUES			Hit Ratio = $5x10^{-5}$
X1, X2			0.11, 0.31		UI	
Y1, Y2			95, 350		mV	

Note:
1. The single ended input voltage tolerance is the allowable range of the instantaneous input signals

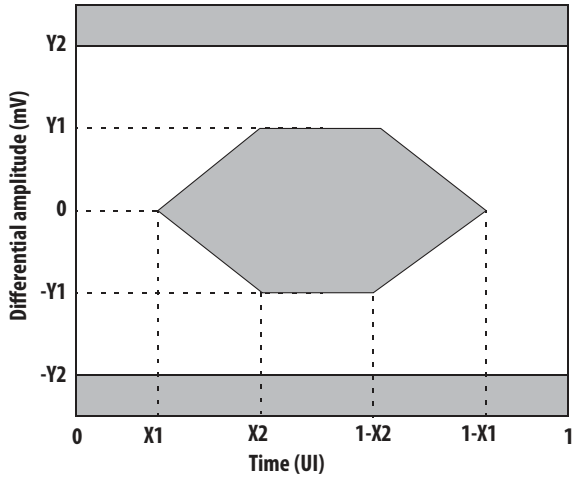


Figure 3. Electrical Eye Mask Coordinates at Hit ratio 5 x 10^{-5} hits per sample

Receiver Electrical Characteristics

The following characteristics are defined over the Recommended Operating Conditions unless otherwise noted. Typical values are for T_C = 40° C, V_{cc33} = 3.3 V

Parameter (From Table 86A-3 of IEEE 802.3ba)	Test Point	Min	Typ	Max	Units	Notes/Conditions
Single-ended output voltage tolerance	TP4	-0.3		4	V	Referred to signal common
AC common mode voltage (RMS)	TP4			7.5	mV	RMS
Termination mismatch at 1 MHz	TP4			5	%	
Differential output return loss	TP4	See IEEE 802.3ba 86A.4.2.1			dB	10 MHz to 11.1 GHz
Common-mode output return loss	TP4	See IEEE 802.3ba 86A.4.2.2			dB	10 MHz to 11.1 GHz
Output transition time 20% to 80%	TP4	28			ps	
J2 Jitter output	TP4			0.41	UI	Modified from IEEE 802.3 specification to support BER of 1E-15
J9 Jitter output	TP4			0.62	UI	Modified from IEEE 802.3 specification to support BER of 1E-15
Eye Mask coordinates:	TP4	SPECIFICATION VALUES				Hit Ratio = $5x10^{-5}$
X1, X2			0.29, 0.5		UI	
Y1, Y2			150, 425		mV	

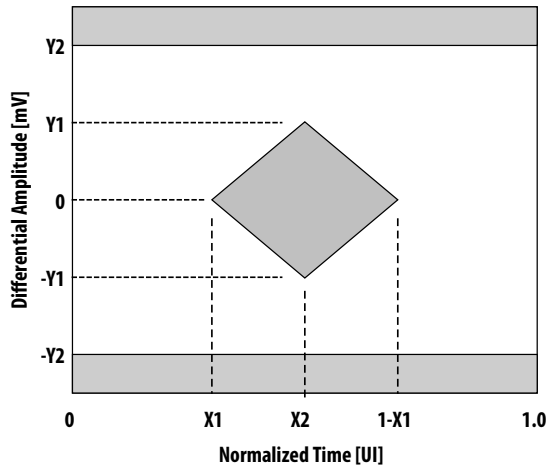
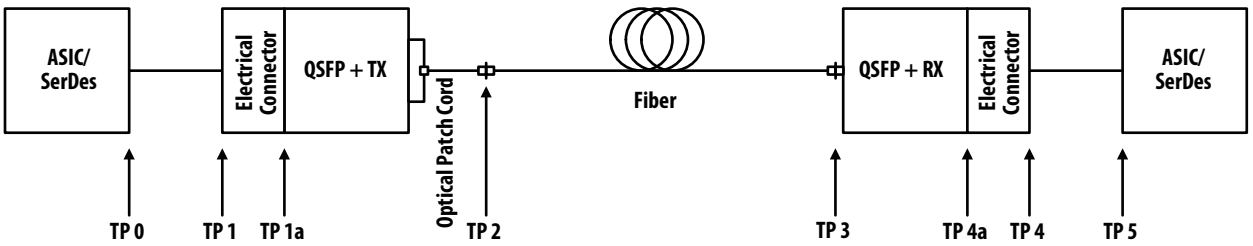


Figure 4. Rx Electrical Eye Mask Coordinates (TP4) at Hit ratio 5 x 10^{-5} hits per sample



TP0 : Host ASIC transmitter output at ASIC package contact on the Host board
TP1 : Host ASIC transmitter output across the Host Board at the input side of the Host QSFP+ electrical connector
TP1a : Host ASIC transmitter output across the Host board at the output side of the Host QSFP+ electrical connector
TP2 : QSFP+ transmitter optical output at the end of a 2 m to 5 m patch cord
TP3 : QSFP+ receiver optical input at the end of the fiber
TP4a : QSFP+ receiver electrical output at the input side of the Host QSFP+ electrical connector
TP4 : QSFP+ receiver electrical output at the output side of the Host QSFP+ electrical connector
TP5 : Host ASIC receiver input at ASIC package contact on the Host board

Figure 5. Test point definitions

Regulatory Compliance Table

Feature	Test Method	Performance
Electrostatic Discharge (ESD) to the Electrical Contacts	JEDEC Human Body Model (HBM) (JESD22-A114-B) JEDEC Charge Device Model (CDM) (JESD22-C101D)	High Speed contacts withstand 1 kV; all other contacts withstand 2 kV Active Cable withstands 250 V
Electrostatic Discharge (ESD) to Optical Connector	GR1089	10 discharges of 8 kV on the electrical faceplate with device inserted into a panel
Electrostatic Discharge (ESD) to Optical Connector	Variation of EN 61000-4-2	Air discharge of 15 kV (min) to connector without damage
Electromagnetic Interference (EMI)	FCC Part 15 CENELEC EN55022 (CISPR 22A) VCCI Class 1	Typically passes with 10 dB margin. Actual performance dependent on enclosure design
Immunity	Variation of EN 61000-4-3	Typically minimum effect from a 10V/m field swept from 80 MHz to 1 GHz applied to the Active Cable-end without a chassis enclosure
Laser Eye Safety and Equipment Type Testing	EN 60825-1:2007	P_{out}: EN AEL & US FDA CDRH Class 1M
Component Recognition	Underwriters Laboratories and Canadian Standards Association Joint Component Recognition for Information Technology Equipment including Electrical Business Equipment	
RoHS Compliance	BS EN 1122:2001 Mtd B by ICP for Cadmium, EPA Method 3051A by ICP for Lead and Mercury, EPA Method 3060A & 7196A by UV/Vis Spectrophotometry for Hexavalent Chromium. EPA Method 3540C/3550B by GC/MS for PPB and PBDE BS EN method by ICP and EPA methods by ICP, UV/Vis Spectrophotometry and GC/MS.	Less than 100 ppm of cadmium, Less than 1000 ppm of lead, mercury, hexavalent chromium, polybrominated biphenyls, and polybrominated biphenyl esters.
Flammability		Module: UL 94V-0 Cable: OFNR, LSZH

QSFP+ Pad Layout

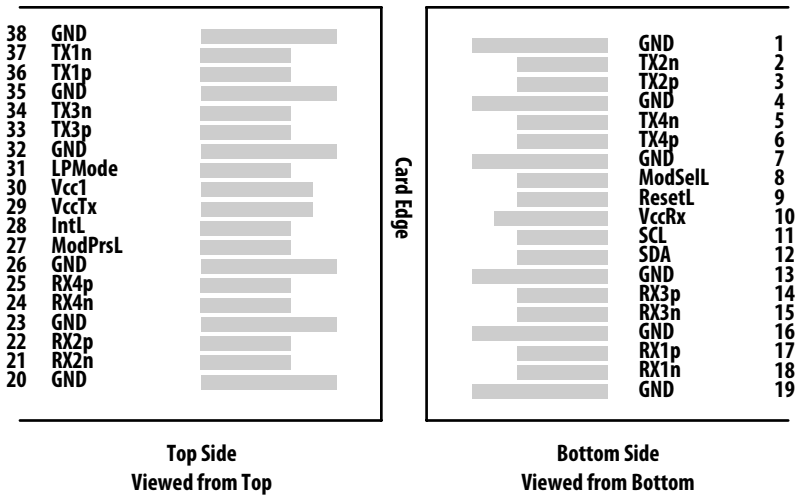


Figure 6. Pad Layout

Pin	Logic	Symbol	Description	Plug Sequence	Notes
1		GND	Ground	1	1
2	CML-I	Tx2n	Transmitter Inverted Data Input	3	
3	CML-I	Tx2p	Transmitter Non-Inverted Data Input	3	
4		GND	Ground	1	1
5	CML-I	Tx4n	Transmitter Inverted Data Input	3	
6	CML-I	Tx4p	Transmitter Non-Inverted Data Input	3	
7		GND	Ground	1	1
8	LVTTL-I	ModSelL	Module Select	3	
9	LVTTL-I	ResetL	Module Reset	3	
10		Vcc Rx	+3.3V Power supply receiver	2	2
11	LVCMOS-I/O	SCL	2-wire serial interface clock	3	
12	LVCMOS-I/O	SDA	2-wire serial interface data	3	
13		GND	Ground	1	1
14		Rx3p	Receiver Non-Inverted Data Input	3	
15	CML-O	Rx3n	Receiver Inverted Data Input	3	
16	CML-O	GND	Ground	1	1
17		Rx1p	Receiver Non-Inverted Data Input	3	
18	CML-O	Rx1n	Receiver Inverted Data Input	3	
19	CML-O	GND	Ground	1	1
20		GND	Ground	1	1
21	CML-O	Rx2n	Receiver Inverted Data Input	3	
22	CML-O	Rx2p	Receiver Non-Inverted Data Input	3	
23		GND	Ground	1	1
24	CML-O	Rx4n	Receiver Inverted Data Input	3	
25	CML-O	Rx4p	Receiver Non-Inverted Data Input	3	
26		GND	Ground	1	
27	LVTTL-O	ModPrsL	Module Present	3	
28	LVTTL-O	IntL	Interrupt	3	
29		Vcc Tx	+3.3V Power supply transmitter	2	2
30		Vcc1	+3.3V Power Supply	2	2
31	LVTTL-I	LPMode	Low Power Mode	3	
32		GND	Ground	1	1
33	CML-I	Tx3p	Transmitter Non-Inverted Data Input	3	
34	CML-I	Tx3n	Transmitter Inverted Data Input	3	
35		GND	Ground	1	1
36	CML-I	Tx1p	Transmitter Non-Inverted Data Input	3	
37	CML-I	Tx1n	Transmitter Inverted Data Input	3	
38		GND	Ground	1	1

Notes:

1. GND is the symbol for signal supply (power) common for the QSFP+ AOC. All are common within the QSFP+ AOC and all device voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal-common ground plane
2. Vcc Rx, Vcc1 and Vcc Tx are the receiver and transmitter power supplies and shall be applied concurrently.

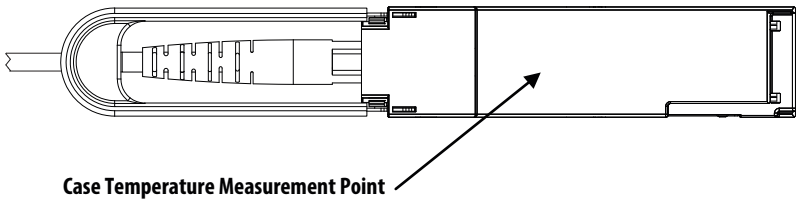


Figure 7. Case Temperature Measurement Point

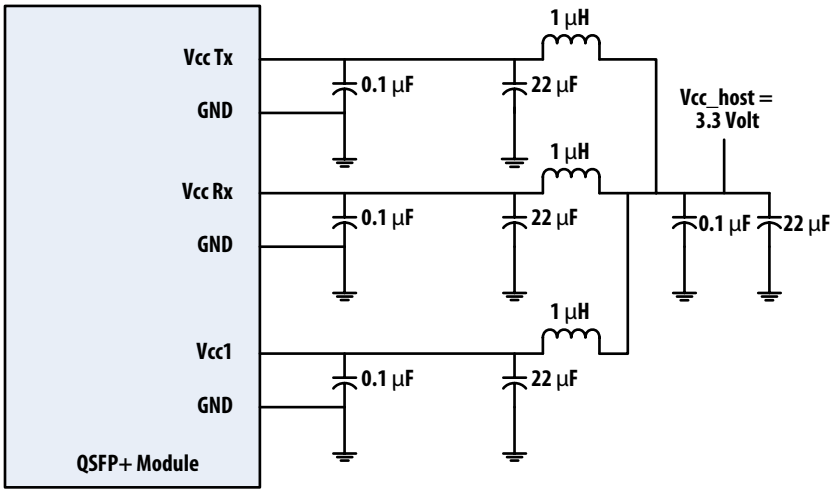


Figure 8. Recommended Host Board Power Supply Filter

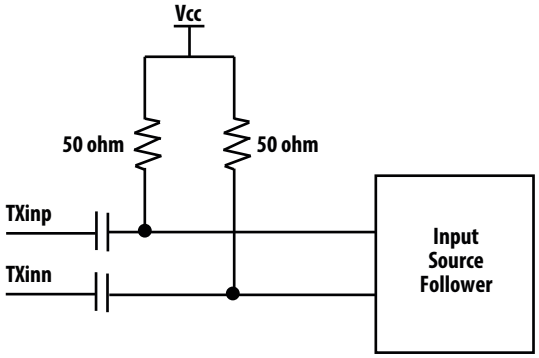


Figure 9. Input Termination Schematic

Package Outline

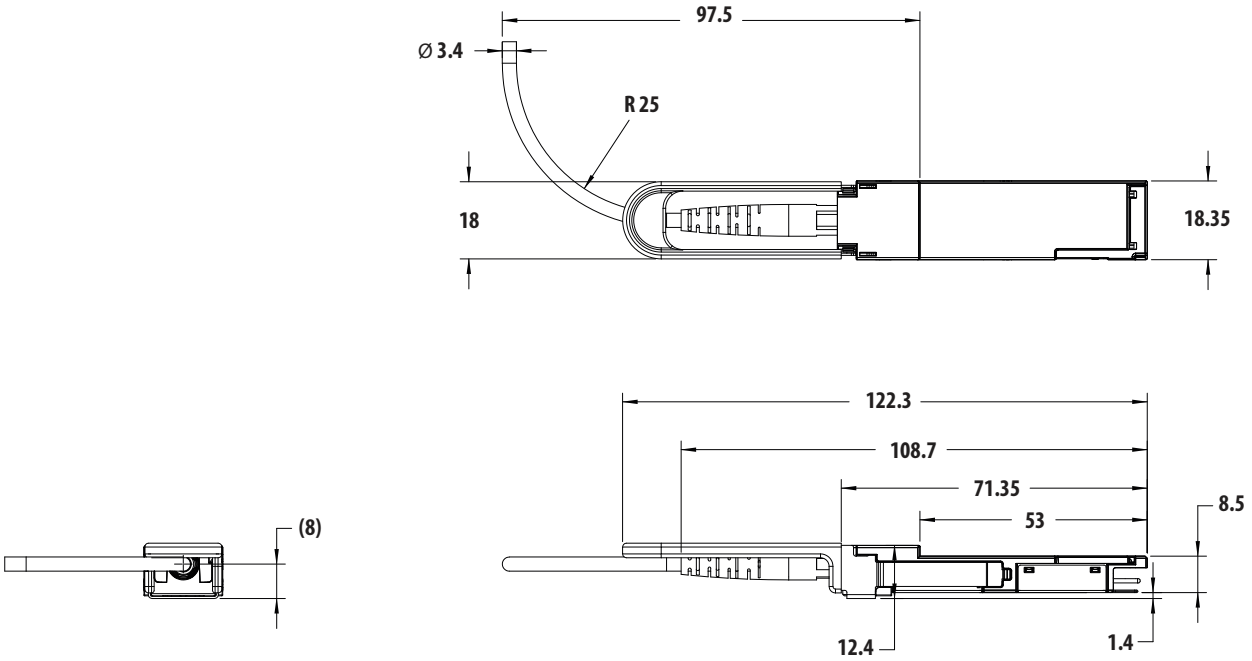
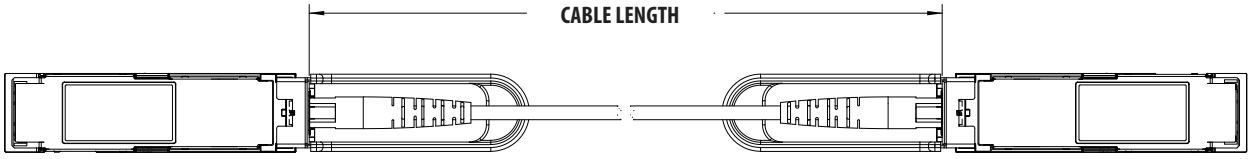
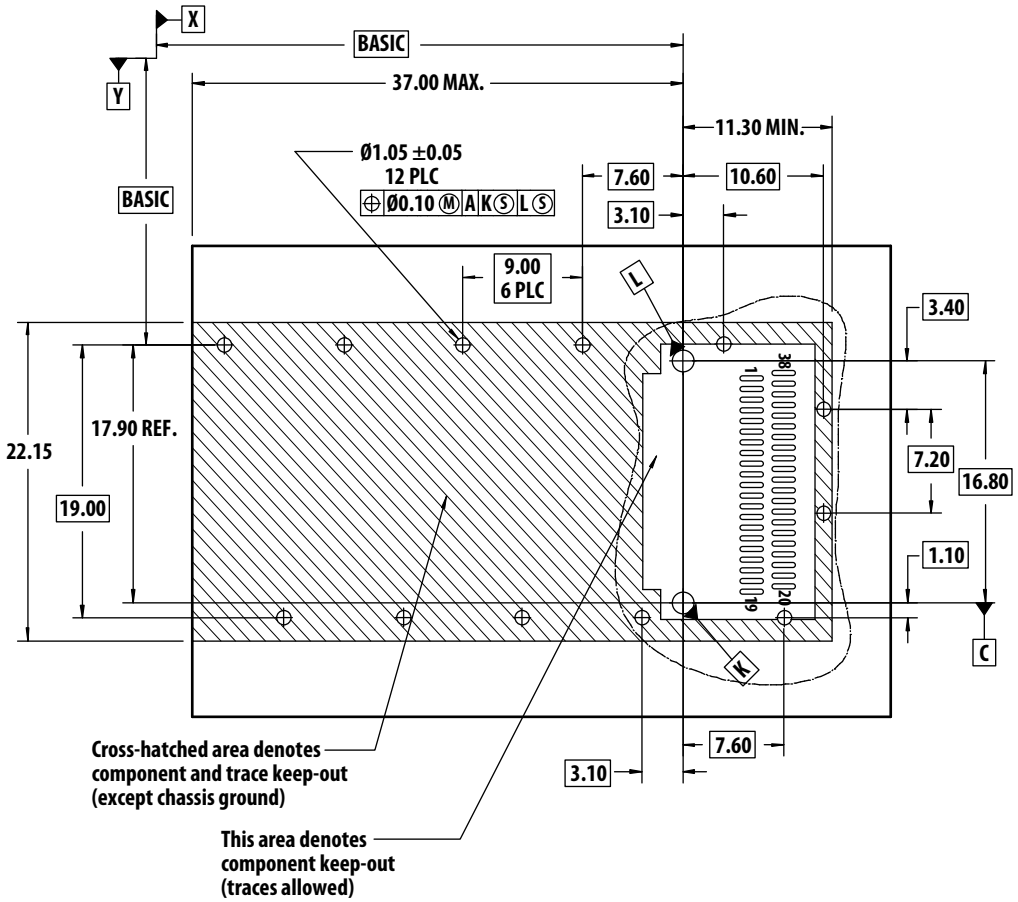


Figure 10. Mechanical Package Outline, Connector and Bend Radius – Dimensions in Millimeters



Part Number	Length	Cable Length Tolerance
AFBR-7QER01Z	1 m	+20/-0 cm
AFBR-7QER02Z	2 m	+20/-0 cm
AFBR-7QER03Z	3 m	+20/-0 cm
AFBR-7QER05Z	5 m	+20/-0 cm
AFBR-7QER07Z	7 m	+20/-0 cm
AFBR-7QER10Z	10 m	+20/-0 cm
AFBR-7QER15Z	15 m	+2%/-0%
AFBR-7QER20Z	20 m	+2%/-0%

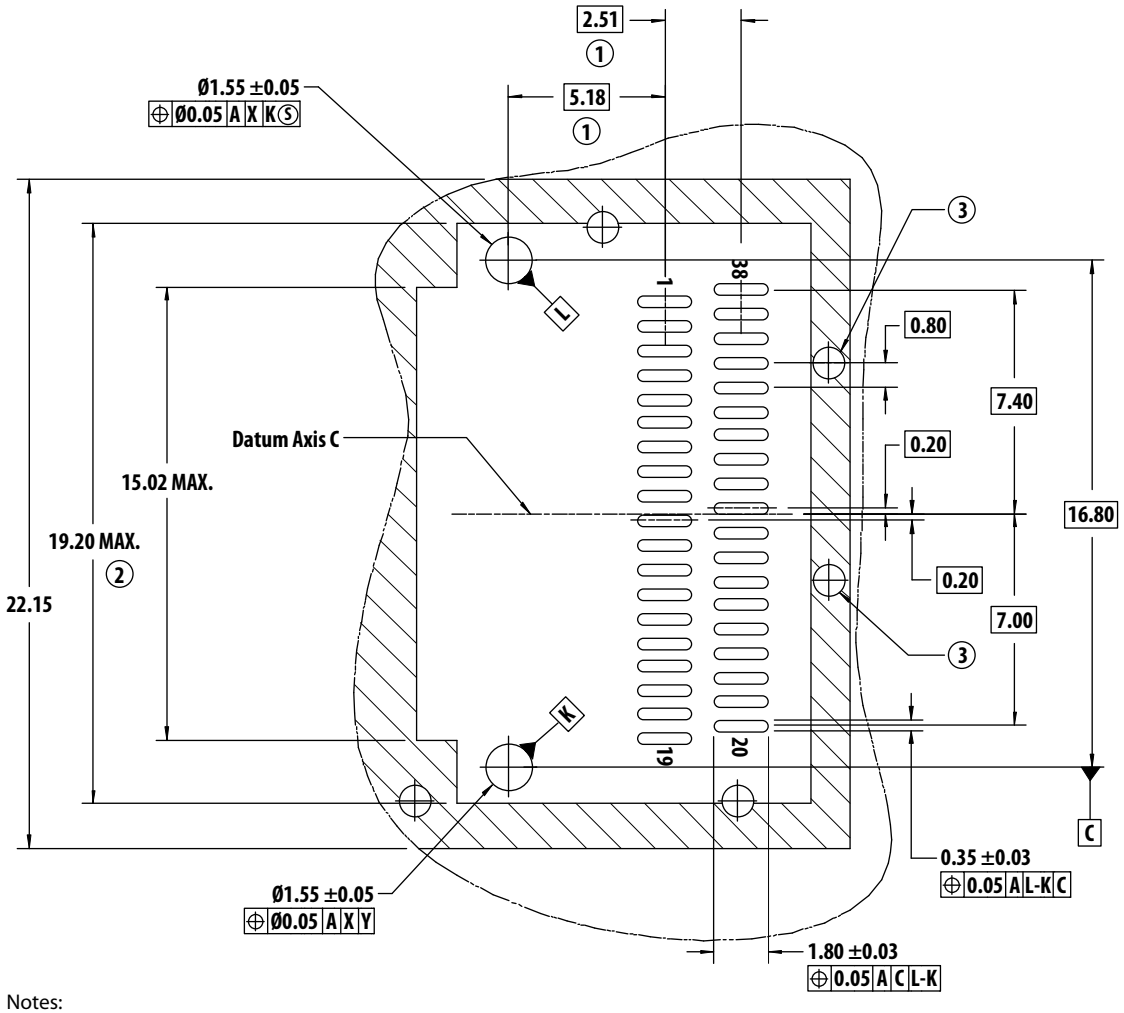
Figure 11. Cable Length Definition and Tolerances



Notes:
1. Datum X & Y are established by the customer's fiducial
2. Datum A is the top surface of the host board
3. Location of the edge of PCB is application specific
4. Finished hole size

All dimensions in mm

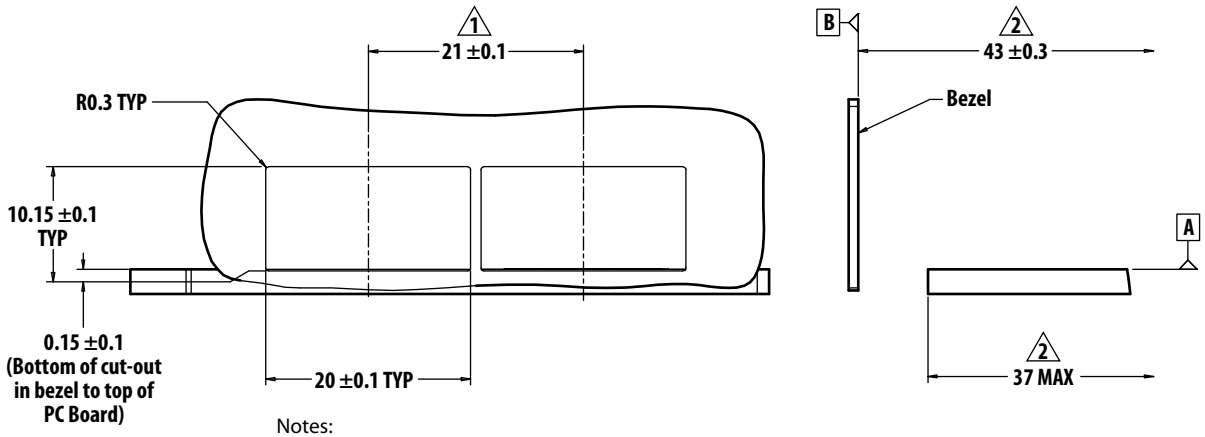
Figure 12. QSFP+ Host Board Mechanical Footprint



Notes:
1. Centerline of Pad
2. Surface traces permitted within this length
3. Indicated holes are optional

All dimensions in mm

Figure 13. QSFP+ Host Board Mechanical Footprint Detail



Notes:
1. Minimum pitch dimension for individual cages.
2. Dimension baseline is datum K or L.
3. Not recommended for PCI applications.

All dimensions in mm

Figure 14. Host Board Bezel Design

Control Interface & Memory Map

The control interface combines dedicated signal lines for ModSelL, LPMode, ResetL, ModPrsL, IntL with two-wire serial (TWS), interface clock (SCL) and data (SDA), signals to provide users functionality over an efficient and easily used interface. The TWS interface is implemented as a slave device and compatible with industry standard two-wire serial protocol. It is scaled for 3.3 V LVTTL. Outputs are high-Z in the high state to support busing of these signals. Signal and timing characteristics are further defined in the Control I/O Characteristics section. For more details, see QSFP+ SFF-8436.

ModSelL

The ModSelL is an input signal. When held low by the host, the module responds to 2-wire serial communication commands. The ModSelL allows the use of multiple QSFP+ devices on a single 2-wire interface bus. When the ModSelL is "High", the module will not respond to or acknowledge any 2-wire interface communication from the host. ModSelL signal input node is biased to the "High" state in the module. In order to avoid conflicts, the host system shall not attempt 2-wire interface communications within the ModSelL de-assert time after any QSFP+ device is deselected. Similarly, the host must wait at least for the period of the ModSelL assert time before communicating with the newly selected device. The assertion and de-assertion periods of different devices may overlap as long as the above timing requirements are met.

ResetL

The ResetL signal is pulled to Vcc in the QSFP+ Active Optical Cable. A low level on the ResetL signal for longer than the minimum pulse length (t_Reset_init) initiates a complete Active Cable-end reset, returning all user module settings to their default state. Module Reset Assert Time (t_init) starts on the rising edge after the low level on the ResetL pin is released. During the execution of a reset (t_init) the host shall disregard all status bits until the Active cable-end indicates a completion of the reset interrupt. The Active Cable-end indicates this by posting an IntL signal with the Data_Not_Ready bit negated. Note that on power up (including hot insertion) the Active Cable-end will post this completion of reset interrupt without requiring a reset.

LPMode

Low power mode. When held high by host, the module is held at low power mode. When held low by host, the module operates in the normal mode. For class 1 power level modules (1.5 W), low power mode has no effect.

ModPrsL

ModPrsL is pulled up to Vcc_Host on the host board and grounded in the Active Cable-end. The ModPrsL is asserted "Low" when module is inserted into the host connector, and deasserted "High" when the Active Cable-end is physically absent from the host connector.

IntL

IntL is an output signal. When "Low", it indicates a possible operational status critical to the host system. The host identifies the source of the interrupt using the 2-wire serial interface. The IntL signal is an open collector output and must be pulled to host supply voltage on the host board. A corresponding soft status IntL signal is also available in the device memory page 0 address 2 bit 1.

Soft Status and Control

A number of soft status signals and controls are available in each end of the AFBR-7QERxxZ Active Optical Cable and are accessible through the TWS interface. Soft status signal are receiver LOS, Soft controls include transmitter disable (Tx_Dis), receiver squelch disable (Rx_SqDis), and masking of status signal in triggering IntL. All soft status signals and controls are on a per channel basis. All soft control entries are volatile.

Receiver LOS

The receiver LOS status signal is on page 0 address 3 bits 0-3 for channels 1-4 respectively. Receiver LOS is based on loss of optical input, due to transmitter disable or fiber break. This status register is latched and it is cleared on read.

Transmitter Disable

The transmitter disable control is on page 0 address 86 bits 0-3 for channels 1-4 respectively.

Receiver Squelch Disable

The receiver squelch disable control is on page 3 address 240 bits 4-7 for channels 1-4 respectively. AFBR-7QERxxZ Active Optical Cable have receiver output squelch function enabled as default.

I/O Timing for Control and Status Functions

The following characteristics are defined over the Recommended Operating Conditions unless otherwise noted. Typical values are for Tc = 40° C, Vcc = 3.3 V

Parameter	Symbol	Min	Typ	Max	Units	Reference
Initialization Time	t_init		150	2000	ms	Time from power on, hot plug or rising edge of Reset until the Active Cable-end is fully functional. This time does not apply to non Power level 0 devices in the Low Power state
LPMode Assert Time	ton_LPMode			N.A.	ms	Always in Power Level 1
Interrupt Assert Time	ton_IntL			200	ms	Time from occurrence of condition triggering IntL until Vout: IntL = Vol
Interrupt De-assert Time	Toff_IntL			500	μs	Time from clear on read operation of associated flag until Vout: IntL = Voh. This includes deassert times for RX LOS/ flag bits
Reset Init Assert Time	t_reset_init			2	μs	A Reset is generated by a low level longer than the minimum reset pulse time present on the ResetL pin
Reset Assert Time	t_reset			2000	ms	Time from rising edge on the ResetL pin until the Active Cable-end is fully functional
Serial Bus Hardware Ready Time	t_serial			2000	ms	Time from power on until Active Cable-end responds to data transmission over the 2-wire serial bus
Monitor Data Ready Time	t_data			2000	ms	Time from power on to data not ready, bit 0 of Byte 2, deasserted and IntL asserted
RX LOS Assert Time	ton_los			100	ms	Time from RX LOS state to RX LOS bit set and IntL asserted
Flag Assert Time	ton_Flag			200	ms	Time from occurrence of condition triggering flag to associated flag bit set and IntL asserted.
Mask Assert Time	ton_Mask			100	ms	Time from mask bit set until associated IntL assertion is inhibited
Mask Deassert Time	toff_Mask			100	ms	Time from mask bit cleared until associated IntL operation resumes
Power Set Assert Time	ton_Pdown			100	ms	Time from P_Down but set until Active Cable-end power consumption enters power level 1
Power Set Deassert Time	toff_Pdown			300	ms	Time from P_Down bit cleared until the Active Cable-end is fully functional
RX Squelch Assert Time	ton_Rxsq			80	μs	Time from loss of RX input signal until the squelched output condition is reached
RX Squelch Deassert Time	toff_Rxsq			80	μs	Time from resumption of RX input signals until normal RX output condition is reached
TX Disable Assert Time	ton_txdis			100	ms	Time from TX Disable bit set until optical output falls below 10% of nominal
TX Disable Deassert Time	toff_txdis			400	ms	Time from TX Disable bit cleared until optical output rises above 90% of nominal
RX Output Disable Assert Time	ton_rxdis			100	ms	Time from RX Output Disable bit set until RX output falls below 10% of nominal
RX Output Disable Deassert Time	toff_rxdis			100	ms	Time from RX Output Disable bit cleared until RX output rises above 90% of nominal
Squelch Disable Assert Time	ton_sqdis			100	ms	This applies to RX and TX Squelch and is the time from bit set until squelch functionality is disabled
Squelch Disable Deassert Time	toff_sqdis			100	ms	This applies to RX and TX Squelch and is the time from bit cleared until squelch functionality is enabled

Memory Map

The memory is structured as a single address, multiple page approach. The address is given as A0xh. The structure of the memory is shown in Figure 15. The memory space is arranged into a lower, single page, address space of 128 bytes and multiple upper address space pages of 128 bytes each. This structure permits timely access to addresses in the lower page, e.g., Interrupt Flags and Monitors. Less time critical entries, e.g. serial ID information and threshold settings are available with the Page Select function. For a more detailed description of the QSFP+ memory map see the QSFP+ SFF-8436 Specification or the Avago Technologies QSFP+ AOC Memory Map document.

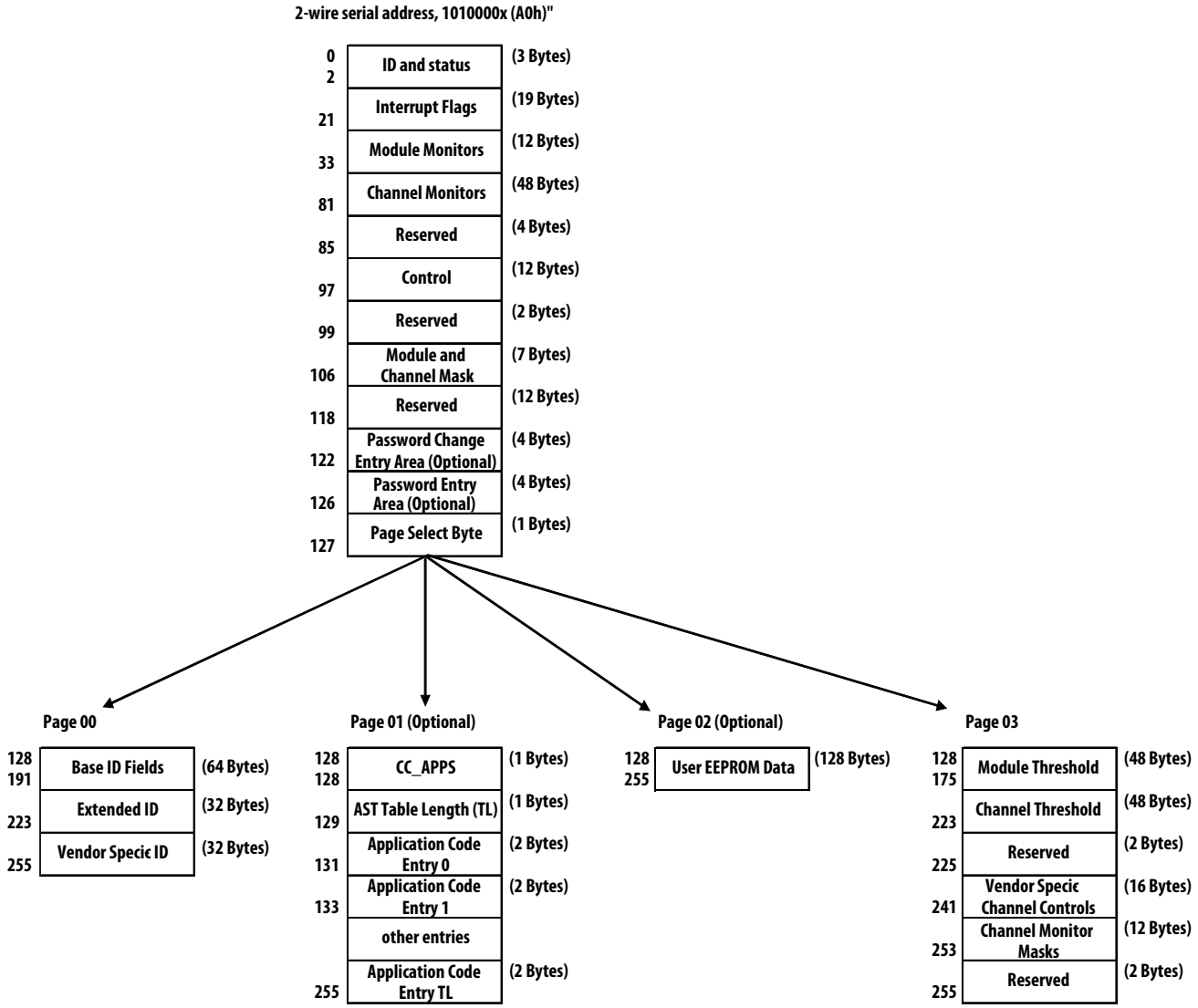


Figure 15. Two-Wire Serial Address A0xh Page Structure

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