

December 1996

High-Speed CMOS Dual 4-Input Multiplexers

Features

- Advanced 0.8 micron CMOS Technology
- These Devices are Pin Compatible with Bipolar FAST™ Series at a Higher Speed and Lower Power Consumption
- 25Ω Series Resistor On All Outputs (FCT2XXX Only)
- TTL Input and Output Levels
- Low Ground Bounce Outputs (25Ω Series Only)
- Extremely Low Static Power
- Hysteresis on All Inputs

Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
CD74FCT153TM	-40 to 85	16 Ld SOIC	M16.3-P
CD74FCT153ATM	-40 to 85	16 Ld SOIC	M16.3-P
CD74FCT153CTM	-40 to 85	16 Ld SOIC	M16.3-P
CD74FCT153TNM	-40 to 85	16 Ld SOIC	M16.15-P
CD74FCT153ATNM	-40 to 85	16 Ld SOIC	M16.15-P
CD74FCT153CTNM	-40 to 85	16 Ld SOIC	M16.15-P
CD74FCT153TQM	-40 to 85	16 Ld QSOP	M16.15A-P
CD74FCT153ATQM	-40 to 85	16 Ld QSOP	M16.15A-P
CD74FCT153CTQM	-40 to 85	16 Ld QSOP	M16.15A-P
CD74FCT253TM	-40 to 85	16 Ld SOIC	M16.3-P
CD74FCT253ATM	-40 to 85	16 Ld SOIC	M16.3-P
CD74FCT253CTM	-40 to 85	16 Ld SOIC	M16.3-P
CD74FCT253TNM	-40 to 85	16 Ld SOIC	M16.15-P
CD74FCT253ATNM	-40 to 85	16 Ld SOIC	M16.15-P
CD74FCT253CTNM	-40 to 85	16 Ld SOIC	M16.15-P
CD74FCT253TQM	-40 to 85	16 Ld QSOP	M16.15A-P
CD74FCT253ATQM	-40 to 85	16 Ld QSOP	M16.15A-P
CD74FCT253CTQM	-40 to 85	16 Ld QSOP	M16.15A-P
CD74FCT2153TM	-40 to 85	16 Ld SOIC	M16.3-P
CD74FCT2153ATM	-40 to 85	16 Ld SOIC	M16.3-P
CD74FCT2153CTM	-40 to 85	16 Ld SOIC	M16.3-P
CD74FCT2153TNM	-40 to 85	16 Ld SOIC	M16.15-P
CD74FCT2153ATNM	-40 to 85	16 Ld SOIC	M16.15-P
CD74FCT2153CTNM	-40 to 85	16 Ld SOIC	M16.15-P
CD74FCT2153TQM	-40 to 85	16 Ld QSOP	M16.15A-P
CD74FCT2153ATQM	-40 to 85	16 Ld QSOP	M16.15A-P
CD74FCT2153CTQM	-40 to 85	16 Ld QSOP	M16.15A-P
CD74FCT2253TM	-40 to 85	16 Ld SOIC	M16.3-P
CD74FCT2253ATM	-40 to 85	16 Ld SOIC	M16.3-P
CD74FCT2253CTM	-40 to 85	16 Ld SOIC	M16.3-P
CD74FCT2253TNM	-40 to 85	16 Ld SOIC	M16.15-P
CD74FCT2253ATNM	-40 to 85	16 Ld SOIC	M16.15-P
CD74FCT2253CTNM	-40 to 85	16 Ld SOIC	M16.15-P
CD74FCT2253TQM	-40 to 85	16 Ld QSOP	M16.15A-P
CD74FCT2253ATQM	-40 to 85	16 Ld QSOP	M16.15A-P
CD74FCT2253CTQM	-40 to 85	16 Ld QSOP	M16.15A-P

NOTE: When ordering, use the entire part number. Add the suffix 96 to obtain the variant in the tape and reel.

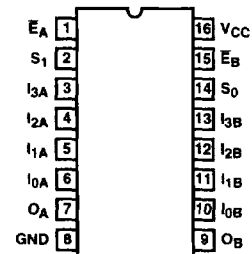
Description

The CD74FCT153T, CD74FCT253T, CD74FCT2153T and CD74FCT2253T are high-speed dual 4-input multiplexers. The CD74FCT153T and CD74FCT2153T have TTL outputs, while the CD74FCT253T and CD74FCT2253T have three-state outputs. The output buffers are designed with a poweroff disable allowing 'live insertion' of boards when used as back-plane drivers.

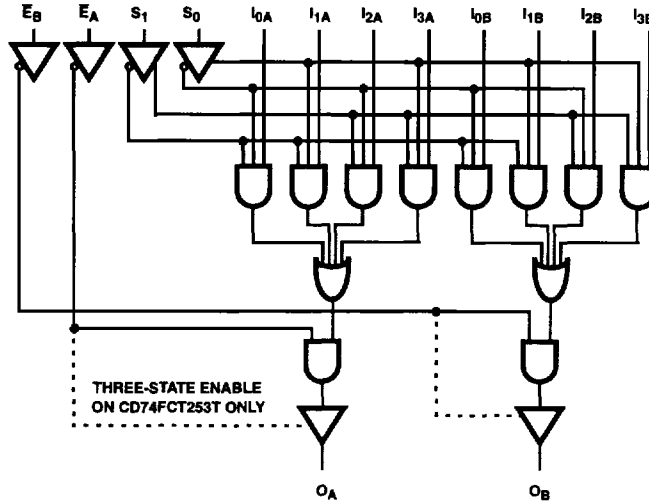
The CD74FCT2153T and CD74FCT2253T devices have a built-in 25Ω series resistor on all outputs to reduce noise due to reflections, thus eliminating the need for an external terminating resistor.

Pinout

CD74FCT153T, CD74FCT253T,
CD74FCT2153T, CD74FCT2253T
(QSOP, SOIC)
TOP VIEW



Functional Block Diagram



TRUTH TABLE (NOTE 1)

INPUTS				OUTPUTS			
				CD74FCT153, CD74FCT2153		CD74FCT253, CD74FCT2253	
EA	EB	S1	S0	OA	OB	OA	OB
H	X	X	X	L	X	Z	X
X	H	X	X	X	L	X	Z
L	L	L	L	I0A	I0B	I0A	I0B
L	L	L	H	I1A	I1B	I1A	I1B
L	L	H	L	I2A	I2B	I2A	I2B
L	L	H	H	I3A	I3B	I3A	I3B

NOTE:

- 1. H = High Voltage Level
- L = Low Voltage Level
- X = Don't Care
- Z = High Impedance

Pin Description

PIN NAME	DESCRIPTION
I0A-I3A, I0B-I3B	Data Inputs
S0, S1	Select Inputs
EA, EB	Enable Input
OA, OB	Data Outputs
GND	Ground
VCC	Power

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 OCTAL 5V FCT
 5V FCT 25Ω

CD74FCT153T, CD74FCT253T, CD74FCT2153T, CD74FCT2253T

Absolute Maximum Ratings

DC Input Voltage	-0.5V to 7.0V
DC Output Current	120mA

Operating Conditions

Operating Temperature Range	-40°C to 85°C
Supply Voltage to Ground Potential	
Inputs and V _{CC} Only	-0.5V to 7.0V
Supply Voltage to Ground Potential	
Outputs and D/O Only	-0.5V to 7.0V

Thermal Information

Thermal Resistance (Typical, Note 2)	θ_{JA} (°C/W)
16 Lead SOIC (150 mil) Package	110
16 Lead SOIC (300 mil) Package	97
16 Lead QSOP Package	140
Maximum Junction Temperature	150°C
Maximum Storage Temperature Range	-65°C to 150°C
Maximum Lead Temperature (Soldering 10s)	300°C
(Lead Tips Only)	

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

- θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

PARAMETER	SYMBOL	(NOTE 3)		MIN	(NOTE 4)	MAX	UNITS
		TEST CONDITIONS					
DC ELECTRICAL SPECIFICATIONS Over the Operating Range, $T_A = -40^\circ\text{C}$ to 85°C , $V_{CC} = 5.0\text{V} \pm 5\%$							
Output HIGH Voltage	V_{OH}	$V_{CC} = \text{Min}$, $V_{IN} = V_{IH}$ or V_{IL}	$I_{OH} = -15.0\text{mA}$	2.4	3.0	-	V
Output LOW Voltage	V_{OL}	$V_{CC} = \text{Min}$, $V_{IN} = V_{IH}$ or V_{IL}	$I_{OL} = 48\text{mA}$	-	0.3	0.50	V
Output LOW Voltage	V_{OL}	$V_{CC} = \text{Min}$, $V_{IN} = V_{IH}$ or V_{IL}	$I_{OL} = 12\text{mA}$ (25 Ω series)	-	0.3	0.50	V
Input HIGH Voltage	V_{IH}	Guaranteed Logic HIGH Level		2.0	-	-	V
Input LOW Voltage	V_{IL}	Guaranteed Logic LOW Level		-	-	0.8	V
Input HIGH Current	I_{IH}	$V_{CC} = \text{Max}$	$V_{IN} = V_{CC}$	-	-	1	μA
Input LOW Current	I_{IL}	$V_{CC} = \text{Max}$	$V_{IN} = \text{GND}$	-	-	-1	μA
High Impedance Output Current	I_{OZH} , I_{OZL}	$V_{CC} = \text{Max}$	$V_{OUT} = 2.7\text{V}$			1	μA
			$V_{OUT} = 0.5\text{V}$			-1	μA
Clamp Diode Voltage	V_{IK}	$V_{CC} = \text{Min}$, $I_{IN} = -18\text{mA}$		-	-0.7	-1.2	V
Short Circuit Current	I_{OS}	$V_{CC} = \text{Max}$ (Note 5), $V_{OUT} = \text{GND}$		-60	-120	-	mA
Power Down Disable	I_{OFF}	$V_{CC} = \text{GND}$, $V_{OUT} = 4.5\text{V}$		-	-	100	μA
Input Hysteresis	V_H			-	200	-	mV
CAPACITANCE $T_A = 25^\circ\text{C}$, $f = 1\text{MHz}$							
Input Capacitance (Note 6)	C_{IN}	$V_{IN} = 0\text{V}$		-	6	10	pF
Output Capacitance (Note 6)	C_{OUT}	$V_{OUT} = 0\text{V}$		-	8	12	pF
POWER SUPPLY SPECIFICATIONS							
Quiescent Power Supply Current	I_{CC}	$V_{CC} = \text{Max}$	$V_{IN} = \text{GND}$ or V_{CC}	-	0.1	500	μA
Supply Current per Input at TTL HIGH	ΔI_{CC}	$V_{CC} = \text{Max}$	$V_{IN} = 3.4\text{V}$ (Note 7)	-	0.5	2.0	mA
Supply Current per Input per MHz (Note 8)	I_{CCD}	$V_{CC} = \text{Max}$, Outputs Open Other Inputs at GND One Bit Toggling 50% Duty Cycle	$V_{IN} = V_{CC}$ $V_{IN} = \text{GND}$	-	0.15	0.25	mA/ MHz
Total Power Supply Current (Note 10)	I_C	$V_{CC} = \text{Max}$, Outputs Open $I_I = 10\text{MHz}$, 50% Duty Cycle Other Inputs at GND One Bit Toggling	$V_{IN} = V_{CC}$ $V_{IN} = \text{GND}$	-	3.2	6.5 (Note 9)	mA
			$V_{IN} = 3.4\text{V}$ $V_{IN} = \text{GND}$	-	3.5	7.5 (Note 9)	mA

CD74FCT153T, CD74FCT253T, CD74FCT2153T, CD74FCT2253T

Switching Specifications Over Operating Range

PARAMETER	SYMBOL	(NOTE 11) TEST CONDITIONS	T		AT		CT		UNIT
			(NOTE 12) MIN	MAX	(NOTE 12) MIN	MAX	(NOTE 12) MIN	MAX	
CD74FCT153T, CD74FCT2153T									
Propagation Delay Sn to O	t _{PLH} , t _{PHL}	C _L = 50pF R _L = 500Ω	1.5	9.0	1.5	6.6	1.5	5.6	ns
Propagation Delay In to O	t _{PLH} , t _{PHL}		1.5	7.0	1.5	5.2	1.5	4.5	ns
Propagation Delay E to O	t _{PLH} , t _{PHL}		1.5	7.0	1.5	5.2	1.5	4.8	ns
CD74FCT253T, CD74FCT2253T									
Propagation Delay Sn to O	t _{PLH} , t _{PHL}	C _L = 50pF R _L = 500Ω	1.5	9.0	1.5	6.6	1.5	5.6	ns
Propagation Delay In to O	t _{PLH} , t _{PHL}		1.5	7.0	1.5	5.2	1.5	4.5	ns
Output Enable Time E to O	t _{PZH} , t _{PZL}		1.5	9.0	1.5	6.0	1.5	5.0	ns
Output Enable Time E to O (Note 13)	t _{PHZ} , t _{PLZ}		1.5	7.0	1.5	6.0	1.5	5.0	ns

NOTES:

- For conditions shown as Max or Min, use appropriate value specified under Electrical Specifications for the applicable device type.
- Typical values are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
- Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
- This parameter is determined by device characterization but is not production tested.
- Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
- This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
- Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
- $$I_C = I_{\text{QUIESCENT}} + I_{\text{INPUTS}} + I_{\text{DYNAMIC}}$$

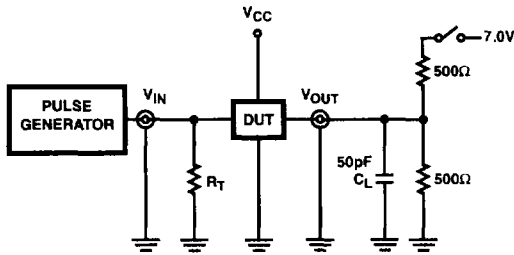
$$I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$$

I_{CC} = Quiescent Current
 ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
 D_H = Duty Cycle for TTL Inputs High
 N_T = Number of TTL Inputs at D_H
 I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
 f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
 f_i = Input Frequency
 N_i = Number of Inputs at f_i
 All currents are in milliamps and all frequencies are in megahertz.
- See test circuit and wave forms.
- Minimum limits are guaranteed but not tested on Propagation Delays.
- This parameter is guaranteed but not production tested.

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**OCTAL 5V FCT
5V FCT 25Ω**

Test Circuits and Waveforms



SWITCH POSITION	
TEST	SWITCH
t_{PLZ}, t_{PZL}	Closed
$t_{PHZ}, t_{PZH}, t_{PLH}, t_{PHL}$	Open

DEFINITIONS:

C_L = Load capacitance, includes jig and probe capacitance.
 R_T = Termination resistance, should be equal to Z_{OUT} of the Pulse Generator.

NOTE:

14. Pulse Generator for All Pulses: Rate ≤ 1.0 MHz; $Z_{OUT} \leq 50\Omega$;
 $t_r, t_f \leq 2.5$ ns.

FIGURE 1. TEST CIRCUIT

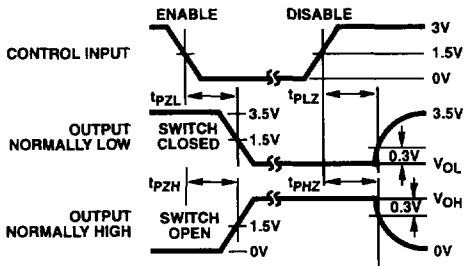


FIGURE 2. ENABLE AND DISABLE TIMING

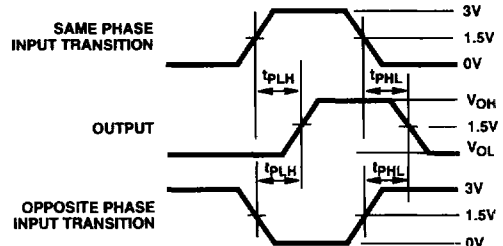


FIGURE 3. PROPAGATION DELAY