19-5284; Rev 2; 5/11

EVALUATION KIT AVAILABLE

Industry's Lowest-Power Ambient Light Sensor with ADC

MAX9635

General Description

The MAX9635 ambient light sensor features an I2C digital output that is ideal for a number of portable applications such as smartphones, notebooks, and industrial sensors. At less than 1µA operating current, it is the lowest power ambient light sensor in the industry and features an ultra-wide 22-bit dynamic range from 0.045 lux to 188,000 lux.

Low-light operation allows easy operation in dark glass applications.

The on-chip photodiode's spectral response is optimized to mimic the human eye's perception of ambient light and incorporates IR and UV blocking capability. The adaptive gain block automatically selects the correct lux range to optimize the counts/lux.

The IC is designed to operate from a 1.7V to 3.6V supply voltage range and consumes only 0.65µA in full operation. It is available in a small, 2mm x 2mm x 0.6mm OTDFN package.

Applications

Tablet PCs/Notebook Computers

TVs/Projectors/Displays

Digital Lighting Management

Portable Devices

Cellular Phones/Smartphones

Security Systems

Features

- **Wide 0.045 Lux to 188,000 Lux Range**
- **Small, 2mm x 2mm x 0.6mm OTDFN**
- **VCC = 1.7V to 3.6V**
- **ICC = 0.65µA Operating Current**
- **-40°C to +85°C Temperature Range**

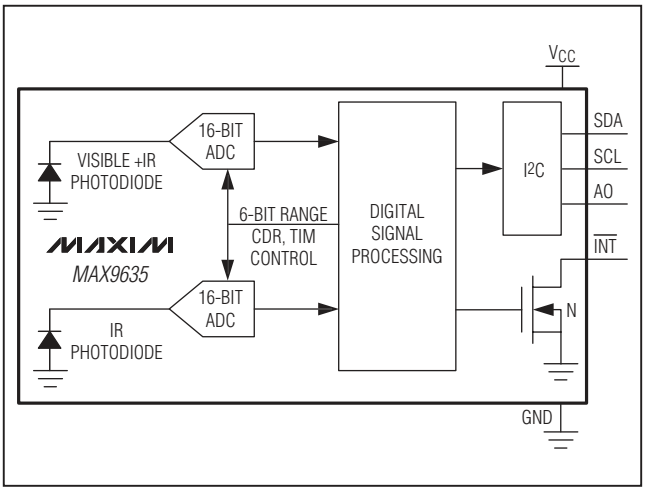
Ordering Information

PART	PIN-PACKAGE	TEMP RANGE
MAX9635EDT+	6 OTDFN-EP*	-40°C to +85°C

+Denotes a lead(Pb)-free/RoHS-compliant package.

**EP = Exposed pad.*

Block Diagram



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ABSOLUTE MAXIMUM RATINGS

$\overline{INT}$ to GND ..... -0.3V to (V_{CC} + 0.3V)
All Other Pins to GND ..... -0.3V to +4V
$\overline{INT}$ Short-Circuit Current Duration 10s
All Other Pins Short-Circuit Current Duration ..... Continuous
Continuous Input Current into Any Terminal ..... ±20mA
Continuous Power Dissipation
6 OTDFN (derate 11.9mW/°C above +70°C) 953mW
Operating Temperature Range ..... -40°C to +85°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = 1.8V, T_{MIN} to T_{MAX} = -40°C to +85°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
OPTICAL CHARACTERISTICS						
Maximum Lux Sensitivity		Fluorescent light		0.045		Lux/LSB
Saturation Ambient Lux Level		Sunlight		188,000		Lux
Total Error	TE	Green LED 538nm response, T_A = +25°C (Note 2)			15	%
Light Source Matching		Fluorescent/incandescent light		10		%
Infrared Transmittance at 940nm	IRR	T_A = +25°C (Note 3)		0	0.5	%
Ultraviolet Transmittance at 363nm	UVR	T_A = +25°C (Note 3)		1.2		%
Dark Level Count	0LUX	0 lux, T_A = +25°C, 800ms range		0	0.045	Lux
Maximum Signal Integration Time		Has 50/60Hz rejection		800		ms
Minimum Signal Integration Time		Automatic mode, has 50/60Hz rejection		100		ms
		Manual mode only		6.25		
ADC Conversion Time	ACT	100ms range, T_A = +25°C	99.6	100	100.4	ms
		100ms range	97	103	107	
POWER SUPPLY						
Power-Supply Voltage	V_{CC}	Guaranteed by TE test	1.7		3.6	V
Power-Supply Current	I_{CC}	T_A = +25°C, 90 lux, I^2C inputs inactive		0.65	1.2	µA
		T_A = -40°C to +85°C			1.6	
DIGITAL I/O CHARACTERISTICS						
Output Low Voltage SDA, $\overline{INT}$	V_{OL}	I_{SINK} = 6mA		0.06	0.4	V
$\overline{INT}$ Leakage Current		T_A = +25°C		0.01	20	nA
SCL, SDA, A0 Input Current	I_{IH}, I_{IL}	T_A = +25°C		0.01	20	nA
I^2C Input Low Voltage	V_{IL_I2C}	SDA, SCL			0.3 x V_{CC}	V
I^2C Input High Voltage	V_{IH_I2C}	SDA, SCL	0.7 x V_{CC}			V
Address Input Low Voltage	V_{IL_A0}	A0			0.3	V
Address Input High Voltage	V_{IH_A0}	A0	V_{CC} - 0.3V			V
Input Capacitance				3		pF

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = 1.8V, T_{MIN} to T_{MAX} = -40°C to +85°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
I²C TIMING						
Serial-Clock Frequency	f_{SCL}				400	kHz
Bus Free Time Between a STOP and a START Condition	t_{BUF}		1.3			µs
Hold Time (REPEATED) START Condition	$t_{HD,STA}$		0.6			µs
Low Period of the SCL Clock	t_{LOW}		1.3			µs
High Period of the SCL Clock	t_{HIGH}		0.6			µs
Setup Time for a Repeated START Condition	$t_{SU,STA}$		0.6			µs
Data Hold Time	$t_{HD,DAT}$	(Note 4)	0		0.9	µs
Data Setup Time	$t_{SU,DAT}$		100			ns
Fall Time of SDA Transmitting	t_F	$I_{SINK} \leq 6mA$, t_R and t_F are measured between 0.3 x V_{DD} and 0.7 x V_{DD}		100		ns
Setup Time for STOP Condition	$t_{SU,STO}$		0.6			µs
Pulse Width of Spike Suppressed	t_{SP}	Input filters on the SDA and SCL inputs suppress noise spikes	0		50	ns

Note 1: All devices are 100% production tested at T_A = +25°C. Temperature limits are guaranteed by design.

Note 2: Guaranteed by design. Green 538nm LED chosen for production so that the IC responds to 100 lux fluorescent light with 100 lux.

Note 3: With respect to green LED 538nm response.

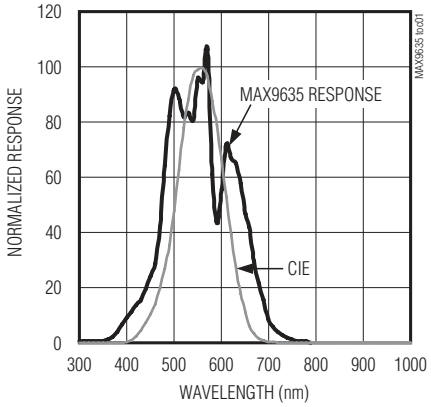
Note 4: A master device must provide a hold time of at least 300ns for the SDA signal (referred to V_{IL} of the SCL signal) to bridge the undefined region of SCL's falling edge.

Industry's Lowest-Power Ambient Light Sensor with ADC

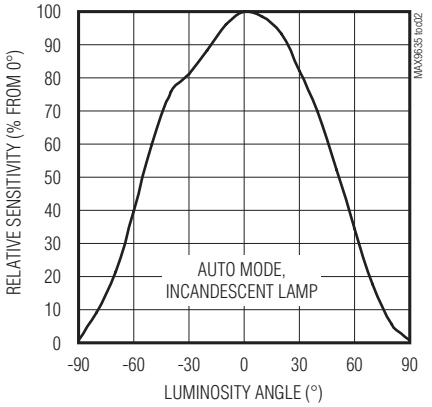
Typical Operating Characteristics

(V_{CC} = 1.8V, default power upsetting; unless otherwise noted.)

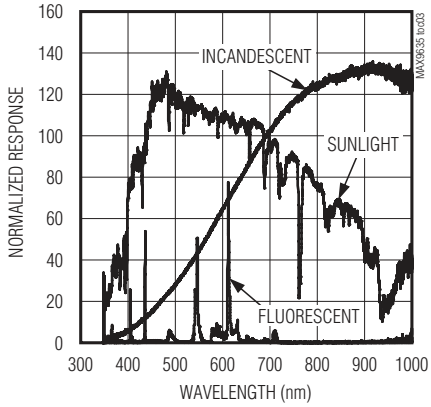
SPECTRUM RESPONSE



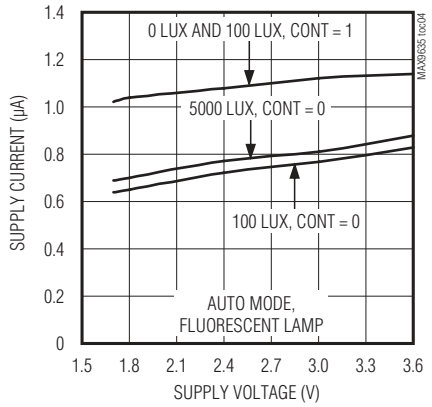
RADIATION PATTERN



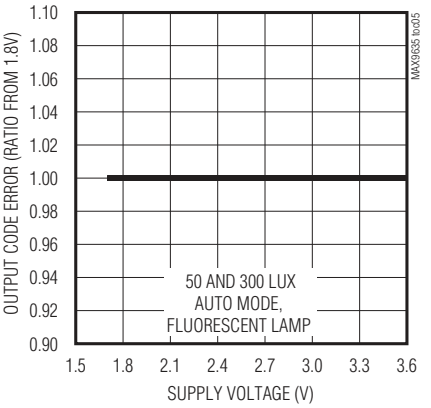
SPECTRUM OF LIGHT SOURCES FOR MEASUREMENT



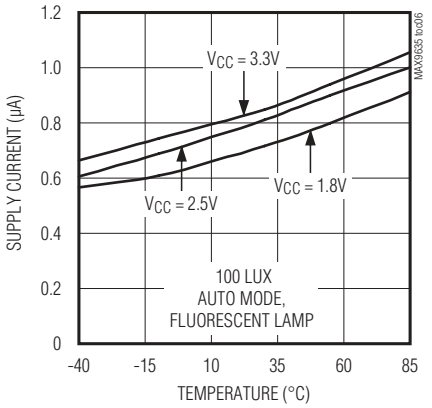
SUPPLY CURRENT vs. SUPPLY VOLTAGE



OUTPUT CODE ERROR vs. SUPPLY VOLTAGE



SUPPLY CURRENT vs. TEMPERATURE

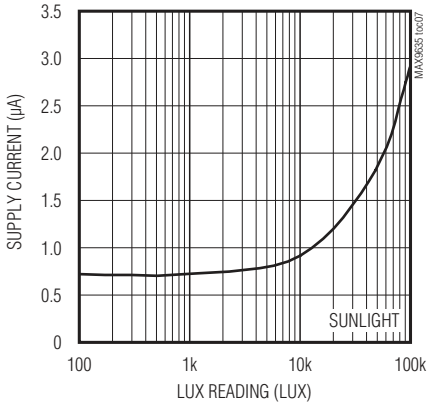


Industry's Lowest-Power Ambient Light Sensor with ADC

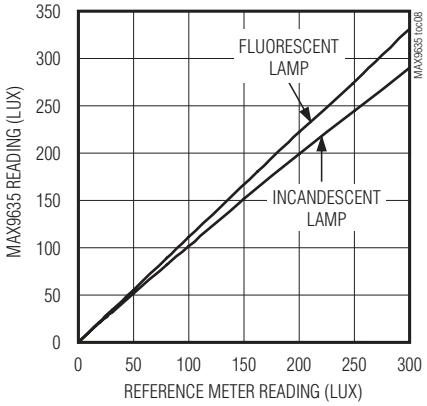
Typical Operating Characteristics (continued)

(V_{CC} = 1.8V, default power upsetting; unless otherwise noted.)

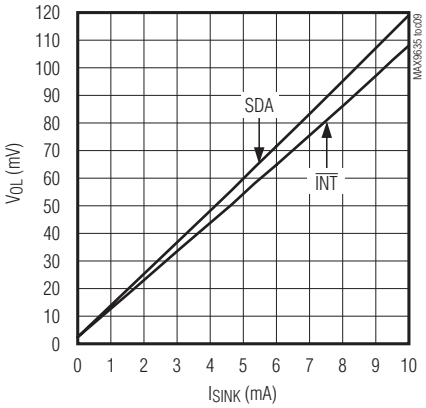
SUPPLY CURRENT vs. LUX READING



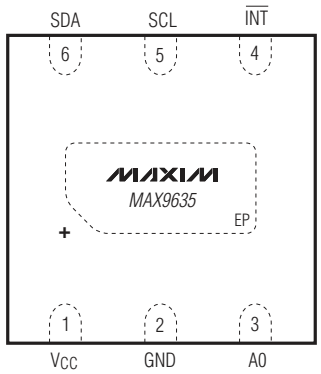
LIGHT SENSITIVITY vs. LUX LEVEL



SDA, $\overline{INT}$ OUTPUT LOW VOLTAGE vs. SINK CURRENT



Pin Configuration



OTDFN
(2mm x 2mm)

Pin Description

PIN	NAME	FUNCTION
1	V_{CC}	Power Supply
2	GND	Ground
3	A0	Address Select. Pull high to select address 0x96 or low to select address 0x94.
4	$\overline{INT}$	Interrupt Output. Use an external pullup resistor.
5	SCL	I²C Clock Bus
6	SDA	I²C Data Bus
—	EP	Exposed Pad. Connect EP to ground.

Industry's Lowest-Power Ambient Light Sensor with ADC

Detailed Description

The MAX9635 is an ambient light sensor with integrated photodiode and ADC with an I²C digital interface. To measure ambient light, the die is placed inside an optically transparent (OTDFN) package. A photodiode inside the IC converts the light to a current that is then processed by low-power circuitry into a digital bit stream. This is digitally processed and stored in an output register that is read by an I²C interface. An on-chip programmable interrupt function eliminates the need for continually polling the device for data and results in significant power saving.

A package-level optical filter prevents ultraviolet and infrared from reaching the photodiode. Its optical response is also designed to match the spectral response of the human eye. A second photodiode array, sensitive primarily to the infrared spectrum, is then used to match flourescent and incandescent light response from the part.

Two key features of the IC analog design are its ultra-low current consumption (typically 0.65µA) and an extremely wide dynamic light range that extends from 0.045 lux to 188,000 lux—more than a 4,000,000 to 1 range. The on-chip autoranging scheme requires no user intervention for the gain-range setting.

The IC can be customized to operate at enhanced sensitivity in applications where it needs to operate behind a dark glass.

The default integration time of the ADC is 100ms, giving it inherent rejection of 50Hz and 60Hz ripple common in certain line-powered light sources.

Human Eye CIE Curve and Different Light Sources

The IC is designed to detect brightness in the same way as human eyes do. To achieve this, the sensor needs to have a spectral sensitivity that is similar to that of human eyes. Figure 1 shows the spectral sensitivity of the IC and the human eye (CIE curve).

As can be seen, the human eye has its peak sensitivity at 555nm (green), while that of blue (~470nm) and red (~630nm) is much lower. The human eye also is blind to infrared (> 700nm) and ultraviolet (< 400nm) radiation.

Light sources can have similar visible brightness (lux), but different IR radiation content (because the human eye is blind to it). The differences in the light spectra affect brightness measurement because some of this infrared radiation is picked up by silicon photodiodes. For example, light sources with high IR content, such as an incandescent bulb or sunlight, would suggest a much brighter environment than our eyes would perceive them to be. Other light sources, such as fluorescent and LED-based systems, have very little infrared content. The IC exhibits good IR rejection and internal IR compensation scheme to minimize these effects and give an accurate lux response.

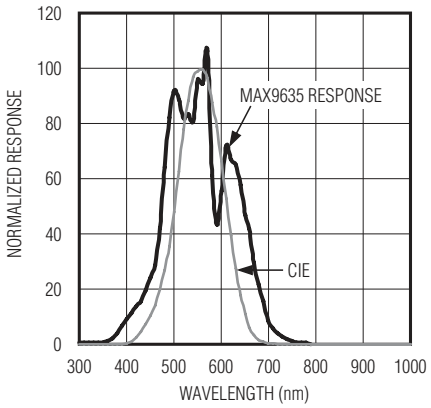


Figure 1. Spectral Sensitivity of the MAX9635 and Human Eye

Register and Bit Descriptions

Table 1. Register Map

REGISTER	BIT								REGISTER ADDRESS	POWER-ON RESET STATE	R/W
	7	6	5	4	3	2	1	0			
STATUS											
Interrupt Status	—	—	—	—	—	—	—	INTS	0x00	0x00	R
Interrupt Enable	—	—	—	—	—	—	—	INTE	0x01	0x00	R/W
CONFIGURATION											
Configuration	CONT	MANUAL	—	—	CDR	TIM[2:0]			0x02	0x03	R/W
LUX READING											
Lux High Byte	E3	E2	E1	E0	M7	M6	M5	M4	0x03	0x00	R
Lux Low Byte	—	—	—	—	M3	M2	M1	M0	0x04	0x00	R
THRESHOLD SET											
Upper Threshold High Byte	UE3	UE2	UE1	UE0	UM7	UM6	UM5	UM4	0x05	0xFF	R/W
Lower Threshold High Byte	LE3	LE2	LE1	LE0	LM7	LM6	LM5	LM4	0x06	0x00	R/W
Threshold Timer	T7	T6	T5	T4	T3	T2	T1	T0	0x07	0xFF	R/W

Interrupt Status 0x00

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	REGISTER ADDRESS
—	—	—	—	—	—	—	INTS	0x01

If the INTE bit is set to 1, then the INTS status bit is asserted if the light intensity exceeds either upper or lower threshold limits (as specified by registers 0x05 and 0x06, respectively) for a period longer than that defined by the Threshold Timer register (0x07). This bit resets to 0 after the host reads this register. See Table 2.

This bit is also reflected on the $\overline{INT}$ pin. When the INTS bit is set, the $\overline{INT}$ pin is asserted low, and when the INTS bit is set to 0, the $\overline{INT}$ pin is pulled high by an external resistor.

Once this bit is set, it can be cleared either by reading the Interrupt Status register 0x00 or by writing a 0 to the Interrupt Enable register 0x01.

Table 2. Interrupt Status Register

BIT 0	OPERATION
0	No interrupt trigger event has occurred.
1	Ambient light intensity is outside the threshold window range for a longer than specified time.

Interrupt Enable 0x01

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	REGISTER ADDRESS
—	—	—	—	—	—	—	INTS	0x01

Industry's Lowest-Power Ambient Light Sensor with ADC

Interrupt events set the INTS bit (register 0x00, bit 0) and the $\overline{INT}$ pin only if the INTE bit is set to 1. If the INTE bit is set (interrupt is enabled) and the interrupt condition is triggered, then the $\overline{INT}$ pin is pulled low (asserted) and the INTS bit in the Interrupt Status register is set to 1. See Table 3.

Table 3. Interrupt Enable Register

BIT 0	OPERATION
0	The $\overline{INT}$ pin and the INTS bit are not asserted even if an interrupt event has occurred.
1	Detection of an interrupt event triggers a hardware interrupt ($\overline{INT}$ pin is pulled low) and sets the INTS bit (register 0x00, bit 0).

Configuration 0x02

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	REGISTER ADDRESS
CONT	MANUAL	—	—	CDR	TIM[2:0]			0x02

Continuous Mode

Table 4. Continuous Mode Register

BIT 7	OPERATION
0	Default mode. The IC measures lux intensity only once every 800ms regardless of integration time. This mode allows the part to operate at its lowest possible supply current.
1	Continuous mode. The IC continuously measures lux intensity. That is, as soon as one reading is finished, a new one begins. If integration time is 6.25ms, readings are taken every 6.25ms. If integration time is 800ms, readings are taken every 800ms. In this mode, the part consumes slightly higher power than in the default mode.

Note: *Continuous mode is independent of the manual configuration mode setting.*

Manual Configuration Mode

In automatic mode (MANUAL = 0), reading the contents of TIM[2:0] and CDR bits reflects the automatically generated values from an internal timing register and are read-only. In manual mode (MANUAL = 1), the contents of TIM[2:0] and CDR bits can be modified by the users through the I²C bus.

Table 5. Manual Configuration Register

BIT 6	OPERATION
0	Default mode of configuration is used for the IC. In this mode, CDR and TIM[2:0] bits are automatically determined by the internal autoranging circuitry of the IC.
1	Manual mode of configuration is used for the IC. In this mode, CDR and TIM[2:0] bits can be programmed by the user.

Current Division Ratio (CDR)

The CDR bit controls the current division ratio. The photodiode current is divided as shown in Table 6.

Table 6. Current Division Ratio Register

BIT 3	OPERATION
0	Current not divided. All of the photodiode current goes to the ADC.
1	Current divided by 8. Only 1/8 of the photodiode current goes to the ADC. This mode is used in high-brightness situations.

Integration Timer Bits (TIM[2:0])

The TIM[2:0] bits can be used to program the signal integration time.

In automatic mode (MANUAL = 0), integration time is automatically selected by the on-chip algorithm to be either 100ms/200ms/400ms/800ms. In manual mode (MANUAL = 1), integration time can be varied by the user all the way from 6.25ms to 800ms. See Table 7.

Table 7. Integration Time

TIM[2:0]	INTEGRATION TIME (ms)	COMMENTS
000	800	This is a preferred mode for boosting low-light sensitivity.
001	400	—
010	200	—
011	100	This is a preferred mode for high-brightness applications.
100	50	Manual mode only.
101	25	Manual mode only.
110	12.5	Manual mode only.
111	6.25	Manual mode only.

Lux High-Byte Register 0x03

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	REGISTER ADDRESS
E3	E2	E1	E0	M7	M6	M5	M4	0x03

Bits in Lux High-Byte register 0x03 give the 4 bits of exponent E3:E0 and 4 most significant bits of the mantissa byte M7:M4, and represent the lux reading of ambient light. The remaining 4 bits of the mantissa byte M3:M0 are in the Lux Low-Byte register 0x04 and enhance resolution of the lux reading from the IC.

Exponent (E[3:0]): Exponent bits of the lux reading (0000 to 1110). **Note:** A reading of 1111 represents an overrange condition.

Mantissa (M[7:4]): Four most significant bits of mantissa byte of the lux reading (0000 to 1111).

Lux = $2^{(exponent)}$ x mantissa x 0.72

Exponent = 8xE3 + 4xE2 + 2xE1 + E0

Mantissa = 8xM7 + 4xM6 + 2xM5 + M4

A code of 0000 0001 calculates to be 0.72 lux.

A code of 1110 1111 calculates to be 176,947 lux.

A code of 1110 1110 calculates to be 165,151 lux.

Update of the contents of this register is internally disabled during I^2C read operations to ensure proper data transfer between internal ADC and I^2C registers. Update of I^2C registers is resumed when the master sends a STOP command.

If user wants to read both the Lux High-Byte register 0x03 and Lux Low-Byte register 0x04, then the master should not send a STOP command between the reads of the two registers. Instead a REPEATED START command should be used. This ensures accurate data is obtained from the I^2C registers (by disabling internal updates during the read process).

Industry's Lowest-Power Ambient Light Sensor with ADC

Lux Low-Byte Register 0x04

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	REGISTER ADDRESS
—	—	—	—	M3	M2	M1	M0	0x04

Bits in Lux Low-Byte register 0x04 give the 4 least significant bits of the mantissa byte representing the lux reading of ambient light. Combined with the Lux High-Byte register 0x03, it extends the resolution and dynamic range of lux measurements of the IC.

E3–E0: Exponent bits of lux reading

M7–M0: Mantissa byte of lux reading

Lux = $2^{(exponent)}$ x mantissa x 0.045

Exponent = 8xE3 + 4xE2 + 2xE1 + E0

Mantissa = 128xM7 + 64xM6 + 32xM5 + 16xM4 + 8xM3 + 4xM2 + 2xM1 + M0

Combining contents of register 0x03 and 0x04:

A code of 0000 0000 0001 calculates to be 0.045 lux.

A code of 0000 0001 0000 calculates to be 0.72 lux.

A code of 0001 0001 0001 calculates to be 0.765 lux.

A code of 1110 1111 1111 calculates to be 188,006 lux.

A code of 1110 1111 1110 calculates to be 187, 269 lux.

The Lux High-Byte 0x03 and Lux Low-Byte 0x04 register updates are internally disabled at the start of a valid address transmission from the master. Updating reinitiates at the next valid STOP condition. This prevents erroneous readings, in the event an update occurs between readings of registers 0x03 and 0x04.

Update of the contents of this register is internally disabled during I²C read operations to ensure proper data transfer between internal ADC and I²C registers. Update of I²C registers is resumed when the master sends a STOP command.

If the user wants to read both the Lux High-Byte register 0x03 and Lux Low-Byte register 0x04, then the master should not send a STOP command between the reads of the two registers. Instead a REAPEATED START command should be used. This ensures accurate data is obtained from the I²C registers (by disabling internal updates during the read process).

Upper Threshold High-Byte Register 0x05

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	REGISTER ADDRESS
UE3	UE2	UE1	UE0	UM7	UM6	UM5	UM4	0x05

The Upper Threshold register exponent with the four most significant bits of the mantissa sets the upper trip level for interrupt functionality. This upper limit is relevant only if the INTE bit in the Interrupt Enable register is set. If the lux level is greater than this light level for a time greater than that specified in the Threshold Timer register, the INTS bit in the Interrupt Status register is set and the $\overline{INT}$ pin is pulled low.

Mantissa (UM[7:4]): Four most significant bits of mantissa upper threshold

Exponent (UE[3:0]): Exponent bits upper threshold

Upper lux threshold = $2^{(exponent)}$ x mantissa x 0.045

Exponent = 8xUE3 + 4xUE2 + 2xUE1 + UE0

Mantissa = 128xUM7 + 64xUM6 + 32xUM5 + 16xUM4 + 15

Lower Threshold High-Byte Register 0x06

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	REGISTER ADDRESS
LE3	LE2	LE1	LE0	LM7	LM6	LM5	LM4	0x06

The Lower Threshold register exponent with the four most significant bits of the mantissa sets the lower trip level for interrupt functionality. This lower limit is relevant only if the INTE bit in the Interrupt Enable register is set. If the lux level is below this light level for a time greater than that specified in the Threshold Timer register, the INTS bit in the Interrupt Status register is set and the $\overline{INT}$ pin is pulled low.

Mantissa (LM[7:4]): Four most significant bits of mantissa lower threshold

Exponent (LE[3:0]): Exponent bits lower threshold

Lower lux threshold = $2^{(exponent)}$ x mantissa x 0.045

Exponent = 8xLE3 + 4xLE2 + 2xLE1 + LE0

Mantissa = 128xLM7 + 64xLM6 + 32xLM5 + 16xLM4

Threshold Timer Register 0x07

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	REGISTER ADDRESS
T7	T6	T5	T4	T3	T2	T1	T0	0x07

If the INTE bit = 1 and the ambient light level exceeds either threshold limit for a time longer than that specified by the Threshold Timer register, then the INTS bit is set to 1 and the $\overline{INT}$ pin is pulled low.

The value in this register sets the time used to control this delay. A value of 0x00 in this register (with INTE bit = 1 in the Interrupt Enable register) configures the IC to assert the interrupt pin as soon as the light level exceeds either threshold. Time delay = (128xT7 + 64xT6 + 32xT5 + 16xT4 + 8xT3 + 4xT2 + 2xT1 + T0) x 100ms.

Applications Information

Auto and Manual Modes

In auto mode configuration (default setting), CDR and TIM bits are internally generated. The autoranging circuit uses two different methods to change its sensitivity. For light intensities greater than 700 lux, a current divider reduces the photodiode's current by a factor of 8. The default, as in the previous example, is a division of 1: current goes directly into the I to F converter. As light intensity decreases, the autoranging circuit increases the integration time from 100ms to 200ms to 400ms, or to 800ms. The combination of the current divider and the different integration times give the A/D a range 8 times higher, as well as 8 times lower, than its nominal 16-bit range. This gives a dynamic range of 22 bits or slightly over 4,000,000 to 1.

In manual mode, the user has access to 4 bits (CDR and TIM[2:0]) to override the autoranging circuitry. These affect the integration time of the A/D and the current division ratio. See the register description for manual configuration mode (0x02, bit 6).

Data Format of Lux Reading

The IC has a user-friendly digital output format. It consists of a 4-bit exponent followed by an 8-bit mantissa. In its highest sensitivity mode, 1 count represents 0.045 lux. The mantissa has a maximum value of 255, and the exponent has a maximum value of 14. This gives a maximum range: 255 x 2^{14} = 4,177,920. At 0.045 lux/LSB, the maximum lux reading is 188,000 lux. Any reading greater than that (i.e., exponent = 15) is considered to be an overload. No conversion formulas are needed as in the case of dual-diode ambient light sensors.

The IC's output (registers 0x03 and 0x04) comprises a 12-bit result that represents the ambient light expressed in units of lux.

Here is how lux is calculated:

Lux = ($2^{(exponent)}$ x mantissa) x 0.045

The exponent is a 4-bit number ranging from 0000 to 1110 (zero to 14).

The mantissa is an 8-bit number ranging from 0000 0000 to 1111 1111 (zero to 255).

Industry's Lowest-Power Ambient Light Sensor with ADC

The count is multiplied by 0.045, which is the LSB.

Because of the logarithmic nature of autoranging circuitry implemented on the IC, resolution of ambient lux readings scale with the absolute measurement. Table 8 lists the lux resolution and the lux ranges obtained from the IC.

Interrupt Settings

Interrupt is enabled by setting bit 0 of register 0x01 to 1 (see Table 1). $\overline{INT}$, an open-drain output, pulls low when an interrupt condition occurs (lux readings that exceed threshold limits for a period greater than that set by the Time register). The interrupt status bit is cleared automatically if register 0x00 is read or if the interrupt is disabled (INTE = 0).

Threshold Register Data Format

The IC's interrupt circuit requires the upper and lower limit thresholds to be in a specific format to be properly interpreted. The upper and lower limits, from registers 0x05 and 0x06 must match the lux high-byte format. This consists of the 4 bits of the exponent and the 4 most significant bits of the mantissa (E3 E2 E1 E0 M7 M6 M5 M4).

In this case, there is the following formula:

Lower lux threshold = ($2^{(exponent)}$ x mantissa) x 0.045

The exponent is a 4-bit number ranging from 0000 to 1110 (zero to 14).

The mantissa is an 8-bit number ranging from 0000 0000 to 1111 0000 (zero to 240).

Upper lux threshold = ($2^{(exponent)}$ x mantissa) x 0.045

The exponent is a 4-bit number ranging from 0000 to 1110 (zero to 14).

The mantissa is an 8-bit number ranging from 0000 1111 to 1111 1111 (15 to 255).

In the auto range mode (MANUAL = 0), the upper threshold and lower threshold bytes must be in a format that matches the format used in register 0x03, the lux high byte. There are only two rules to follow:

- For very low lux levels (light levels below 11.5 lux), set the exponent to zero, the code is merely: 0000 MMMM where the 4 zeroes are the exponent, and the MMMM represent the 4 most significant bits of the mantissa.
- For all other conditions (light levels above 11.5 lux) where the exponent is not zero, the format is: EEEE 1MMM. Notice that bit M7 (most significant bit) must always be a 1. The other bits do not matter. EEEE is limited to a maximum value of 1110. The maximum usable setting is a code of 1110 1111.

In manual mode (MANUAL = 1), Table 9 gives the range of exponent (E3 E2 E1 E0) that can be used for each TIM[2:0] and CDR bit setting.

Table 8. Lux per LSB in Automatic Mode

LUX (MIN)	LUX (MAX)	LUX PER LSB IN AUTOMATIC MODE	COUNTS (MIN)	COUNTS (MAX)
0	11.5	0.045	0	256
11.5	23.0	0.09	256	512
23.0	46.1	0.18	512	1024
46.1	92.2	0.36	1024	2048
92.2	184.3	0.72	2048	4096
184.3	368.6	1.44	4096	8192
368.6	737.3	2.88	8192	16,384
737.3	1474.6	5.76	16,384	32,768
1474.6	2949.1	11.52	32,768	65,536
2949.1	5898.2	23.04	65,536	131,072
5898.2	11,796.5	46.08	131,072	262,144
11,796.5	23,593.0	92.16	262,144	524,288
23,593.0	47,185.9	184.32	524,288	1,048,576
47,185.9	94,371.8	368.64	1,048,576	2,097,152
94,371.8	188,006.4	737.28	2,097,152	4,177,920

Table 9. Recommended Manual Mode Settings for Configuration Register (0x02) and Threshold Registers (0x05, 0x06)

APPLICATION CONDITIONS				RECOMMENDED SETTINGS FOR CONFIGURATION REGISTER (0x02)		RANGE OF EXPONENTS FOR UPPER AND LOWER THRESHOLD REGISTERS (0x05 AND 0x06)	
LUX LSB (MIN)	LUX (MAX)	LUX LSB (MAX)	INTEGRATION TIME (ms)	TIM[2:0]	CDR	EXPONENT (MIN)	EXPONENT (MAX)
0.045	2938	11.52	800	000	0	0000	1000
0.09	5875	23.04	400	001	0	0001	1001
0.18	11,750	46.08	200	010	0	0010	1010
0.36	23,501	92.16	100	011	0	0011	1011
			800	000	1		
0.72	47,002	184.32	50	100	0	0100	1100
			400	001	1		
1.44	94,003	368.64	25	101	0	0101	1101
			200	010	1		
2.88	188,006	737.28	12.5	110	0	0110	1110
			100	011	1		
5.76	188,006	737.28	6.25	111	0	0111	1110
			50	100	1		
11.52	188,006	737.28	25	101	1	1000	1110
23.04	188,006	737.28	12.5	110	1	1001	1110
46.08	188,006	737.28	6.25	111	1	1010	1110

Note: *In manual mode, exceeding the lux (max) causes an overload error (exponent = 1111).*

Typical Operating Sequence

To utilize the ultra-low power consumption of the IC in end applications, an interrupt pin is provided to eliminate the need for the system to poll the device continuously. Since every clock and data bit transmitted on I²C can consume up to 1mA (assuming 1.8kΩ pullup resistor to a 1.8V rail), minimizing the number of I²C transactions on the data bus can save a lot of power. In addition, eliminating the need to poll the device frees up processing resources for the master, improving overall system performance.

The typical sequence of communication with the IC is as follows:

1) Master reads lux reading from registers 0x03 and 0x04.
2) Master sets the upper lux threshold and lower lux threshold in registers 0x05 and 0x06 so that a user-programmed window is defined around the current lux readings.
3) Master sets suitable threshold timer data in register 0x07.
4) Master works on other tasks until alerted by the $\overline{INT}$ pin going low. This is where the master spends much of its time.
5) When alerted by the $\overline{INT}$ pin going low, the master reads the Interrupt Status register 0x00 to confirm the source of interrupt was the IC. The master takes appropriate action.
6) Repeat from Step 1.

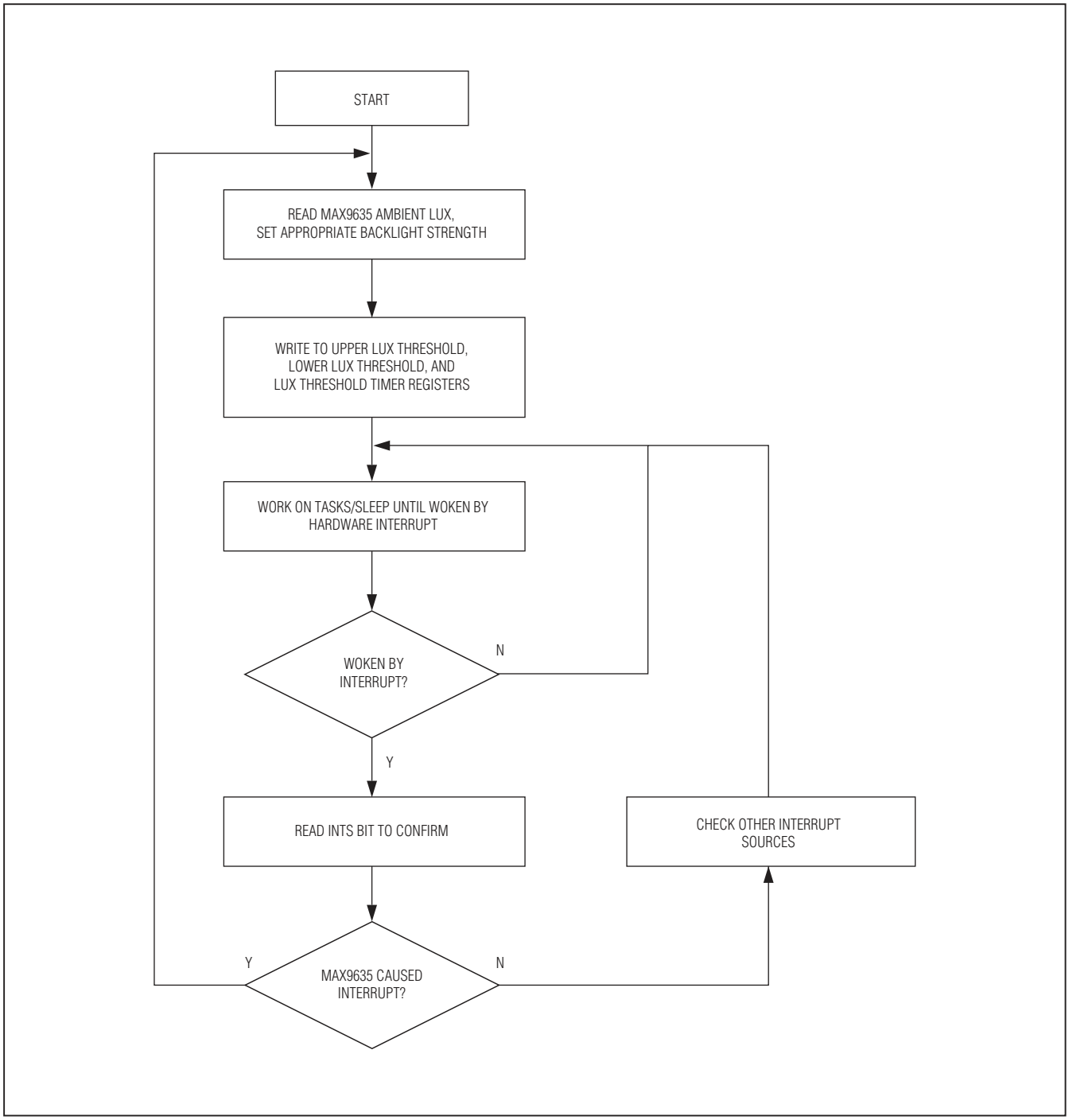


Figure 2. Typical Operating Sequence

I²C Serial Interface

The IC features an I2C/SMBus™-compatible, 2-wire serial interface consisting of a serial-data line (SDA) and a serial-clock line (SCL). SDA and SCL facilitate communication between the IC and the master at clock rates up to 400kHz. Figure 3 shows the 2-wire interface timing diagram. The master generates SCL and initiates data transfer on the bus. A master device writes data to the IC by transmitting the proper slave address followed by the register address and then the data word. Each transmit sequence is framed by a START (S) or REPEATED START (Sr) condition and a STOP (P) condition. Each word transmitted to the IC is 8 bits long and is followed by an acknowledge clock pulse. A master reading data from the IC transmits the proper slave address followed by a series of nine SCL pulses. The IC transmits data on SDA in sync with the master-generated SCL pulses. The master acknowledges receipt of each byte of data. Each read sequence is framed by a START or REPEATED START condition, a not acknowledge, and a STOP condition. SDA operates as both an input and an open-drain output. A pullup resistor, typically greater than 500Ω, is required on the SDA bus. SCL operates as only an input. A pullup resistor, typically greater than 500Ω, is required on SCL if there are multiple masters on the bus, or if the master in a single-master system has an open-drain SCL output. Series resistors in line with SDA and SCL are optional. Series resistors protect the digital inputs of the IC from high-voltage spikes on the bus lines, and minimize crosstalk and undershoot of the bus signals.

Bit Transfer

One data bit is transferred during each SCL cycle. The data on SDA must remain stable during the high period of the SCL pulse. Changes in SDA while SCL is high are control signals (see the *START* and *STOP Conditions* section). SDA and SCL idle high when the I2C bus is not busy.

START and STOP Conditions

SDA and SCL idle high when the bus is not in use. A master initiates communication by issuing a START condition. A START condition is a high-to-low transition on SDA with SCL high. A STOP condition is a low-to-high transition on SDA while SCL is high (Figure 4). A START condition from the master signals the beginning of a transmission to the IC. The master terminates transmission, and frees the bus, by issuing a STOP condition. The bus remains active if a REPEATED START condition is generated instead of a STOP condition.

Early STOP Conditions

The IC recognizes a STOP condition at any point during data transmission except if the STOP condition occurs in the same high pulse as a START condition. For proper operation, do not send a STOP condition during the same SCL high pulse as the START condition.

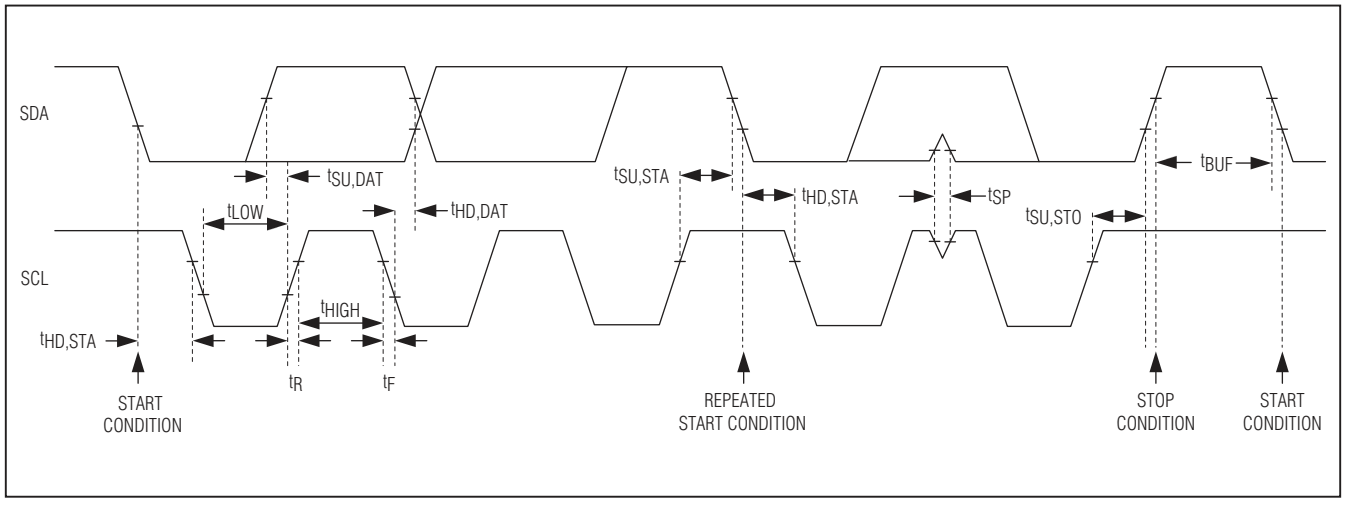


Figure 3. 2-Wire Interface Timing Diagram

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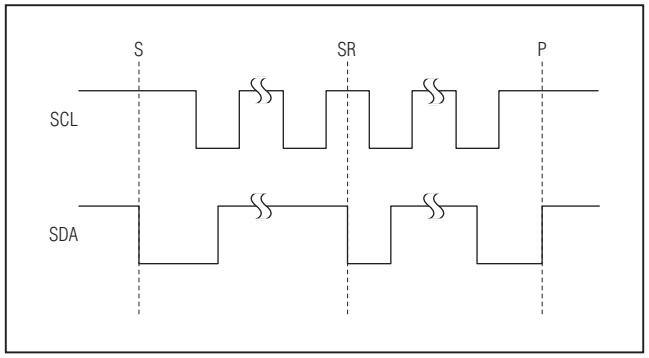


Figure 4. START, STOP, and REPEATED START Conditions

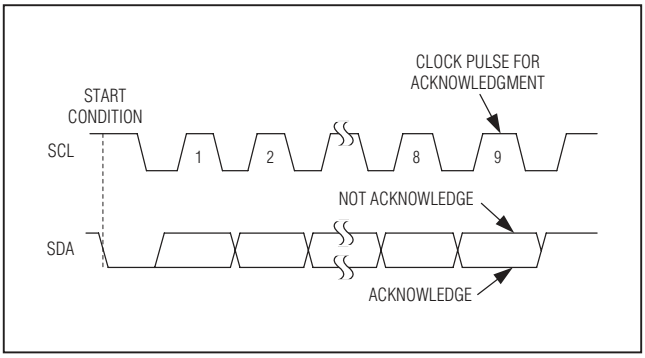


Figure 5. Acknowledge

Slave Address

The slave address is controlled by the A0 pin. Connect A0 to either ground or V_{CC} to set the address. Table 10 shows the two possible addresses for the IC.

Acknowledge

The acknowledge bit (ACK) is a clocked 9th bit that the IC uses to handshake receipt each byte of data when in write mode (see Figure 5). The IC pulls down SDA during the entire master-generated ninth clock pulse if the previous byte is successfully received. Monitoring ACK allows for detection of unsuccessful data transfers. An unsuccessful data transfer occurs if a receiving device is busy or if a system fault has occurred. In the event of an unsuccessful data transfer, the bus master can retry communication. The master pulls down SDA during the ninth clock cycle to acknowledge receipt of data when the IC is in read mode. An acknowledge is sent by the master after each read byte to allow data transfer to continue. A not acknowledge is sent when the master reads the final byte of data from the IC, followed by a STOP condition.

Write Data Format

A write to the IC includes transmission of a START condition, the slave address with the R/$\overline{W}$ bit set to 0, one byte of data to configure the internal register address pointer, one or more bytes of data, and a STOP condition. Figure 6 illustrates the proper frame format for writing one byte of data to the IC.

Table 10. Slave Address

A0	SLAVE ADDRESS FOR WRITING	SLAVE ADDRESS FOR READING
GND	0x94	0x95
V_{CC}	0x96	0x97

The slave address with the R/$\overline{W}$ bit set to 0 indicates that the master intends to write data to the IC. The IC acknowledges receipt of the address byte during the master-generated ninth SCL pulse.

The second byte transmitted from the master configures the IC's internal register address pointer. The pointer tells the IC where to write the next byte of data. An acknowledge pulse is sent by the IC upon receipt of the address pointer data.

The third byte sent to the IC contains the data that is written to the chosen register. The master signals the end of transmission by issuing a STOP condition.

Read Data Format

To read a byte of data, the register pointer must first be set through a write operation (Figure 7). Send the slave address with the R/$\overline{W}$ set to 0, followed by the address of the register that needs to be read. After a repeated start condition, send the slave address with the R/$\overline{W}$ bit set to 1 to initiate a read operation. The IC then sends an acknowledge pulse followed by the contents of the register to be read. Transmitted data is valid on the rising edge of the master-generated serial clock (SCL).

Sensor Position

The photo sensitive area of the IC is 0.37mm x 0.37mm and much smaller than the device itself. When placing the part behind a light guide, only this sensitive area has to be taken into account. Figure 8 shows the position and size of the photo sensitive area within the package.

Chip Information

PROCESS: BiCMOS

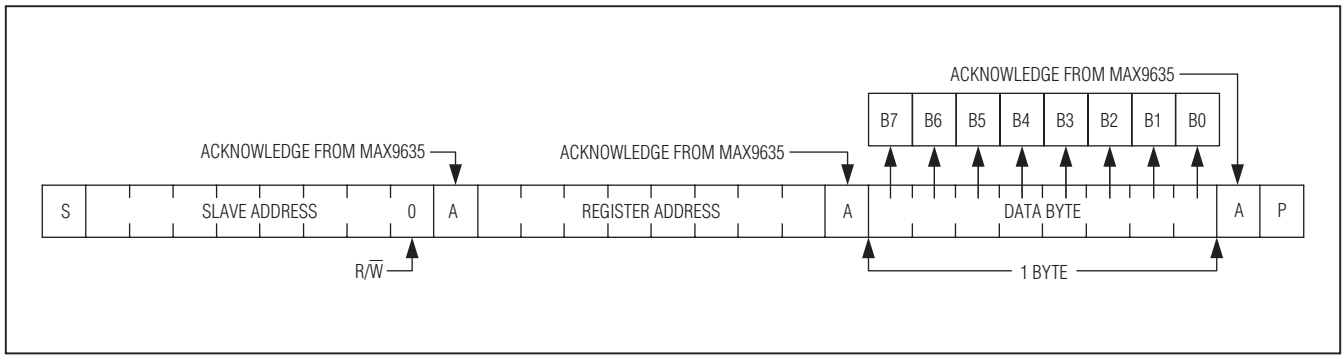


Figure 6. Writing 1 Byte of Data to the IC

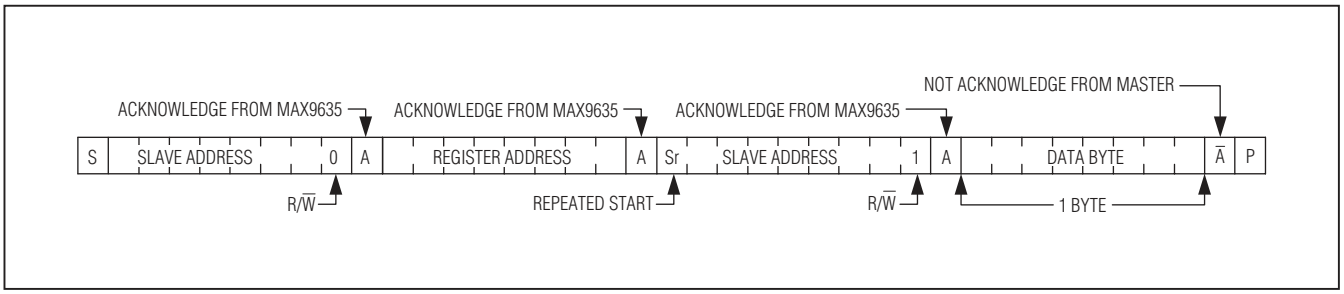


Figure 7. Reading One Indexed Byte of Data from the IC

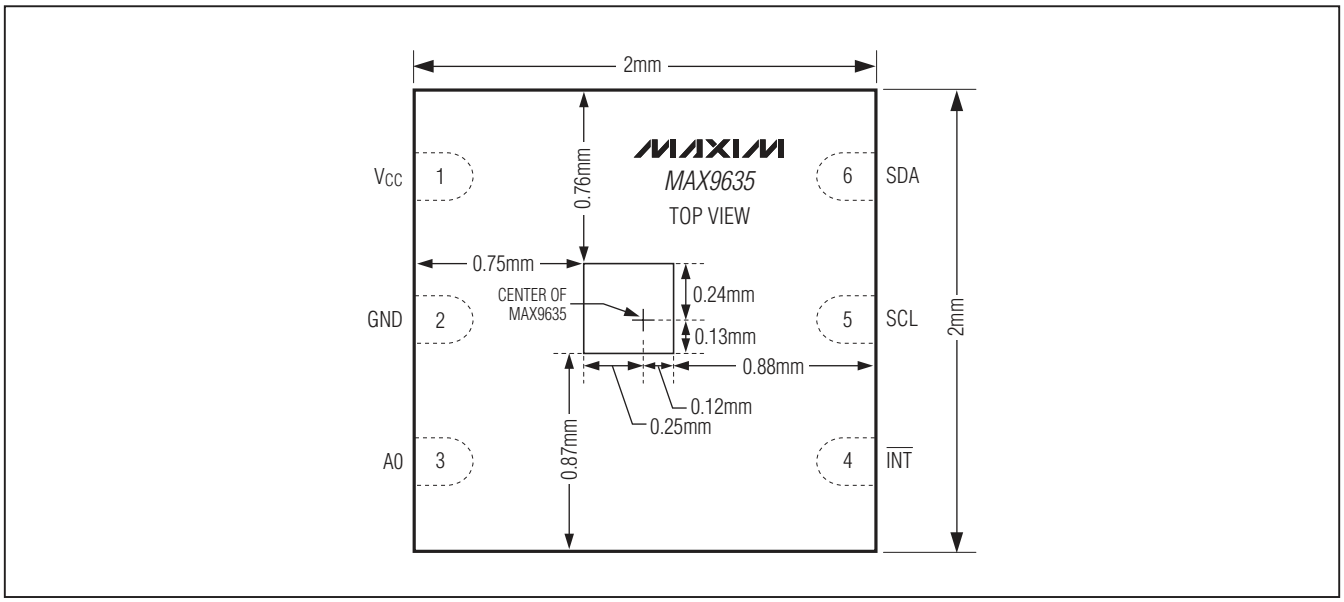
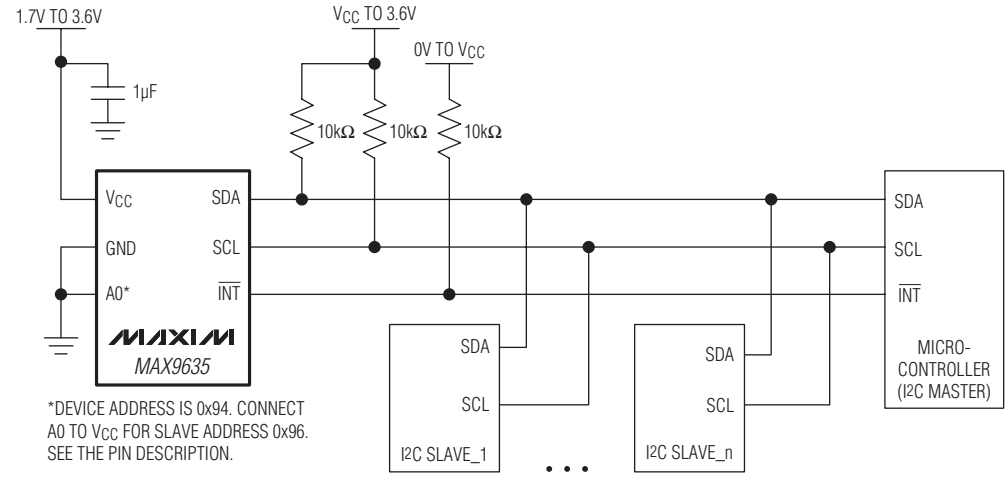


Figure 8. Sensor Position

Industry's Lowest-Power Ambient Light Sensor with ADC

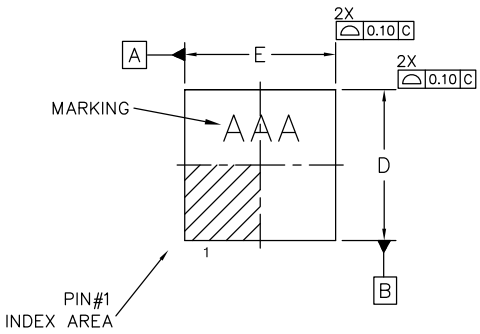
Typical Application Circuit



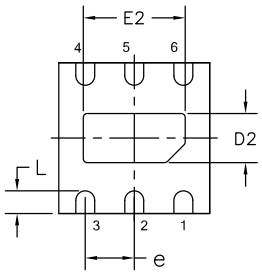
Package Information

For the latest package outline information and land patterns (footprints), go to **www.maxim-ic.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
6 OTDFN	D622N+1	21-0490	90-0344



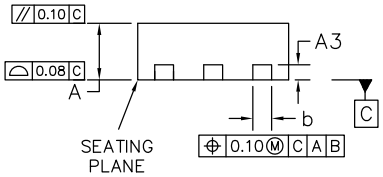
TOP VIEW



BOTTOM VIEW

SYMBOL	COMMON DIMENSIONS		
	MIN.	NOM.	MAX.
A3	0.195	0.203	0.211
b	0.20	0.25	0.30
D	1.925	2.000	2.075
E	1.925	2.000	2.075
e	0.65 BSC		
L	0.25	0.30	0.35
PKGCODES: D622N+1; D622N+2			

SYMBOL	DIMENSION VARIATIONS		
	MIN.	NOM.	MAX.
A	0.55	0.60	0.65
E2	1.25	1.35	1.45
D2	0.55	0.65	0.75



SIDE VIEW

NOTES:
1. DIMENSION & TOLERANCING CONFORM TO ASME Y14.5M–1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.20mm AND 0.30mm FROM TERMINAL TIP.
4. MARKING SHOWN IS FOR PACKAGE ORIENTATION PURPOSE ONLY.
5. ALL DIMENSIONS APPLY TO PbFREE (+) PKGCODES ONLY.

–DRAWING NOT TO SCALE–

MAXIM

TITLE: PACKAGE OUTLINE, 6L, 2x2 OPTO TDFN PKG. NiPd PLATING			
APPROVAL	DOCUMENT CONTROL NO. 21–0490	REV. C	1/1

Industry's Lowest-Power Ambient Light Sensor with ADC

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	8/10	Initial release	—
1	2/11	Updated test time and repeatability	2
2	5/11	Updated Note 2	3