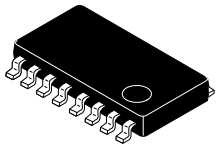
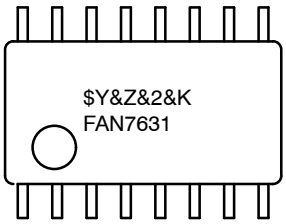
Advanced Pulse Frequency Modulation (PFM) Controller for Half-Bridge Resonant Converters

FAN7631



SOP16
CASE 565BF

MARKING DIAGRAM



FAN7631 = Device Code
$Y = Logo
&Z = Assembly Plant Code
&2 = 2−Digit Date Code
&K = 2−Digits Lot Run Traceability Code

ORDERING INFORMATION

See detailed ordering and shipping information on page 17 of this data sheet.

Related Resources

AN4151 — Half−Bridge LLC Resonant Converter Design Using FSFR−Series Power Switch

Description

The FAN7631 is a pulse−frequency modulation controller for high−efficiency half−bridge resonant converters that includes a high−side gate drive circuit, an accurate current−controlled oscillator, and various protection functions. The FAN7631 features include variable dead time, operating frequency up to 600 kHz, protections such as LUVLO, and a selectable latch or A/R protection using the LS pin for user convenience.

The Zero−Voltage−Switching (ZVS) technique reduces the switching losses and improves the efficiency significantly. ZVS also reduces the switching noise noticeably, which allows a small Electromagnetic Interference (EMI) filter.

Offering everything necessary to build a reliable and robust resonant converter, the FAN7631 simplifies designs and improves productivity and performance. The FAN7631 can be applied to resonant converter topologies such as series resonant, parallel resonant, and LLC resonant converters.

Features

- Variable Frequency Control with 50% Duty Cycle for Half−Bridge Resonant Converter Topologies
- High Efficiency with Zero−Voltage−Switching (ZVS)
- Up to 600 kHz Operating Frequency
- Built−in High−Side Gate Driver
- High Gate−Driving Current: +500 mA/−1000 mA
- Programmable Dead Time with a Resistor
- Pulse Skipping and Burst Operation for Frequency Limit (Programmable) at Light−Load Condition
- Simple Remote On/Off Control with Latch or Auto−Restart (A/R) Using FI or LS Pin
- Protection Functions: Over−Voltage Protection (OVP), Overload Protection (OLP), Over−Current Protection (OCP), Abnormal Over−Current Protection (AOCP), Internal Thermal Shutdown (TSD), and High Precise Line Under−Voltage Lockout (LUVLO)
- Level−Change OCP Function During Startup

Applications

- PDP and LCD Tvs
- Desktop PCs and Servers
- Video Game Consoles
- Adapters
- Telecom Power Supplies

APPLICATION CIRCUIT DIAGRAM

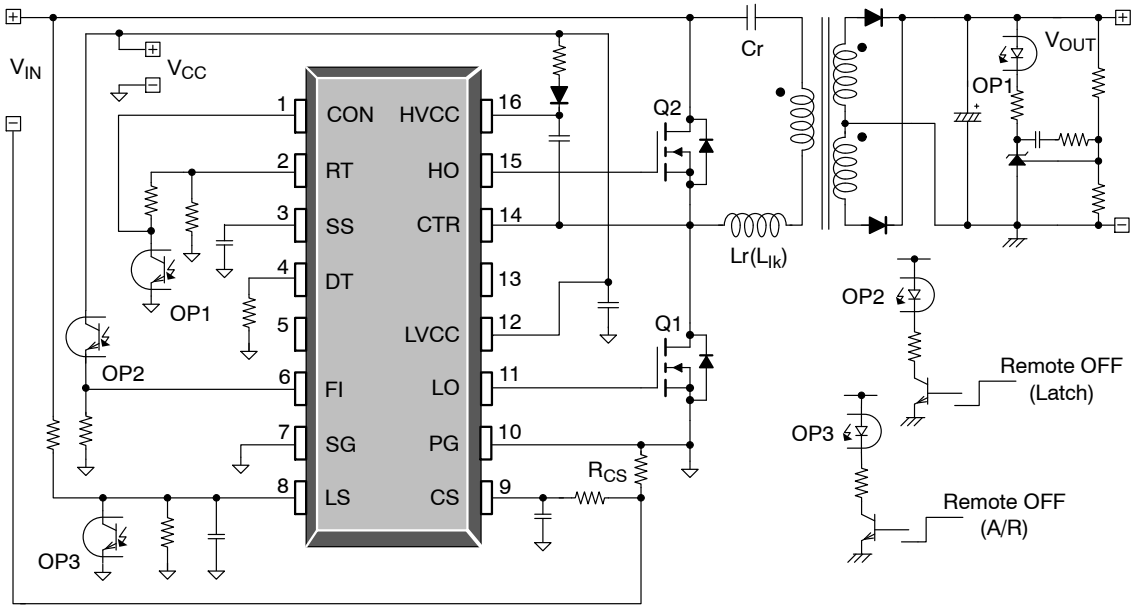


Figure 1. Typical Application Circuit (Resonant Half−Bridge Converter)

BLOCK DIAGRAM

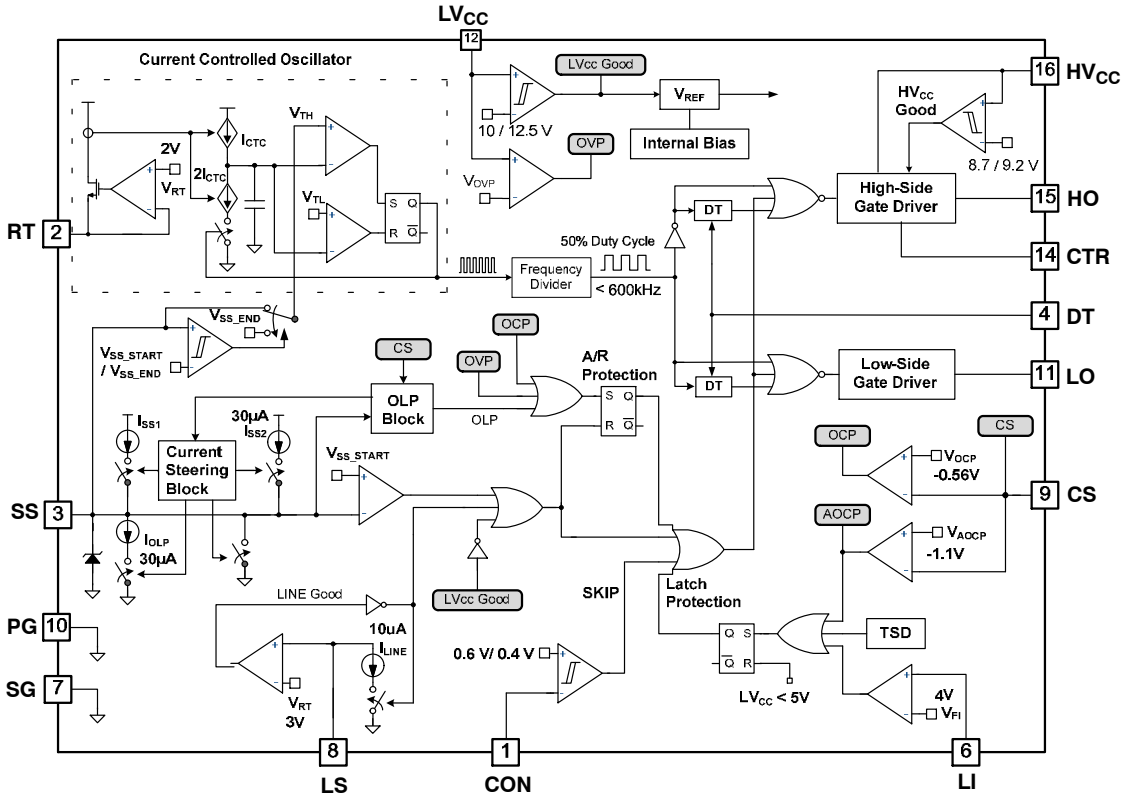


Figure 2. Internal Block Diagram

PIN CONFIGURATION

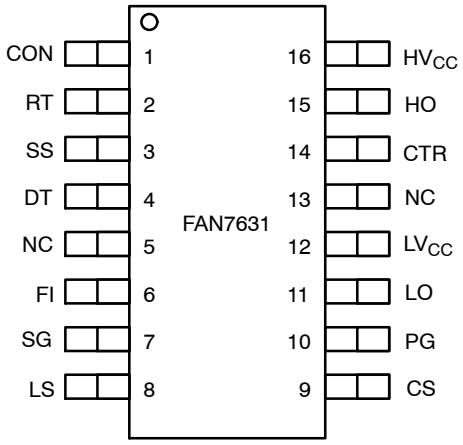


Figure 3. Package Pin Assignments (SOP16)

PIN DEFINITIONS

Pin No.	Name	Description
1	CON	This pin is used to enable / disable the gate drive outputs for pulse−skipping operation. When the voltage of this pin is above 0.6 V, the gate drive outputs are enabled. When the voltage of this pin drops below 0.4 V, gate drive signals for both MOSFETs are disabled.
2	RT	This pin programs the switching frequency. Typically, an opto−coupler is connected to this pin to control the switching frequency for the output voltage regulation.
3	SS	This pin is used to program the soft−start time and overload protection delay. It also programs the restart delay when the converter auto recovers from the protection states. Typically, a small capacitor is connected on this pin.
4	DT	This pin is to adjust the dead time using an external resistor.
5	NC	No connection
6	FI	User protection function / fault input. This pin can be used as a latch protection, which is operated when a voltage applied to this pin is higher than $4V_{DC}$.
7	SG	This pin is the ground of the control part.
8	LS	This pin senses the line voltage for line under−voltage lockout (LUVLO).
9	CS	This pin senses the current flowing through the main MOSFET. Typically, negative voltage is applied on this pin.
10	PG	This pin is the power ground. This pin typically connects to the source of the low−side MOSFET.
11	LO	This pin is used for the low−side gate−driving signal.
12	LV_{CC}	This pin is for the supply voltage of the control IC and low−side gate−driving circuit.
13	NC	No connection
14	CTR	This pin is connected to the drain of the low−side MOSFET. Typically, a transformer is connected to this pin.
15	HO	This pin is used for the high−side gate−driving signal.
16	HV_{CC}	This pin is used for the supply voltage of the high−side gate−driving circuit.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Min	Max	Unit
HV_{CC} to V_{CTR}	High−Side V_{CC} Pin to Center Voltage	−0.3	25.0	V
HV_{CC}	High−Side Floating Supply Voltage	−0.3	625.0	V
V_{HO}	High−Side Gate\−Driving Voltage	V_{CTR} − 0.3	HV_{CC} + 0.3	V
V_{CTR}	High−Side Offset Voltage	HV_{CC} − 25	HV_{CC} + 0.3	V
	Allowable Negative V_{CTR} at 15V_{DC} Applied HV_{CC} to CTR Pin	−9.8	−7.0	V
LV_{CC}	Low−Side Supply Voltage	−0.3	25.0	V
V_{LO}	Low−Side Gate Driving Voltage	−0.3	LV_{CC}	V
V_{CON}	Control Pin Input Voltage	−0.3	LV_{CC}	V
V_{CS}	Current Sense (CS) Pin Input Voltage	−5.0	1.0	V
V_{RT}	RT Pin Input Voltage	−0.3	5.0	V
f_{SW}	Recommended Switching Frequency	10	600	kHz
V_{LS}	LS Pin Input Voltage	−0.3	LV_{CC}	V
V_{FI}	FI Pin Input Voltage	−0.3	LV_{CC}	V
V_{SS}	SS Pin Input Voltage	−0.3	Internally Clamped (Note 1)	V
V_{DT}	DT Pin Input Voltage	−0.3	Internally Clamped (Note 1)	V
dV_{CTR}/dt	Allowable CTR Voltage Slew Rate	−	50	V/ns
P_D	Total Power Dissipation	−	1.24	W
T_J	Maximum Junction Temperature (Note 2)	−	+150	°C
	Recommended Operating Junction Temperature (Note 2)	−40	+130	
T_{STG}	Storage Temperature Range	−55	+150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. V_{SS} and V_{DT} are internally clamped at 5.0 V, which has a tolerance between 4.75 V and 5.25 V.
2. The maximum value of the recommended operating junction temperature is limited by thermal shutdown.

THERMAL CHARACTERISTICS

Symbol	Parameter	Value	Unit
θ_{JA}	Junction−to−Ambient Thermal Impedance	102	°C/W

ELECTRICAL CHARACTERISTICS (T_A = 25°C and LV_{CC} = 17 V unless otherwise specified)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
SUPPLY SECTION						
I_{LK}	Offset Supply Leakage Current	HV_{CC} = V_{CTR}	–	–	50	μA
I_QHV_{CC}	Quiescent HV_{CC} Supply Current	$HV_{CC, START}$ − 0.1 V, V_{CTR} = 0 V	–	50	120	μA
I_QLV_{CC}	Quiescent LV_{CC} Supply Current	$LV_{CC, START}$ − 0.1 V, V_{CTR} = 0 V	–	100	200	μA
I_OHV_{CC}	Operating HV_{CC} Supply Current (RMS Value) (Note 3)	f_{OSC} = 100 kHz, C_{Load} = 1 nF, V_{CON} > 0.6 V, V_{CTR} = 0 V	–	3.0	4.5	mA
		f_{OSC} = 300 kHz, C_{Load} = 1 nF, V_{CON} > 0.6 V, V_{CTR} = 0 V	–	8	10	mA
		f_{OSC} = 300 kHz, V_{CON} < 0.4 V, V_{CTR} = 0 V (No Switching)	–	100	200	μA
I_OLV_{CC}	Operating LV_{CC} Supply Current (RMS Value) (Note 3)	f_{OSC} = 100 kHz, C_{Load} = 1 nF, V_{CON} > 0.6 V, V_{CTR} = 0 V	–	5	7	mA
		f_{OSC} = 300 kHz, C_{Load} = 1 nF, V_{CON} > 0.6 V, V_{CTR} = 0 V	–	10	14	mA
		f_{OSC} = 300 kHz, V_{CON} < 0.4 V, V_{CTR} = 0 V (No Switching)	–	2.6	3.5	mA
UVLO SECTION						
$LV_{CC, START}$	LV_{CC} UVLO Turn−On Threshold		11.2	12.5	13.8	V
$LV_{CC, STOP}$	LV_{CC} UVLO Turn−Off Threshold		8.9	10.0	11.1	V
$LV_{CC, HYS}$	LV_{CC} UVLO Hysteresis		–	2.5	–	V
$HV_{CC, START}$	HV_{CC} UVLO Turn−On Threshold		8.2	9.2	10.2	V
$HV_{CC, STOP}$	LV_{CC} UVLO Turn−Off Threshold		7.8	8.7	9.6	V
$HV_{CC, HYS}$	HV_{CC} UVLO Hysteresis		–	0.5	–	V
OSCILLATOR & FEEDBACK SECTION						
V_{BH}	Pulse Skip Disable Threshold Voltage		0.54	0.60	0.66	V
V_{BL}	Pulse Skip Enable Threshold Voltage		0.36	0.40	0.44	V
V_{RT}	Regulated RT Voltage		1.5	2.0	2.5	V
f_{OSC}	Output Oscillation Frequency	R_T = 11.6 kΩ, C_{SS} = 1 nF	48	50	52	kHz
		R_T = 2.7 kΩ, C_{SS} = 1 nF	188	200	212	
DC	Output Duty Cycle	R_T = 11.6 kΩ, C_{Load} = 100 pF	49	50	51	%
		R_T = 2.7 kΩ, C_{Load} = 100 pF	48	50	52	
SOFT−START AND RESTART SECTION						
I_{SS1}	Soft−Start Current 1	V_{CSS} = 0 V, LV_{CC} = 17 V	3	–	–	mA
I_{SS2}	Soft−Start Current 2	V_{CSS} = 1.6 V, LV_{CC} = 17 V	25	30	35	μA
V_{SS_START}	Soft−Start Start Voltage	C_{SS} = 1 nF, V_{CON} = 3 V	1.5	1.6	1.7	V
V_{SS_END}	Soft−Start End Voltage	C_{SS} = 1 nF, V_{CON} = 3 V	4.0	4.2	4.4	V
V_{SSC}	Clamped Soft−Start Voltage	C_{SS} = 1 nF, V_{CON} = 3 V	4.75	5.00	5.25	V
f_{OSC_SS}	Initial Output Oscillation Frequency During Soft−Start	R_T = 11.6 kΩ, V_{CSS} = 1.6 V	–	300	–	kHz
		R_T = 5.8 kΩ	–	530	–	
		R_T = 2.7 kΩ	600	–	–	
$V_{RT−CON}$	RT−CON Voltage for Startup		–	60	120	mV

ELECTRICAL CHARACTERISTICS (T_A = 25°C and LV_{CC} = 17 V unless otherwise specified) (continued)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
OUTPUT SECTION						
I_{source}	Peak Sourcing Current	LV_{CC} = HV_{CC} = 17 V, T_J = 40°C ~ 130°C	500	–	–	mA
I_{sink}	Peak Sinking Current	HV_{CC} = 17 V, T_J = 40°C ~ 130°C	1000	–	–	mA
t_r	Rising Time	HV_{CC} = 17 V, C_{Load} = 1 nF	–	40	–	ns
t_f	Falling Time		–	20	–	ns
V_{HOH}	High Level of High−Side Gate Signal (V_{HVCC}−V_{HO})	I_O = 20 mA	–	–	1.0	V
V_{HOL}	Low Level of High−Side Gate Signal		–	–	0.6	V
V_{LOH}	High Level of Low−Side Gate Signal (V_{LVCC}−V_{LO})		–	–	1.0	V
V_{LOL}	Low Level of Low−Side Gate Signal		–	–	0.6	V
PROTECTION SECTION						
I_{OLP}	OLP Sink Current		25	30	35	μA
V_{OLP}	OLP Threshold Voltage		−0.42	−0.37	−0.32	V
t_{BOL}	OLP Blanking Time (Note 3)		150	200	250	ns
V_{OCP}	OCP Threshold Voltage		−0.62	−0.56	−0.50	V
t_{BO}	OCP Blanking Time (Note 3)		150	200	250	ns
V_{AOCP}	AOCP Threshold Voltage		−1.21	−1.10	−0.99	V
t_{BAO}	AOCP Blanking Time (Note 3)		–	50	–	ns
t_{DA}	Delay Time (Low Side) Detecting from V_{AOCP} to Switch Off (Note 3)		–	250	400	ns
V_{OVP}	LV_{CC} Over−Voltage Protection		21	23	25	V
V_{LINE}	Line UVLO Threshold Voltage	V_{LS} Sweep, 40°C ~ 130°C	2.88	3.00	3.12	V
I_{LINE}	Line UVLO Hysteresis Current	V_{LS} = 2 V	9	10	11	μA
T_{SD}	Thermal Shutdown Temperature (Note 3)		130	140	150	°C
V_{FI}	Fault Input Threshold Voltage for Latch Operation		3.8	4.0	4.2	V
I_{LR}	Latch−Protection Sustain LV_{CC} Supply Current	LV_{CC} = 7.5 V	–	100	150	μA
V_{LR}	Latch−Protection Reset LV_{CC} Supply Voltage		5	–	–	V
DEAD−TIME CONTROL SECTION						
D_T	Dead Time	R_{DT} = 2.7 kΩ, C_{Load} = 1 nF	100	150	200	ns
		R_{DT} = 18 kΩ, C_{Load} = 1 nF	250	350	450	
		Short, C_{Load} = 1 nF	–	50	–	
		Open, C_{Load} = 1 nF	–	1000	–	
	Recommended Dead Time Range		100	–	600	

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. This parameter, although guaranteed, is not tested in production.

TYPICAL CHARACTERISTICS (These characteristic graphs are normalized at T_A = 25°C)

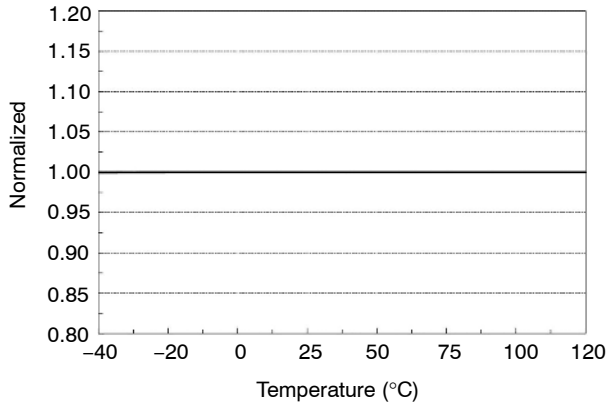


Figure 4. LV_{CC} Start Voltage vs. Temperature

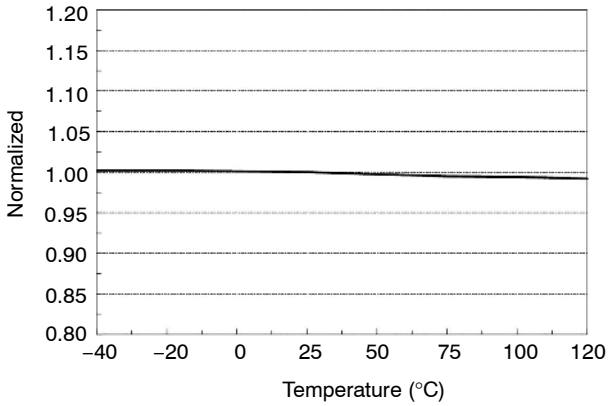


Figure 5. LV_{CC} Stop Voltage vs. Temperature

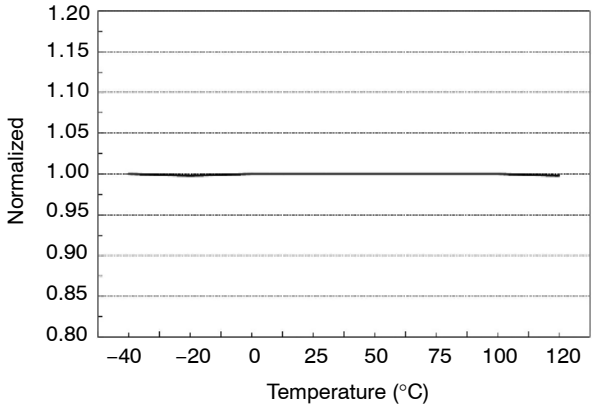


Figure 6. HV_{CC} Start Voltage vs. Temperature

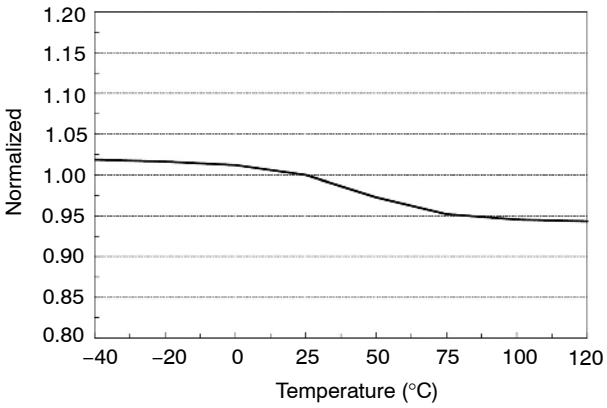


Figure 7. HV_{CC} Stop Voltage vs. Temperature

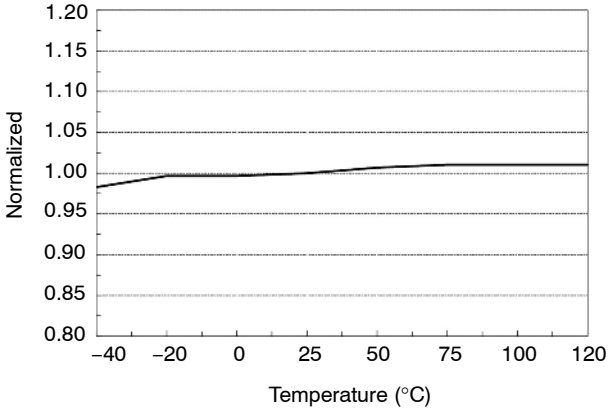


Figure 8. Pulse Skip Disable vs. Temperature

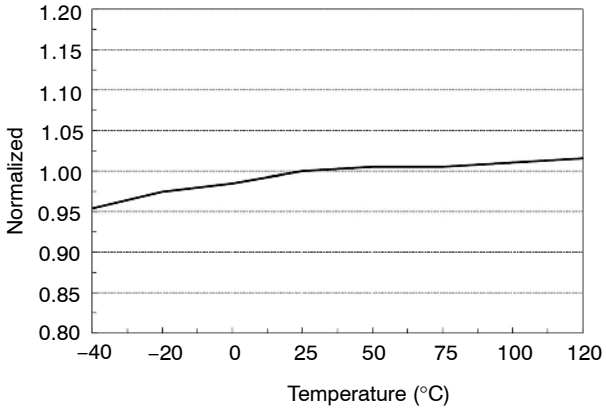


Figure 9. Pulse Skip Enable Voltage vs. Temperature

TYPICAL CHARACTERISTICS (These characteristic graphs are normalized at T_A = 25°C) (continued)

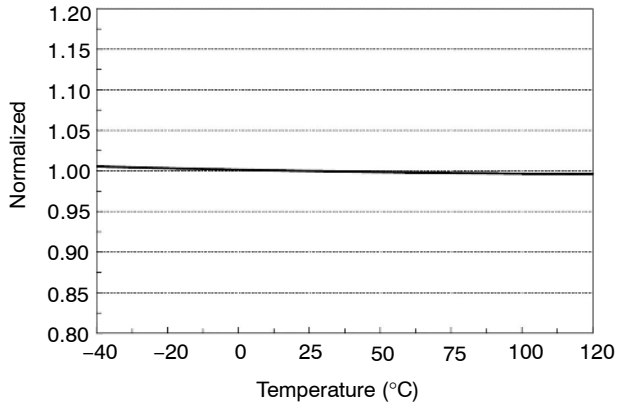


Figure 10. Regulated R_T Voltage vs. Temperature

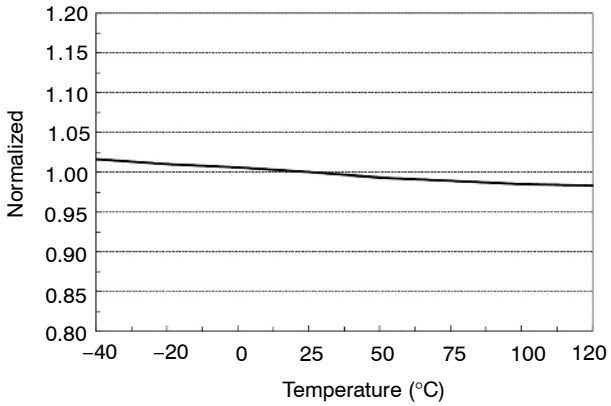


Figure 11. Output Oscillation Frequency (R_T = 11.6 kΩ) vs. Temperature

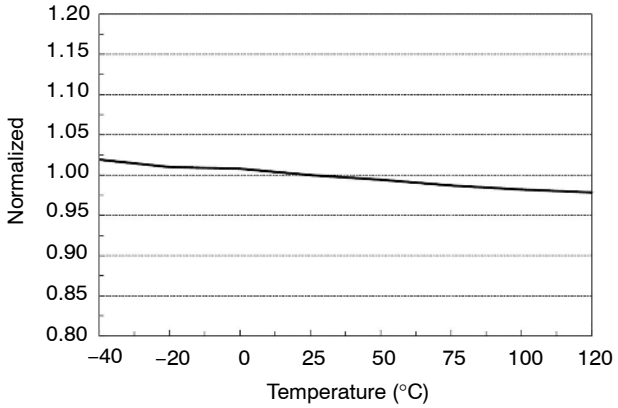


Figure 12. Output Oscillation Frequency (R_T = 2.7 kΩ) vs. Temperature

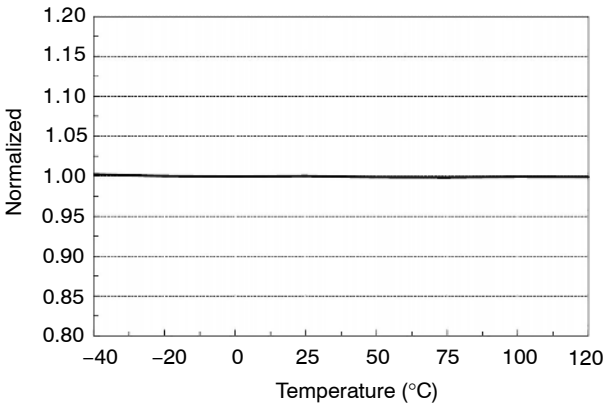


Figure 13. Output Duty Cycle (R_T = 11.6 kΩ) vs. Temperature

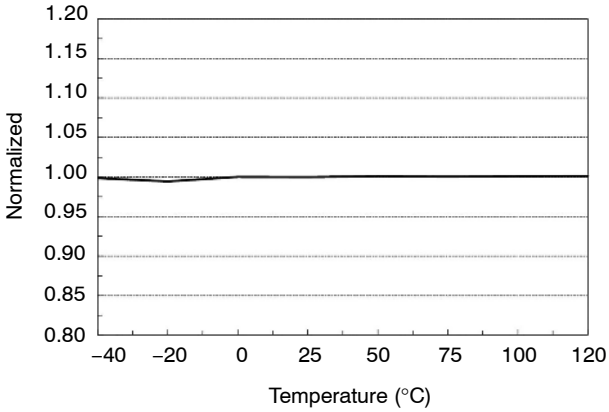


Figure 14. Output Duty Cycle (R_T = 2.7 kΩ) vs. Temperature

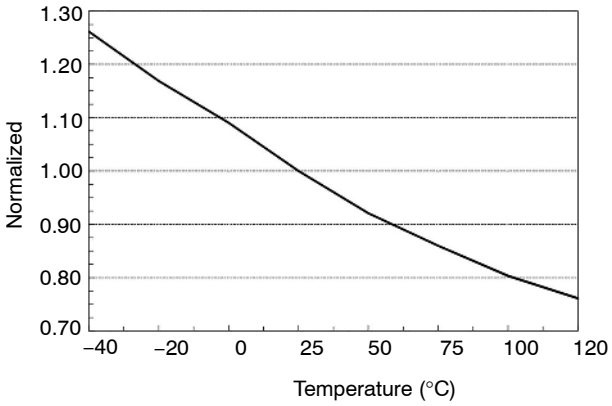


Figure 15. I_{SS1} vs. Temperature

TYPICAL CHARACTERISTICS (These characteristic graphs are normalized at T_A = 25°C) (continued)

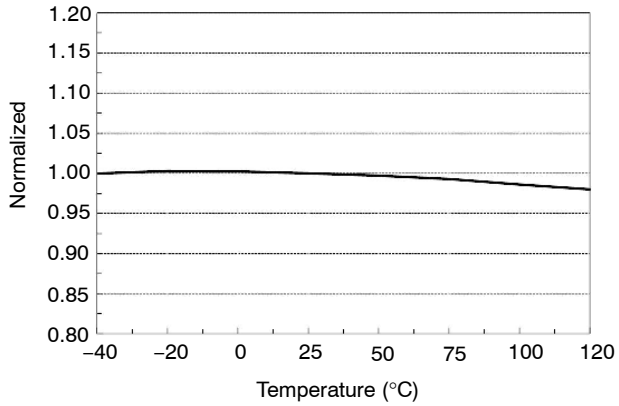


Figure 16. I_{SS2} vs. Temperature

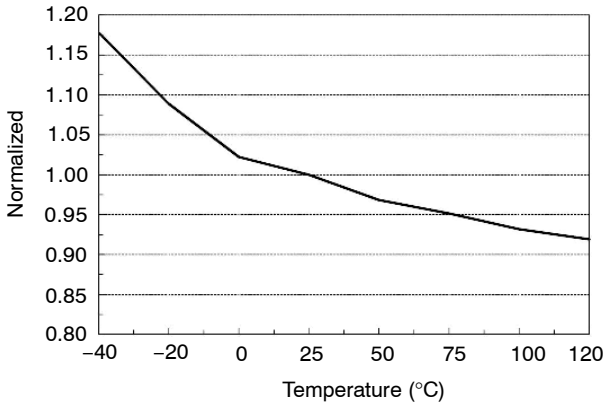


Figure 17. f_{OSC_SS} (R_T = 11.6 kΩ) vs. Temperature

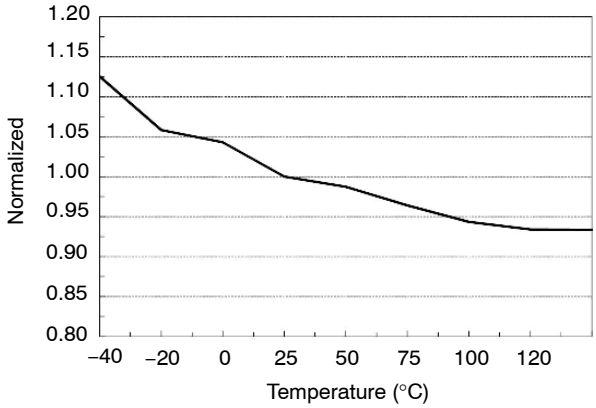


Figure 18. f_{OSC_SS} (R_T = 2.7 kΩ) vs. Temperature

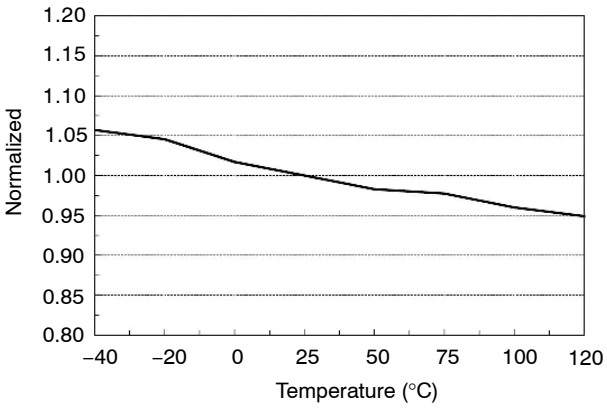


Figure 19. V_{OLP} vs. Temperature

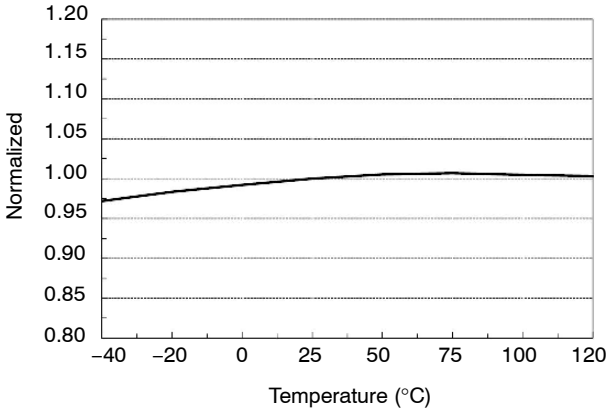


Figure 20. I_{OLP} vs. Temperature

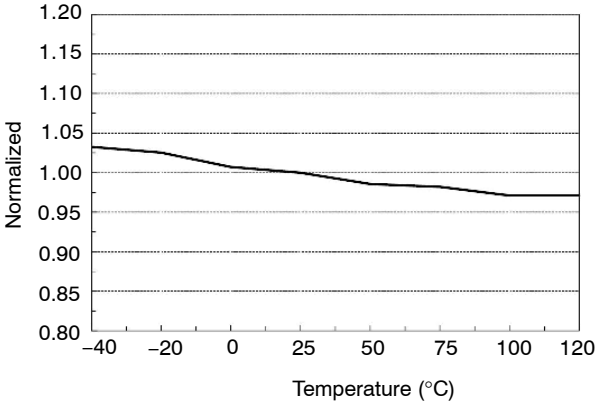


Figure 21. V_{OCP} vs. Temperature

TYPICAL CHARACTERISTICS (These characteristic graphs are normalized at T_A = 25°C) (continued)

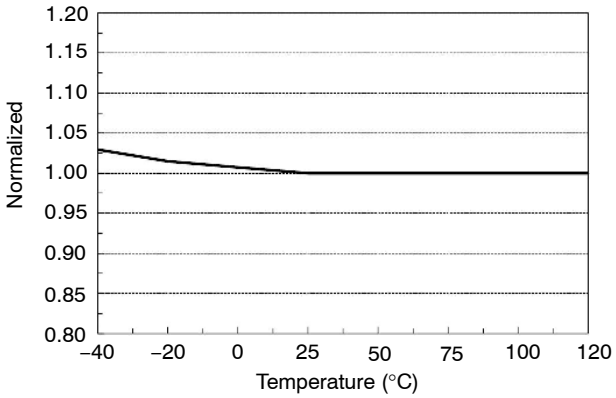


Figure 22. V_{AOCP} vs. Temperature

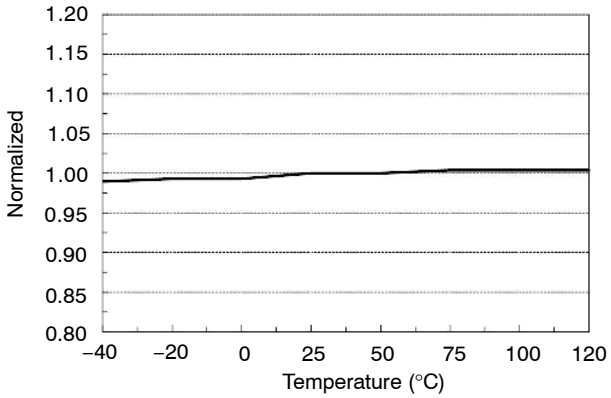


Figure 23. V_{OVP} vs. Temperature

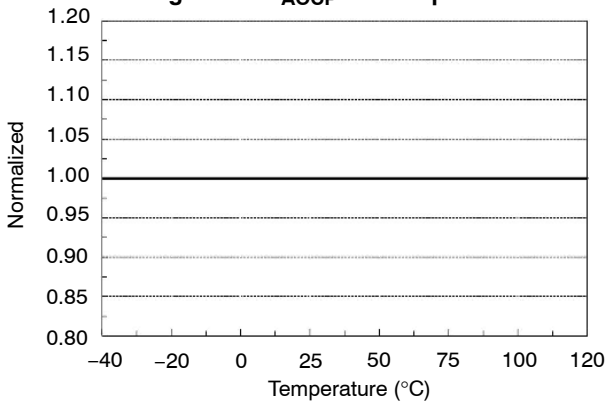


Figure 24. V_{LINE} vs. Temperature

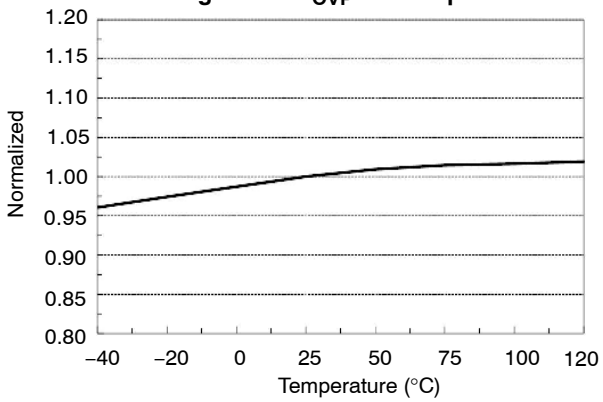


Figure 25. I_{LINE} vs. Temperature

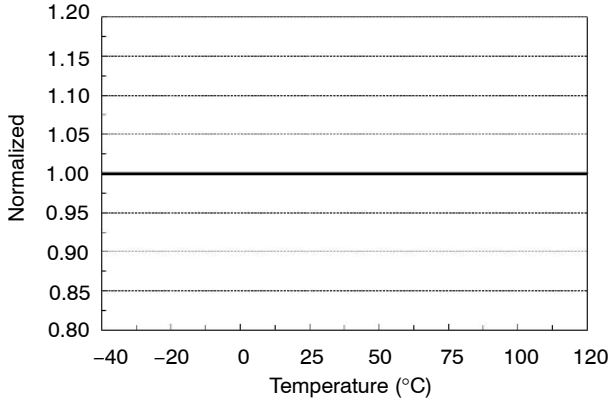


Figure 26. V_{FI} vs. Temperature

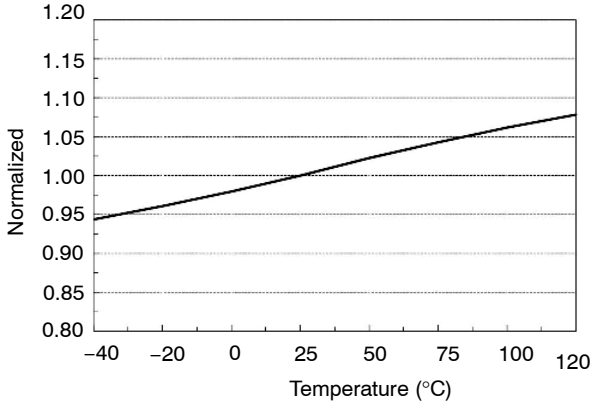


Figure 27. Dead Time (D_T = 150 ns) vs. Temperature

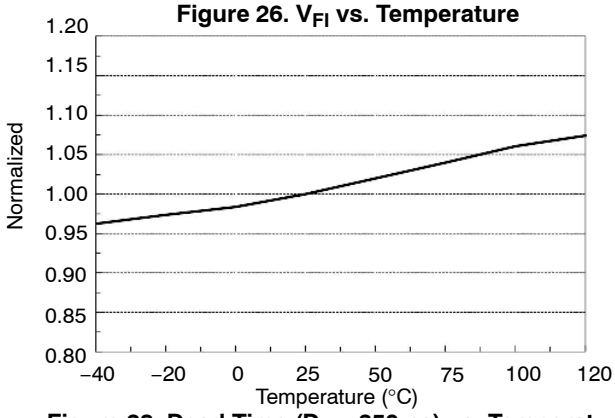


Figure 28. Dead Time (D_T = 350 ns) vs. Temperature

FUNCTIONAL DESCRIPTION

Internal Oscillator

Figure 29 shows the simplified circuit of internal current−controlled oscillator and typical circuit configuration for the RT pin. Internally, the voltage on the RT pin is regulated at 2 V by the V/I converter. The charging / discharging current for the oscillator capacitor, C_T, is obtained by mirroring the current flowing out of the RT pin (I_{CTC}). By comparing the capacitor voltage with V_{TH} and V_{TL} and driving S/R flip−flop with the comparator outputs, the clock signal is obtained. Thus, the switching frequency increases as the RT pin current increases.

As can be seen in Figure 29, an opto−coupler transistor is typically connected to the RT pin through R_{max} to modulate the switching frequency. During an overload condition, the opto−coupler is fully turned off and I_{CTC} is solely determined by R_{min}, which sets the minimum frequency. Meanwhile, the maximum switching frequency is obtained when the opto−coupler is fully turned on. Considering the typical saturation voltage of opto−transistor (0.2 V), the maximum frequency can be obtained by R_{max} and R_{min} as:

$$f_{min} = \frac{11,6\ k\Omega}{R_{min}} \times 50\ kHz$$

$$f_{max} = \left(\frac{11,6\ k\Omega}{R_{min}} + \frac{10.4\ k\Omega}{R_{max}}\right) \times 50\ kHz \quad \text{(eq. 1)}$$

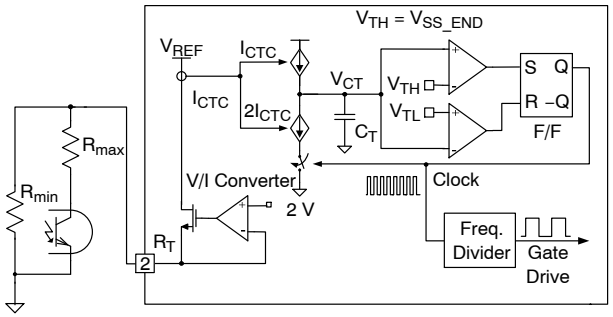


Figure 29. Current−Controlled Oscillator

Gate Driver and Dead Time Programming

The FAN7631 employs a gate drive circuit with high driving capability (source: 0.5 A / sink: 1 A) to cover a wide variety of applications. The two gate drive signals (LO and HO) are complimentary; each signal has 50% duty cycle, including the dead time, as shown in Figure 30.

The dead time can be programmed by the resistor, R_{DT}, as shown in Figure 31. Internally, the voltage on the DT pin is regulated at 1.4 V by the V/I converter and I_{DT} programs the dead time using R_{DT}. To improve the noise immunity of the dead time circuit, a sample−and−hold circuit is internally employed. However, severe noises in a high−power application can affect the dead time circuit operation and it is therefore recommended to use a bypass capacitor of around 10 nF in parallel with the R_{DT}. As a protective measure against abnormal conditions, such as DT pin short−to−ground and lift open, shuntresistor and series resistor $R_{DT,Short}$ and $R_{DT,Open}$ are internally connected to the DT pin. Even when this pin is shorted to ground and lifted open, the dead time is limited to 50 ns (short to ground) and 1000 ns (lifted open). Since the internal resistors have relatively large tolerance, it is recommended to set the dead time between 150 ns and 600 ns to minimize the dead time variation by the internal resistor tolerance.

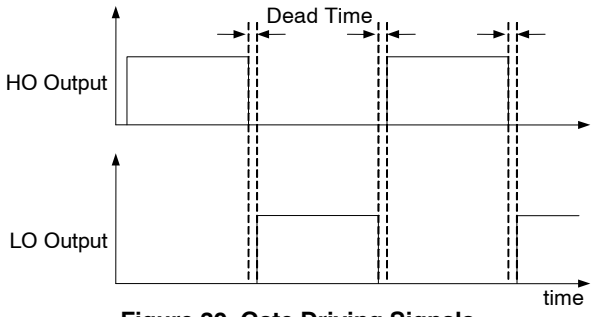


Figure 30. Gate Driving Signals

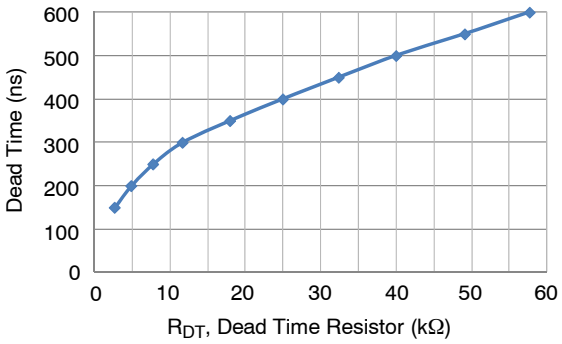


Figure 31. Dead Time vs. R_{DT}

Soft−Start

Since the voltage gain of the resonant converter is inversely proportional to the switching frequency, the soft−start is implemented by sweeping down the switching frequency from a high initial frequency until the output voltage is established. The current−steering circuit connected to SS pin adaptively changes the sinking and sourcing current of the SS pin to set soft−start time, OLP shutdown delay, and restart time. As illustrated in Figure 32, the sourcing current, I_{SS1} (3 mA), is enabled at the beginning of startup, which rapidly raises V_{SS} up to V_{SS_START} (1.6 V). Then the sourcing current is switched to I_{SS2} (30 μA) and gate drive signals are enabled. Due to the small value of I_{SS2}, the SS pin voltage slowly rises, allowing slow decrease of the switching frequency.

To minimize the frequency variation while the output capacitance of the opto−transistor is charged up, softstart is

delayed until the CON pin voltage (opto−coupler transistor voltage) reaches the RT pin voltage. Thus, the initial switching frequency is not affected by R_{max} and is solely determined as six times the minimum switching frequency set by R_{min} as in Equation 1. The maximum switching frequency is also internally limited at 600 kHz.

When V_{SS} reaches V_{SS_END} (4.2 V), soft−start ends. Then, the high threshold of V_{CT} comparator, V_{TH}, is clamped at V_{SS_END} while V_{SS} keeps increasing until it reaches V_{SSC} (5 V). The soft−start time is given as:

$$t_{SS} = C_{SS} \frac{2.6}{3 \times 10^{-5}} \qquad \text{(eq. 2)}$$

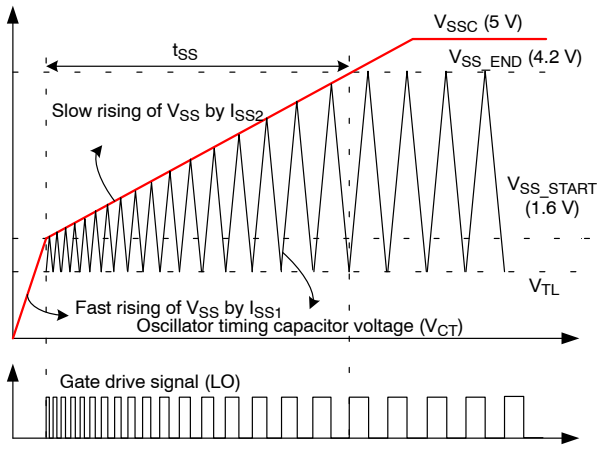


Figure 32. Soft−Start Waveforms

Current Sensing

FAN7631 employs a negative voltage sensing method to sense the drain current of the MOSFET. This allows sensing the current without a leading edge spike caused by the low−side MOSFET's driving current. Therefore, the resistive−sensing method requires only a small RC filter. The capacitive−sensing method is also available.

Resistive Sensing Method

The FAN7631 can sense the drain current as a negative voltage, as shown in Figure 33. An RC filter with a time constant of 1/30~1/10 of the operating period is typical.

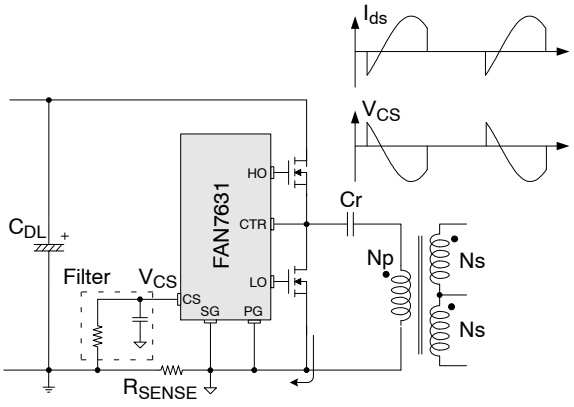


Figure 33. Resistive Sensing

Capacitive Sensing Method

The MOSFET drain current can be sensed using an additional capacitor in parallel with the resonant capacitor, as shown in Figure 34. While the low−side switch is turned on, the current, I_{CB}, through CB introduces V_{SENSE} across R_{SENSE}. The I_{CB} is a fraction of the transformer primary−side current, I_p, determined by the current divider with capacitors C_r and C_B as:

$$i_{CB} = \frac{C_B}{C_r + C_B} i_p \cong \frac{C_B}{C_r} i_p \qquad \text{(eq. 3)}$$

Generally, 1/100~1/1000 is adequate for the ratio of C_B/C_r. R_D is used as a damper for reducing noise generated by the switching transition. To prevent the damping resistor from affecting the current divider ratio, the resistor should be much smaller than the impedance of C_B at the switching frequency, calculated as:

$$R_D << \frac{1}{2\pi f_S C_B} \qquad \text{(eq. 4)}$$

Then, V_{SENSE} can be obtained as:

$$V_{Sense} = \frac{C_B}{C_r} R_{sense} i_p \qquad \text{(eq. 5)}$$

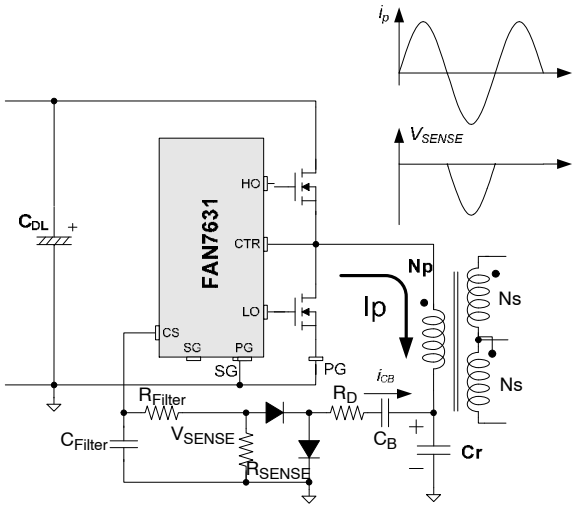


Figure 34. Capacitive Sensing

Protection Circuit

The FAN7631 has several self−protective functions: Overload Protection (OLP), Over−Current Protection (OCP), level−change OCP, Abnormal Over−Current Protection (AOCP), Over−Voltage Protection (OVP), Thermal Shutdown (TSD), Fault Input (FI), and Line Under−Voltage Lockout (LUVLO or also called brownout). Level−change OCP, OLP, OCP, OVP, and LUVLO are Auto−Restart Mode protections while AOCP, TSD, and fault input are Latch Mode protections.

Once auto−restart protection is triggered, switching is instantly terminated and the MOSFETs remain off. Then the FAN7631 keeps attempting to restart after the restart delay until the protection situation is removed. When a Latch

Mode protection is triggered, the FAN7631 remains off until LV_{CC} drops to V_{LR} (5 V) and then rises above $LV_{CC,START}$ (12.5 V).

Overload Protection (OLP)

When the sensed voltage on the CS pin drops below V_{OLP} (−0.37 V) for more than OLP blanking time, t_{BOL} (200 ns), C_{SS} starts to be discharged by sinking current I_{OLP}. If the sensed voltage on the CS pin does not drop below V_{OLP} in the next switching cycle, the current on the SS pin is switched to charging current I_{SS1}, restoring V_{SS} as illustrated in Figure 35. If the CS pin voltage drops below V_{OLP} for in next consecutive switching cycle until C_{SS} voltage, V_{SS}, reaches V_{SS_START} (1.6 V); OLP is triggered and the gate drive signals remain off. Once the OLP is triggered, FAN7631 repeats charging and discharging C_{SS} four times, then restarts. The OLP delay, t_{OLP}, and self auto−restart time, t_{AR}, are given as:

$$t_{OLP} = C_{SS} \frac{3.4}{3 \times 10^{-5}} \quad \text{(eq. 6)}$$

$$t_{AR} = 8 \times C_{SS} \frac{2.6}{3 \times 10^{-5}} \quad \text{(eq. 7)}$$

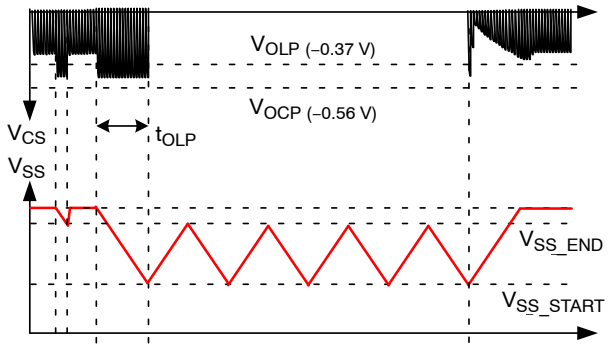


Figure 35. Overload Protection (OLP)

Over−Current Protection (OCP)

When the CS pin voltage drops below V_{OCP} (−0.54 V) for longer than the OCP blanking time, t_{BO} (200 ns), OCP is triggered, terminating switching operation. Then, FAN7631 repeats charging and discharging C_{SS} four times before restarting.

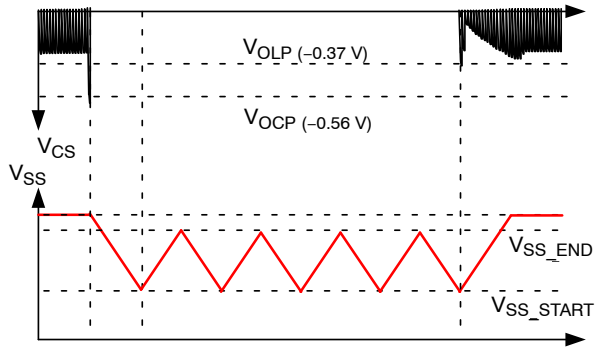


Figure 36. Over−Current Protection (OCP)

Abnormal Over−Current Protection (AOCP)

If the secondary−side rectifier diodes are shorted, a large current with extremely high di/dt can flow through the MOSFET before OCP is triggered. AOCP is triggered with a short blanking time of 50 ns, t_{BAO}, when the sensed voltage drops below −1.10 V, terminating the switching operation. Once the protection is triggered, V_{SS} is discharged by an internal switch. Since it is a Latch Mode protection, the protection is reset when LV_{CC} drops to V_{LR} (5 V).

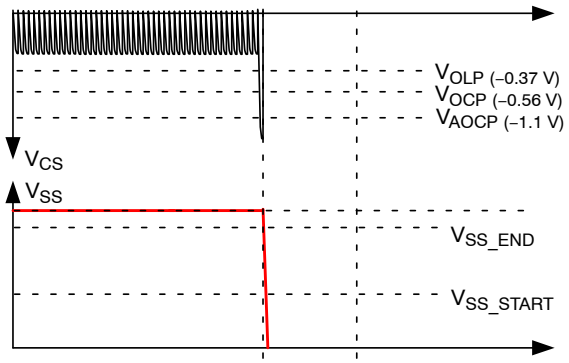


Figure 37. Abnormal Over−Current Protection (AOCP)

Level−Change Over−Current Protection (OCP)

Even with soft−start, there can be large overshoot current for the initial several switching cycles until the resonant capacitor voltage reaches its steady−state value. To prevent the startup failure by OCP, the OCP threshold is changed to V_{AOCP} level while the Latch Mode AOCP is disabled during soft−start.

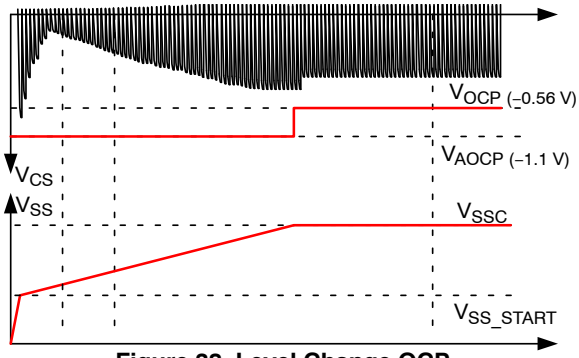


Figure 38. Level Change OCP

Over−Voltage Protection (OVP)

When the LV_{CC} reaches 23 V, OVP is triggered. This protection is used when auxiliary winding of the transformer is utilized to supply V_{CC} to the FAN7631.

Thermal Shutdown (TSD)

The thermal shutdown function is integrated to detect abnormal over−temperature, such as abnormal ambient temperature rising or over−driving of gate drive circuit. If the junction temperature exceeds T_{SD} (130°C), thermal shutdown is triggered in Latch Mode.

Line−UVLO

FAN7631 includes a precise line−UVLO (or brownout) function with programmable hysteresis voltage, as can be seen in Figure 39. When the line voltage is recovered, it starts up with soft−start, as shown in Figure 39. A hysteresis voltage between the start and stop voltage is programmable by I_{LINE} and external resistor R1. In normal operation, the comparator's output is HIGH and I_{LINE} is disabled I_{LINE} is activated when the comparator's output is LOW, introducing hysteresis.

If necessary, C_{Filter} can be used to reduce noise interference. Generally, hundreds of pico−farad to tens of nano−farad is adequate depending on the level of noise.

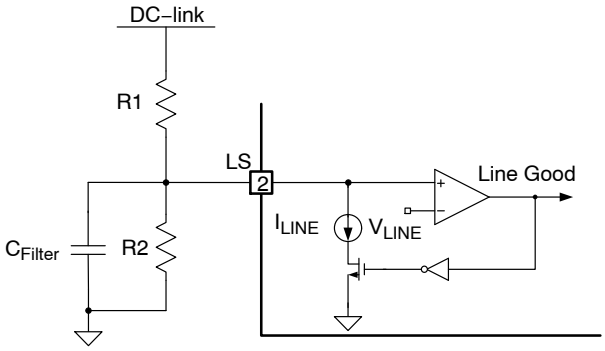


Figure 39. Line−UVLO

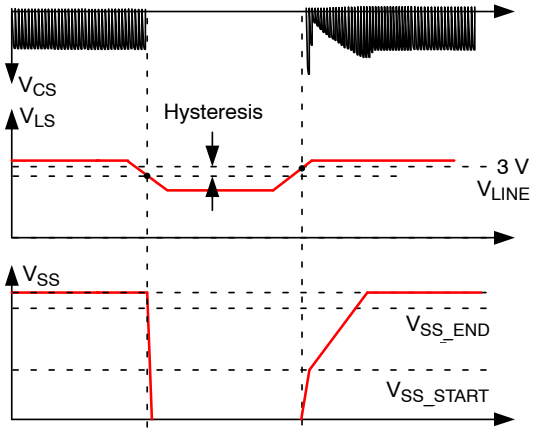


Figure 40. Line UVLO Waveforms

The DC link input−voltages for start and stop are calculated as:

$$V_{DL,\,STOP} = V_{LINE} \times \frac{R1 + R2}{R2}$$

$$V_{DL,\,START} = V_{DL,\,STOP} + I_{LINE} \times R1 \qquad \text{(eq. 8)}$$

Simple Remote−On/Off

The power stage can be shut down with Latch Mode or Auto−Restart Mode, as shown in Figure 41. For the Latch Mode protection, the FI pin is used, which stops the switching immediately once the voltage on FI pin is pulled above V_{FI} (4 V) using an opto−coupler. To configure an external protection with Auto−Restart Mode, an optocoupler can be used on the LS pin. When voltage on the LS pin is pulled below V_{LINE} (3 V), line UVLO is triggered. When LS pin voltage is pulled HIGH, above 3 V, FAN7631 starts up softly.

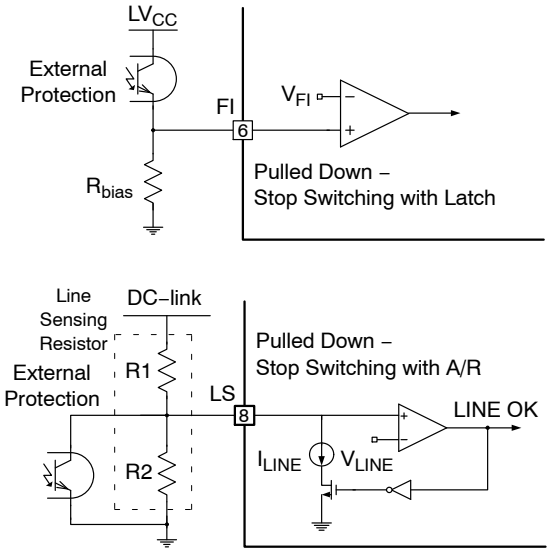


Figure 41. External Protection Circuits (Top: Latch Mode, Bottom: A/R Mode)

Skip Cycle Operation

The FAN7631 provides the pulse−skip function to prevent the switching frequency from increasing too much at noload condition. Figure 42 shows the internal block diagram for the control (CON) pin and its external configuration. The CON pin is typically connected to the collector terminal of the opto−coupler and the FAN7631 stops switching when the CON pin voltage drops below 0.4 V. FAN7631 resumes switching when the CON pin voltage rises above 0.6 V. The frequency that causes pulse skipping is given as:

$$f_{SKIP} = \left(\frac{5.8\ k\Omega}{R_{min}} + \frac{4.6\ k\Omega}{R_{max}}\right) \times 100\ kHz \qquad \text{(eq. 9)}$$

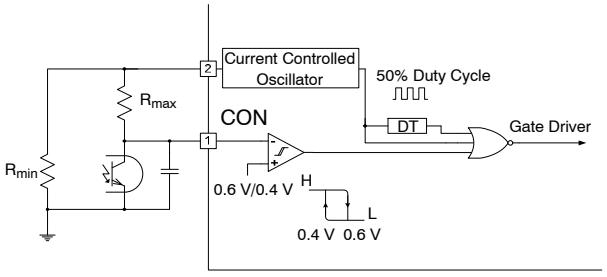


Figure 42. Pulse−Skipping Circuit

PCB Layout Guideline

Figure 43 shows the PCB layout guideline to minimize the usage of jumpers. Good PCB layout improves power system efficiency and reliability and minimizes EMI. The Power Ground (PG) and Signal Ground (SG) should meet at a single point. Jumpers should be avoided, especially for the ground trace.

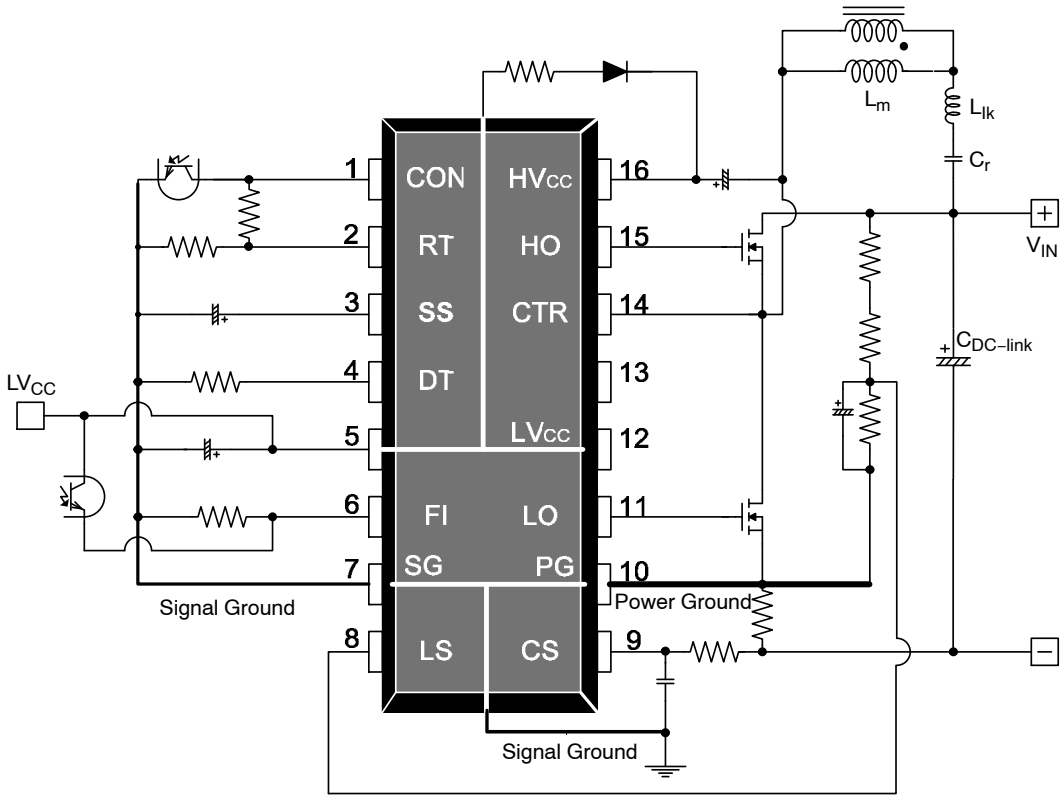


Figure 43. PCB Layout Guideline

TYPICAL APPLICATION CIRCUIT
(Half−Bridge LLC Resonant Converter)

Application	Device	Input Voltage Range	Rated Output Power	Output Voltage (Rated Current)
LCD TV	FAN7631	400 V (20 ms Hold−Up Time)	192 W	24 V−8 A

Features

- High efficiency (>94% at 400 V_{DC} input).
- Reduced EMI noise through zero−voltage−switching (ZVS).
- Enhanced system reliability with various protection functions.

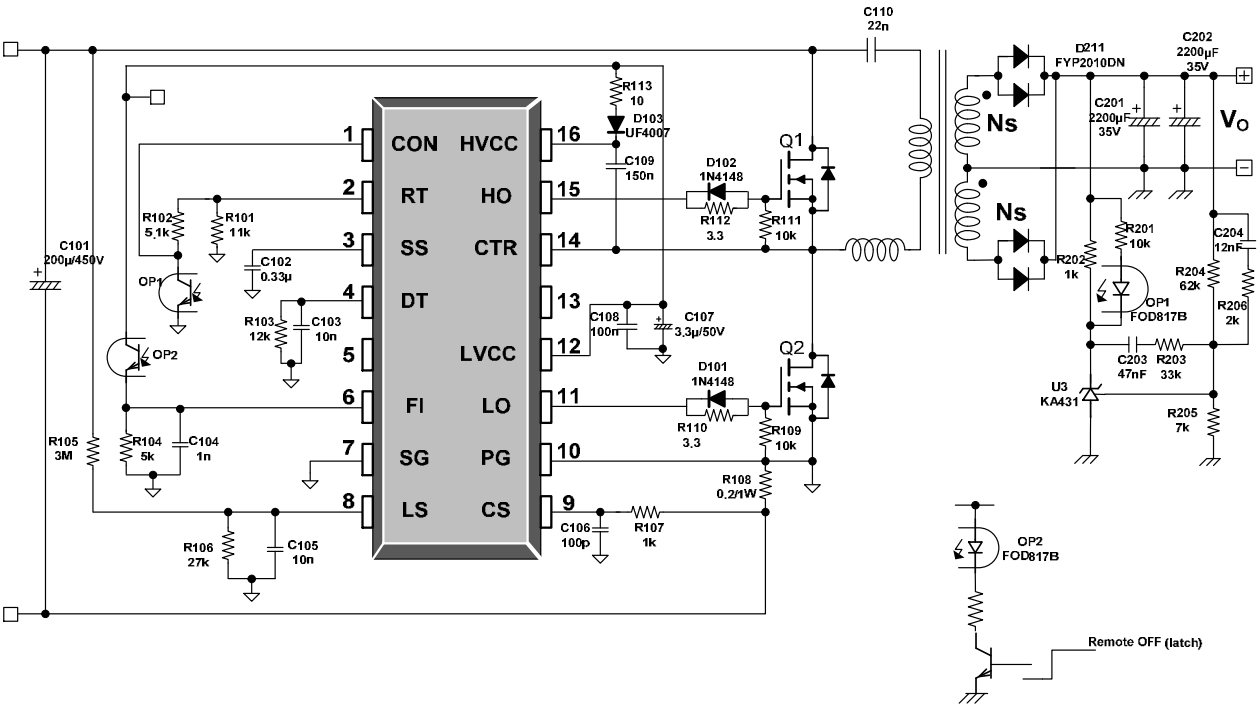


Figure 44. Typical Application Circuit

TYPICAL APPLICATION CIRCUIT (continued)

Usually, the LLC resonant converter requires large leakage inductance value. To obtain a large leakage inductance, sectional winding method is used.

- Core: EER3542 (Ae = 107 mm^2)
- Bobbin: EER3542 (Horizontal)

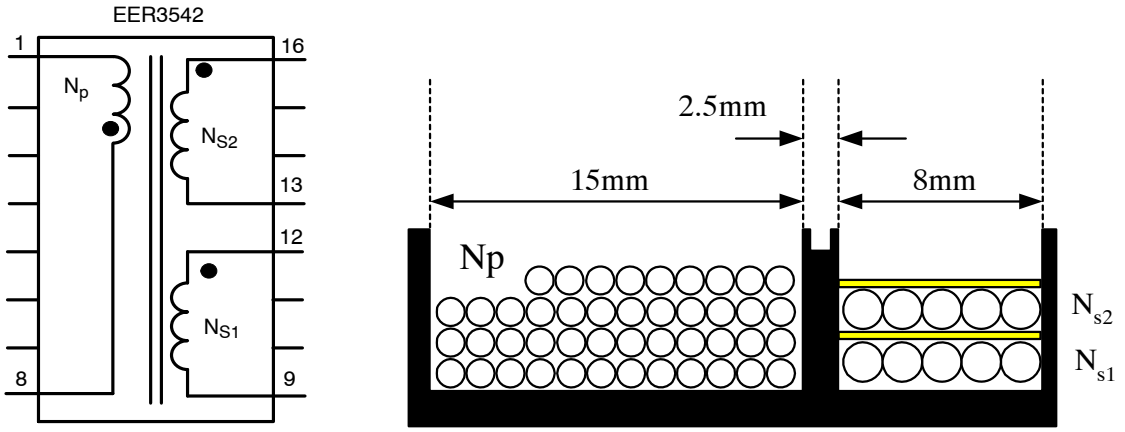


Figure 45. Winding Specifications

Table 1. WINDING SPECIFICATIONS

	Pin (S → F)	Wire	Turns	Winding Method
N_p	8 → 1	0.12 ϕ → 30 (Litz Wire)	45	Section Winding
N_{S1}	12 → 9	0.1 ϕ → 100 (Litz Wire)	5	Section Winding
N_{S2}	16 → 13	0.1 ϕ → 100 (Litz Wire)	5	Section Winding

	Pin	Specifications	Remark
Primary−Side Inductance (L_P)	1−8	630 μH ±5%	100 kHz, 1 V
Primary−Side Effective Leakage (L_R)	1−8	145 μH ±5%	Short One of the Secondary Windings

ORDERING INFORMATION

Part Number	Operating Temperature Range	Package	Shipping†
FAN7631SJX	−40°C ~ 130°C	16−Lead, Small−Outline Package (SOP)	2000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

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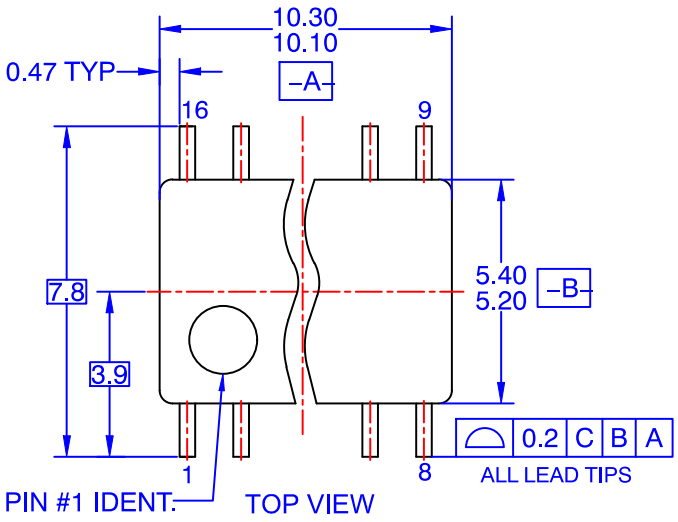
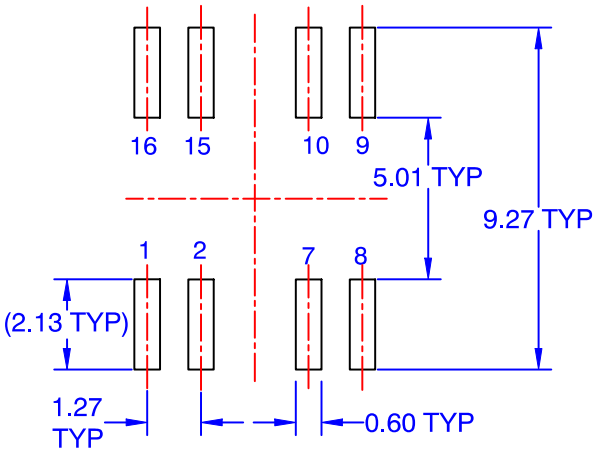
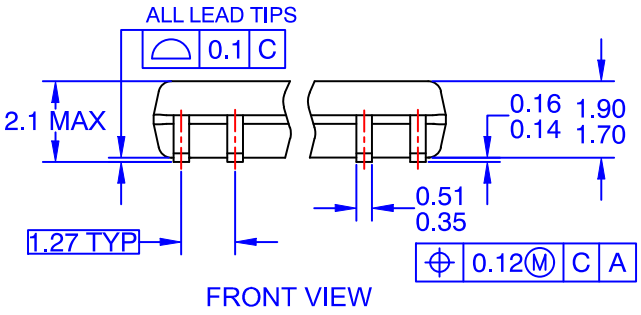
DATE 31 DEC 2016

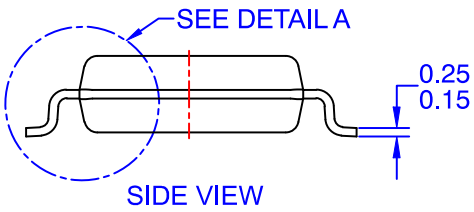




LAND PATTERN RECOMMENDATION



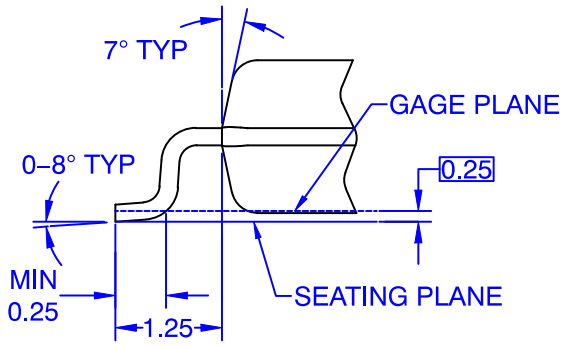
FRONT VIEW



SIDE VIEW

NOTES:

A. CONFORMS TO EIAJ EDR–7320 REGISTRATION, ESTABLISHED IN DECEMBER, 1998.
B. DIMENSIONS ARE IN MILLIMETERS.
C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.



DETAIL A

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