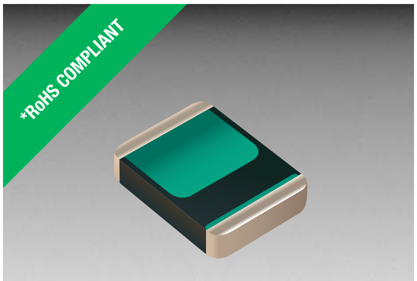

BOURNS®

Features

- Formerly a KEKOVARICON product
- Three model sizes available - 3255, 4032 and 2220 (available on request)
- Leadless chip form - zero inductance facilitating extremely fast response time to transient surges
- Broad range of current and energy handling capabilities
- +125 °C Continuous operating temperature
- Tolerant of common water cleaning procedures and humidity (climatic category 55/125/56)
- Available in tape and reel packaging for automatic pick-and-place
- RoHS compliant*

DV Series - Medium Voltage Varistors

General Information

The DV series of medium voltage varistors is designed to protect electronic equipment against high voltage surges in the medium voltage region. They offer excellent transient energy absorption due to improved energy volume distribution and power dissipation. Compared to other Bourns® medium voltage SMD varistors, DV series varistors have a very low profile.

DV series varistors are designed for surface mounting and are available In two model sizes - 3225 and 4032 (the 2220 size is also available upon request). These transient voltage suppressors cover an operating voltage V_{rms} from 11 to 300 V, featuring maximum surge currents from 100 A to 1200 A.

Absolute Maximum Ratings

Parameter	Value	Units
Continuous:		
Steady State Applied Voltage		
DC Voltage Range (V_{dc})	14 to 385	V
AC Voltage Range (V_{rms})	11 to 300	V
Transient:		
Non-Repetitive Surge Current, 8/20 µs Waveform (I_{max})	100 to 1200	A
Non-Repetitive Surge Energy, 10/1000 µs Waveform (W_{max})	0.6 to 30	J
Operating Ambient Temperature	-40 to +125	°C
Storage Temperature Range	-55 to +150	°C
Threshold Voltage Temperature Coefficient	< +0.05	%/°C
Response Time	< 5	ns
Climatic Category	55 / 125 / 56	

BOURNS®

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The Americas: Tel: +1-951 781-5500 • Email: americus@bourns.com
www.bourns.com

Additional Information

Click these links for more information:

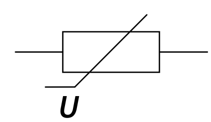
PRODUCT SELECTOR | TECHNICAL LIBRARY | INVENTORY | SAMPLES | CONTACT

Agency Recognition

Standard	UL 1449
File Number	E313168**

**Not all rated voltages are UL recognized; check the file for details.

Varistor Symbol



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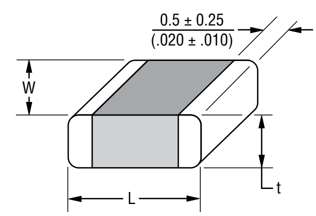
WARNING Cancer and Reproductive Harm - www.P65Warnings.ca.gov

Device Ratings

Model	V_{rms}	V_{dc}	V_n @ 1 mA	V_c	I_c	W_{max} 10/1000 μs	P max.	I_{max} 8/20 μs	C Typ. @ 1 kHz
	V	V	V	V	A	J	W	A	pF
DV 11 K 3225	11	14	18	36	2.5	0.6	0.01	100	2500
DV 11 K 4032	11	14	18	36	5	1.1	0.02	250	4300
DV 14 K 3225	14	18	22	43	2.5	0.7	0.01	100	2200
DV 14 K 4032	14	18	22	43	5	1.3	0.02	250	3500
DV 17 K 3225	17	22	27	53	2.5	0.9	0.01	100	1750
DV 17 K 4032	17	22	27	53	5	1.6	0.02	250	3000
DV 20 K 3225	20	26	33	65	2.5	1.1	0.01	100	1650
DV 20 K 4032	20	26	33	65	5	2.0	0.02	250	2300
DV 25 K 3225	25	31	39	77	2.5	1.2	0.01	100	1500
DV 25 K 4032	25	31	39	77	5	2.4	0.02	250	1900
DV 30 K 3225	30	38	47	93	2.5	1.5	0.01	100	1000
DV 30 K 4032	30	38	47	93	5	2.8	0.02	250	1600
DV 35 K 3225	35	45	56	110	2.5	1.8	0.01	100	800
DV 35 K 4032	35	45	56	110	5	3.4	0.02	250	1400
DV 40 K 3225	40	56	68	135	2.5	2.2	0.01	100	700
DV 40 K 4032	40	56	68	135	5	4.1	0.02	250	1200
DV 50 K 3225	50	65	82	135	5	2.5	0.10	400	400
DV 50 K 4032	50	65	82	135	10	6.5	0.25	1200	580
DV 60 K 3225	60	85	100	165	5	3.0	0.10	400	300
DV 60 K 4032	60	85	100	165	10	7.0	0.25	1200	530
DV 75 K 3225	75	100	120	200	5	4.0	0.10	400	240
DV 75 K 4032	75	100	120	200	10	9.0	0.25	1200	480
DV 95 K 3225	95	125	150	250	5	6.0	0.10	400	210
DV 95 K 4032	95	125	150	250	10	11.0	0.25	1200	310
DV 115 K 3225	115	150	180	300	5	6.5	0.10	400	200
DV 115 K 4032	115	150	180	300	10	13.0	0.25	1200	270
DV 130 K 3225	130	170	205	340	5	7.0	0.10	400	150
DV 130 K 4032	130	170	205	340	10	15.0	0.25	1200	250
DV 140 K 3225	140	180	220	360	5	7.5	0.10	400	180
DV 140 K 4032	140	180	220	360	10	18.0	0.25	1200	240
DV 150 K 3225	150	200	240	395	5	9.0	0.10	400	150
DV 150 K 4032	150	200	240	395	10	18.5	0.25	1200	220
DV 175 K 3225	175	225	270	455	5	9.5	0.10	400	130
DV 175 K 4032	175	225	270	455	10	21.0	0.25	1200	200
DV 230 K 3225	230	300	360	595	5	10.0	0.10	400	110
DV 230 K 4032	230	300	360	595	10	23.0	0.25	1200	170
DV 250 K 3225	250	320	390	650	5	11.0	0.10	400	100
DV 250 K 4032	250	320	390	650	10	25.0	0.25	1200	160
DV 275 K 3225	275	350	430	710	5	13.0	0.10	400	90
DV 275 K 4032	275	350	430	710	10	29.0	0.25	1200	150
DV 300 K 3225	300	385	470	775	5	15.0	0.10	400	85
DV 300 K 4032	300	385	470	775	10	30.0	0.25	1200	140

Product Dimensions

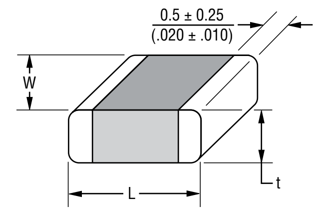
Model	Dimension		
	L ± 0.5 / (.020)	W ± 0.4 / (.016)	t (Max.)
DV 11 K 3225	8.0 / (.315)	6.3 / (.248)	1.4 / (.055)
DV 11 K 4032	10.0 / (.394)	8.0 / (.315)	1.4 / (.055)
DV 14 K 3225	8.0 / (.315)	6.3 / (.248)	1.6 / (.063)
DV 14 K 4032	10.0 / (.394)	8.0 / (.315)	1.6 / (.063)
DV 17 K 3225	8.0 / (.315)	6.3 / (.248)	1.8 / (.071)
DV 17 K 4032	10.0 / (.394)	8.0 / (.315)	1.8 / (.071)
DV 20 K 3225	8.0 / (.315)	6.3 / (.248)	1.8 / (.071)
DV 20 K 4032	10.0 / (.394)	8.0 / (.315)	1.8 / (.071)
DV 25 K 3225	8.0 / (.315)	6.3 / (.248)	2.0 / (.079)
DV 25 K 4032	10.0 / (.394)	8.0 / (.315)	2.0 / (.079)
DV 30 K 3225	8.0 / (.315)	6.3 / (.248)	2.0 / (.079)
DV 30 K 4032	10.0 / (.394)	8.0 / (.315)	2.0 / (.079)
DV 35 K 3225	8.0 / (.315)	6.3 / (.248)	2.0 / (.079)
DV 35 K 4032	10.0 / (.394)	8.0 / (.315)	2.0 / (.079)
DV 40 K 3225	8.0 / (.315)	6.3 / (.248)	2.0 / (.079)
DV 40 K 4032	10.0 / (.394)	8.0 / (.315)	2.0 / (.079)
DV 50 K 3225	8.0 / (.315)	6.3 / (.248)	2.0 / (.079)
DV 50 K 4032	10.0 / (.394)	8.0 / (.315)	2.0 / (.079)
DV 60 K 3225	8.0 / (.315)	6.3 / (.248)	2.0 / (.079)
DV 60 K 4032	10.0 / (.394)	8.0 / (.315)	2.0 / (.079)
DV 75 K 3225	8.0 / (.315)	6.3 / (.248)	2.0 / (.079)
DV 75 K 4032	10.0 / (.394)	8.0 / (.315)	2.0 / (.079)
DV 95 K 3225	8.0 / (.315)	6.3 / (.248)	2.0 / (.079)
DV 95 K 4032	10.0 / (.394)	8.0 / (.315)	2.0 / (.079)
DV 115 K 3225	8.0 / (.315)	6.3 / (.248)	2.0 / (.079)
DV 115 K 4032	10.0 / (.394)	8.0 / (.315)	2.0 / (.079)
DV 130 K 3225	8.0 / (.315)	6.3 / (.248)	2.0 / (.079)
DV 130 K 4032	10.0 / (.394)	8.0 / (.315)	2.0 / (.079)
DV 140 K 3225	8.0 / (.315)	6.3 / (.248)	2.0 / (.079)
DV 140 K 4032	10.0 / (.394)	8.0 / (.315)	2.0 / (.079)



DIMENSIONS: MM / (INCHES)

Product Dimensions (Continued)

Model	Dimension		
	L ± 0.5 (.020)	W ± 0.4 (.016)	t (Max.)
DV 150 K 3225	8.0 (.315)	6.3 (.248)	2.0 (.079)
DV 150 K 4032	10.0 (.394)	8.0 (.315)	2.0 (.079)
DV 175 K 3225	8.0 (.315)	6.3 (.248)	2.0 (.079)
DV 175 K 4032	10.0 (.394)	8.0 (.315)	2.0 (.079)
DV 230 K 3225	8.0 (.315)	6.3 (.248)	2.0 (.079)
DV 230 K 4032	10.0 (.394)	8.0 (.315)	2.0 (.079)
DV 250 K 3225	8.0 (.315)	6.3 (.248)	2.0 (.079)
DV 250 K 4032	10.0 (.394)	8.0 (.315)	2.0 (.079)
DV 275 K 3225	8.0 (.315)	6.3 (.248)	2.0 (.079)
DV 275 K 4032	10.0 (.394)	8.0 (.315)	2.0 (.079)
DV 300 K 3225	8.0 (.315)	6.3 (.248)	2.0 (.079)
DV 300 K 4032	10.0 (.394)	8.0 (.315)	2.0 (.079)



DIMENSIONS: $\frac{\text{MM}}{\text{(INCHES)}}$

How to Order

DV20K3225R2yy

Series Designator
DV = DV Series

Max. Continuous Operating Voltage (V_{rms})

V_n Tolerance
K = ±10 %

Model Size
- 3225
- 4032

Packaging
R2 = Reel

Special Requirements
- yy = Unique two-digit suffix assigned to each customer requesting special parameters. Please contact Bourns for more information.

Instructions for Creating Orderable Part Number:

1) Start with base part number in characteristics table (example: DV20K3225).

2) Add Packaging: R2 (example part number becomes DV20K3225R2).

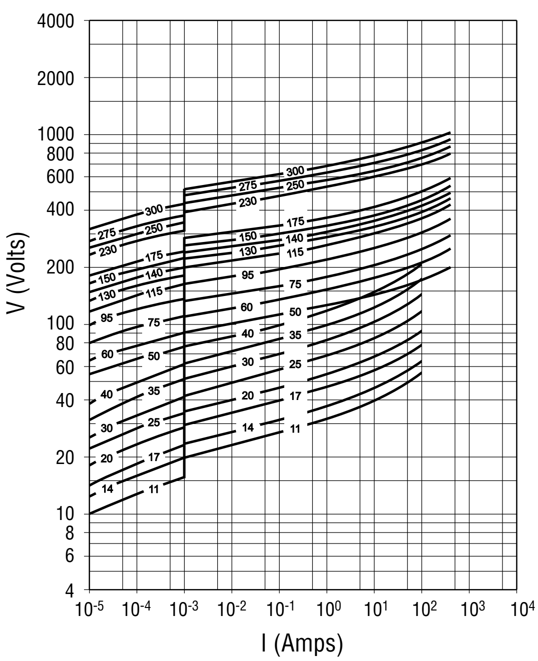
3) Part number can have no spaces or lower case letters.

Typical Part Marking

No marking.

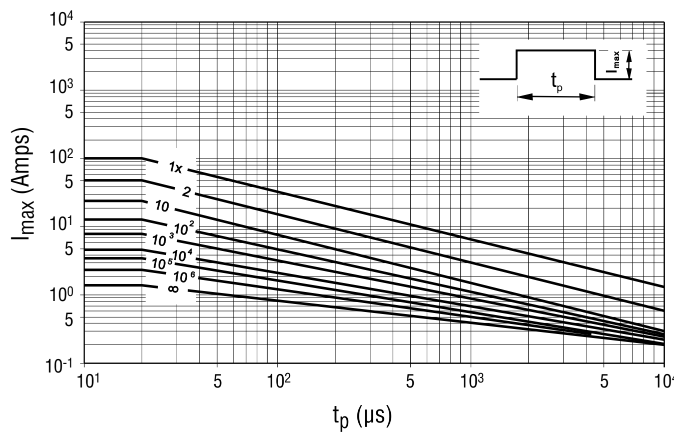
Protection Level

Model Size 3225 - (DV11 ~ DV300)

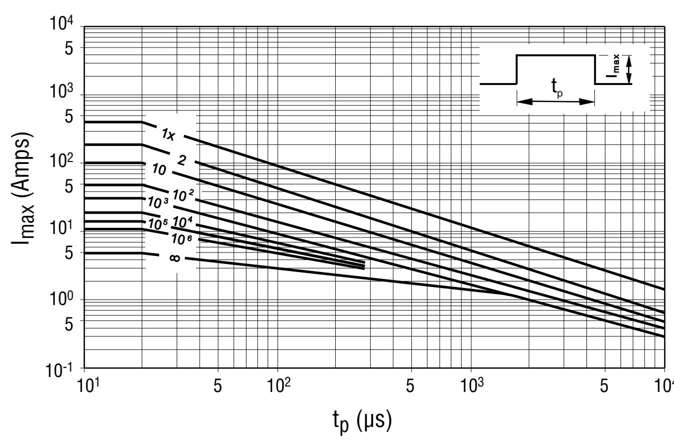


Pulse Rating Curves

Model Size 3225 - (DV11 ~ DV40)

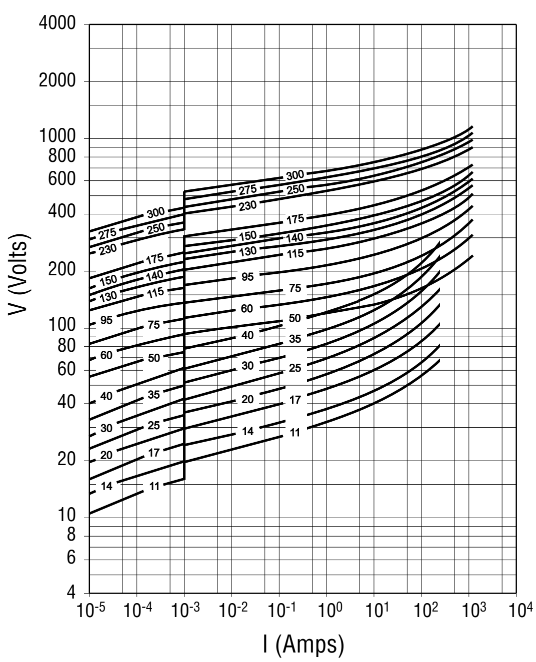


Model Size 3225 - (DV50 ~ DV300)



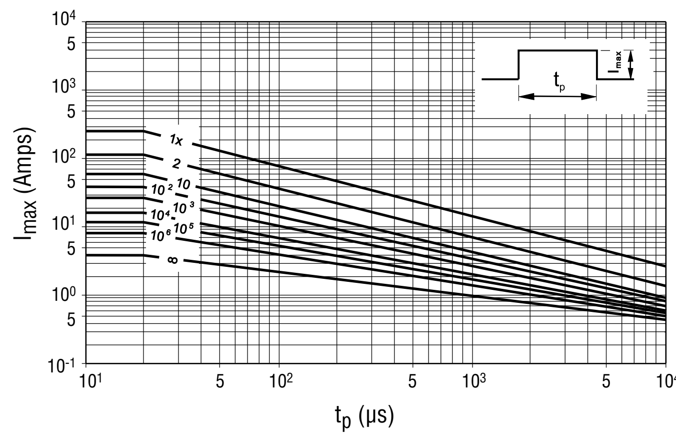
Protection Level

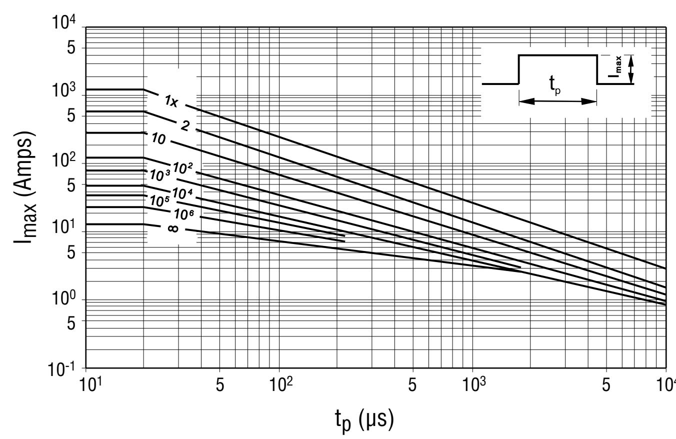
Model Size 4032 - (DV11 ~ DV300)



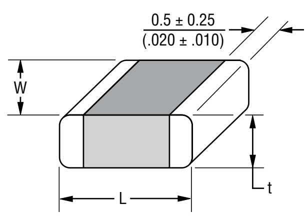
Pulse Rating Curves

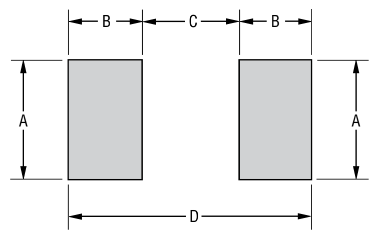
Model Size 4032 - (DV11 ~ DV40)





Soldering Pad Configuration





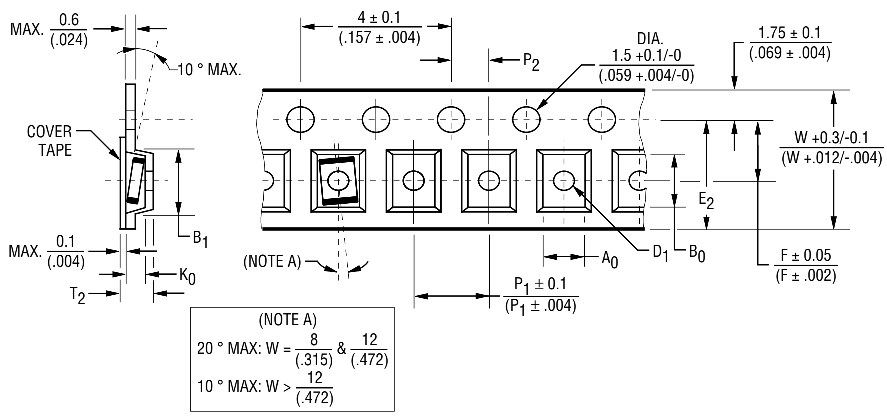
DIMENSIONS: MM / (INCHES)

Size	Voltage Range (V)	Dimension							
		L ± 0.5 (.020)	W ± 0.4 (.016)	M ± 0.25 (.010)	t (Max.)	A	B	C	D
3225	11 to 300	8.0 (.315)	6.3 (.248)	0.5 (.020)	2.0 (.079)	6.8 (.268)	1.5 (.059)	6.5 (.256)	9.5 (.374)
4032	11 to 300	10.0 (.394)	8.0 (.315)	0.5 (.020)	2.0 (.079)	6.8 (.268)	1.5 (.059)	8.7 (.343)	11.7 (.461)

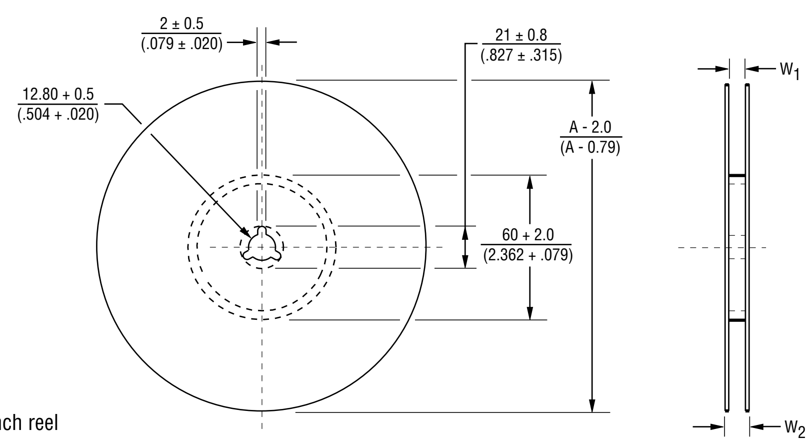
Packaging Specifications

Conforms to IEC Publication 286-3 Ed. 4: 2007-06

Tape



Reel



2,000 pieces per 13-inch reel

Dimension	Model Size	
	3225	4032
Size	7 (.276)	8.6 (.339)
A_0	7.8 (.307)	10.8 (.425)
B_0	3.7 (.146)	
K_0 MAX.	12.1 (.476)	
B_1 MAX.	1.5 (.059)	
D_1 DIA. MAX.	14.25 (.561)	
e_2	12 (.472)	

Dimension	Model Size	
	3225	4032
P_1	7.5 (.295)	
F	16.0 (.630)	
W	9.5 (.374)	
T_2 MAX.	16.4 + 2 (.646 + .079)	
W_1	22.4 (.882)	
W_2 MAX.	15.9 (.626) to 19.4 (.764)	
A DIA.	330 (12.992)	

DIMENSIONS: MM / (INCHES)

Soldering Recommendations for SMD Components

Popular soldering techniques used for surface mounted components are Wave and Infrared Reflow processes. Both processes can be performed with Pb-containing or Pb-free solders. The terminations for these soldering techniques are Barrier Type End Terminations.

End Termination	Designation	Recommended and Suitable for	RoHS Compliant
Barrier Type End Termination	DV Series…R1	Pb-containing and Pb-free soldering	Yes

Wave Soldering

This process is generally associated with discrete components mounted on the underside of printed circuit boards, or for large top-side components with bottom-side mounting tabs to be attached, such as the frames of transformers, relays, connectors, etc. SMD varistors to be wave soldered are first glued to the circuit board, usually with an epoxy adhesive. When all components on the PCB have been positioned and an appropriate amount of time is allowed for adhesive curing, the completed assembly is then placed on a conveyor and run through a single, double wave process.

Infrared Reflow Soldering

These reflow processes are typically associated with top-side component placement. This technique utilizes a mixture of adhesive and solder compounds (and sometimes fluxes) that are blended into a paste. The paste is then screened onto PCB soldering pads specifically designed to accept a particular sized SMD component. The recommended solder paste wet layer thickness is 100 to 300 μm. Once the circuit board is fully populated with SMD components, it is placed in a reflow environment, where the paste is heated to slightly above its eutectic temperature. When the solder paste reflows, the SMD components are attached to the solder pads.

Solder Fluxes

Solder fluxes are generally applied to populated circuit boards to keep oxides from forming during the heating process and to facilitate the flowing of the solder. Solder fluxes can be either a part of the solder paste compound or separate materials, usually fluids. Recommended fluxes are:

- non-activated (R) fluxes, whenever possible
- mildly activated (RMA) fluxes of class L3CN
- class ORLO

Activated (RA), water soluble or strong acidic fluxes with a chlorine content > 0.2 wt. % are NOT RECOMMENDED. The use of such fluxes could create high leakage current paths along the body of the varistor components.

When a flux is applied prior to wave soldering, it is important to completely dry any residual flux solvents prior to the soldering process.

Thermal Shock

To avoid the possibility of generating stresses in the varistor chip due to thermal shock, a preheat stage to within 100 °C of the peak soldering process temperature is recommended. Additionally, SMD varistors should not be subjected to a temperature gradient greater than 4 °C/sec., with an ideal gradient being 2 °C/sec. Peak temperatures should be controlled. Wave and Reflow soldering conditions for SMD varistors with Pb-containing solders are shown on the next page in Fig. 1 and 2 respectively, while Wave and Reflow soldering conditions for SMD varistors with Pb-free solders are shown in Fig. 1 and 3.

Whenever several different types of SMD components are being soldered, each having a specific soldering profile, the soldering profile with the least heat and the minimum amount of heating time is recommended. Once soldering has been completed, it is necessary to minimize the possibility of thermal shock by allowing the hot PCB to cool to less than 50 °C before cleaning.

Soldering Recommendations for SMD Components (Continued)

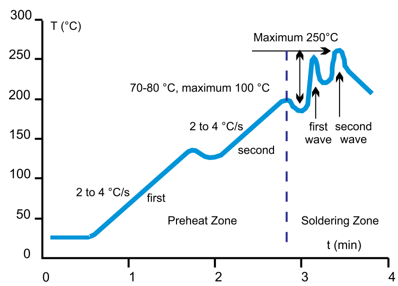


Fig. 1. Wave Soldering Temperature Profile for Pb-free and Pb-containing Soldering

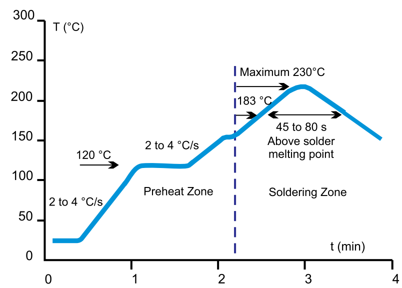


Fig. 2. Infrared Reflow Temperature Profile for Pb-containing Soldering

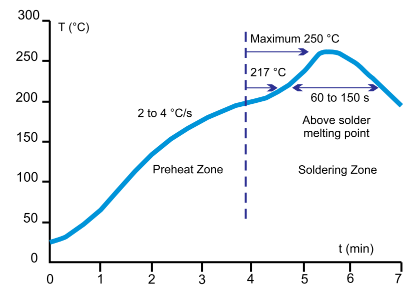


Fig. 3. Reflow Temperature Profile for Pb-free Soldering

Inspection Criteria

When Wave or Infrared Reflow processes are used, the inspection criteria to determine acceptable solder joints will depend on several key variables, principally termination material process profiles.

Pb-containing Wave and IR Reflow Soldering

Typical “before” and “after” soldering results for Barrier Type End Terminations can be seen in Fig. 4. Barrier type terminated varistors form a reliable electrical contact and metallurgical bond between the end terminations and the solder pads. The bond between these two metallic surfaces is exceptionally strong and has been tested by both vertical pull and lateral (horizontal) push tests. The results, in both cases, meet or exceed established industry standards for adhesion.

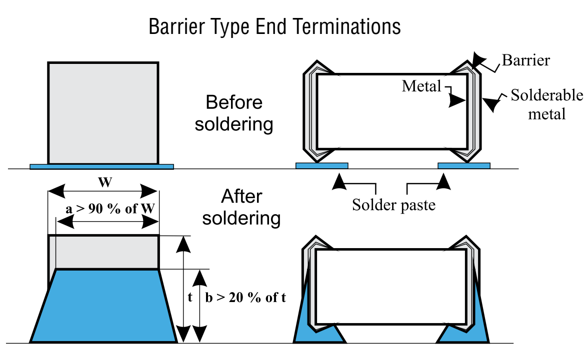


Fig. 4 Soldering Criteria for Wave and IR Reflow Pb-containing Soldering

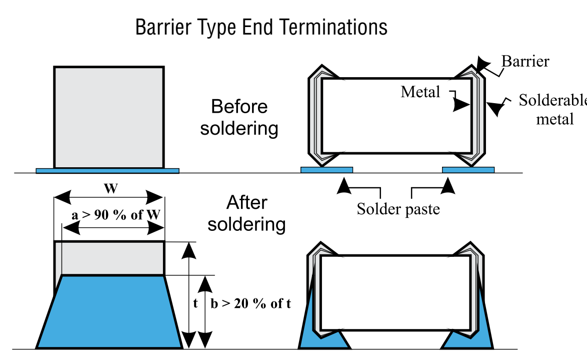


Fig. 5 Soldering Criteria for Wave and IR Reflow Pb-free Soldering

Pb-free Wave and IR Reflow Soldering

Solder forms a metallurgical junction with the entire volume of the end termination, i.e., it diffuses from pad to end termination across the inner side, forming a “mirror” or “negative meniscus. The height of the solder penetration can be clearly seen on the end termination and is always 30 % higher than the chip height.

Since barrier type terminations on Bourns® chips do not require the use of sometimes problematic nickel and tin-alloy electroplating processes, these varistors are truly considered environmentally friendly.

Soldering Recommendations for SMD Components (Continued)

Solder Test and Retained Samples

Reflow soldering test based on J-STD-020D.1 and soldering test by dipping based on IEC 60068- 2 for Pb-free solders are performed on each production lot as shown in the following chart. Test results and accompanying samples are retained for a minimum of two (2) years. The solderability of a specific lot can be checked at any time within this period, should a customer require this information.

Test	Resistance to Flux	Solderability	Static Leaching (Simulation of Reflow Soldering)	Dynamic Leaching (Simulation of Wave Soldering)
Soldering method	Dipping	Dipping	Dipping	Dipping with Agitation
Flux	L3CN, ORL0	L3CN, ORL0, R	L3CN, ORL0, R	L3CN, ORL0, R
Pb Solder	62Sn / 36Pb / 2Ag			
Pb Soldering Temperature (°C)	235 ± 5	235 ± 5	260 ± 5	235 ± 5
Pb-Free Solder	Sn96 / Cu0,4-0,8 / 3-4Ag			
Pb-Free Soldering Temperature (°C)	250 ± 5	250 ± 5	280 ± 5	250 ± 5
Soldering Time (sec.)	2	210	10	> 15
Burn-in Conditions	V_{dcmax}, 48 hours	-	-	-
Acceptance Criterion	dVn < 5 %, i_{dc} must stay unchanged	> 95 % of end termination must be covered by solder	> 95 % of end termination must be intact and covered by solder	> 95 % of end termination must be intact and covered by solder

Rework Criteria - Soldering Iron

Unless absolutely necessary, the use of soldering irons is NOT recommended for reworking varistor chips. If no other means of rework is available, the following criteria must be strictly followed:

- Do not allow the tip of the iron to directly contact the top of the chip
- Do not exceed the following soldering iron specifications:
  - Output Power......................................30 Watts Maximum
  - Temperature of Soldering Iron Tip.......280 °C Maximum
  - Soldering Time....................................10 Seconds Maximum

Storage Conditions

SMD varistors should be used within 1 year of purchase to avoid possible soldering problems caused by oxidized terminals. The storage environment should be controlled, with humidity less than 40 % and temperature between -25 and +45 °C. Varistor chips should always be stored in their original packaged unit.

When varistor chips have been in storage for more than 1 year, and when there is evidence of solderability difficulties, Bourns can often “refresh” the terminations to eliminate these problems.

Reliability Testing Procedures

Varistor test procedures comply with CECC 42200, IEC 1051-1/2 (and AEC-Q200, if applicable for automotive grade products). Test results are available upon customer request. Special tests can be performed upon customer request.

Reliability Parameter	Test	Tested According to	Condition to be Satisfied after Testing
AC/DC Bias Reliability	AC/DC Life Test	CECC 42200, Test 4.20 or IEC 1051-1, Test 4.20, AEC-Q200 Test 8 - 1000 h at UCT	$\lvert\delta V_n (1\ mA)\rvert < 10\ \%$
Pulse Current Capability	I_{max} 8/20 μs	CECC 42200, Test C 2.1 or IEC 1051-1, Test 4.5 10 pulses in the same direction at 2 pulses per minute at maximum peak current for 10 pulses	$\lvert\delta V_n (1\ mA)\rvert < 10\ \%$ no visible damage
Pulse Energy Capability	W_{max} 10/1000 μs	CECC 42200, Test C 2.1 or IEC 1051-1, Test 4.5 10 pulses in the same direction at 1 pulse every 2 minutes at maximum peak current for 10 pulses	$\lvert\delta V_n (1\ mA)\rvert < 10\ \%$ no visible damage
WLD Capability	WLD x 10	ISO 7637, Test pulse 5, 10 pulses at rate of 1 per minute	$\lvert\delta V_n (1\ mA)\rvert < 15\ \%$ no visible damage
V_{jump} Capability	V_{jump} 5 min.	Increase of supply voltage to $V \geq V_{jump}$ for 1 minute	$\lvert\delta V_n (1\ mA)\rvert < 15\ \%$ no visible damage
Environmental and Storage Reliability	Climatic Sequence	CECC 42200, Test 4.16 or IEC 1051-1, Test 4.17 a) Dry heat, 16h, UCT, Test Ba, IEC 68-2-2 b) Damp heat, cyclic, the first cycle: 55 °C, 93 % RH, 24 h, Test Db 68-2-4 c) Cold, LCT, 2 h, Test Aa, IEC 68-2-1 d) Damp heat cyclic, remaining 5 cycles: 55 °C, 93 % RH, 24 h/cycle, Test Bd, IEC 68-2-30	$\lvert\delta V_n (1\ mA)\rvert < 10\ \%$
	Thermal Shock	CECC 42200, Test 4.12, Test Na, IEC 68-2-14, AEC-Q200 Test 16, 5	$\lvert\delta V_n (1\ mA)\rvert < 10\ \%$ no visible damage
	Steady State Damp Heat	CECC 42200, Test 4.17, Test Ca, IEC 68-2-3, AEC-Q200 Test 6, 56 days, 40 °C, 93 % RH, AEC-Q200 Test 7: Bias, Rh, T all at 85.	$\lvert\delta V_n (1\ mA)\rvert < 10\ \%$
	Storage Test	IEC 68-2-2, Test Ba, AEC-Q200 Test 3, 1000 h at maximum storage temperature	$\lvert\delta V_n (1\ mA)\rvert < 5\ \%$

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Reliability Testing Procedures (Continued)

Reliability Parameter	Test	Tested According to	Condition to be Satisfied after Testing
Mechanical Reliability	Solderability	CECC 42200, Test 4.10.1, Test Ta, IEC 68-2-20 solder bath and reflow method	Solderable at shipment and after 2 years of storage, criteria: >95% must be covered by solder for reflow meniscus
	Resistance to Soldering Heat	CECC 42200, Test 4.10.2, Test Tb, IEC 68-2-20 solder bath nad reflow method	$\lvert \delta V_n$ (1 mA)$\rvert < 5$ %
	Terminal Strength	JIS-C-6429, App. 1, 18N for 60 sec. - same for AEC-Q200 Test 22	No visual damage
	Board Flex	JIS-C-6429, App. 2, 2 mm min. AEC-Q200 test 21 - Board flex: 2 mm flex min.	$\lvert \delta V_n$ (1 mA)$\rvert < 2$ % No visible damage
	Vibration	CECC 42200, Test 4.15, Test Fc, IEC 68-2-6, AEC-Q200 Test 14 Frequency range 10 to 55 Hz (AEC: 10-2000 Hz) Amplitude 0.75 m/s^2 or 98 m/s^2 (AEC: 5 g for 20 minutes) Total duration 6 h (3x2 h) (AEC: 12 cycles each of 3 directions) Waveshape - half sine	$\lvert \delta V_n$ (1 mA)$\rvert < 2$ % No visible damage
	Mechanical Shock	CECC 42200, Test 4.14, Test Ea, IEC 68-2-27, AEC-Q200 Test 13. Acceleration = 490 m/s^2 (AEC: MIL-STD-202-Method 213), Pulse duration = 11 ms, Waveshape - half sine; Number of shocks = 3x6	$\lvert \delta V_n$ (1 mA)$\rvert < 10$ % No visible damage
Electrical Transient Conduction	ISO-7637-1 Pulses	AEC-Q200 Test 30: Test pulses 1 to 3. Also other pulses - freestyle.	$\lvert \delta V_n$ (1 mA)$\rvert < 10$ % No visible damage

Terrminology

Term	Symbol	Definition
Rated AC Voltage	V_{rms}	Maximum continuous sinusoidal AC voltage (<5 % total harmonic distortion) which may be applied to the component under continuous operation conditions at +25 °C
Rated DC Voltage	V_{dc}	Maximum continuous DC voltage (<5 % ripple) which may be applied to the component under continuous operating conditions at +25 °C
Supply Voltage	V	The voltage by which the system is designated and to which certain operating characteristics of the system are referred; V_{rms} = 1.1 x V
Leakage Curreent	I_{dc}	The current passing through the varistor at V_{dc} and at +25 ° or at any other specified temperature
Varistor Voltage	V_n	Voltage across the varistor measured at a given reference current (I_n)
Reference Current	I_n	Reference current = 1 mA DC
Clamping Voltage Protection Level	V_c	The peak voltage developed across the varistor under standard atmospheric conditions, when passing an 8/20 μs class current pulse
Class Current	I_c	A peak value of current which is 1/10 of the maximum peak current for 100 pulses at two per minute for the 8/20 μs pulse
Voltage Clamping Ratio	V_c/V_{app}	A figure of merit measure of the varistor clamping effectiveness as defined by the symbols V_c/V_{app}, where (V_{app} = V_{rms} or V_{dc})
Jump Start Transient	V_{jump}	The jump start transient results from the temporary application of an overvoltage in excess of the rated battery voltage. The circuit power supply may be subjected to a temporary overvoltage condition due to the voltage regulation failing or it may be deliberately generated when it becomes necessary to boost start the car.
Rated Single Pulse Transient Energy	W_{max}	Energy which may be dissipated for a single 10/1000 μs pulse of a maximum rated current, with rated AC voltage or rated DC voltage also applied, without causing device failure
Load Dump Transient	WLD	Load Dump is a transient which occurs in automotive environments. It is an exponentially decaying positive voltage which occurs in the event of a battery disconnect while the alternator is still generating charging current with other loads remaining on the alternator circuit at the time of battery disconnect.
Rated Peak Single Pulse Transient Current	I_{max}	Maximum peak current which may be applied for a single 8/20 μs pulse, with rated line voltage also applied, without causing device failure
Rated Transient Average Power Dissipation	P	Maximum average power which may be dissipated due to a group of pulses occurring within a specified isolated time period, without causing device failure at 25 °C
Capacitance	C	Capacitance between two terminals of the varistor measured @ 1 kHz
Non-linearity Exponent	α	A measure of varistor nonlinearity between two given operating currents, I_n and I_1 as described by I = k V exp(a), where: - k is a device constant, - $I_1 < I < I_n$ and - a log (I_1/I_n)/log(V_1/V_n) = 1/log (V_1/V_n), where: - I_r is reference current (1 mA) and V_n is varistor voltage - I_1 = 10 I_n, V_1 is the voltage measured at I_1
Response Time	tr	The time lag between application of a surge and varistor's "turn-on" conduction action
Varistor Voltage Temperature Coefficient	TC	(V_n @ 85 °C - V_n @ 25 °C) / (V_n @ 25 °C) x 60 °C) x 100
Insulation Resistance	IR	Minimum resistance between shorted terminals and varistor surface
Isolation Voltage		The maximum peak voltage which may be applied under continuous operating conditions between the varistor terminations and any conducting mounting surface
Operating Temperature		The range of ambient temperature for which the varistor is designed to operate continuously as defined by the temperature limits of its climatic category
Climatic Category	LCT/UCT/DHD	LCT & UCT = Lower and Upper Category Temperature - the minimum and maximum ambient temperatures for which a varistor has been designed to operate continuously. DHD = Dump Heat Test Duration
Storage Temperature		Storage temperature range without voltage applied
Current/Energy Derating		Derating of maximum values when operated above UCT

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C1753 05/17/18R