Ultralow Power Step-Down Regulator for Energy Harvesting

Data Sheet

ADP5304

FEATURES

- Input supply voltage range: 2.15 V to 6.50 V
- Operation down to 2.00 V typical
- Ultralow, 260 nA typical quiescent current with no load
- Selective output voltage from 1.2 V to 3.6 V (or 0.8 V to 5.0 V)
- ±2.5% output accuracy over the full temperature range
- Output current up to 50 mA in hysteresis mode
- VINOK flag to monitor the input voltage
- 100% duty cycle operation mode
- Quick output discharge (QOD) option
- Undervoltage lockout (UVLO), overcurrent protection (OCP), and thermal shutdown (TSD) protection
- 10-lead, 3 mm × 3 mm LFCSP package
- –40°C to +125°C operating junction temperature range

APPLICATIONS

- Energy (gas, water) metering
- Energy harvesting applications
- Portable and battery-powered equipment
- Medical applications
- Keep-alive power supply

TYPICAL APPLICATION CIRCUIT

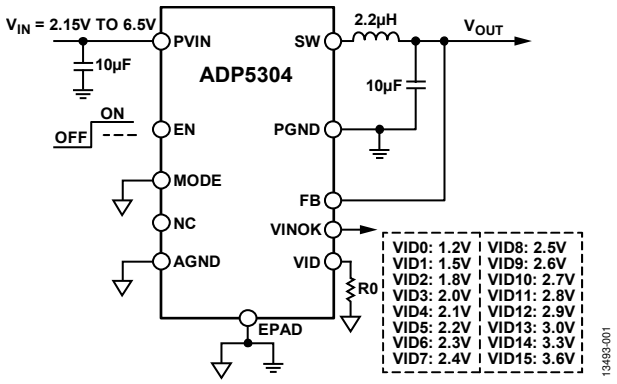

Figure 1.

GENERAL DESCRIPTION

The ADP5304 is a high efficient, ultralow quiescent current step-down regulator that draws only 260 nA of quiescent current to regulate the output at no load.

The ADP5304 runs from an input voltage range of 2.15 V to 6.50 V, allowing the use of the multiple alkaline, NiMH, and Lithium cells, or the use of a high impedance power source. The output voltage is selectable from 0.8 V to 5.0 V by an external VID resistor to ground. The total solution requires only four tiny external components.

The ADP5304 operates in hysteresis mode via connecting the MODE pin to ground. In hysteresis mode, the regulator achieves excellent efficiency at a power of less than 1 mW and provides up to 50 mA of output load. The device enables very efficient power management to achieve the collection of small amounts of energy from the high impedance battery or the energy harvester to charge up the conventional capacitor or super capacitor.

The ADP5304 integrates an ultralow power comparator with a factory programmable voltage reference to monitor the voltage of the input power source. The voltage reference, with hysteresis, is the threshold for the stopping and the starting of the switching, allowing the use of the high impedance power source.

Other key features of the ADP5304 include separate enabling and a QOD. Safety features, such as OCP, TSD, and input UVLO are also included.

The ADP5304 is available in 10-lead, 3 mm × 3 mm LFCSP package rated for the –40°C to +125°C junction temperature range.

Rev. 0 Document Feedback

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Technical Support www.analog.com

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REVISION HISTORY

10/15—Revision 0: Initial Version

DETAILED FUNCTIONAL BLOCK DIAGRAM

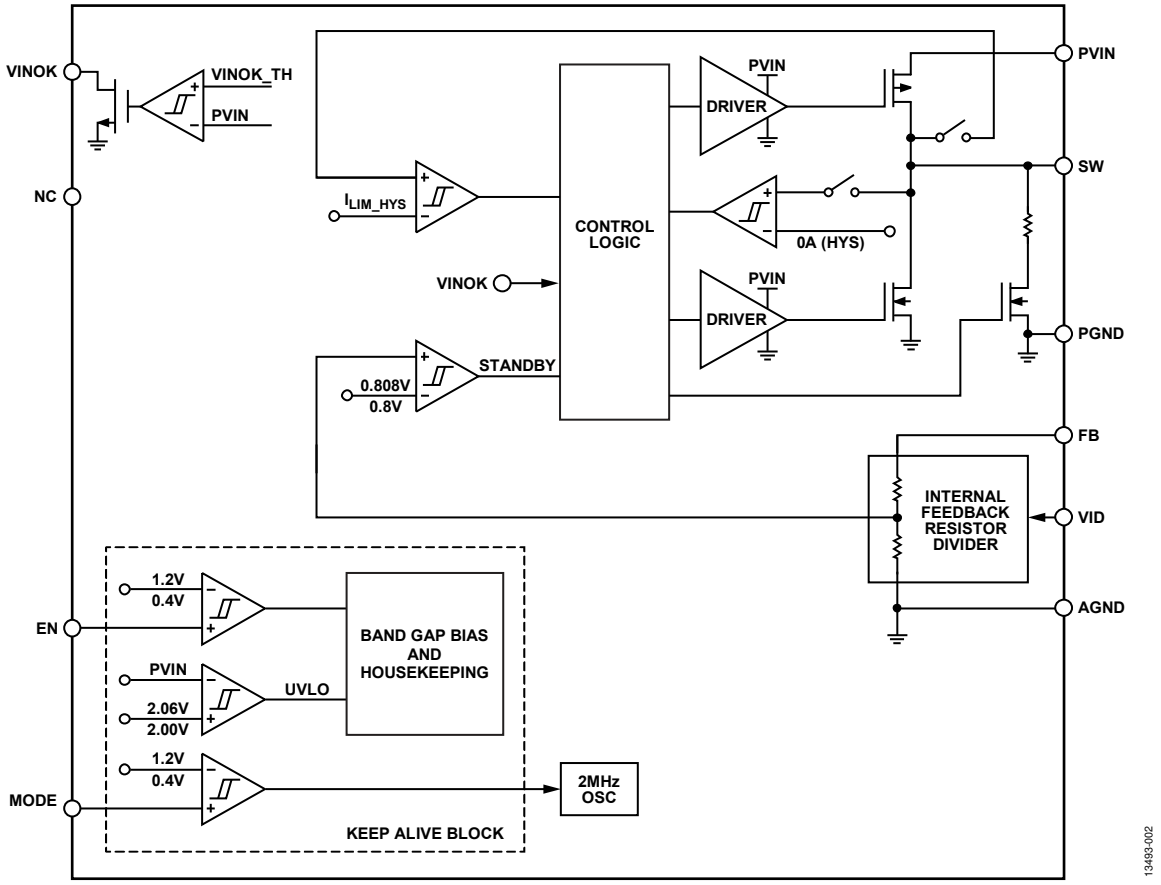

Figure 2.

SPECIFICATIONS

V_{IN} = 3.6 V, V_{OUT} = 2.5 V, T_J = −40°C to +125°C for minimum and maximum specifications, and T_A = 25°C for typical specifications, unless otherwise noted.

Table 1.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
INPUT SUPPLY VOLTAGE RANGE	V_{IN}	2.15		6.50	V	
SHUTDOWN CURRENT	$I_{SHUTDOWN}$		18	40	nA	V_{EN} = 0 V, −40°C ≤ T_J ≤ +85°C
			18	130	nA	V_{EN} = 0 V, −40°C ≤ T_J ≤ +125°C
QUIESCENT CURRENT						
Operating Quiescent Current	I_Q		260	360	nA	−40°C ≤ T_J ≤ +85°C
			260	500	nA	−40°C ≤ T_J ≤ +125°C
			640	1500	nA	100% duty cycle operation, V_{IN} = 3.0 V, V_{OUT} set as 3.3 V
UNDERVOLTAGE LOCKOUT	UVLO					
UVLO Threshold						
Rising	V_{UVLO_RISING}		2.06	2.14	V	
Falling	$V_{UVLO\_FALLING}$	1.90	2.00		V	
EN PIN						
Input Voltage Threshold						
High	V_{IH}	1.2			V	
Low	V_{IL}			0.4	V	
Input Leakage Current	$I_{EN\_LEAKAGE}$			25	nA	
FB PIN						
Output Options by VID Resistor	V_{OUT_OPT}	0.8		5.0	V	0.8 V to 5.0 V in different factory option
Fixed VID Code Threshold Accuracy from Active Mode to Standby Mode	V_{FB_FIX}	−0.75		+0.75	%	T_J = 25°C
		−2.5		+2.5	%	−40°C ≤ T_J ≤ +125°C
Adjustable VID Code Threshold Accuracy from Active Mode to Standby Mode	V_{FB_ADJ}	−3		+3	%	−40°C ≤ T_J ≤ +125°C
Hysteresis of Threshold Accuracy from Active Mode to Standby Mode	$V_{FB\ (HYS)}$		1		%	
Feedback Bias Current	I_{FB}		66	95	nA	Output Option 0, V_{OUT} = 2.5 V
			25	45	nA	Output Option 1, V_{OUT} = 1.3 V
SW PIN						
High-Side Power FET On Resistance	$R_{DS\ (ON)\ H}$		386	520	mΩ	Pin to pin measurement
Low-Side Power FET On Resistance	$R_{DS\ (ON)\ L}$		299	470	mΩ	Pin to pin measurement
Peak Current	I_{LIM}		265		mA	
Minimum On Time	t_{MIN_ON}		40	70	ns	
VINOK PIN						
VINOK Monitor Threshold Range	$V_{VINOK\ (RISE)}$	2.05		5.15	V	Factory programmable
VINOK Monitor Accuracy Range		−1.5		+1.5	%	T_J = 25°C
		−3		+3	%	−40°C ≤ T_J ≤ +125°C
VINOK Monitor Threshold Hysteresis	$V_{VINOK\ (HYS)}$		1.5		%	
VINOK Rising Delay	t_{VINOK_RISE}		190		µs	
VINOK Falling Delay	t_{VINOK_FALL}		130		µs	
Leakage Current for the VINOK Pin	$I_{VINOK\_LEAKAGE}$		0.1	1	µA	
Output Low Voltage for the VINOK Pin	V_{VINOK_LOW}		50	100	mV	I_{VINOK} = 100 µA
SOFT START						
Default Soft Start Time	t_{SS}		350		µs	Factory trim, 1 bit (350 µs, 2800 µs)
Start-Up Delay	t_{START_DELAY}		2		ms	Delay from the EN pin being pulled high
C_{OUT} DISCHARGE SWITCH ON RESISTANCE	R_{DIS}		290		Ω	
THERMAL SHUTDOWN						
Threshold	T_{SHDN}		142		°C	
Hysteresis	T_{HYS}		127		°C	

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
PVIN to PGND	−0.3 V to +7 V
SW to PGND	−0.3 V to PVIN + 0.3 V
FB to AGND	−0.3 V to +7 V
VID to AGND	−0.3 V to +7 V
EN to AGND	−0.3 V to +7 V
VINOK to AGND	−0.3 V to +7 V
MODE to AGND	−0.3 V to +7 V
NC to AGND	−0.3 V to +7 V
PGND to AGND	−0.3 V to +0.3 V
Storage Temperate Range	−65°C to +150°C
Operating Junction Temperature Range	−40°C to +125°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 3. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
10-Lead, 3 mm × 3 mm LFCSP	57	0.86	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

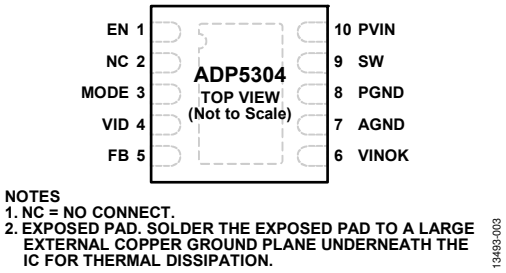

Figure 3. Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	EN	Enable Input for the Regulator. A logic low on this pin disables the regulator.
2	NC	No Connect. Connect this pin to ground.
3	MODE	Operating Mode Pin. Connect this pin to ground; the regulator operates in hysteresis mode.
4	VID	Voltage Configuration Pin. Connect one resistor from this pin to ground to configure the output voltage of the regulator.
5	FB	Feedback Sensing Input for the Regulator.
6	VINOK	Input Power-Good Signal. This open-drain output is the power-good signal for the input voltage.
7	AGND	Analog Ground.
8	PGND	Power Ground.
9	SW	Switching Node Output for the Regulator.
10	PVIN	Power Input for the Regulator.
	EPAD	Exposed Pad. Solder the exposed pad to a large external copper ground plane underneath the IC for thermal dissipation.

TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} =3.6 V, V_{OUT} = 2.5 V, L1 = 2.2 µH, C_{IN} = C_{OUT} = 10 µF, f_{SW} = 2 MHz, T_A = 25°C, unless otherwise noted.

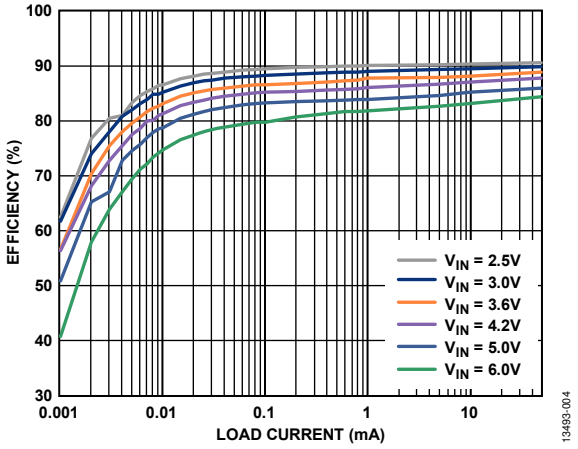

Figure 4. Hysteresis Efficiency vs. Load Current, V_{OUT} = 1.2 V

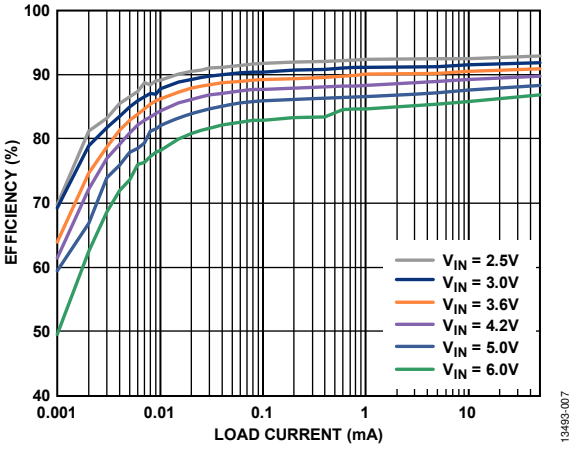

Figure 7. Hysteresis Efficiency vs. Load Current, V_{OUT} = 1.5 V

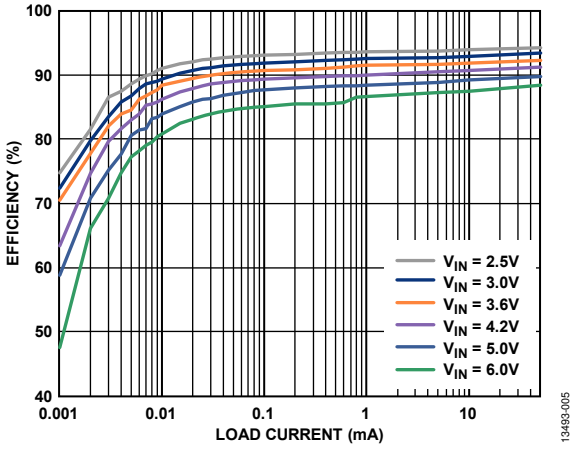

Figure 5. Hysteresis Efficiency vs. Load Current, V_{OUT} = 1.8 V

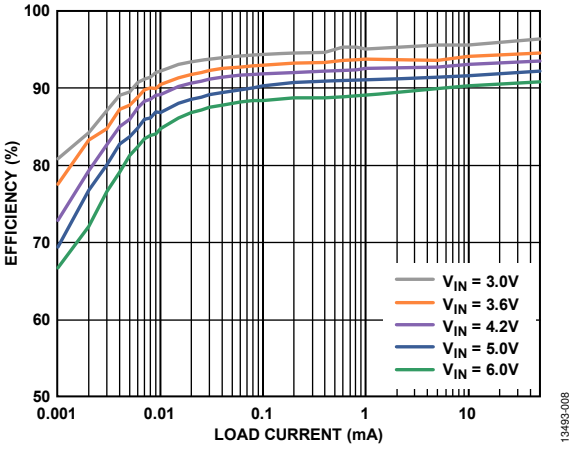

Figure 8. Hysteresis Efficiency vs. Load Current, V_{OUT} = 2.5 V

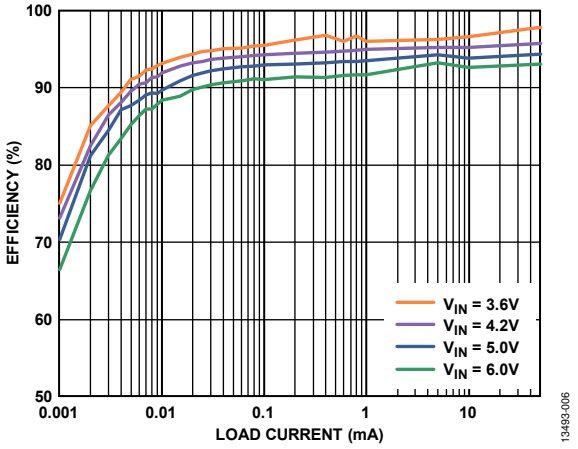

Figure 6. Hysteresis Efficiency vs. Load Current, V_{OUT} = 3.3 V

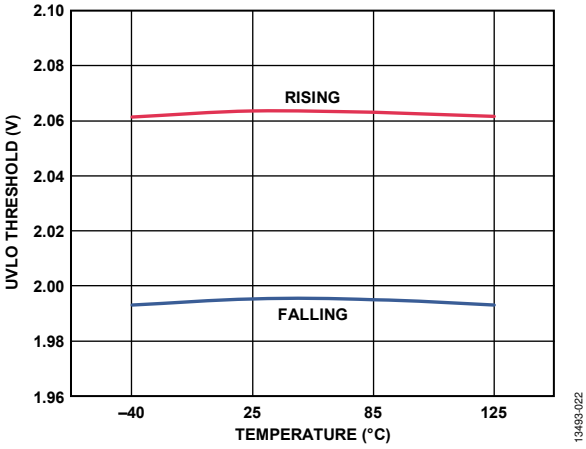

Figure 9. UVLO Threshold, Rising and Falling vs. Temperature

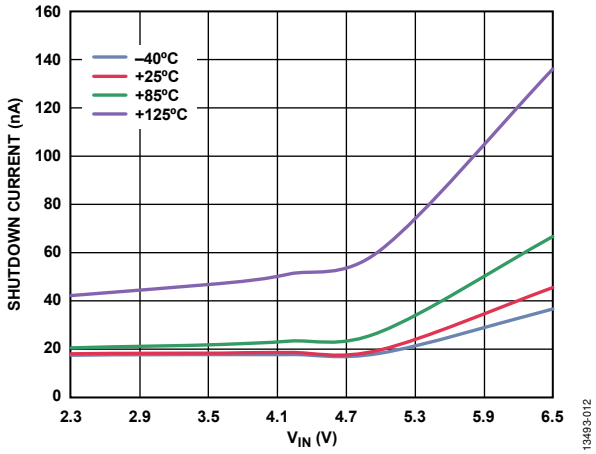

Figure 10. Shutdown Current vs. V_{IN}, EN = Low

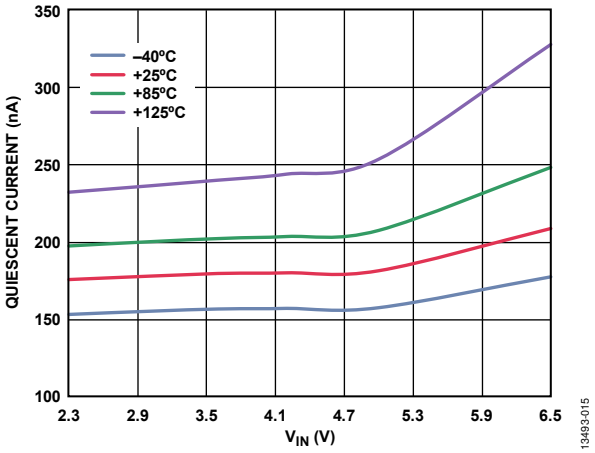

Figure 13. Quiescent Current vs. V_{IN}

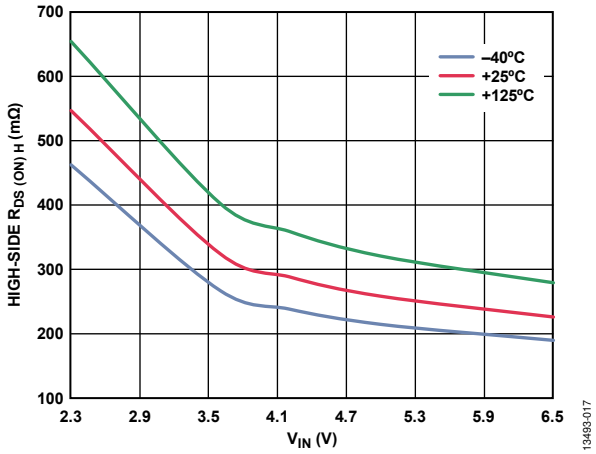

Figure 11. High-Side $R_{DS(ON)H}$ vs. V_{IN}

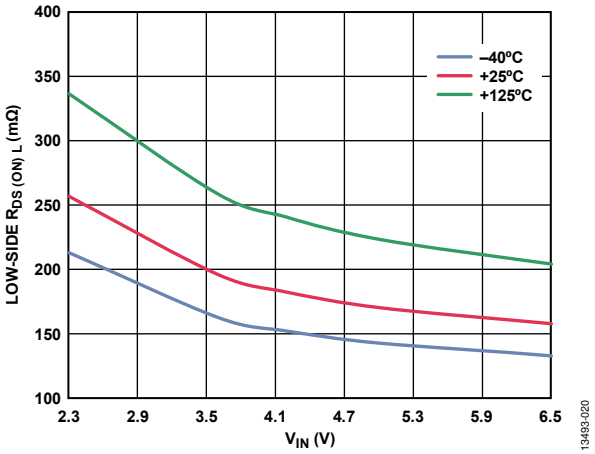

Figure 14. Low-Side $R_{DS(ON)L}$ vs. V_{IN}

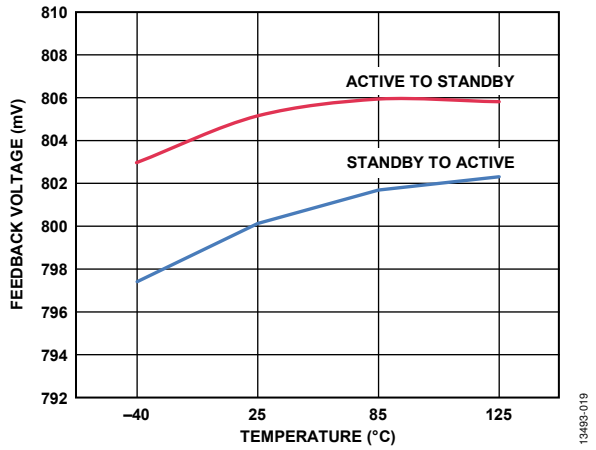

Figure 12. Feedback Voltage vs. Temperature

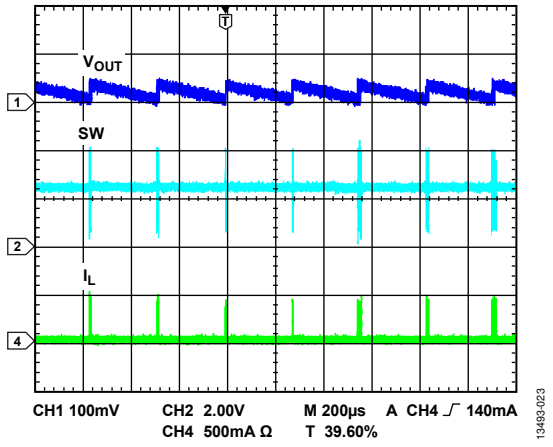

Figure 15. Steady Waveform, I_{LOAD} = 1 mA (I_L is the Inductor Current)

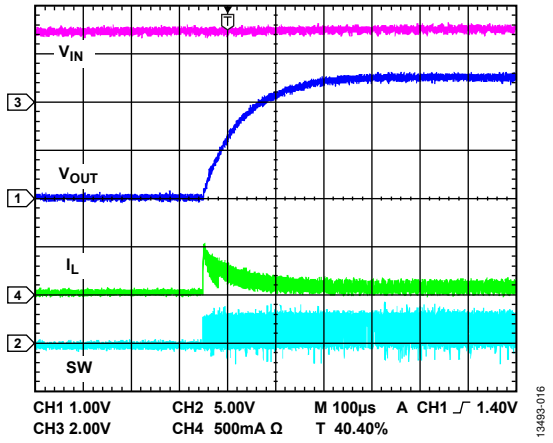

Figure 16. Soft Start, I_{LOAD} = 50 mA

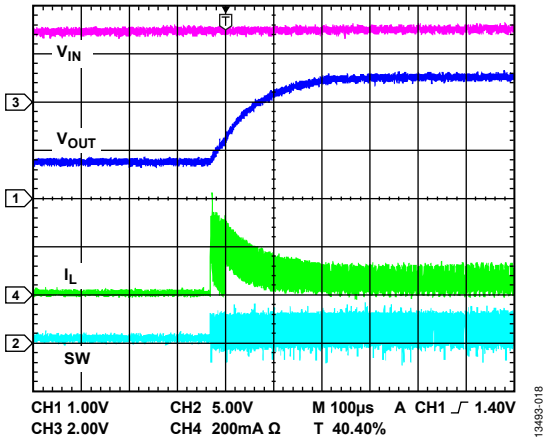

Figure 19. Soft Start with Precharge Function

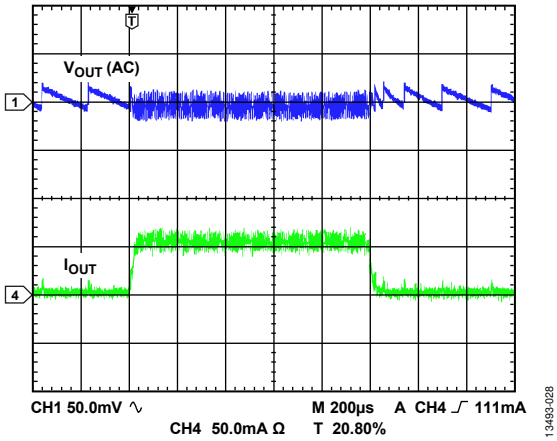

Figure 17. Load Transient, I_{LOAD} from 0 mA to 50 mA

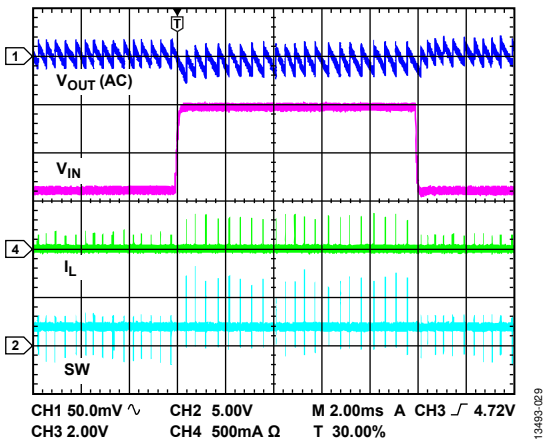

Figure 20. Line Transient, I_{LOAD} = 10 µA

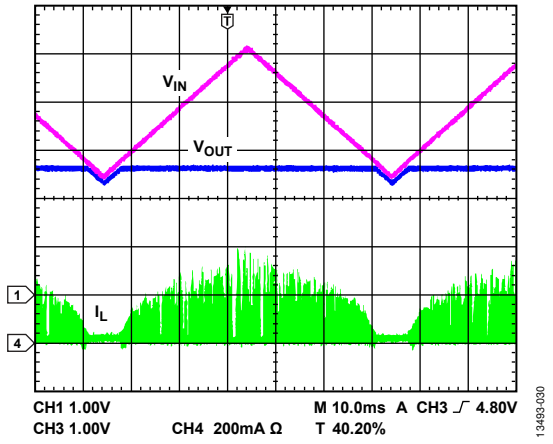

Figure 18. Input Voltage Ramp-Up and Ramp-Down

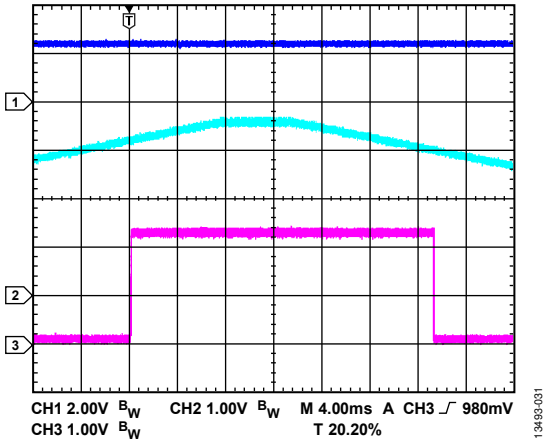

Figure 21. VINOK Function at a 3.0 V VINOK Threshold

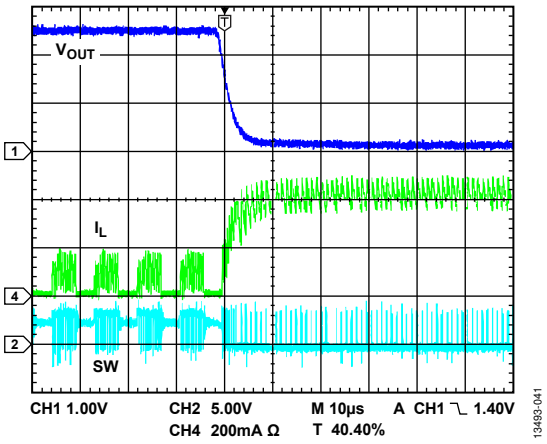

Figure 22. Output Short Protection

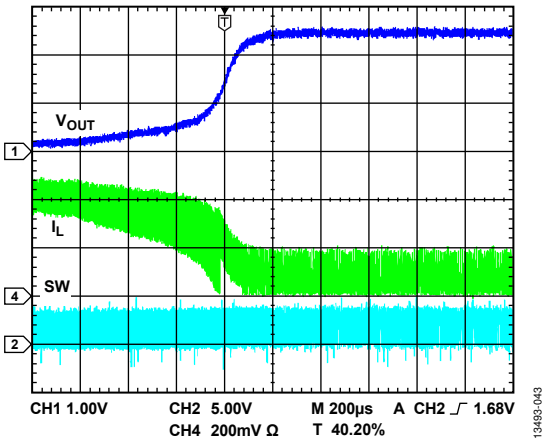

Figure 24. Output Short Recovery

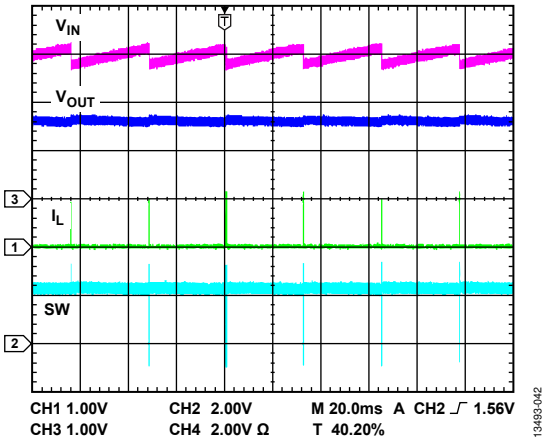

Figure 23. 260 µA Current Source Charge Up, 100 µF Output Capacitor with 100 µA Load Current, and 3.0 V VINOK Threshold

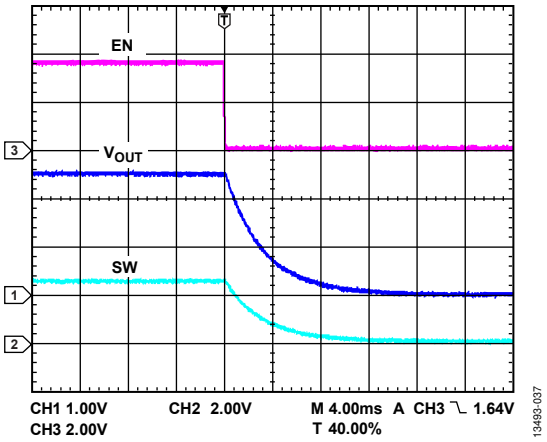

Figure 25. Quick Output Discharge Function

THEORY OF OPERATION

The ADP5304 is a high efficient, ultralow quiescent current step-down regulator in a 10-lead LFCSP package, designed to meet demanding performance and board space requirements. The device enables direct connection to a wide input voltage range of 2.15 V to 6.50 V, allowing the use of high impedance power sources or energy harvester sources.

BUCK REGULATOR OPERATIONAL MODE

The ADP5304 buck regulator operates in hysteresis mode and charges the output voltage slightly higher than its nominal output voltage with PWM pulses via the regulation of constant peak inductor current. When the output voltage increases until the output sense signal exceeds the hysteresis upper threshold, the regulator enters the standby mode. In standby mode, the high-side and low-side MOSFET and a majority of the circuitry are disabled to allow a low quiescent current, as well as high efficiency performance. During standby mode, the output capacitor supplies the energy into the load and the output voltage decreases until it falls below the hysteresis comparator lower threshold. Then, the buck regulator wakes up into active mode and generates the PWM pulses to charge the output again.

The buck regulator is forced to operate in hysteresis mode via connecting the MODE pin to ground. The regulator only draws 260 nA of quiescent current to regulate the output under zero load, which allows the regulator to act as keep-alive power supply in battery-powered applications or energy harvesting systems.

ADJUSTABLE AND FIXED OUTPUT VOLTAGES

The ADP5304 provides adjustable output voltage settings via the connection of one resistor through the VID pin to AGND. The VID detection circuitry works in the start-up period, and the voltage ID code is sampled and held into the internal register and does not change until the next power recycle. Furthermore, the ADP5304 provides a fixed output voltage programmed via the factory fuse. In this condition, connect the VID pin to the PVIN pin.

For output voltage settings, the feedback resistor divider is built in to the ADP5304, and the feedback pin (FB) must be tied directly to the output. An ultralow power voltage reference and an integrated high impedance (50 MΩ, typical) feedback divider network contribute to low quiescent current. Table 5 lists the output voltage options by the VID pin configurations. It is recommended to use a 1% resistor.

Table 5. Output Voltage Options by the VID Pin

VID Configuration	V_{OUT}, Factory Option 0 (V)	V_{OUT}, Factory Option 1 (V)
Short to ground	3.0	3.1
Short to PVIN	2.5	1.3
R_{VID} = 499 kΩ	3.6	5.0
R_{VID} = 316 kΩ	3.3	4.5
R_{VID} = 226 kΩ	2.9	4.2
R_{VID} = 174 kΩ	2.8	3.9
R_{VID} = 127 kΩ	2.7	3.4
R_{VID} = 97.6 kΩ	2.6	3.2
R_{VID} = 76.8 kΩ	2.4	1.9
R_{VID} = 56.2 kΩ	2.3	1.7
R_{VID} = 43 kΩ	2.2	1.6
R_{VID} = 32.4 kΩ	2.1	1.4
R_{VID} = 25.5 kΩ	2.0	1.1
R_{VID} = 19.6 kΩ	1.8	1.0
R_{VID} = 15 kΩ	1.5	0.9
R_{VID} = 11.8 kΩ	1.2	0.8

UNDERVOLTAGE LOCKOUT (UVLO)

The undervoltage lockout circuitry monitors the input voltage level on the PVIN pin. If input voltage falls below 2.00 V (typical), the regulator turns off. After the input voltage rises above 2.06 V (typical), the soft start period initiates, and when the EN pin is high, the regulator enables.

ENABLE/DISABLE

The ADP5304 includes a separate enable (EN) pin. A logic high on the EN pin starts the regulator. Due to the low quiescent current design, it is typical for the regulator to start switching after a delay of a few milliseconds from the EN pin being pulled high.

A logic low on the EN pin immediately disables the regulator and brings the regulator into extremely low current consumption.

VINOK FUNCTION

The ADP5304 includes an open-drain VINOK output that can be used to indicate the input voltage status. The VINOK output becomes active high when the input voltage on the PVIN pin is above the reference threshold. When the input voltage falls below the reference threshold, the VINOK pin goes low. Note that a relatively long validation time of 130 µs typical exists for the VINOK output status to change due to the ultralow power comparator design.

The ADP5304 VINOK threshold also determines the time when the buck regulator starts and stops switching. When the input voltage is below the threshold, the regulator stops switching in hysteresis mode. After the input source charges the input capacitor voltage above a hysteresis from the threshold, the regulator resumes switching. The regulator operates the input voltage in a hysteresis window around the threshold considered as the maximum power point tracking (MPPT). The high impedance input power source or small input power application employs the ADP5304 to charge the large output capacitor via trickle charging.

Different VINOK thresholds are factory programmable from 2.05 V to 5.15 V in 50 mV steps. To order a device with options other than the default options, contact your local Analog Devices, Inc., sales or distribution representative.

CURRENT LIMIT

The buck regulators in the ADP5304 have protection circuitry that limits the direction and the amount of current to a certain level that flows through the high-side MOSFET and the low-side MOSFET in cycle by cycle mode. The positive current limit on the high-side MOSFET limits the amount of current that can flow from the input to the output. The negative current limit on the low-side MOSFET prevents the inductor current from reversing direction and flowing out of the load.

SHORT-CIRCUIT PROTECTION

The buck regulators in the ADP5304 include frequency foldback to prevent current runaway on a hard short. When the output voltage at the feedback pin (FB) falls below 0.3 V typical, indicating the possibility of a hard short at the output, the switching frequency in active mode reduces to half of the internal oscillator frequency. The reduction in the switching frequency allows more time for the inductor to discharge, preventing a runaway of output current.

SOFT START

The ADP5304 has an internal soft start function that ramps the output voltage in a controlled limitation upon startup, thereby limiting the inrush current. This prevents possible input voltage drops when a battery or a high impedance power source is connected to the input of the device. The typical soft start time or the regulator is 350 µs.

A different soft start time (2800 µs) can be programmed for ADP5304 via the factory fuse (see Table 11).

STARTUP WITH PRECHARGED OUTPUT

The buck regulators in the ADP5304 include a precharged start-up feature to protect the low-side FETs from damage during startup. If the output voltage is precharged before the regulator is turned on, the regulator prevents reverse inductor current—which discharges the output capacitor—until the internal soft start reference voltage exceeds the precharged voltage on the feedback pin.

100% DUTY OPERATION

When the input voltage approaches the output voltage, the ADP5304 stops switching and enters 100% duty cycle operation. It connects the output via the inductor and the internal high-side power switch to the input. When the input voltage is charged again and the required duty cycle falls to 95% typical, the buck immediately restarts switching and regulation without allowing overshoot on the output voltage. The ADP5304 draws an ultralow quiescent current of only 640 nA typical during 100% duty cycle operation.

ACTIVE DISCHARGE

The regulator in the ADP5304 integrates an optional, factory programmable discharge switch from the switching node to ground. This switch turns on when its associated regulator is disabled, which helps discharge the output capacitor quickly. The typical value of the discharge switch is 290 Ω for the regulator.

By default, the discharge function is not enabled. The active discharge function can be enabled by the factory fuse

THERMAL SHUTDOWN

If the ADP5304 junction temperature exceeds 142°C, the thermal shutdown circuit turns the IC off, except for the internal linear regulator. Extreme junction temperatures can be the result of high current operation, poor circuit board design, or high ambient temperature. A 15°C hysteresis is included so that the ADP5304 does not return to operation after thermal shutdown until the junction temperature falls below 127°C. When the device exits thermal shutdown, a soft start is initiated for each enabled channel.

APPLICATIONS INFORMATION

This section describes the external components selection for the ADP5304. The typical application circuit is shown in Figure 26.

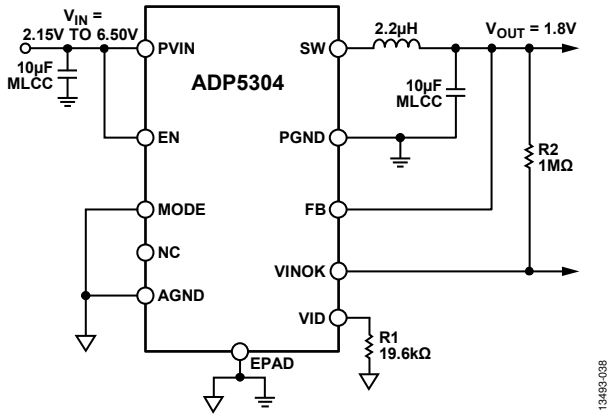

Figure 26. Typical Application Circuit

EXTERNAL COMPONENT SELECTION

The ADP5304 is optimized for operation with a 2.2 µH inductor and 10 µF output capacitors for various output voltages using the closed-loop compensation and adaptive slope compensation circuits. The selection of components depends on the efficiency, the load current transient, and other application requirements. The trade-offs among performance parameters, such as efficiency and transient response, are made by varying the choice of external components.

SELECTING THE INDUCTOR

The high switching frequency of the ADP5304 allows the use of small surface-mount power inductors. The dc resistance (DCR) value of the selected inductor affects efficiency. In addition, it is recommended to select a multilayer inductor rather than a magnetic iron inductor because the high switching frequency increases the core temperature rise and enlarges the core loss.

A minimum requirement of the dc current rating of the inductor is for it to be equal to the maximum load current plus half of the inductor current ripple (ΔI_L), as shown by the following equations:

$$\Delta I_L = V_{OUT} + \left(\frac{1 - V_{OUT}/V_{IN}}{L \times f_{SW}} \right)$$

$$I_{PK} = I_{LOAD\,(MAX)} + \left(\frac{\Delta I_L}{2} \right)$$

where I_{PK} is the peak inductor current.

Use the inductor series from the different vendors shown in Table 6.

OUTPUT CAPACITOR

Output capacitance is required to minimize the voltage overshoot, the voltage undershoot, and the ripple voltage present on the output. Capacitors with low equivalent series resistance (ESR) values produce the lowest output ripple. Furthermore, use capacitors such as X5R and X7R dielectric capacitors. Do not use Y5V and Z5U capacitors, because they are unsuitable choices due to their large capacitance variation over temperature and their dc bias voltage changes. Because ESR is important, select the capacitor using the following equation:

$$ESR_{COUT} \leq \frac{V_{RIPPLE}}{\Delta I_L}$$

where:
ESR_{COUT} is the ESR of the chosen capacitor.
V_{RIPPLE} is the peak-to-peak output voltage ripple.

Increasing the output capacitor value has no effect on stability and may reduce output ripple and enhance load transient response. ADP5304 can charge up the conventional capacitor or super capacitor. When choosing the output capacitor value, it is important to account for the loss of capacitance due to output voltage dc bias.

Use the capacitor series from the different vendors shown in Table 7.

Table 6. Recommended Inductors

Vendor	Model	Inductance (µH)	Dimensions (mm)	DCR (mΩ)	I_{SAT}[1] (A)
TDK	MLP2016V2R2MT0S1	2.2	2.0 × 1.6 × 0.85	280	1.0
Wurth	74479889222	2.2	2.5 × 2.0 × 1.2	250	1.7
Coilcraft	LPS3314-222MR	2.2	3.3 × 3.3 × 1.3	100	1.5

[1] I_{SAT} is the dc current at which the inductance drops 30% (typical) from its value without current.

Table 7. Input and Output Capacitors

Vendor	Model	Capacitance (µF)	Size
Murata	GRM188D71A106MA73	10	0603
Murata	GRM21BR71A106KE51	10	0805
Murata	GRM31CR60J107ME39	100	1206

INPUT CAPACITOR

An input capacitor is required to reduce the input voltage ripple, input ripple current, and source impedance. Place the input capacitor as close as possible to the PVIN pin. A low ESR X7R or X5R capacitor is highly recommended to minimize the input voltage ripple.

Use the following equation to determine the rms input current:

$$I_{RMS} \geq I_{LOAD\ (MAX)} \sqrt{\frac{V_{OUT}\left(V_{IN} - V_{OUT}\right)}{V_{IN}}}$$

For most applications, a 10 µF capacitor is sufficient. The input capacitor can be increased without any limit for better input voltage filtering.

LAYOUT RECOMMENDATIONS

Figure 27 shows the typical printed circuit board (PCB) layout for the ADP5304.

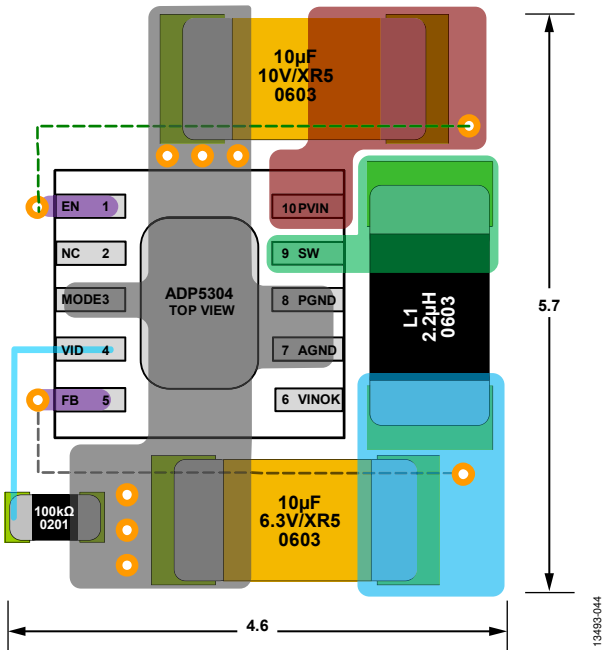

Figure 27. PCB Layout for the ADP5304

TYPICAL APPLICATION CIRCUITS

The ADP5304 can be used as a keep-alive, ultralow power step-down regulator to extend the battery life and load pulse current capability with super capacitors (see Figure 28), and as a battery-powered equipment or wireless sensor network controlled by a microcontroller or a processor (see Figure 29). The VINOK function can achieve the maximum power point tracking.

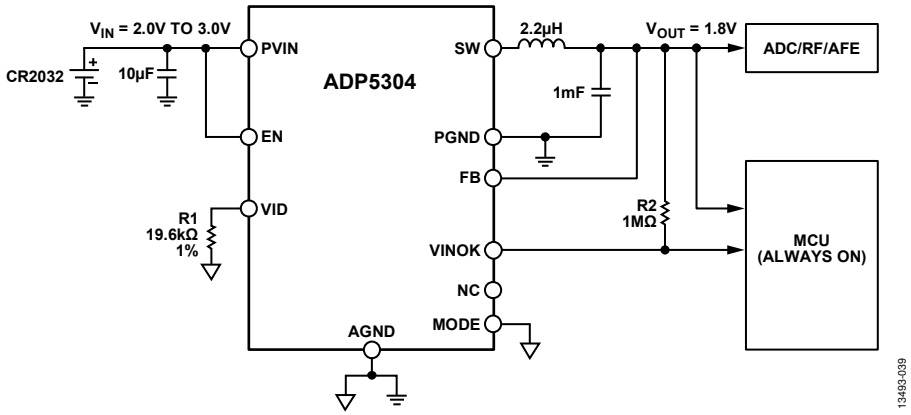

Figure 28. Typical ADP5304 Application with a Coin Cell Battery (CR2032)

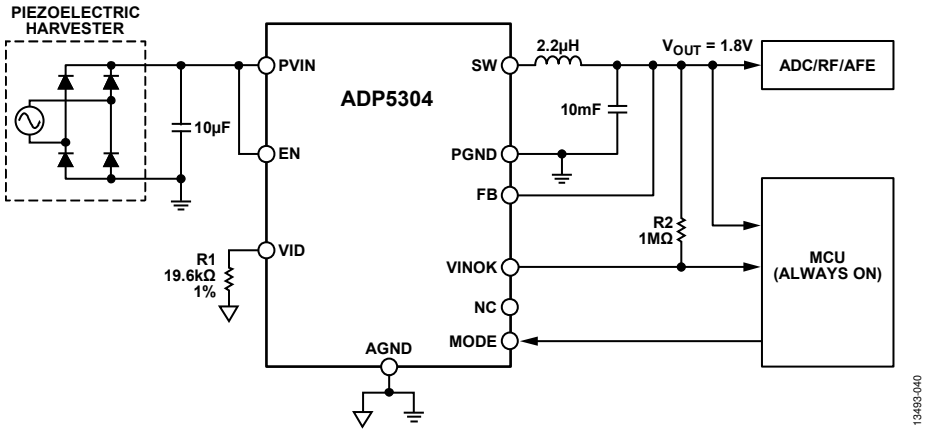

Figure 29. Typical ADP5304 Application with a Piezoelectric Harvester

FACTORY PROGRAMMABLE OPTIONS

To order a device with options other than the default options, contact your local Analog Devices sales or distribution representative.

Table 8. Output Voltage VID Setting Options

Option	Description
Option 0	VID resistor to set the output voltage as follows: 1.2 V, 1.5 V, 1.8 V, 2.0 V, 2.1 V, 2.2 V, 2.3 V, 2.4 V, 2.5 V, 2.6 V, 2.7 V, 2.8 V, 2.9 V, 3.0 V, 3.3 V, 3.6 V, 3.3 V (default)
Option 1	VID resistor to set the output voltage as follows: 0.8 V, 0.9 V, 1.0 V, 1.1 V, 1.3 V, 1.4 V, 1.6 V, 1.7 V, 1.9 V, 3.1 V, 3.4 V, 3.9 V, 4.2 V, 4.5 V, 5.0 V

Table 9. VINOK Monitor Threshed Options

Option	VINOK Monitor Threshold (V)
Option 0	2.05
Option 1	2.10
Option 2	2.15
Option 3	2.20
…	…
Option 20	3.00 (default)
…	…
Option 62	5.10
Option 63	5.15

Table 10. Output Discharge Functionality Options

Option	Description
Option 0	Output discharge function disabled for buck regulator (default)
Option 1	Output discharge function enabled form buck regulator

Table 11. Soft Start Timer Options

Option	Description
Option 0	350 µs (default)
Option 1	2800 µs

OUTLINE DIMENSIONS

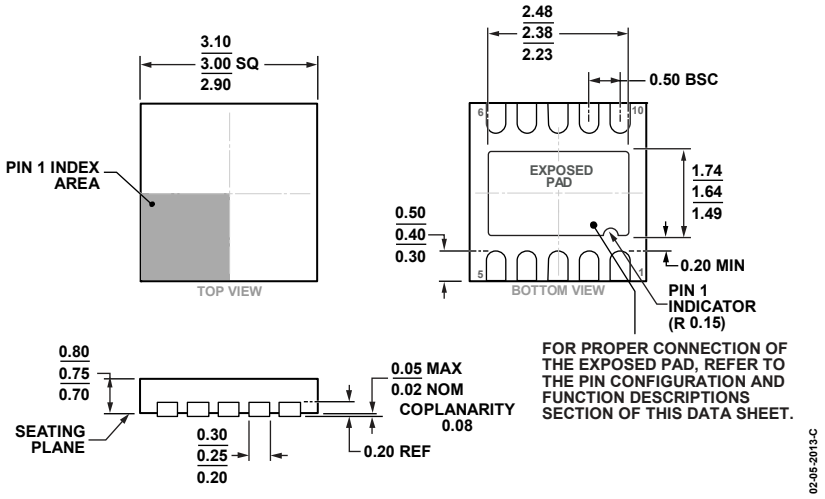

Figure 30. 10-Lead Lead Frame Chip Scale Package [LFCSP_WD]
3 mm × 3 mm Body, Very Very Thin, Dual Lead
(CP-10-9)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
ADP5304ACPZ-1-R7	−40°C to +125°C	10-Lead Lead Frame Chip Scale Package [LFCSP_WD] Without Output Discharge, VINOK Threshold = 3.00 V	CP-10-9
ADP5304ACPZ-2-R7	−40°C to +125°C	10-Lead Lead Frame Chip Scale Package [LFCSP_WD] Without Output Discharge, VINOK Threshold = 4.00 V	CP-10-9
ADP5304-EVALZ		Evaluation Board	

[1] Z = RoHS Compliant Part.