

General Description

- The AON7409 combines advanced trench MOSFET technology with a low resistance package to provide extremely low $R_{DS(ON)}$. This device is ideal for load switch and battery protection applications.

- RoHS and Halogen-Free Compliant.

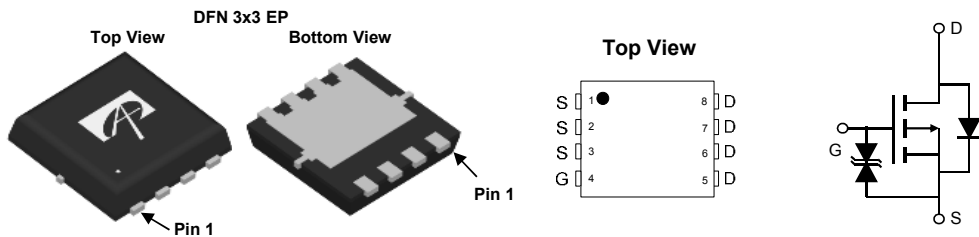
Product Summary

| | |
|-----------------------------------|-----------------|
| V_{DS} | -30V |
| I_D (at $V_{GS}=-10V$) | -32A |
| $R_{DS(ON)}$ (at $V_{GS}=-10V$) | < 8.5m Ω |
| $R_{DS(ON)}$ (at $V_{GS}=-4.5V$) | < 17m Ω |

Typical ESD protection

100% UIS Tested
 100% R_g Tested

HBM Class 2



Absolute Maximum Ratings $T_A=25^\circ\text{C}$ unless otherwise noted

| Parameter | Symbol | Maximum | Units |
|--|----------------|-------------------------|------------------|
| Drain-Source Voltage | V_{DS} | -30 | V |
| Gate-Source Voltage | V_{GS} | ± 25 | V |
| Continuous Drain Current ^G | I_D | $T_C=25^\circ\text{C}$ | -32 |
| | | $T_C=100^\circ\text{C}$ | -25 |
| Pulsed Drain Current ^C | I_{DM} | -128 | A |
| Continuous Drain Current | I_{DSM} | $T_A=25^\circ\text{C}$ | -16 |
| | | $T_A=70^\circ\text{C}$ | -12.5 |
| Avalanche Current ^C | I_{AS} | 40 | A |
| Avalanche energy $L=0.1\text{mH}$ ^C | E_{AS} | 80 | mJ |
| Power Dissipation ^B | P_D | $T_C=25^\circ\text{C}$ | 96 |
| | | $T_C=100^\circ\text{C}$ | 38.5 |
| Power Dissipation ^A | P_{DSM} | $T_A=25^\circ\text{C}$ | 3.1 |
| | | $T_A=70^\circ\text{C}$ | 2 |
| Junction and Storage Temperature Range | T_J, T_{STG} | -55 to 150 | $^\circ\text{C}$ |

Thermal Characteristics

| Parameter | Symbol | Typ | Max | Units |
|--|-----------------|--------------|-----|--------------------|
| Maximum Junction-to-Ambient ^A | $R_{\theta JA}$ | 30 | 40 | $^\circ\text{C/W}$ |
| Maximum Junction-to-Ambient ^{A,D} | | Steady-State | 60 | 75 |
| Maximum Junction-to-Case | $R_{\theta JC}$ | 1 | 1.3 | $^\circ\text{C/W}$ |

Electrical Characteristics (T_J=25°C unless otherwise noted)

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|-----------------------------|--|---|------|------|----------|-------|
| STATIC PARAMETERS | | | | | | |
| BV _{DSS} | Drain-Source Breakdown Voltage | I _D =-250μA, V _{GS} =0V | -30 | | | V |
| I _{DSS} | Zero Gate Voltage Drain Current | V _{DS} =-30V, V _{GS} =0V T _J =55°C | | | -1 -5 | μA |
| I _{GSS} | Gate-Body leakage current | V _{DS} =0V, V _{GS} =±25V | | | ±10 | μA |
| V _{GS(th)} | Gate Threshold Voltage | V _{DS} =V _{GS} , I _D =-250μA | -1.6 | -2.1 | -2.7 | V |
| I _{D(ON)} | On state drain current | V _{GS} =-10V, V _{DS} =-5V | -128 | | | A |
| R _{DS(ON)} | Static Drain-Source On-Resistance | V _{GS} =-10V, I _D =-16A T _J =125°C | | 6.8 | 8.5 | mΩ |
| | | V _{GS} =-4.5V, I _D =-10A | | 9.6 | 11.5 | |
| g _{FS} | Forward Transconductance | V _{DS} =-5V, I _D =-16A | | -43 | | S |
| V _{SD} | Diode Forward Voltage | I _S =-1A, V _{GS} =0V | | -0.7 | -1 | V |
| I _S | Maximum Body-Diode Continuous Current ^G | | | | -32 | A |
| DYNAMIC PARAMETERS | | | | | | |
| C _{iss} | Input Capacitance | V _{GS} =0V, V _{DS} =-15V, f=1MHz | | 2142 | | pF |
| C _{oss} | Output Capacitance | | | 474 | | pF |
| C _{riss} | Reverse Transfer Capacitance | | | 363 | | pF |
| R _g | Gate resistance | V _{GS} =0V, V _{DS} =0V, f=1MHz | | 2.3 | 4.6 | Ω |
| SWITCHING PARAMETERS | | | | | | |
| Q _{g(10V)} | Total Gate Charge | V _{GS} =-10V, V _{DS} =-15V, I _D =-16A | | 41 | 58 | nC |
| Q _{g(4.5V)} | Total Gate Charge | | | 18.5 | 27 | nC |
| Q _{gs} | Gate Source Charge | | | 15 | | nC |
| Q _{gd} | Gate Drain Charge | | | 6 | | nC |
| t _{D(on)} | Turn-On DelayTime | V _{GS} =-10V, V _{DS} =-15V, R _L =0.9Ω, R _{GEN} =3Ω | | 13 | | ns |
| t _r | Turn-On Rise Time | | | 12 | | ns |
| t _{D(off)} | Turn-Off DelayTime | | | 34 | | ns |
| t _f | Turn-Off Fall Time | | | 18.5 | | ns |
| t _{rr} | Body Diode Reverse Recovery Time | I _F =-16A, dI/dt=500A/μs | | 17.5 | | ns |
| Q _{rr} | Body Diode Reverse Recovery Charge | I _F =-16A, dI/dt=500A/μs | | 44.5 | | nC |

A. The value of R_{θJA} is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, in a still air environment with T_A=25° C. The Power dissipation P_{DSM} is based on R_{θJA} t ≤ 10s value and the maximum allowed junction temperature of 150° C. The value in any given application depends on the user's specific board design.

B. The power dissipation P_D is based on T_{J(MAX)}=150° C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.

C. Repetitive rating, pulse width limited by junction temperature T_{J(MAX)}=150° C. Ratings are based on low frequency and duty cycles to keep initial T_J=25° C.

D. The R_{θJA} is the sum of the thermal impedance from junction to case R_{θJC} and case to ambient.

E. The static characteristics in Figures 1 to 6 are obtained using <300μs pulses, duty cycle 0.5% max.

F. These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of T_{J(MAX)}=150° C. The SOA curve provides a single pulse rating.

G. The maximum current rating is package limited.

H. These tests are performed with the device mounted on 1 in² FR-4 board with 2oz. Copper, in a still air environment with T_A=25° C.

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TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

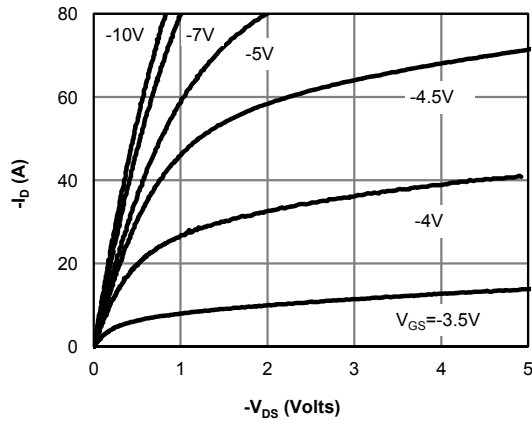


Figure 1: On-Region Characteristics (Note E)

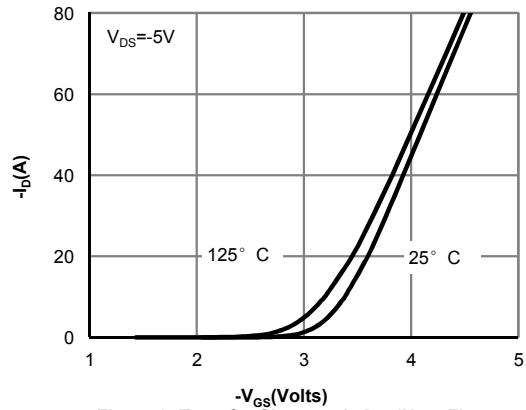


Figure 2: Transfer Characteristics (Note E)

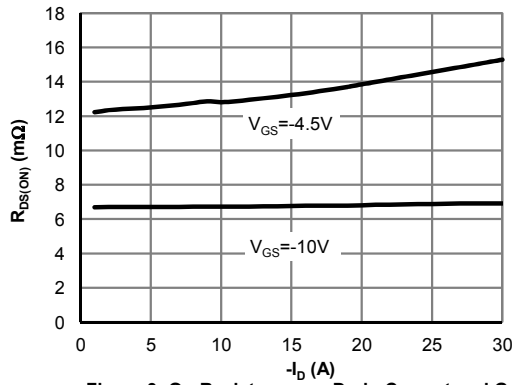


Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)

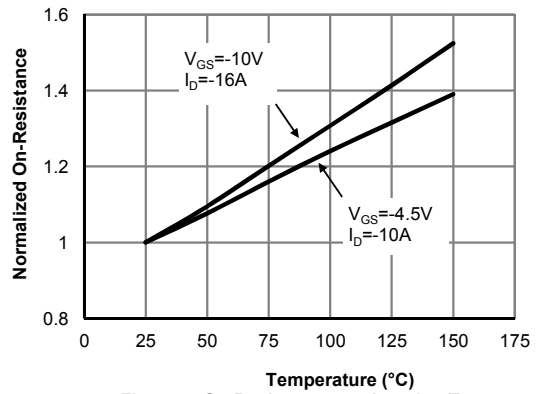


Figure 4: On-Resistance vs. Junction Temperature (Note E)

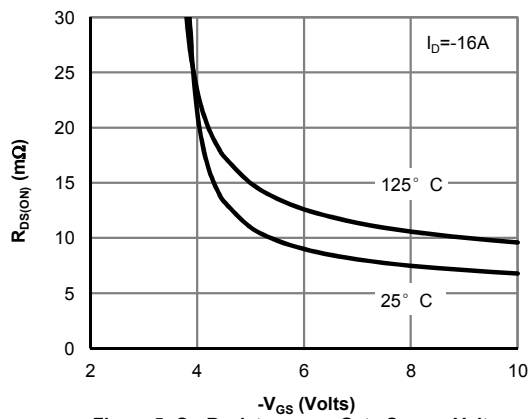


Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)

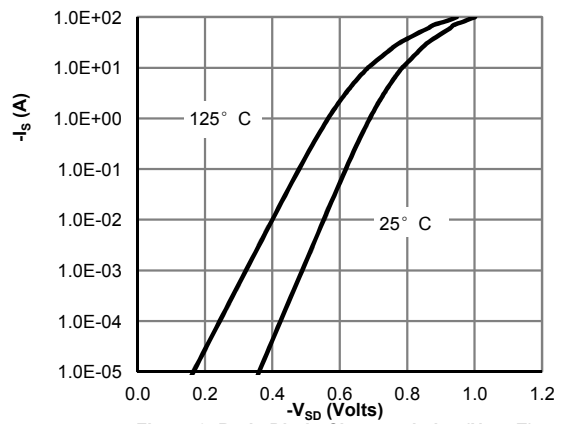


Figure 6: Body-Diode Characteristics (Note E)

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

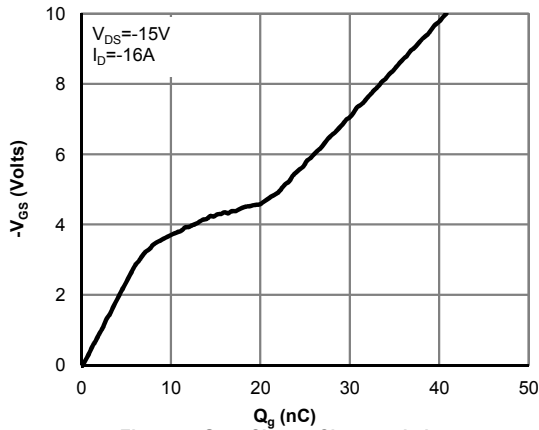


Figure 7: Gate-Charge Characteristics

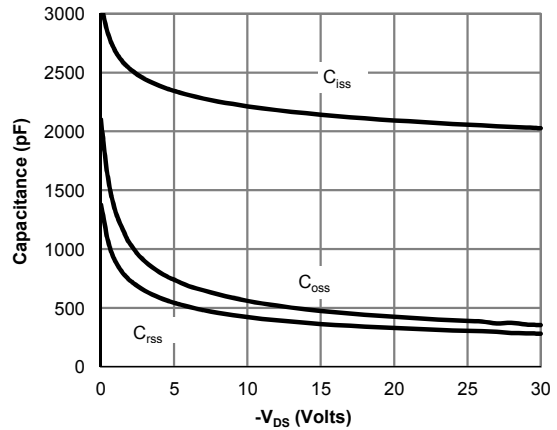


Figure 8: Capacitance Characteristics

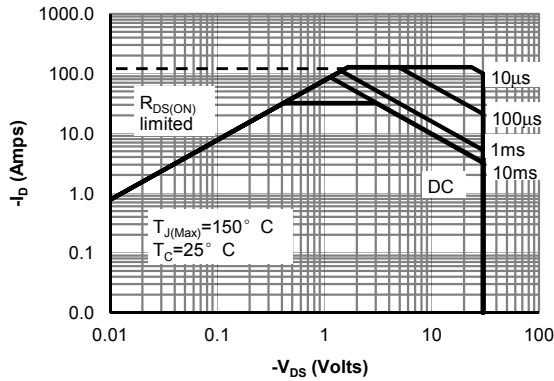


Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

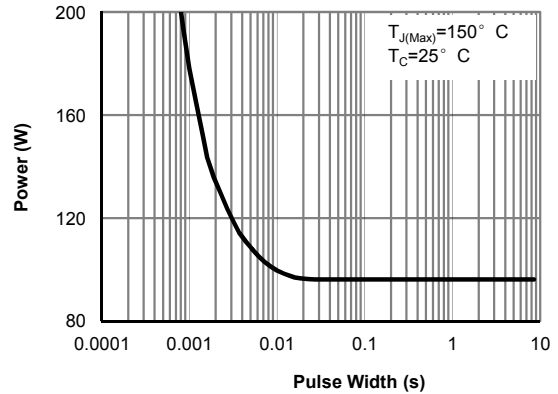


Figure 10: Single Pulse Power Rating Junction-to-Ca (Note F)

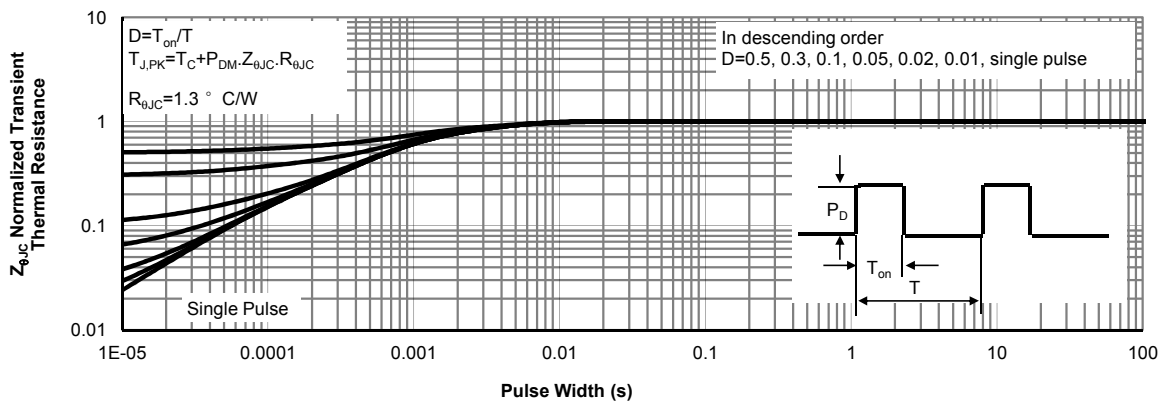


Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

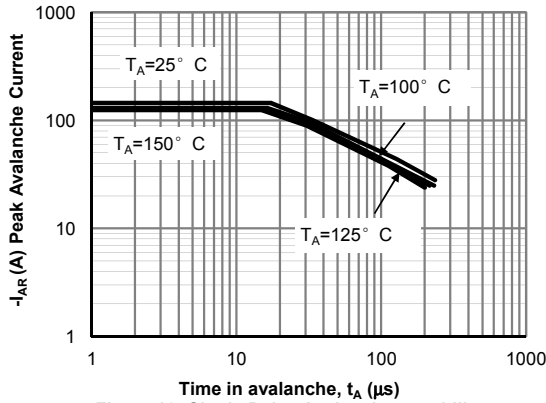


Figure 12: Single Pulse Avalanche capability (Note C)

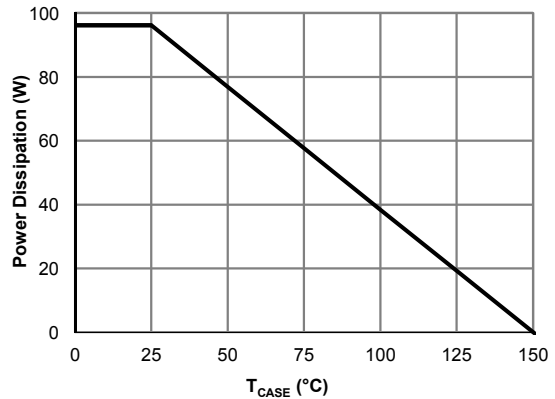


Figure 13: Power De-rating (Note F)

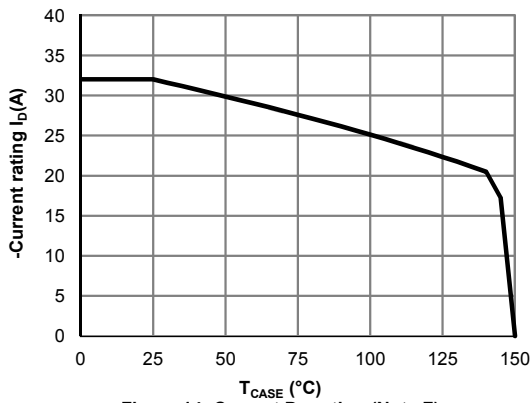


Figure 14: Current De-rating (Note F)

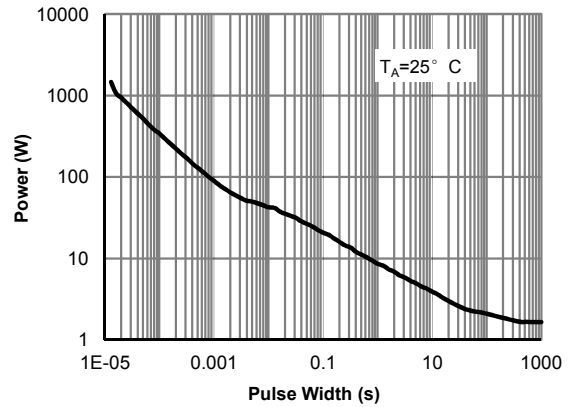


Figure 15: Single Pulse Power Rating Junction-to-Ambient (Note H)

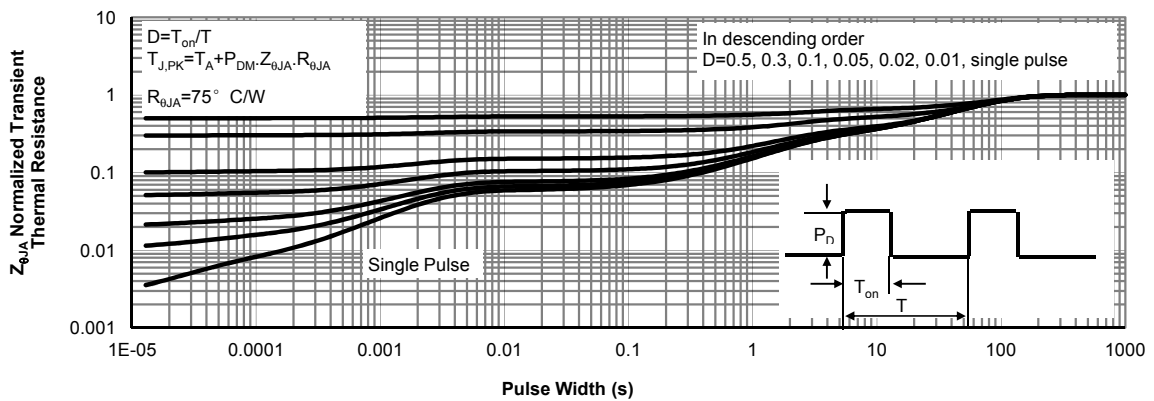
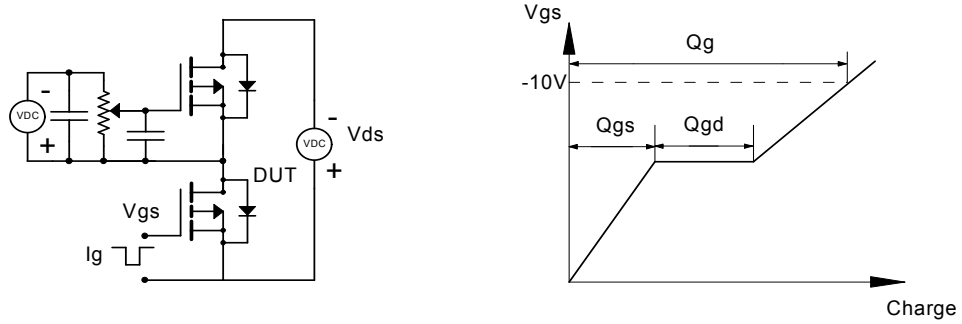
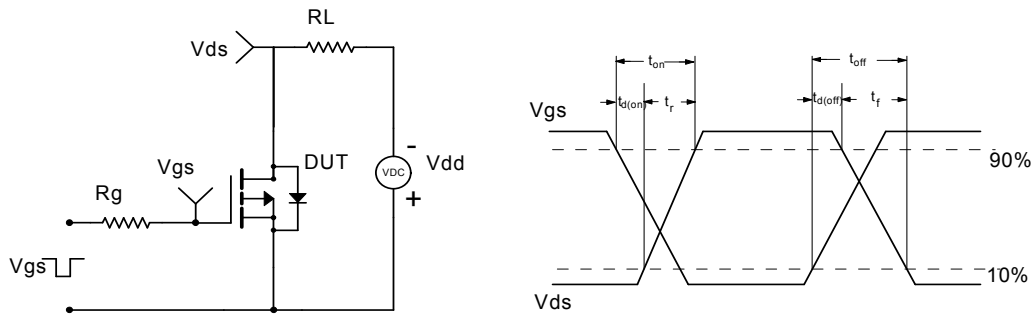


Figure 16: Normalized Maximum Transient Thermal Impedance (Note H)

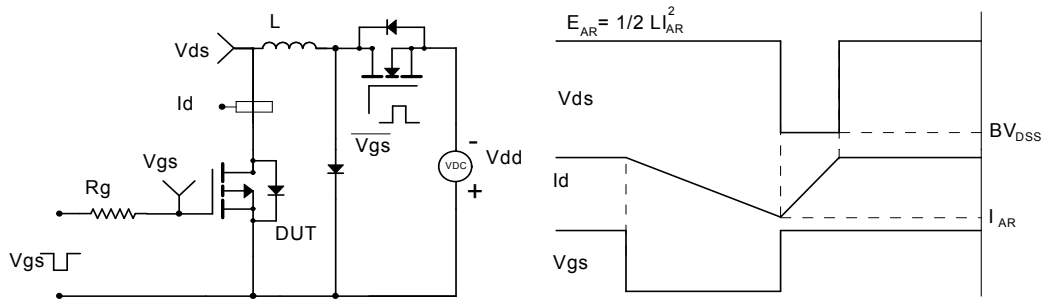
Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms

