HSP48410

Histogrammer/Accumulating Buffer

FN3185
Rev 3.00
July 2004

The Intersil HSP48410 is an 84 lead Histogrammer IC intended for use in image and signal analysis. The on-board memory is configured as 1024 x 24 array. This translates to a pixel resolution of 10 bits and an image size of 4k x 4k with no possibility of overflow.

In addition to Histogramming, the HSP48410 can generate and store the Cumulative Distribution Function for use in Histogram Equalization applications. Other capabilities of the HSP48410 include: Bin Accumulation, Look Up Table, 24-bit Delay Memory, and Delay and Subtract mode.

A Flash Clear pin is available in all modes of operation and performs a single cycle reset on all locations of the internal memory array and all internal data paths.

The HSP48410 includes a fully asynchronous interface which provides a means for communications with a host, such as a microprocessor. The interface includes dedicated Read/Write pins and an address port which are asynchronous to the system clock. This allows random access of the Histogram Memory Array for analysis or conditioning of the stored data.

Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. DWG. #
HSP48410JC-33	0 to 70	84 Ld PLCC	N84.1.15

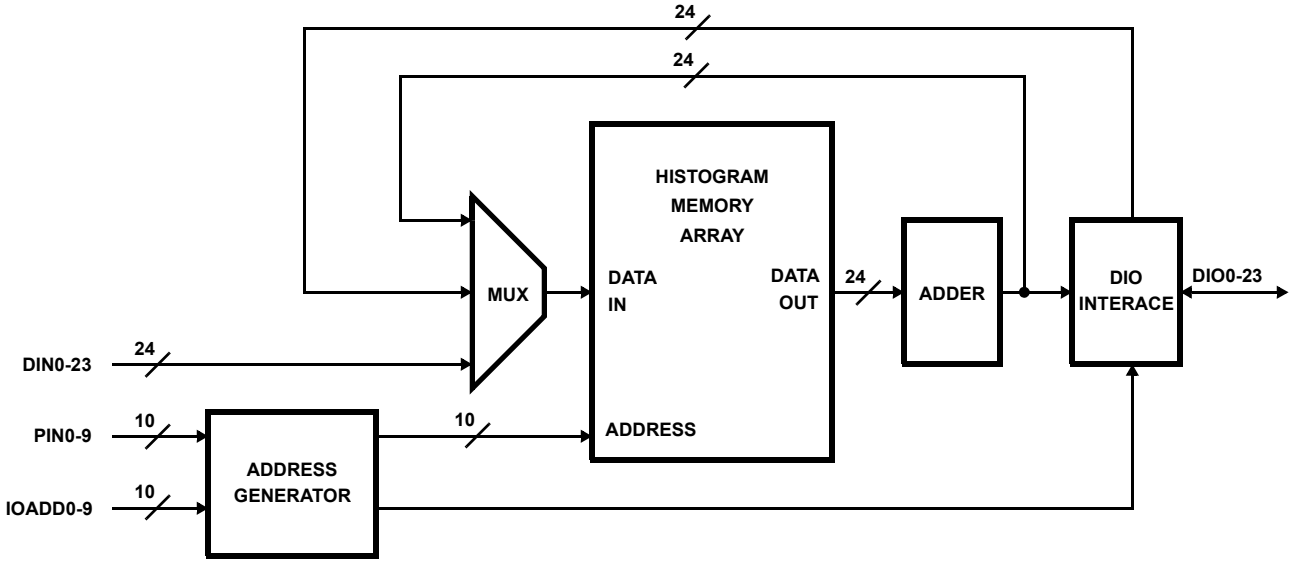
Features

- 10-Bit Pixel Data
- 4k x 4k Frame Sizes
- Asynchronous Flash Clear Pin
- Single Cycle Memory Clear
- Fully Asynchronous 16 or 24-Bit Host Interface
- Generates and Stores Cumulative Distribution Function
- Look Up Table Mode
- 1024 x 24-Bit Delay Memory
- 24-Bit Three State I/O Bus
- DC to 40MHz Clock Rate

Applications

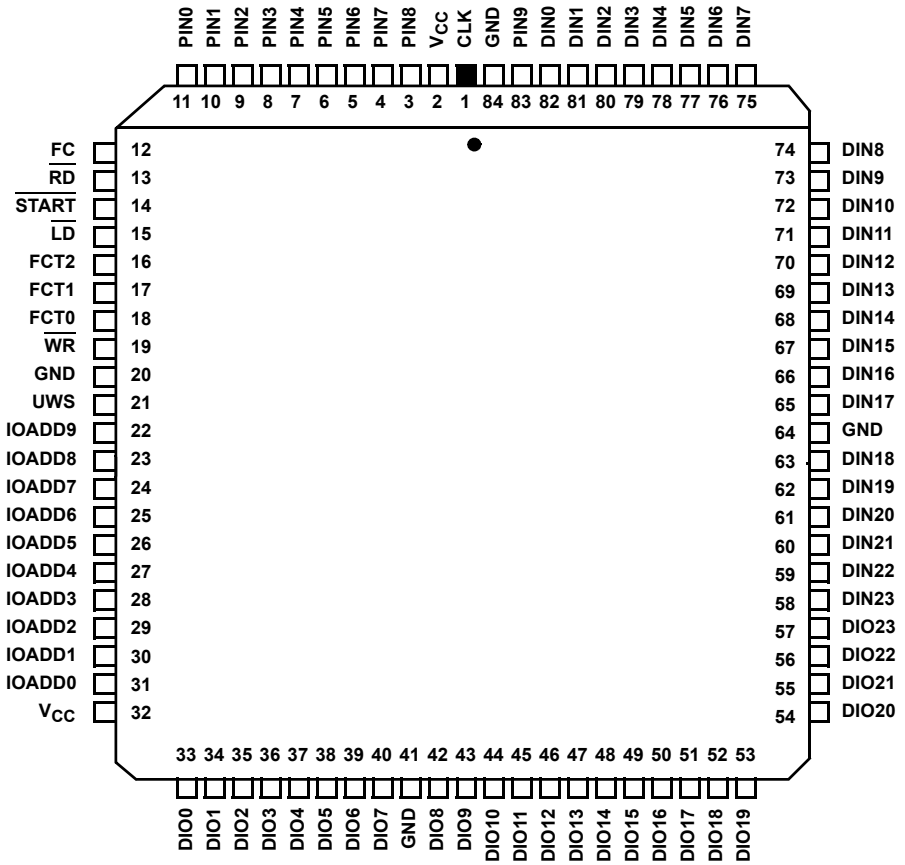
- Histogramming
- Histogram Equalization
- Image and Signal Analysis
- Image Enhancement
- RGB Video Delay Line

Block Diagram



Pinouts

84 LEAD PLCC



Pin Description

NAME	PLCC PIN	TYPE	DESCRIPTION
CLK	1	I	Clock Input. This input has no effect on the chips functionality when the chip is programmed to an asynchronous mode. All signals denoted as synchronous have their timing specified with reference to this signal.
PIN0-9	3-11, 83	I	Pixel Input. This input bus is sampled by the rising edge of clock. It provides the on-chip RAM with address values in Histogram, Bin Accumulate and LUT(write) mode. During Asynchronous modes it is unused.
$\overline{LD}$	15	I	The Load pin is used to load the FCT0-2 bits into the FCT Registers. (See below).
FCT0-2	16-18	I	These three pins are decoded to determine the mode of operation for the chip. The signals are sampled by the rising edge of $\overline{LD}$ and take effect after the rising edge of $\overline{LD}$. Since the loading of this function is asynchronous to CLK, it is necessary to disable the $\overline{START}$ pin during loading and enable $\overline{START}$ at least 1 CLK cycle following the $\overline{LD}$ pulse.
$\overline{START}$	14	I	This pin informs the on-chip circuitry which clock cycle will start and/or stop the current mode of operation. Thus, the modes are asynchronously selected (via $\overline{LD}$) but are synchronously started and stopped. This input is sampled by the rising edge of CLK. The actual function of this input depends on the mode that is selected. $\overline{START}$ must always be held high (disabled) when changing modes. This will provide a smooth transition from one mode to the next by allowing the part to reconfigure itself before a new mode begins. When $\overline{START}$ is high, LUT(read) mode is enabled except for Delay and Delay and Subtract modes.
$\overline{FC}$	12	I	Flash Clear. This input provides a fully asynchronous signal which effectively resets all bits in the RAM Array and the input and output data paths to zero.

Pin Description

NAME	PLCC PIN	TYPE	DESCRIPTION
DIN0-23	58-63, 65-82	I	Data Input Bus. Provides data to the Histogrammer during Bin Accumulate, LUT, Delay and Delay and Subtract modes. Synchronous to CLK.
DIO0-23	33-40, 42-57	I/O	Asynchronous Data Bus. Provides RAM access for a microprocessor in preconditioning the memory array and reading the results of the previous operation. Configurable as either a 24 or 16-bit bus.
IOADD0-9	22-31	I	RAM address in asynchronous modes. Sampled on the falling edge of $\overline{WR}$ or $\overline{RD}$.
UWS	21	I	Upper Word Select. In 16-bit Asynchronous mode, a one on this pin denotes the contents of DIO0-7 as being the upper eight bits of the data in or out of the Histogrammer. A zero means that DIO0-15 are the lower 16 bits. In all other modes, this pin has no effect.
$\overline{WR}$	19	I	Write enable to the RAM for the data on DIO0-23 when the HSP48410 is configured in one of the asynchronous modes. Asynchronous to CLK.
$\overline{RD}$	13	I	Read control for the data on DIO0-23 in asynchronous modes. Output enable for DIO0-23 in other modes. Asynchronous to CLK.
V_{CC}	2, 32		+5V. 0.1µF capacitors between the V_{CC} and GND pins are recommended.
GND	20, 41, 64, 84		Ground

NOTES:

1. An overbar denotes an active low signal.
2. Bit 0 is the LSB on all buses.

Functional Description

The Histogrammer is intended for use in signal and image processing applications. The on-board RAM is 24 bits by 1024 locations. For histogramming, this translates to an image size of 4k x 4k with 10-bit data. A Functional Block Diagram of the part is shown in Figure 1.

In addition to histogramming, the HSP48410 will also perform Histogram Accumulation while feeding the results back into the memory array. The on-board RAM will then contain the Cumulative Distribution Function and can be used for further operation such as histogram equalization.

Other modes are: Bin Accumulate, Look Up Table (LUT), Delay Memory, and Delay and Subtract. The part can also be accessed as a 24-bit by 1024 word asynchronous RAM for preconditioning or reading the results of the histogram.

The Histogrammer can be accessed both synchronously and asynchronously to the system clock (CLK). It was designed to be configured asynchronously by a microprocessor, then switched to a synchronous mode to process data. The result of the processing can then be read out synchronously, or the part can be switched to one of the asynchronous modes so the data may be read out by a microprocessor. All modes are synchronous except for the Asynchronous 16 and 24 modes.

A Flash Clear operation allows the user to reset the entire RAM array and all input and output data paths in a single cycle.

Histogram Memory Array

The Histogram Memory Array is a 24-bit by 1024 deep RAM. Depending on the current mode, its input data comes from either the synchronous input DIN0-23, from the asynchronous data bus DIO0-23, or from the output of the adder. The output data goes to the DIO bus in both synchronous and asynchronous modes.

Address Generator

This section of the circuit determines the source of the RAM address. In the synchronous modes, the address is taken from either the output of the counter or PIN0-9. The pixel input bus is used for Histogram, Bin Accumulate, and LUT(read) modes. All other synchronous modes, i.e. Histogram Accumulate, LUT(write), Delay, and Delay and Subtract use the counter output. The counter is reset on the first rising edge of CLK after a falling edge on $\overline{START}$.

During asynchronous modes, the read and write addresses to the RAM are taken from the IOADD bus on the falling edge of the $\overline{RD}$ and $\overline{WR}$ signals, respectively.

Adder Input

The Adder Input Control Section contains muxes, registers and other logic that provide the proper data to the adder. The configuration of this section is controlled by the output of the Function Decode Section.

DIO Interface

The DIO Interface Section transfers data between the Histogrammer and the outside world. In the synchronous modes, DIO acts as a synchronous output for the data currently being processed by the chip; $\overline{RD}$ acts as the output enable for the DIO bus; $\overline{WR}$ and IOADD0-9 have no effect. When either of the Asynchronous modes are selected (16 or 24-bit), the RAM output is passed directly to the DIO bus on read cycles, and on write cycles, data input on DIO goes to the RAM input port. In this case, data reads and writes are controlled by $\overline{RD}$, $\overline{WR}$ and IOADD0-9.

Function Decode

This section provides the signals needed to configure the part for the different modes. The eight modes are decoded from FCT0-2 on the rising edge of $\overline{LD}$ (see Table 1). The output of this section is a set of signals which control the path of data through the part.

The mode should only be changed while $\overline{START}$ is high. After changing from one mode to another, $\overline{START}$ must be clocked high by the rising edge of CLK at least once.

TABLE 1. FUNCTION DECODE

FCT			MODE
2	1	0	
0	0	0	Histogram
0	0	1	Histogram Accumulate
0	1	0	Delay and Subtract
0	1	1	Look Up Table
1	0	0	Bin Accumulate
1	0	1	Delay Memory
1	1	0	Asynchronous 24
1	1	1	Asynchronous 16

Flash Clear

Flash Clear allows the user to clear the entire RAM with a single pin. When the $\overline{FC}$ pin is low, all bits of the RAM and the data path from the RAM to DIO0-23 are set to zero. The $\overline{FC}$ pin is asynchronous with respect to CLK: the reset begins immediately following a low on this signal. For synchronous modes, in order to ensure consistent results, $\overline{FC}$ should only be active while $\overline{START}$ is high. For asynchronous modes, $\overline{WR}$ must remain inactive while $\overline{FC}$ is low.

Functional Block Diagram

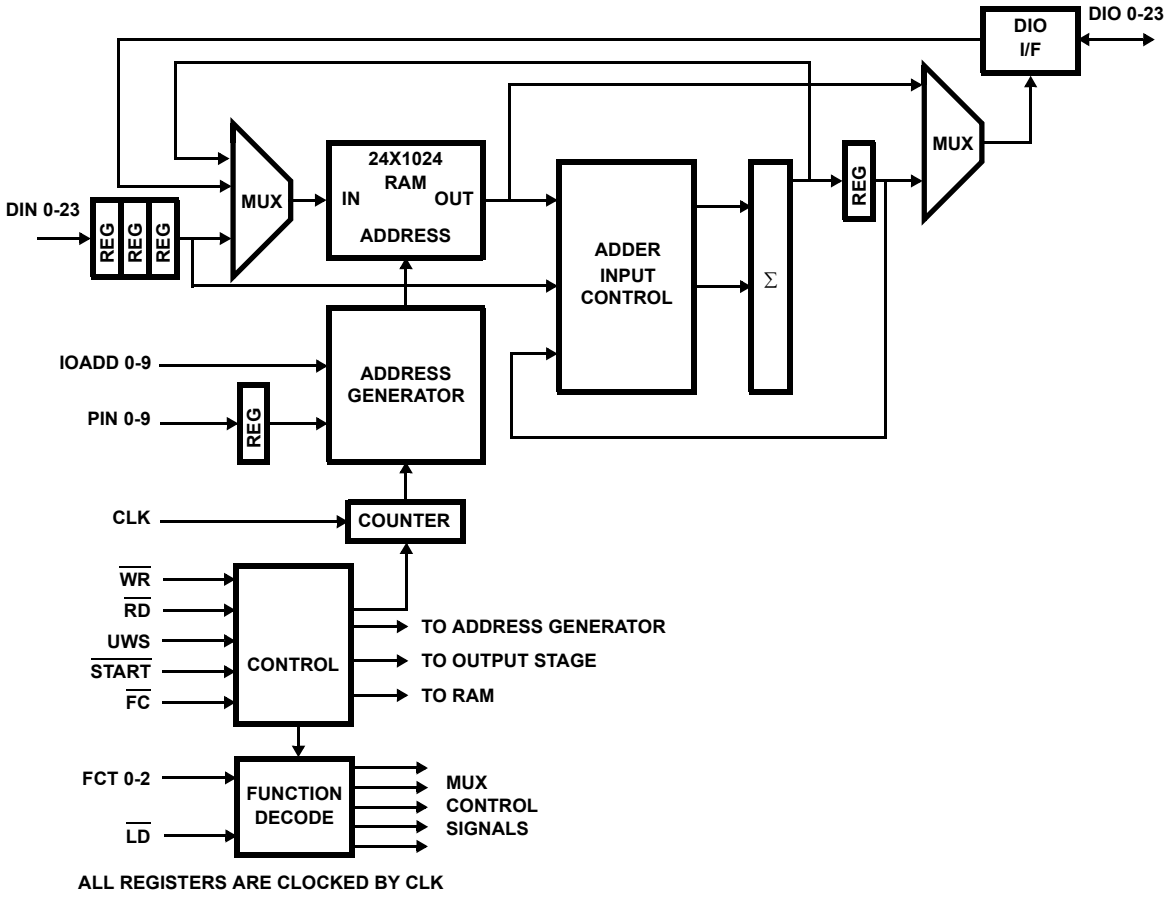


FIGURE 1. FUNCTIONAL BLOCK DIAGRAM

Histogram Mode

This is the fundamental operation for which this chip was intended. When this mode is selected, the chip configures itself as shown in the Block Diagram of Figure 2. The pixel data is sampled on the rising edge of clock and used as the read address to the RAM array. The data contained in that address (or bin) is then incremented by 1 and written back into the RAM at the same address.

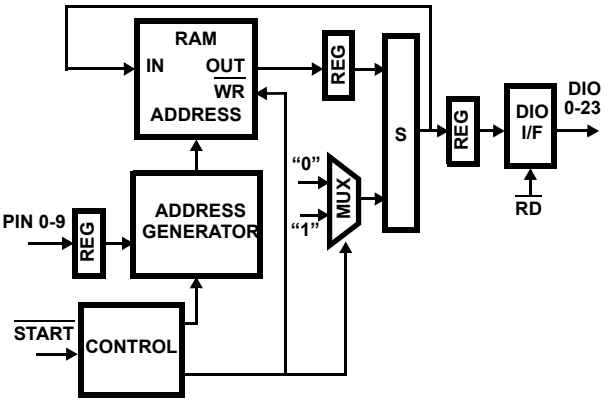


FIGURE 2. HISTOGRAM MODE BLOCK DIAGRAM

At the same time, the new value is also displayed on the DIO bus. This procedure continues until the circuit is interrupted by $\overline{START}$ returning high. When $\overline{START}$ is high, the RAM write is disabled, the read address is taken from the Pixel Input bus, and the chip acts as if it is in LUT(read) mode. Figure 3 shows histogram mode timing. $\overline{START}$ is used to disregard the data on PIN0-9 at DATA2. $\overline{START}$ is sampled on the rising edge of clock, but is delayed internally by 3 cycles to match the latency of the Address Generator. Data is clocked onto the DIO bus on the rising edge of CLK. $\overline{RD}$ acts as output enable.

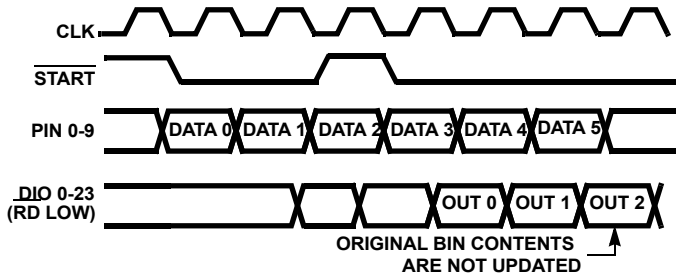


FIGURE 3. HISTOGRAM MODE TIMING

Histogram Accumulate Mode

This function is very similar to the Histogram function. In this case, a counter is used to provide the address data to the RAM. The RAM is sequentially accessed, and the data from each bin is added to the data from the previous bins. This accumulation of data continues until the function is halted. The results of the accumulation are displayed on the DIO bus while simultaneously being written back to the RAM. When the operation is complete, the RAM will contain the Cumulative Distribution Function (CDF) of the image.

Figure 4 shows the configuration for this mode. Once this function is selected, the $\overline{START}$ pin is used to reset the counter and enable writing to the RAM. Write enable is delayed 3 cycles to match the delay in the Address Generator. The $\overline{START}$ pin determines when the accumulation will begin. Before this pin is activated, the counter will be in an unknown state and the DIO bus will contain unpredictable data. Once the $\overline{START}$ pin is sampled low, the data registers are reset in order to clear the accumulation. The output (DIO bus) will then be zero until a nonzero data value is read from the RAM. Timing for this operation is shown in Figure 5.

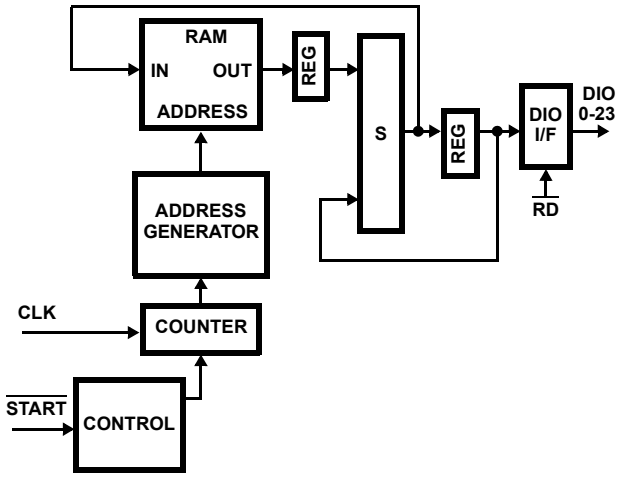


FIGURE 4. HISTOGRAM ACCUMULATE MODE BLOCK DIAGRAM

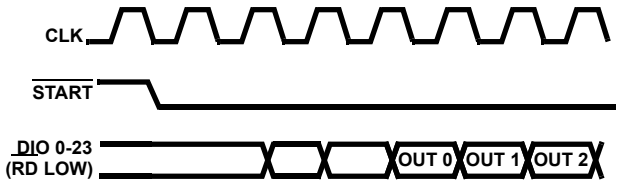


FIGURE 5. HISTOGRAM ACCUMULATE MODE TIMING

The $\overline{START}$ pin must remain low in order to allow the accumulated data to overwrite the original histogram data contained in the RAM. When the $\overline{START}$ pin returns to a high state, the configuration remains intact, but writing to the RAM is disabled and the part is in LUT(read) mode. Note that the counter is not reset at this point. The counter will be reset on the first cycle of CLK that $\overline{START}$ is detected low. To prevent invalid data from being written to the RAM, when the counter reaches its maximum value (1023), further writing to the RAM is disabled and the counter remains at this value until the mode is changed.

At the end of the histogram accumulation, the DIO output bus will contain the last accumulated value. The chip will remain in this state until $\overline{\text{START}}$ becomes inactive. The results of the accumulation can then be read out synchronously by keeping $\overline{\text{START}}$ high, or asynchronously in either of the asynchronous modes.

Bin Accumulate Mode

The functionality of this mode is also similar to the Histogram function. The only difference is that instead of incrementing the bin data by 1, the bin data is added to the incoming DIN bus data. The DIN bus is delayed internally by 3 cycles to match the latency in the address generator. Figure 6 shows the block diagram of the internal configuration for this mode, while the timing is given in Figure 7. Note that in this figure, $\overline{\text{START}}$ is used to disregard the data on DIN0-23 during DATA2.

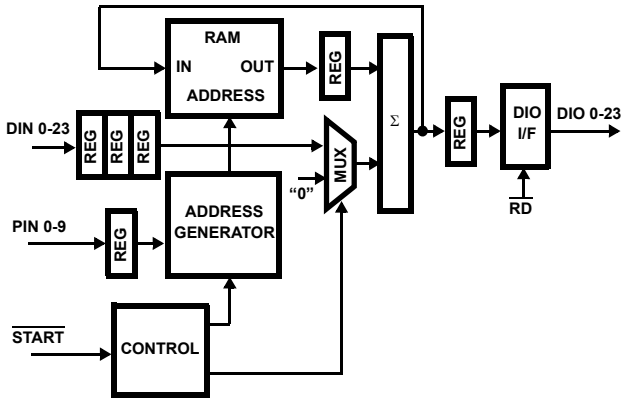


FIGURE 6. BIN ACCUMULATE BLOCK DIAGRAM

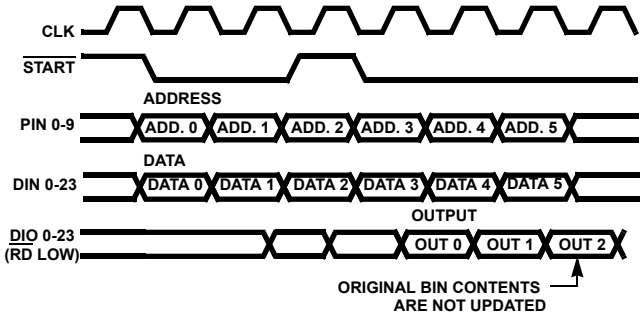


FIGURE 7. BIN ACCUMULATE TIMING

Look Up Table Mode

A Look Up Table (LUT) is used to perform a fixed transformation function on pixel values. This is particularly useful when the transformation is nonlinear and cannot be realized directly with hardware. An example is the remapping of the original pixel values to a new set of values based on the CDF obtained through Histogram Accumulation.

The transformation function can be loaded into the LUT in one of three ways: in LUT mode, through DIN0-23; in either asynchronous mode, over the DIO bus as described below under Asynchronous 16/24 Modes; in the Histogram Accumulate mode the transformation function is calculated internally (see description above). The transformation function can then be utilized by deactivating $\overline{\text{START}}$, putting the part in LUT mode and clocking the data to be transformed onto the PIN bus. Note that it is necessary to wait one clock cycle after changing the mode before clocking data into the part.

The Block Diagram and Timing Diagram for this mode are shown in Figures 8 and 9. The left half of the timing diagram shows LUT(write) mode. On the first CLK that detects $\overline{\text{START}}$ low, the counter is reset and the write enable is activated for the RAM. As long as $\overline{\text{START}}$ remains low, the counter provides the write address to the RAM and data is sequentially loaded through the DIN bus. The DIN bus is delayed internally by 3 cycles to match the latency in the Address Generator. The DIO bus will contain the previous contents of the memory location being updated. When 1024 words have been written to the RAM, the counter stops and further writes to the RAM are disabled. The part stays in this state while $\overline{\text{START}}$ remains low.

When $\overline{\text{START}}$ returns high, the RAM write is disabled, the read address is taken from the PIN bus, and the chip acts as a synchronous LUT. (This is known as LUT(read) mode.) In order to ensure that the internal pipelines are clear, data should not be input to PIN0-9 until the third clock after $\overline{\text{START}}$ goes high.

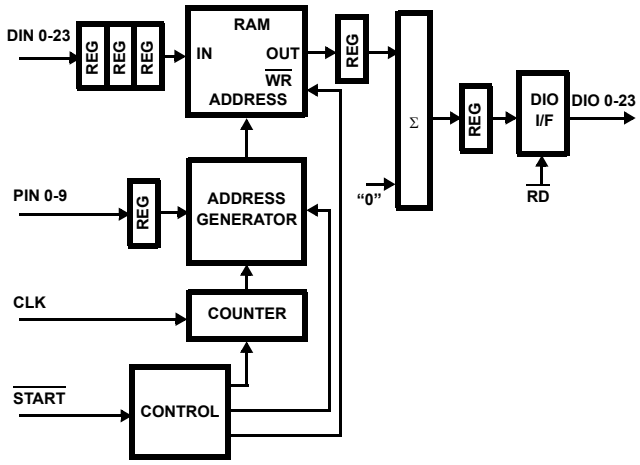


FIGURE 8. LOOK UP TABLE BLOCK DIAGRAM

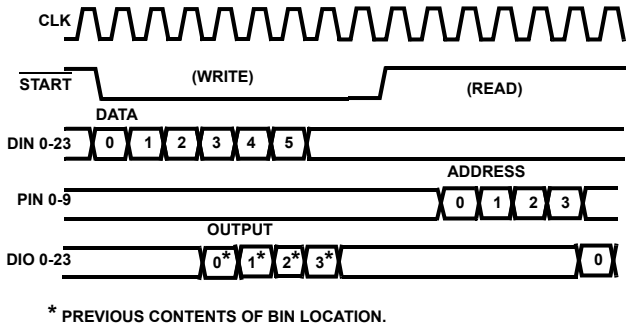


FIGURE 9. LOOK UP TABLE MODE TIMING

Delay Memory (Row Buffer) Mode

As seen by comparing Figures 8 and 10, the configuration for this mode is nearly identical to the LUT mode. In this mode, however, the counter is always providing the address and the write function is always enabled.

In order to force this configuration to act as a row delay register, the $\overline{\text{START}}$ signal must be used to reset the internal counter each time a new row of pixels is being sampled. Because of the inherent latency in the address and data paths, the counter must be reset every N-4 cycles, where N is the desired delay length. For example, if a delay from DIN to DIO of ten cycles is desired, the $\overline{\text{START}}$ signal must be set low every six cycles (see Figure 11). If the internal address counter reaches its maximum count (1023), it holds that value and further writes to the RAM are disabled.

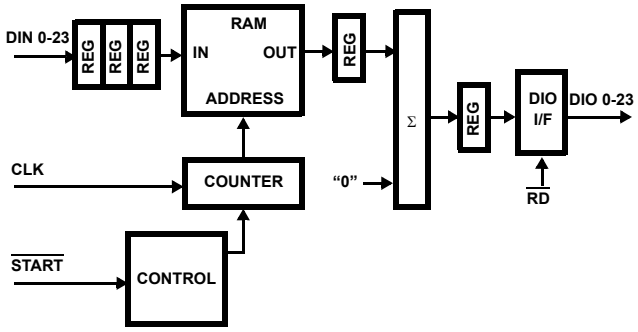


FIGURE 10. DELAY MEMORY BLOCK DIAGRAM

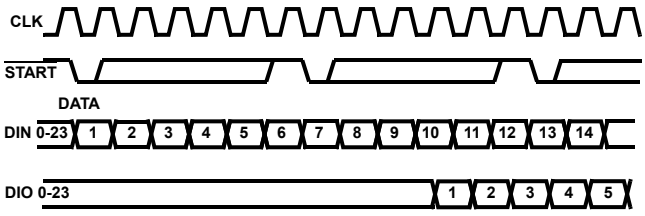


FIGURE 11. DELAY MEMORY MODE TIMING FOR ROW LENGTH OF TEN

Delay and Subtract Mode

This mode is similar to the Delay Memory mode, except the input data is subtracted from the corresponding data stored in RAM (See Figures 12 and 13).

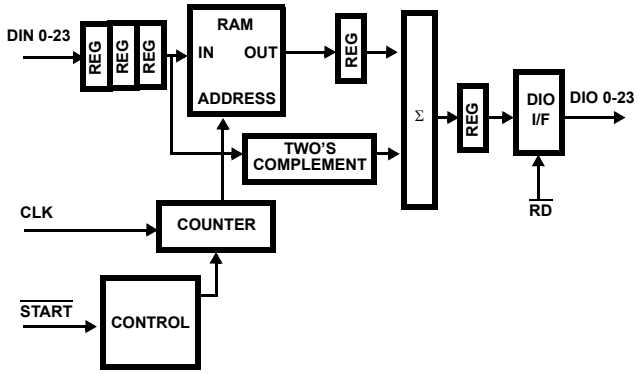


FIGURE 12. DELAY AND SUBTRACT BLOCK DIAGRAM

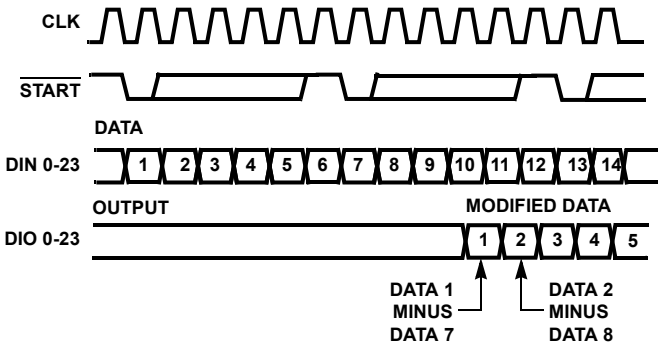


FIGURE 13. DELAY AND SUBTRACT MODE TIMING FOR ROW LENGTH OF TEN

Asynchronous 16/24 Modes

In the Asynchronous modes, the chip acts like a single port RAM. In this mode, the user can read (access) any bin location on the fly by simply setting the 10-bit IO address to the desired bin location. The RAM is then read or written on the following $\overline{\text{RD}}$ or $\overline{\text{WR}}$ pulse. A block diagram for this mode is shown in Figure 14. Note that all registers and pipeline stages are bypassed; $\overline{\text{START}}$ and CLK have no effect in this mode.

Timing waveforms for this mode are also shown in Figure 15. During reading, the read address is latched (internally) on the falling edge of $\overline{\text{RD}}$. During write operations, the address is latched on the falling edge of $\overline{\text{WR}}$ and data is latched on the rising edge of $\overline{\text{WR}}$. Note that reading and writing occur on different ports, so that, in this mode, the write port always latches its address and data values from the $\overline{\text{WR}}$ signal, while the read port always uses $\overline{\text{RD}}$ for latching.

The difference between the Async 16 mode and the Async 24 mode is the number of data bits available to the user. In 16-bit mode, the user can connect the system data bus to the lower 16 bits of the Histogrammer's DIO bus. The UWS pin becomes the LSB of the IO address, which determines if the lower 16 bits or upper 8 bits of the 24-bit Histogrammer data is being used. When UWS is low, the data present at DIO0-15 is the lower 16 bits of the data in the IOADD0-9 location. When UWS is high, the upper 8 bits of the IOADD09 location are present on DIO0-7. (This is true for both reading and writing). Thus, it takes 2 cycles for an asynchronous 24-bit operation when in Async 16 mode. Unused outputs are zeros.

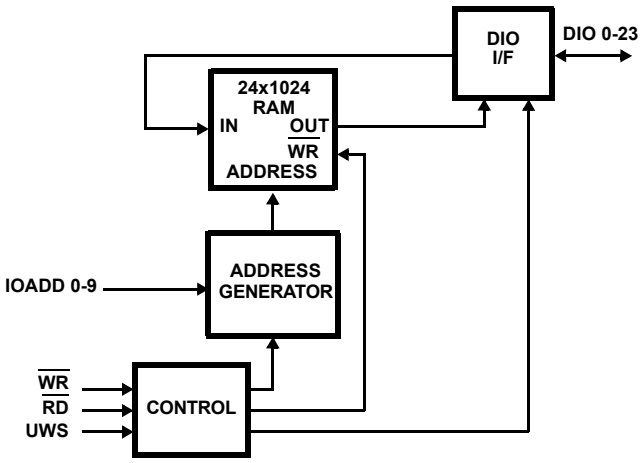


FIGURE 14. ASYNCHRONOUS 16/24 BLOCK DIAGRAM

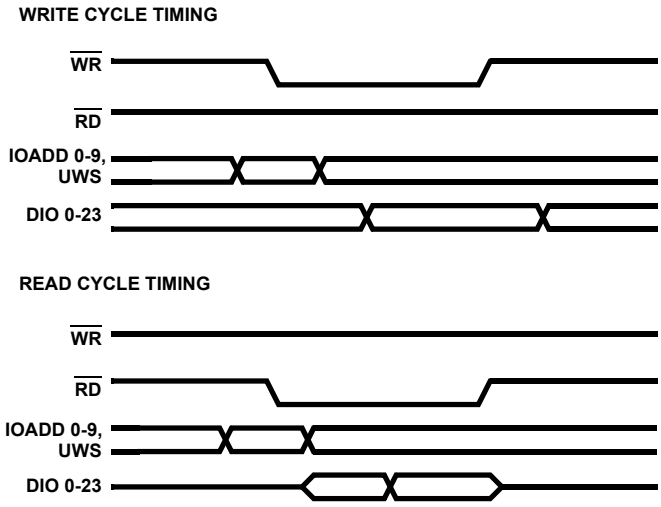


FIGURE 15. ASYNCHRONOUS 16/24 MODE TIMING

Absolute Maximum Ratings

Supply Voltage . . . . . +6.0V
Input, Output Voltage . . . . . GND-0.5V to V_{CC}+0.5V
ESD Classification . . . . . Class 1

Operating Conditions

Voltage Range . . . . . +5V ±5%
Temperature Range . . . . . 0°C to 70°C

Thermal Information

Thermal Resistance (Typical, Note 3)	θ_{JA} (°C/W)
PLCC Package	34

Maximum Storage Temperature Range . . . . . -65°C to 150°C
Maximum Junction Temperature . . . . . 150°C
Maximum Lead Temperature (Soldering 10s) . . . . . 300°C
(PLCC - Lead Tips Only)

Die Characteristics

Gate Count . . . . . 3500 Gates

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

3. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

DC Electrical Specifications

PARAMETER	SYMBOL	MIN	MAX	UNITS	TEST CONDITIONS
Logical One Input Voltage	V_{IH}	2.0	-	V	V_{CC} = 5.25V
Logical Zero Input Voltage	V_{IL}	-	0.8	V	V_{CC} = 4.75V
High Level Clock Input	V_{IHC}	3.0	-	V	V_{CC} = 5.25V
Low Level Clock Input	V_{ILC}	-	0.8	V	V_{CC} = 4.75V
Output High Voltage	V_{OH}	2.6	-	V	I_{OH} = -400µA, V_{CC} = 4.75V
Output Low Voltage	V_{OL}	-	0.4	V	I_{OL} = +2.0mA, V_{CC} = 4.75V
Input Leakage Current	I_L	-10	10	µA	V_{IN} = V_{CC} or GND, V_{CC} = 5.25V
I/O Leakage Current	I_O	-10	10	µA	V_{OUT} = V_{CC} or GND, V_{CC} = 5.25V
Standby Supply Current	I_{CCSB}	D-	500	µA	V_{IN} = V_{CC} or GND, V_{CC} = 5.25V, Outputs Open
Operating Power Supply Current	I_{CCOP}	-	396	mA	f = 33 MHz, V_{IN} = V_{CC} or GND V_{CC} = 5.25V (Notes 4, 5)

NOTES:

4. Power supply current is proportional to operating frequency. Typical rating for I_{CCOP} is 12mA/MHz.
5. Maximum junction temperature must be considered when operating part at high clock frequencies.

Capacitance

T_A = 25°C, Not tested, but characterized at initial design and at major process or design changes.

PARAMETER	SYMBOL	MIN	MAX	UNITS	TEST CONDITIONS
Input Capacitance	C_{IN}	-	12	pF	FREQ = 1 MHz, V_{CC} = Open, all measurements are referenced to device ground.
Output Capacitance	C_{OUT}	-	12	pF	

AC Electrical Specifications

V_{CC} = 5V ± 5%, T_A = 0°C to 70°C (Note 6)

PARAMETER	SYMBOL	NOTES	-40 (40 MHz)		-33 (33 MHz)		UNITS
			MIN	MAX	MIN	MAX	
Clock Period	t_{CP}		25	-	30	-	ns
Clock Low	t_{CH}		10	-	12	-	ns
Clock High	t_{CL}		10	-	12	-	ns
DIN Setup	t_{DS}		12	-	13	-	ns
DIN0-23 Hold	t_{DH}		0	-	0	-	ns
Clock to DIO0-23 Valid	t_{DO}		-	15	-	19	ns
$\overline{FC}$ Pulse Width	t_{FL}		35	-	35	-	ns
FCT0-2 Setup to $\overline{LD}$	t_{FS}		10	-	10	-	ns

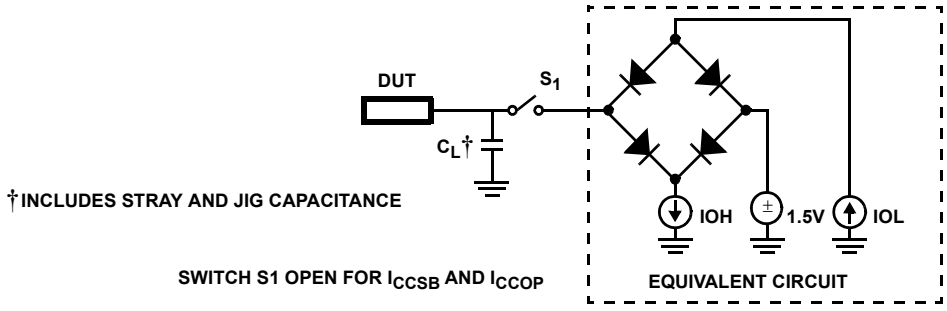
AC Electrical Specifications V_{CC} = 5V ± 5%, T_A = 0°C to 70°C (Note 6) **(Continued)**

PARAMETER	SYMBOL	NOTES	-40 (40 MHz)		-33 (33 MHz)		UNITS
			MIN	MAX	MIN	MAX	
FCT0-2 Hold from $\overline{LD}$	t_{FH}		0	-	0	-	ns
$\overline{START}$ Setup to CLK	t_{SS}		12	-	13	-	ns
$\overline{START}$ Hold from CLK	t_{SH}		0	-	0	-	ns
PIN0-9 Setup Time	t_{PS}		12	-	13	-	ns
PIN0-9 Hold Time	t_{PH}		0	-	0	-	ns
$\overline{LD}$ Pulse Width	t_{LL}		10	-	12	-	ns
$\overline{LD}$ Setup to $\overline{START}$	t_{LS}	Note 7	T_{CP}		T_{CP}	-	ns
$\overline{WR}$ Low	t_{WL}		12	-	15	-	ns
$\overline{WR}$ High	t_{WH}		12	-	15	-	ns
Address Setup	t_{AS}		13	-	15	-	ns
Address Hold	t_{AH}		1	-	1	-	ns
DIO Setup to $\overline{WR}$	t_{WS}		12	-	15	-	ns
DIO Hold from $\overline{WR}$	t_{WH}		1	-	1	-	ns
$\overline{RD}$ Low	t_{RL}		35	-	43	-	ns
$\overline{RD}$ High	t_{RH}		15	-	17	-	ns
$\overline{RD}$ Low to DIO Valid	t_{RD}		-	35	-	43	ns
Read/Write Cycle Time	t_{CY}		55	-	65	-	ns
DIO Valid after $\overline{RD}$ High	t_{OH}	Note 8	-	0	-	0	ns
Output Enable Time	t_{OE}	Note 9	-	18	-	19	ns
Output Disable Time	t_{OD}	Note 8	-	18	-	19	ns
Output Rise Time	t_R	From 0.8V to 2.0V, Note 8	-	6	-	6	ns
Output Fall Time	t_F	From 2.0V to 0.8V, Note 8	-	6	-	6	ns

NOTES:

6. AC Testing is performed as follows: Input levels (CLK) 0.0V and 4.0V; input levels (all other inputs) 0V and 3.0V. Timing reference levels (CLK) = 2.0V, (all others) = 1.5V. Output load circuit with C_L = 40pF. Output transition measured at V_{OH}Š ≥ 1.5V and V_{OL} ≤ 1.5V.
7. There must be at least one rising edge of CLK between the rising edge of $\overline{LD}$ and the falling edge of $\overline{START}$.
8. Characterized upon initial design and after major changes to design and/or process.
9. Transition is measured at ±200mV from steady state voltage with loading as specified in test load circuit with C_L = 40pF.

Test Load Circuit



Waveforms

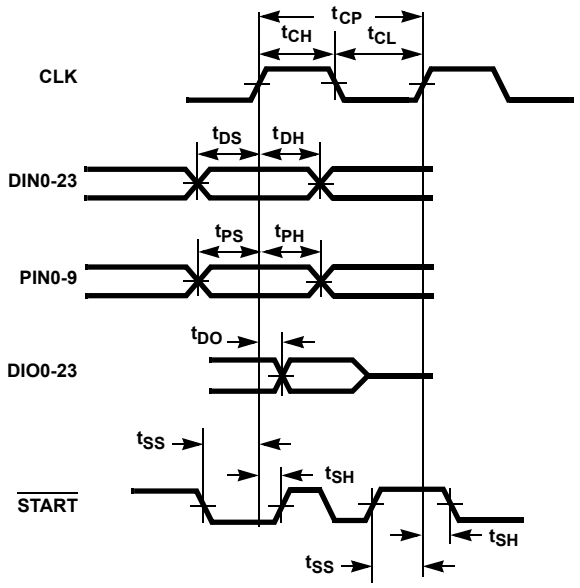


FIGURE 16. SYNCHRONOUS DATA AND CONTROL TIMING

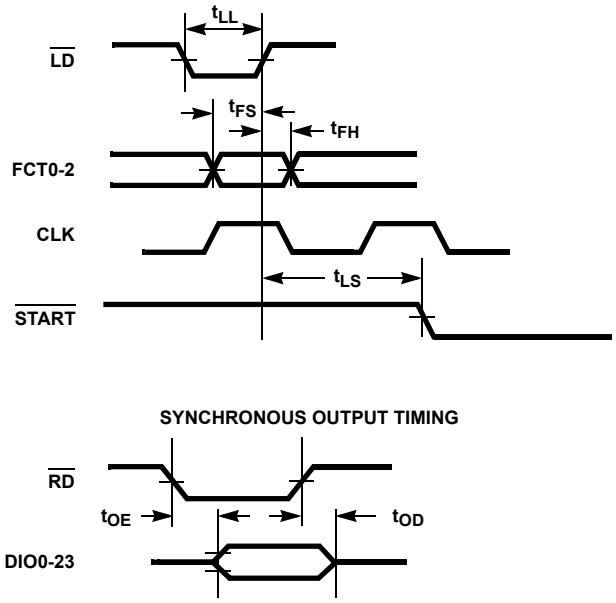


FIGURE 17. FUNCTION LOAD TIMING

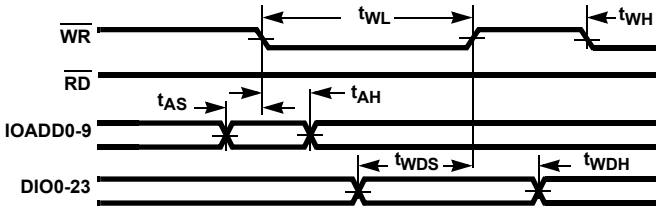


FIGURE 18. WRITE CYCLE TIMING

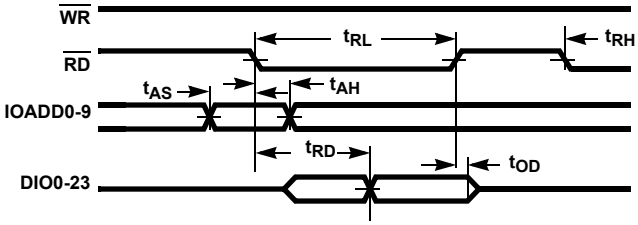


FIGURE 19. READ CYCLE TIMING

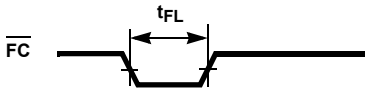


FIGURE 20. FLASH CLEAR TIMING

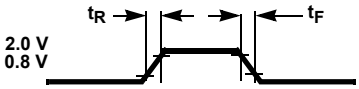


FIGURE 21. OUTPUT RISE AND FALL TIMES