MP6928A

Fast Turn-Off, Dual-Channel Intelligent Rectifier with Adaptive Forward Regulation Voltage and Ultra-Low Sleep Mode Current

DESCRIPTION

The MP6928A is a dual-channel, fast-turn off, intelligent rectifier for synchronous rectification in LLC-resonant converters.

The IC drives two N-channel MOSFETs and regulates their forward voltage drop to adaptive V_{FWD}. The IC turns the MOSFETs off before the switching current goes negative.

The MP6928A has light-load functionality to latch off the gate driver under light-load conditions, thus limiting the current below 150µA.

Fast turn-off enables continuous conduction mode and discontinuous conduction mode. Internal reverse-current protection ensures safe MOSFET operation under high-frequency, continuous current conditions.

The MP6928A requires a minimal number of readily available, standard external components. It is available in an SOIC-8 package.

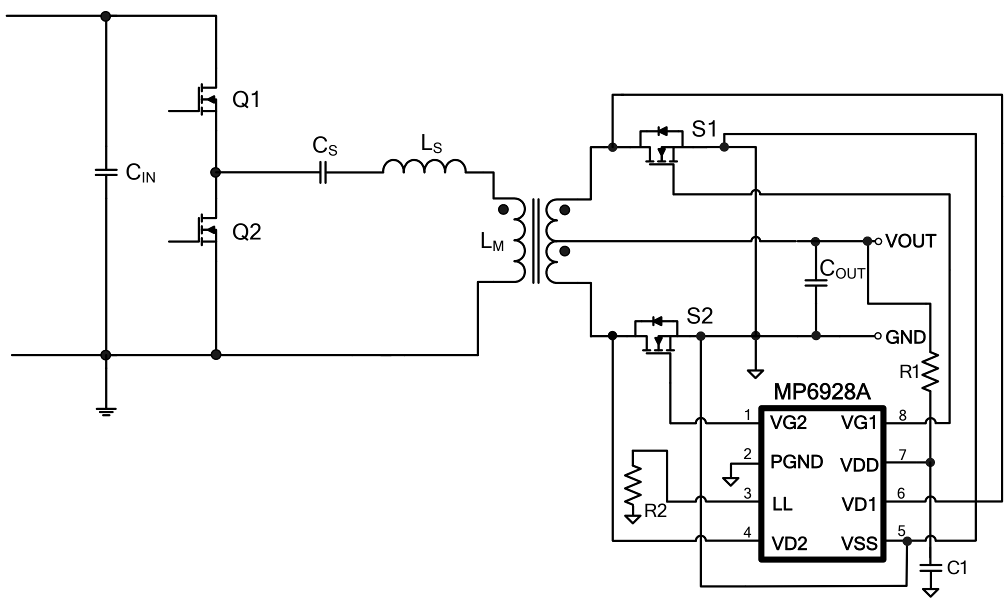
FEATURES

- Works with 12V Standard and 5V Logic Level FETS
- Compatible with Energy Star, 0.5W Standby Requirements
- Fast Turn-Off Total Delay
- 4.3V to 35V Wide VDD Operating Range
- <150µA Quiescent Current
- Supports CCM, CrCM, and DCM Operation
- Supports High-Side and Low-Side Rectification
- Available in an SOIC-8 Package

APPLICATIONS

- AC/DC Adapters
- LCDs & PDP TVs
- Telecom SMPS

TYPICAL APPLICATION



ORDERING INFORMATION

Part Number*	Package	Top Marketing	MSL Rating
MP6928AGS	SOIC-8	*See Below*	2

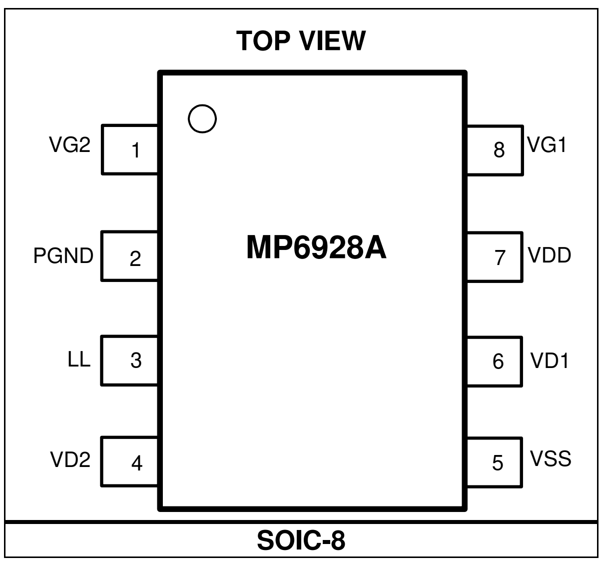
* For Tape & Reel, add suffix –Z (e.g. MP6928AGS–Z).

TOP MARKING (MPQ6526GUE-AEC1)

MP6928A
LLLLLLLL
MPSYWW

MP6928A: Part number
LLLLLLLL: Lot number
MPS: MPS prefix
Y: Year code
WW: Week code

PACKAGE REFERENCE



PIN FUNCTIONS

Pin #	Name	Description
1	VG2	**MOSFET 2 gate driver output.**
2	PGND	**Power ground.**
3	LL	**Light load timing setting.** Connect a resistor from LL to GND to set the light-load exit delay. Leave this pin open to disable light-load mode. Pull LL low to eliminate the light-load exit delay.
4	VD2	**MOSFET 2 voltage-sense drain.**
5	VSS	**Source pin used as reference for VD1 and VD2.**
6	VD1	**MOSFET 1 voltage-sense drain.**
7	VDD	**Supply voltage.**
8	VG1	**MOSFET 1 gate driver output.**

ABSOLUTE MAXIMUM RATINGS (1)

VDD to VSS.............................. -0.3V to +38V
PGND to VSS........................... -0.3V to +0.3V
V_G to VSS....................................... -0.3V to +15V
VD to VSS................................ -1V to +200V
LL to VSS............................... -0.3V to +6.5V
Continuous power dissipation (T_A = 25°C) (2)
SOIC-8...1.4W
Junction temperature...........................150°C
Lead temperature (solder).................... 260°C
Storage temperature .... -55°C to +150°C

ESD Ratings

Human body model (HBM)
VD1, VD2.. 500V
Other pins... 2000V
Charged device model (CDM)
VD1, VD2.. 1000V
Other pins.. 2000V

Recommended Operation Conditions (3)

VDD-VSS.................................... 4.3V to 35V
Operating junction temp (T_J)......... -40°C to +125°C

Thermal Resistance (4) θ_{JA} θ_{JC}

SOIC-8...................................90.......45....°C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance, θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the device will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7, 4-layer PCB.

ELECTRICAL CHARACTERISTICS

VDD = 12V, T_J = -40°C to +125°C, unless otherwise noted.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
VDD voltage range			4.3		35	V
VDD UVLO rising		LL floating, f_{SW} = 50kHz	3.8	4.05	4.3	V
VDD UVLO hysteresis			0.2	0.28	0.39	V
Operating current	I_{CC}	VDD = 12V, C_{LOAD} = 4.7nF, f_{SW} = 100kHz		10	15	mA
Quiescent current	I_Q	VDD = 5V, VSS-VD = 0.5V		4.0	6.0	mA
		VDD = 12V, VSS-VD = 0.5V		1.9	2.5	
Shutdown current		VDD = 3.7V	40	55	70	µA
Light-load mode current		R_{LL} = 50kΩ, VD = 5V	40	85	130	µA
Thermal shutdown (5)				160		°C
Thermal shutdown hysteresis (5)				25		°C
Control Circuitry						
VSS - VD forward voltage (1st stage)	$V_{FWD-HIGH}$		32	52	75	mV
VSS - VD forward voltage (2nd stage)	$V_{FWD-LOW}$		70	105	140	mV
Turn-off threshold (VSS - VD)	$V_{Drv-Off}$		-30	-15	0	mV
Turn-on delay	t_{DON}	C_{LOAD} = 4.7nF, V_{GS} = 2V		180	280	ns
	t_{DON}	C_{LOAD} = 10nF, V_{GS} = 2V		240	380	ns
Input bias current on the VD pin		VD = 180V			1	µA
Turn-on blanking time	t_{BON}	C_{LOAD} = 4.7nF	0.65	1.0	1.45	µs
Turn-off blanking time	t_{BOFF}	C_{LOAD} = 4.7nF	1.15	1.7	2.25	µs
Light-load enter timing threshold	t_{LL}		50	75	100	µs
Light-load enter switch-off threshold ($V_{G1/2}$ - VSS) (6)	V_{LL-GS}			2.5		V
Light-load exit pulse width	t_{EXIT}		0.9	1.55	2.3	µs
Light-load exit delay	$t_{Exit-Delay}$	R_{LL} = 1MΩ	0.65	1.0	1.35	ms
Light-load exit switch-on threshold (V_{DS})	V_{LL-DS}		-330	-215	-100	mV

ELECTRICAL CHARACTERISTICS

VDD = 12V, T_J = -40°C to +125°C, unless otherwise noted.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Gate Driver Selection						
V_G (low)	V_{G-L}	I_{LOAD} = 1mA			0.1	V
V_G (high)	V_{G-H}	VDD ⩾ 9V	8	8.6	9.2	V
		VDD < 9V	VDD - 0.1	VDD		V
Turn-on threshold (V_{DS})	V_{On_DS}		-330	-250	-170	mV
Turn-off propagation delay		VD = VSS		15	45	ns
Turn-off total delay	t_{DOFF}	VDD = 12V, VD = VSS, C_{LOAD} = 4.7nF, R_{GATE} = 0Ω, V_{GS} = 2V		35	85	ns
		VDD = 4.3V, VD = VSS, C_{LOAD} = 4.7nF, R_{GATE} = 0Ω, V_{GS} = 2V		30	80	
	t_{DOFF}	VDD = 12V, VD = VSS, C_{LOAD} = 10nF, R_{GATE} = 0Ω, V_{GS} = 2V		45	100	ns
		VDD = 4.3V, VD = VSS, C_{LOAD} = 10nF, R_{GATE} = 0Ω, V_{GS} = 2V		40	90	
Maximum source current (6)				0.25		A
Pull-down impedance				0.7	1.5	Ω

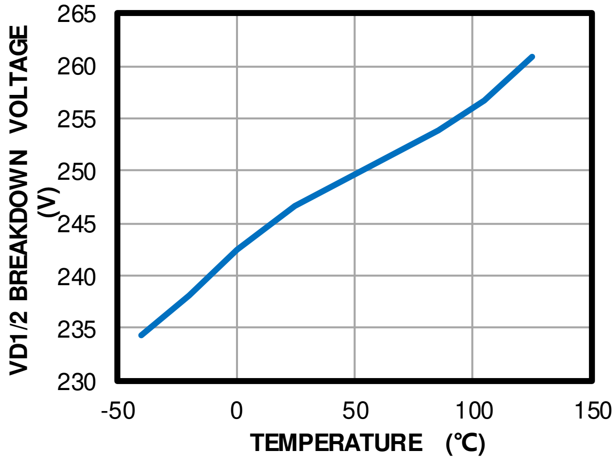
Notes:

5) Guaranteed by characterization.
6) Guaranteed by design.

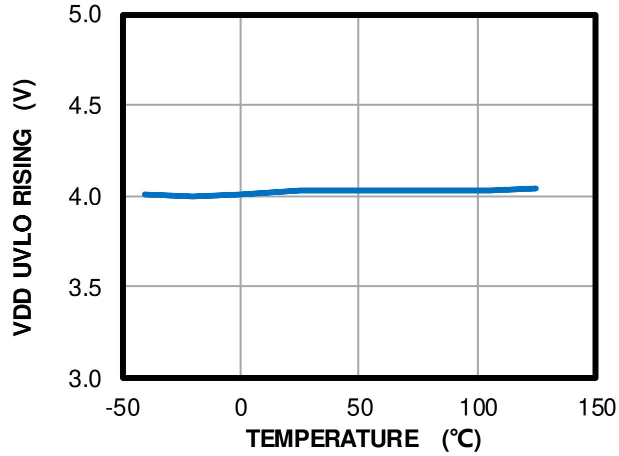
TYPICAL PERFORMANCE CHARACTERISTICS

VDD = 12V, unless otherwise noted.

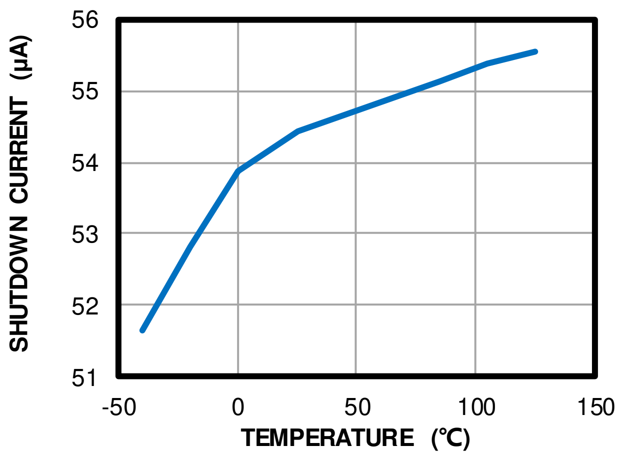
VD1/2 Breakdown Voltage vs. Temperature



VDD UVLO Rising vs. Temperature

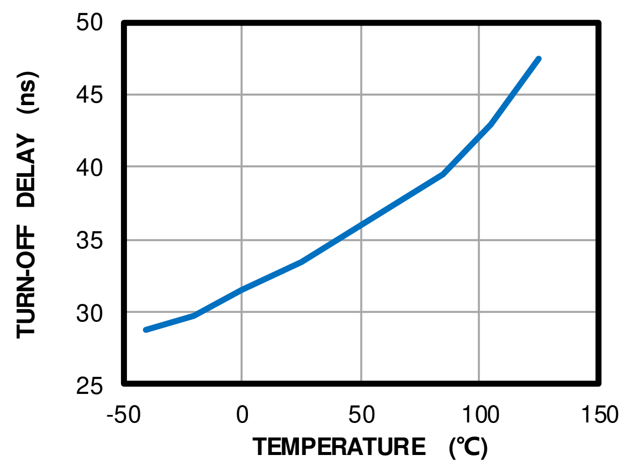


Shutdown Current vs. Temperature



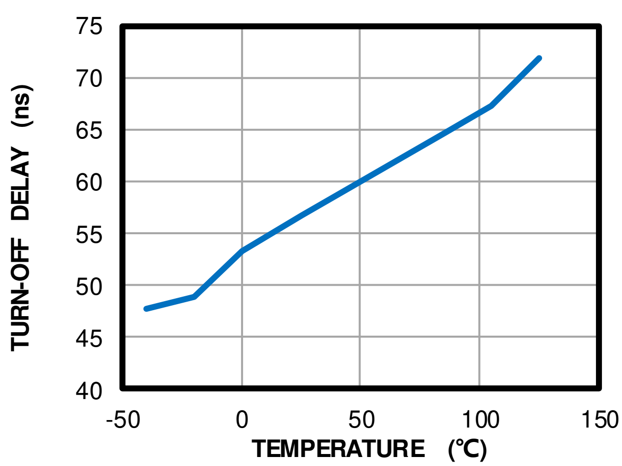
Turn-Off Delay vs. Temperature

C_{LOAD} = 4.7nF



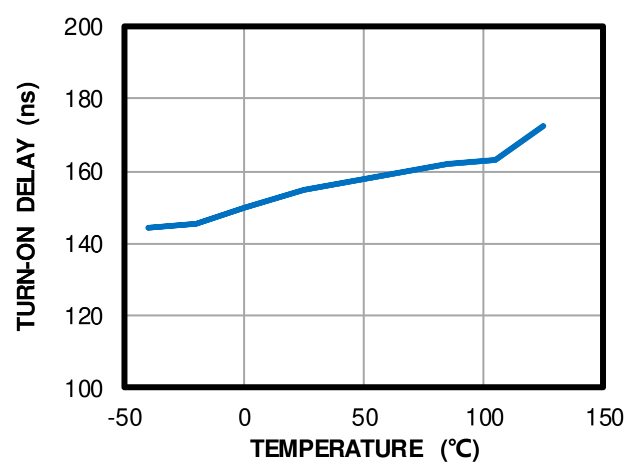
Turn-Off Delay vs. Temperature

C_{LOAD} = 10nF



Turn-On Delay vs. Temperature

C_{LOAD} = 4.7nF

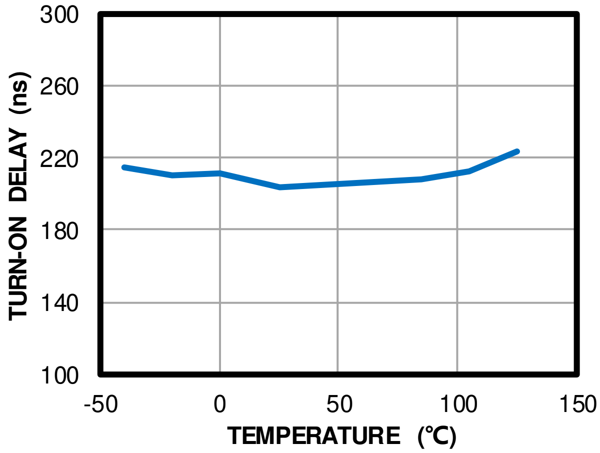


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

VDD = 12V, unless otherwise noted.

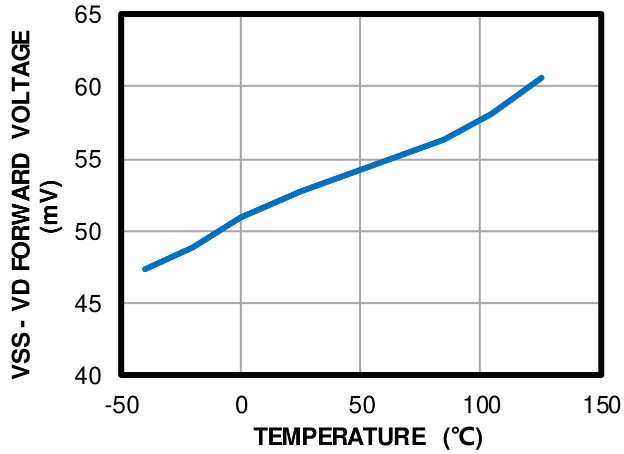
Turn-On Delay vs. Temperature

C_{LOAD} = 10nF



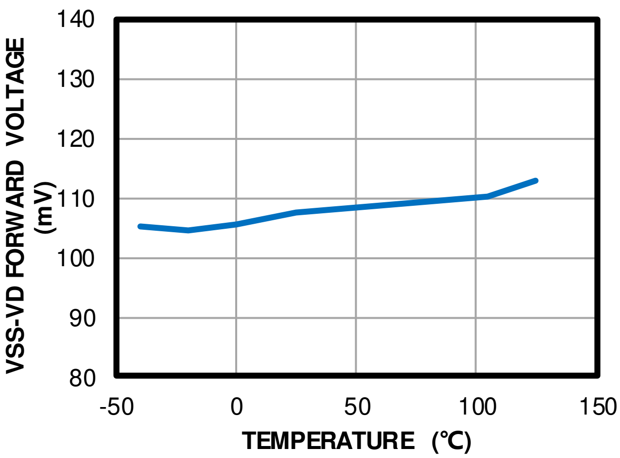
VSS - VD Forward Voltage vs. Temperature

First stage



VSS - VD Forward Voltage vs. Temperature

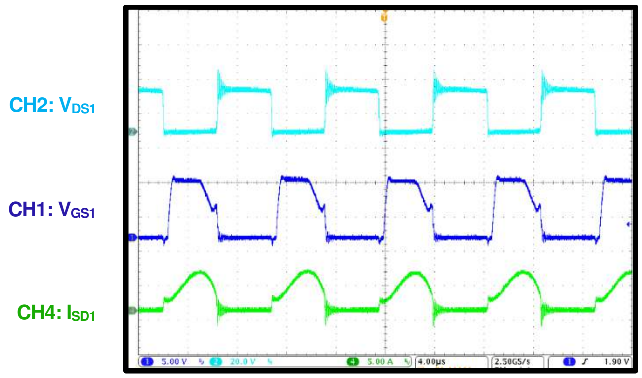
Second stage



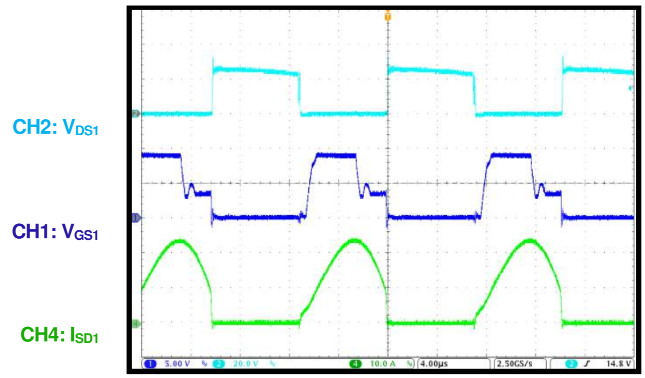
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

VDD = 12V, unless otherwise noted.

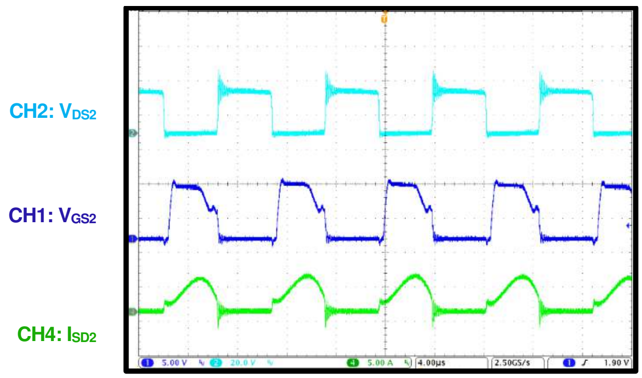
Operation in 180W LLC Converter
V_{IN} = 240V_{AC}, V_{OUT} = 12V, I_{OUT} = 5A



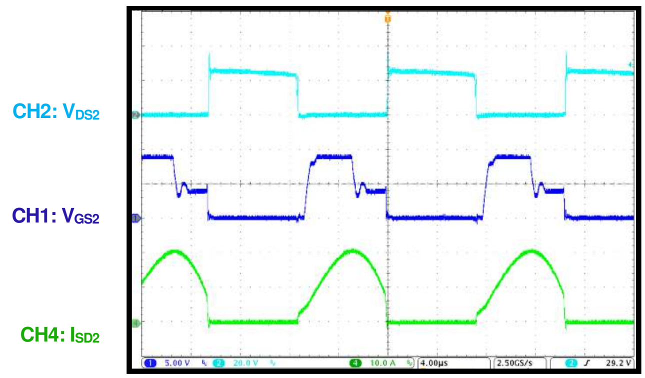
Operation in 180W LLC Converter
V_{IN} = 240V_{AC}, V_{OUT} = 12V, I_{OUT} = 15A



Operation in 180W LLC Converter
V_{IN} = 240V_{AC}, V_{OUT} = 12V, I_{OUT} = 5A



Operation in 180W LLC Converter
V_{IN} = 240V_{AC}, V_{OUT} = 12V, I_{OUT} = 15A



FUNCTIONAL BLOCK DIAGRAM

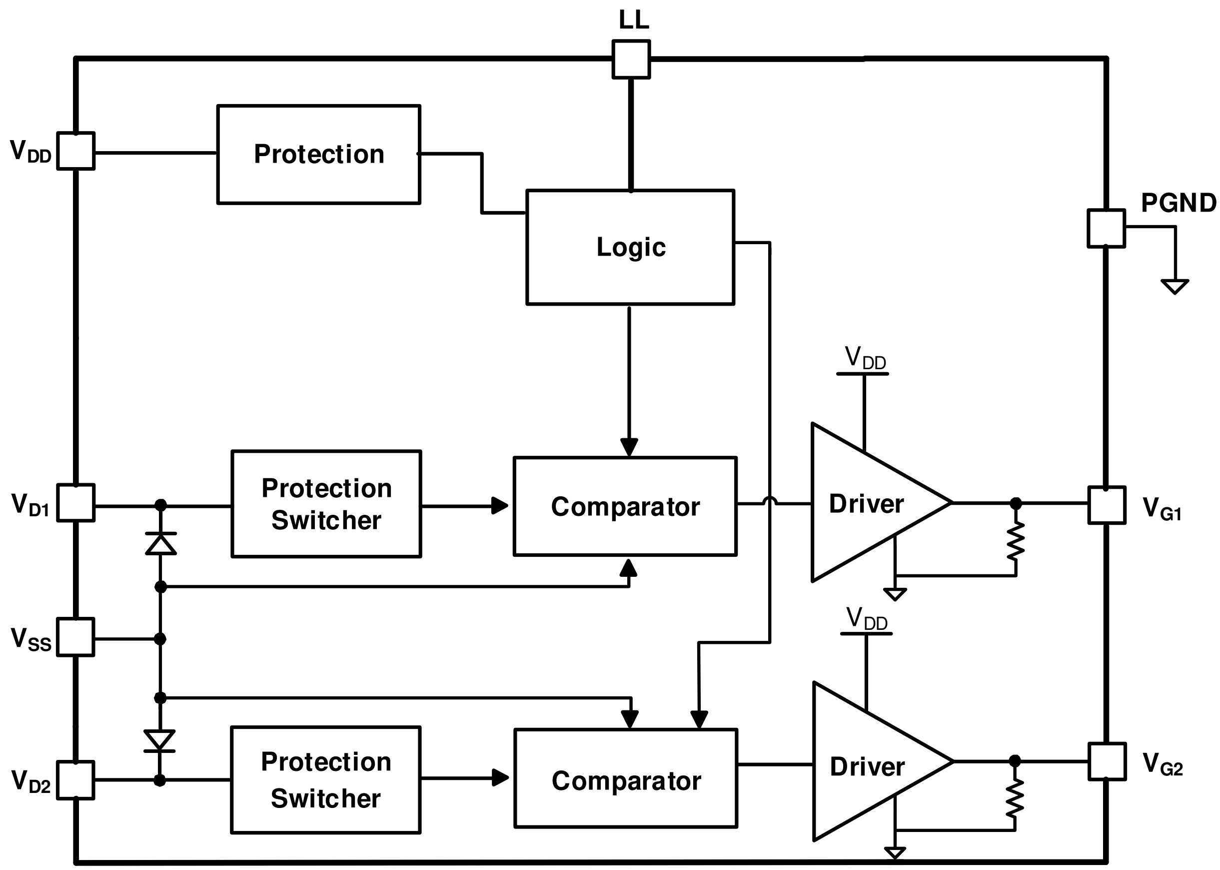


Figure 1: Functional Block Diagram

OPERATION

The MP6928A can operate in discontinuous conduction mode (DCM), continuous conduction mode (CCM), or critical conduction mode (CrCM). When the device operates in DCM or CrCM, the control circuitry controls the gate in forward mode. The gate turns off when the MOSFET current is low. In CCM, the control circuitry turns off the gate during very fast transients.

VD Clamp

Because VD1/2 can go as high as 180V, a high-voltage JFET is used at the input. To prevent excessive currents when VD1/2 drops below -0.7V, place a 1kΩ resistor between VD1/2 and the drain of the external MOSFET.

Under-Voltage Lockout (UVLO)

When VDD falls below the under-voltage lockout (UVLO) threshold (about 4.3V), the MP6928A enters sleep mode and $V_{G1/2}$ remains low.

Thermal Shutdown

If the MP6928A's junction temperature exceeds 165°C, $V_{G1/2}$ is pulled low, and the device stops switching. The IC resumes normal function after the junction temperature drops by 25°C.

Turn-On Phase

When the switching current flows through the MOSFET's body diode, there is a negative voltage drop (VD - VSS) across the body diode. V_{DS} falls below the turn-on threshold of the control circuitry ($V_{LL\text{-}DS}$), which triggers a charge current to turn on the MOSFET (see Figure 2).

Turn-On Blanking Time

The control circuitry offers a blanking function that ensures the MOSFET remains on or off for t_{BON} (about 1µs), which determines the minimum turn-on time. During the turn-on blanking period, the turn-off threshold is not blanked completely and changes to about 100mV (instead of $-V_{Drv\text{-}Off}$, which is about 15mV).

This ensures that the part can always turn off, though it turns off more slowly during the turn-on blanking period. To avoid shoot-through, set the synchronous period below t_{BON} during CCM in the LLC converter.

Conduction Phase

When V_{DS} rises above the forward voltage drop ($-V_{Fwd\text{-}High}$) according to the decrease in switching current, the MP6928A pulls down the gate voltage. This eases the rise of V_{DS} by raising the on resistance of the synchronous MOSFET.

The forward voltage drop switches to a lower level ($-V_{Fwd\text{-}Low}$) when $-V_{Fwd\text{-}High}$ is triggered.

Figure 2 shows how V_{DS} is adjusted to be approximately $-V_{Fwd\text{-}Low}$, even when the current through the MOSFET is fairly low. This function sets a low driver voltage when the synchronous MOSFET turns off, which boosts the turn-off speed.

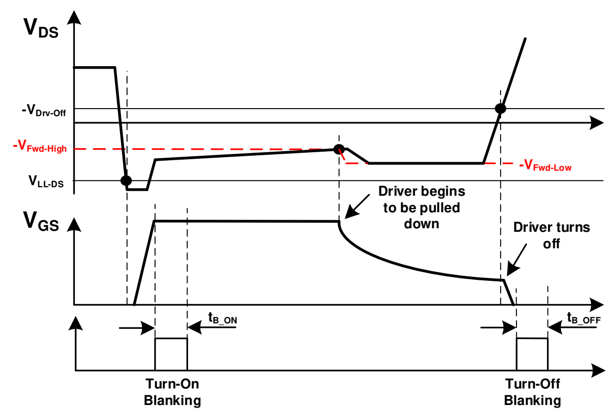


Figure 2: Turn-On/Off Timing Diagram

Turn-Off Phase

When V_{DS} rises to trigger the turn-off threshold, the gate voltage is pulled to zero after a very short turn-off delay (see Figure 2).

Turn-Off Blanking Time

When V_{DS} reaches the turn-off threshold ($-V_{Drv\text{-}Off}$) and the gate driver is pulled to zero, a turn-off blanking time is triggered. This ensures the gate driver is off for a minimum t_{BOFF} to avoid any error triggers on V_{DS}.

The turn-off blanking time is removed when turn on time exceeds t_{BOFF}, and V_{DS} exceeds 2V with a rising edge.

Light-Load Latch-Off Function

To improve efficiency, the MP6928A's gate driver latches off to reduce driver loss under light-load conditions.

When the LLC converter enters burst mode under light load, the MP6928A latches off the gate driver and monitors the switch-off time by comparing the CH1 SR gate (VG1) driver with the light-load enter switch-off threshold (V_{LL-GS}). If the CH1 SR gate driver voltage remains below V_{LL-GS} for the light-load enter timing threshold (t_{LL}, about 75µs), the IC latches off the gate driver to reduce power loss (see Figure 3).

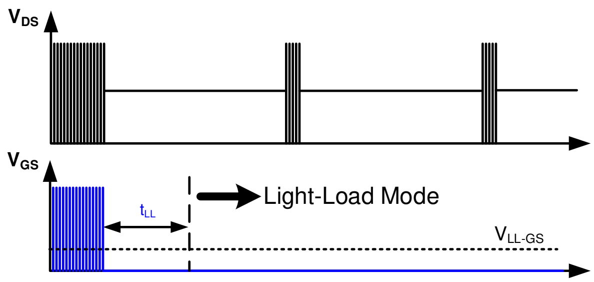


Figure 3: The MP6928A Enters Light-Load Mode

During light-load mode, the MP6928A monitors the MOSFET's body diode conduction time. If the body diode conduction time exceeds t_{Exit} (about 1.55µs) every cycle, the IC identifies that the system is exiting burst mode and initiates the gate driver after a delay time ($t_{Exit-Delay}$) (see Figure 4).

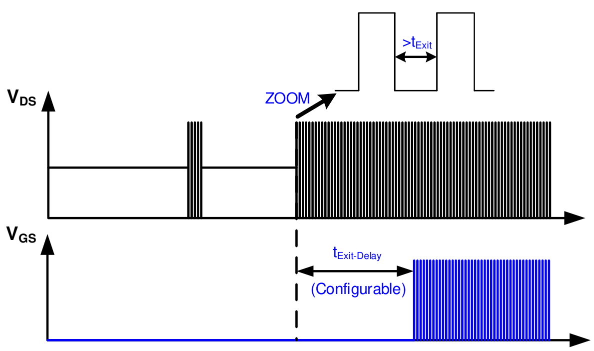


Figure 4: The MP6928A Exits Light-Load Mode

$t_{Exit-Delay}$ is configurable by connecting a resistor (R_{LL}) from the LL pin to GND. By monitoring the LL pin voltage, $t_{Exit-Delay}$ can be calculated with Equation (1):

$$t_{Exit\_Delay} = R_{LL}(k\Omega) \times \frac{50\mu s}{50(k\Omega)} \quad (1)$$

Light-load mode cannot be triggered if LL is floating.

If light-load mode ends during the rectification cycle, the gate driver signal does not appear until the next rectification cycle begins (see Figure 5).

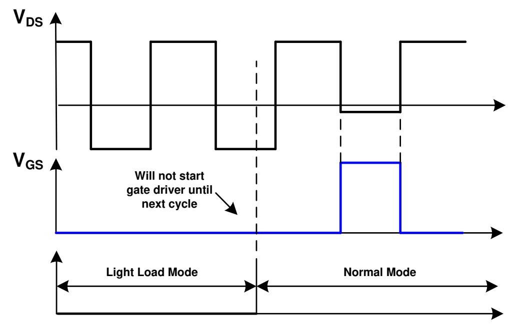


Figure 5: Gate Driver Start after Existing Light-Load Mode

APPLICATION INFORMATION

SR MOSFET Selection and Driver Ability

Power MOSFET selection is a tradeoff between $R_{DS(ON)}$ and Q_G. To achieve high efficiency, a MOSFET with lower $R_{DS(ON)}$ is recommended. A higher Q_G paired with a lower $R_{DS(ON)}$ lowers the turn-on/off speed and increases power loss.

For the MP6928A, V_{DS} is adjusted at V_{FWD} during the driving period. A MOSFET with low $R_{DS(ON)}$ is not recommended because the gate driver may be kept at a fairly low level, even when the system load is high. This means there is no advantage to having a low $R_{DS(ON)}$

Figure 6 shows a typical LLC secondary side waveform. To achieve a fairly high usage of the MOSFET's $R_{DS(ON)}$, it is expected that the MOSFET driver voltage is maximized until the last 25% of the SR conduction period.

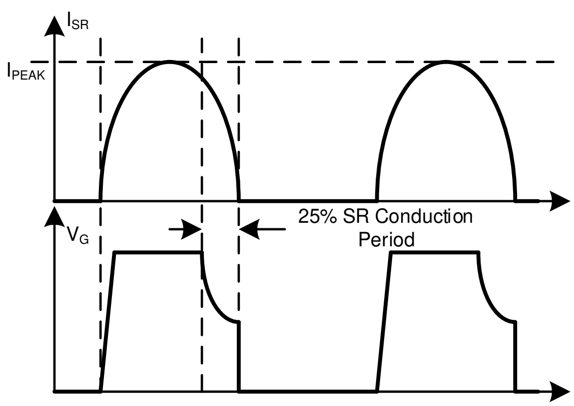


Figure 6: Synchronous Rectification Typical waveform in LLC

Calculate V_{DS} with Equation (2):

$$V_{DS} = -R_{DS(ON)} \times \frac{\sqrt{2}}{2} \times I_{PEAK} = -R_{DS(ON)} \times I_{OUT} = -V_{Fwd\_high} \quad (2)$$

Where V_{DS} is the MOSFET's drain-source voltage.

It is recommended to keep the MOSFET's $R_{DS(ON)}$ above V_{FWD} / I_{OUT} (mΩ). For example, in a 10A application where V_{FWD} is set to 50mV, $R_{DS(ON)}$ should not be below 5mΩ.

The MOSFET's Q_G affects the turn-on/off delay. Figure 2 shows the turn-on delay (t_{DON}) and turn-off delay (t_{DOFF}). t_{DON} indicates how long the body diode conducts before the MOSFET turns on, while t_{DOFF} indicates how long the driver takes to turn off the MOSFET. A longer turn-on delay means MOSFET's body diode conducts for longer, which lowers overall efficiency. A longer turn-off delay increases the risk of shoot-through during CCM.

Figure 7 shows t_{DON} according to different C_{LOAD} values.

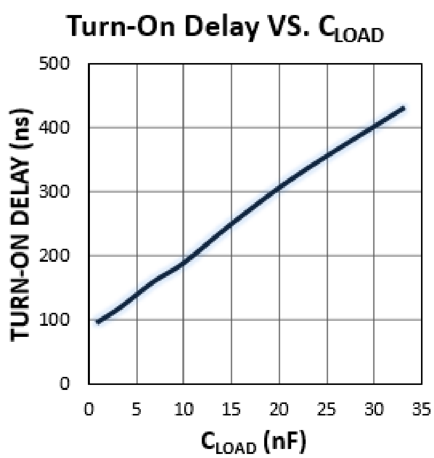


Figure 7: Turn-On Delay vs. C_{LOAD}

Figure 8 shows t_{DOFF} according to different C_{LOAD} values.

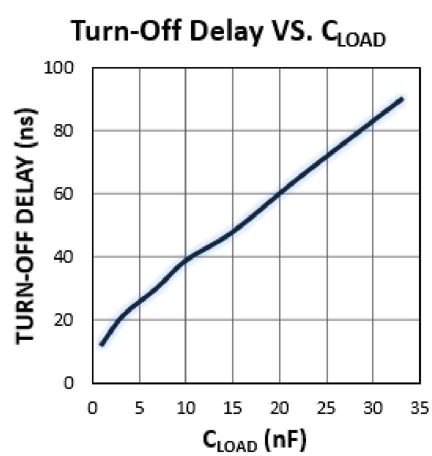


Figure 8: Turn-Off Delay vs. C_{LOAD}

Figure 9 shows how t_{DON} affects system efficiency.

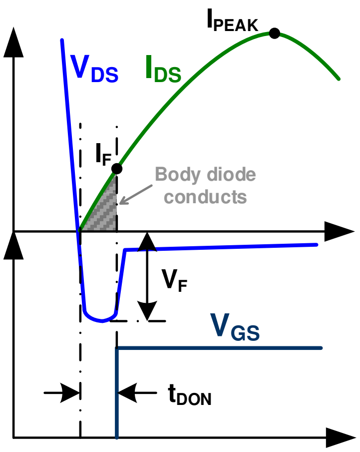


Figure 9: Turn-On Delay Affects Efficiency

During t_{DON}, the body diode of the SR MOSFET conducts, which leads to a power loss (P_{ON}) that can be calculated with Equation (3):

$$P_{ON} \approx \frac{V_F \times I_F}{2} \times 2f_{SW} \times t_{DON} = V_F \times I_F \times f_{SW} \times t_{DON} \quad (3)$$

Where V_F is the body diode forward voltage drop, I_F is the switching current when the turn-on delay (t_{DON}) has ended, and f_{SW} is the switching frequency.

If the switching current is considered to be a complete sine wave, I_F can be estimated with Equation (4):

$$I_F = I_{PEAK} \times \sin(2 \times f_{SW} \times t_{DON} \times \pi) \quad (4)$$

Where I_{PEAK} is the peak switching current through the MOSFET, calculated with Equation (5):

$$I_{PEAK} \approx \frac{\pi}{2} \times I_{OUT} \quad (5)$$

Where I_{OUT} is the system output current.

When plugging the values from Equation (4) and Equation (5) into Equation (3), the turn-on delay power loss (P_{ON}) through the SR MOSFET's body diode can be calculated with Equation (6):

$$P_{ON} = \frac{\pi}{2} \times I_{OUT} \times V_F \times f_{SW} \times t_{DON} \times \sin(2 \times f_{SW} \times t_{DON} \times \pi) \quad (6)$$

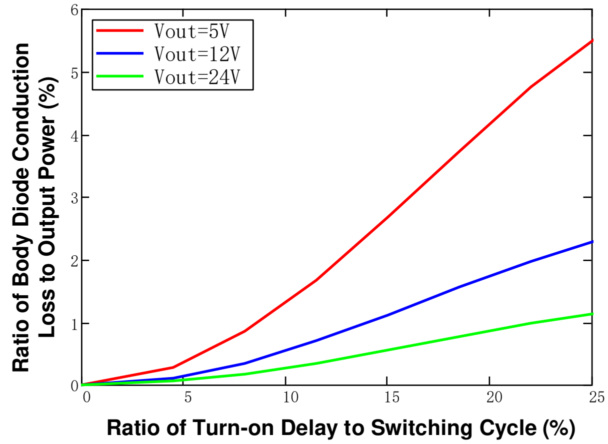


Figure 10: Turn-On Delay vs. Power Loss

Figure 10 shows how different turn-on delay values affect efficiency according to different output voltages. To keep the body diode conduction loss at a fairly low level (below 0.5% of the output power), the turn-on delay should be below 5% of the switching cycle. For example, in a f_{SW} = 200kHz LLC system, the switching cycle is about 5µs. It is recommended to select the MOSFET to make t_{DON} shorter than 250ns.

The turn-off delay (t_{DOFF}) is critical in CCM applications with fast transients. Choose the MOSFET that keeps t_{DOFF} below the CCM current transient duration. Otherwise, the MOSFET may require a lower Q_G, or an external totem pole driver circuit may be added to prevent shoot-through.

PCB Layout Guidelines

PCB layout is critical for stable operation. For the best results, follow the guidelines below:

Sensing for VD/VSS

1. Keep the sensing connections (VD1/VSS, VD2/VSS) as close to each of the MOSFETs (drain/source) as possible.
2. Keep the two channels' sensing loops separated from each other.
3. Make the sensing loop as small as possible (see Figure 11).

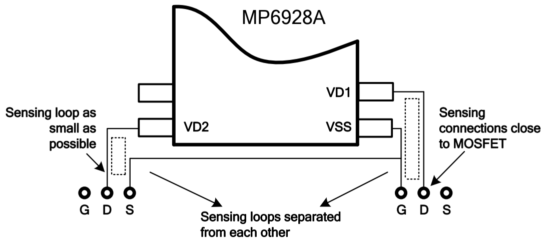


Figure 11: Sensing for VD/VSS

VDD Decoupling Capacitor

Figure 12 shows a layout example of the MP6924A driving SOIC-8 package MOSFETs with two separate, small, sensing loops.

1. Place a minimum 1µF decoupling capacitor from VDD to PGND, and close to the IC for adequate filtering (see Figure 12).

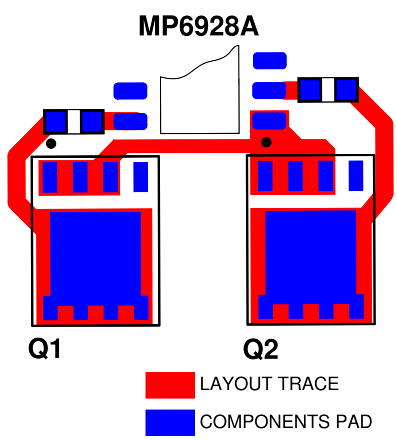


Figure 12: Layout Example for Sensing Loop and VDD Decoupling

System Power Loop

Figure 13 shows a layout example of the power loop trace, which has a minimized loop length. The two channel power traces do not cross one another.

1. Keep the two channels' power loops separated (see Figure 13) to minimize their interaction, which may affect the voltage sensing of the IC.
2. Make the power loop as small as possible to reduce parasitic inductance.

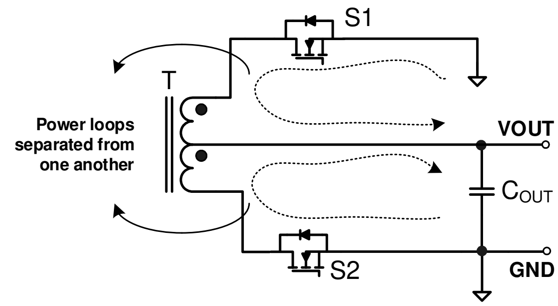


Figure 13: System Power Loop

3. Keep the driver's sensing loop trace away from the power loop trace (see Figure 14). The sensing loop trace and power loop trace can be placed on different layers.

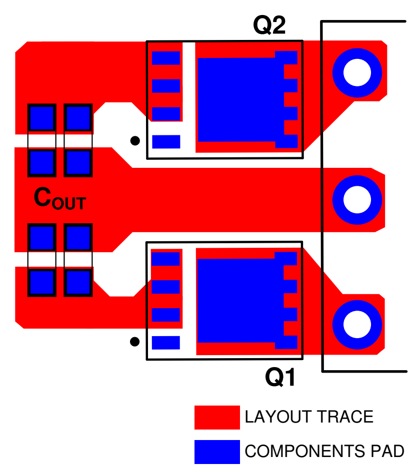
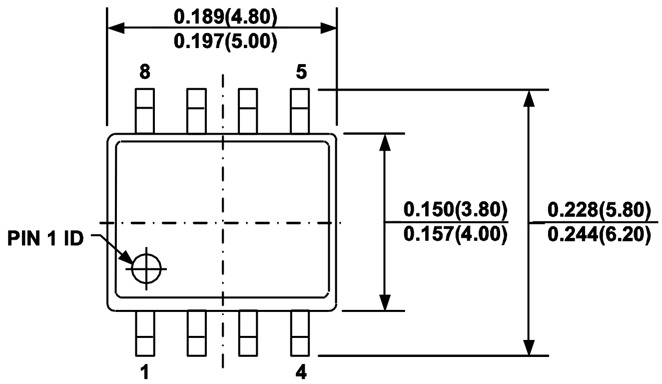


Figure 14: Layout Example for System Power Loop

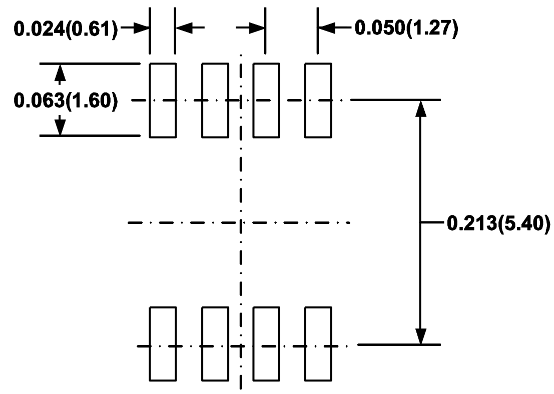
4. Do not place the driver IC inside the power loop, as it may affect MOSFET voltage sensing.

PACKAGE INFORMATION

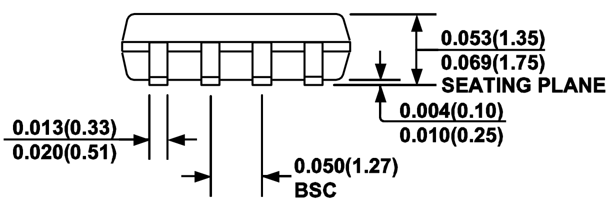
SOIC-8



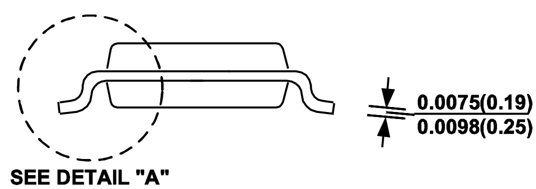
TOP VIEW



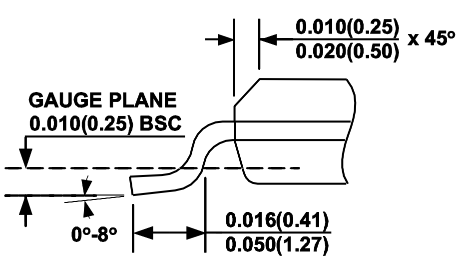
RECOMMENDED LAND PATTERN



FRONT VIEW



SIDE VIEW

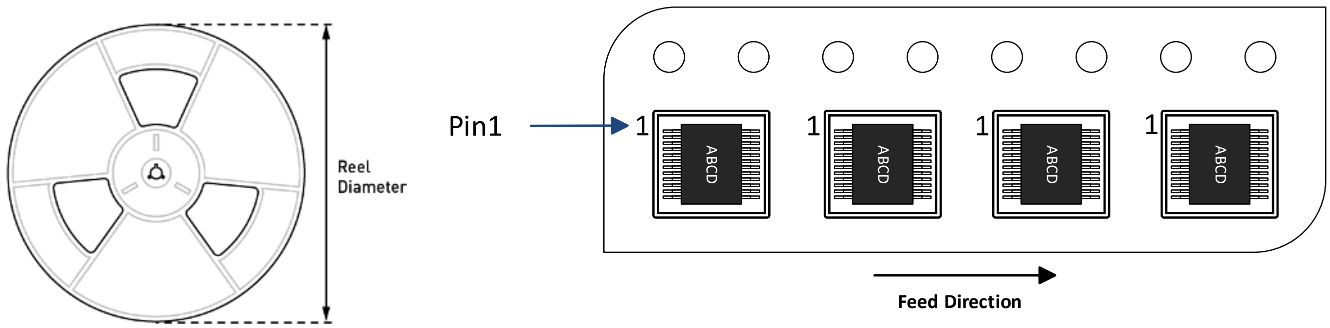


DETAIL "A"

NOTE:

1) CONTROL DIMENSION IS IN INCHES. DIMENSION IN BRACKET IS IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.004" INCHES MAX.
5) DRAWING CONFORMS TO JEDEC MS-012, VARIATION AA.
6) DRAWING IS NOT TO SCALE.

CARRIER INFORMATION



Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MP6928AGS–Z	SOIC-8	2500	100	13in	12mm	8mm

REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	8/10/2020	Initial Release	-