

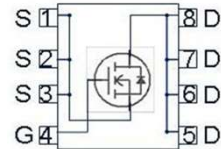
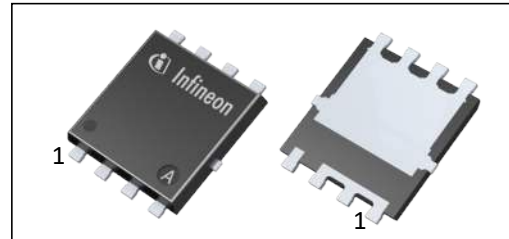
OptiMOS™ -5 Power Transistor

Features

- OptiMOS™ power MOSFET for automotive applications
- N-channel - Enhancement mode - Logic Level
- MSL1 up to 260°C peak reflow
- 175 °C operating temperature
- Green product (RoHS compliant)
- 100% Avalanche tested

Product Summary

V_{DS}	80	V
$R_{DS(on),max}$	14	mΩ
I_D	40	A

PG-TDSON-8-33


Type	Package	Marking
IAUC40N08S5L140	PG-TDSON-8-33	5N08L140

Maximum ratings, at $T_j=25\text{ °C}$, unless otherwise specified

Parameter	Symbol	Conditions	Value	Unit
Drain current	I_D	$T_C=25\text{ °C}$, $V_{GS}=10\text{ V}$, DC ^{1,2)}	40	A
		$T_C=100\text{ °C}$, $V_{GS}=10\text{ V}$, DC ^{1,2)}	28	
Pulsed drain current ²⁾	$I_{D,pulse}$	$T_C=25\text{ °C}$	160	
Avalanche energy, single pulse ²⁾	E_{AS}	$I_D=18\text{ A}$	32	mJ
Avalanche current, single pulse	I_{AS}	-	18	A
Gate source voltage	V_{GS}	-	±20	V
Power dissipation	P_{tot}	$T_C=25\text{ °C}$	56	W
Operating and storage temperature	T_j, T_{stg}	-	-55 ... +175	°C

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	
Thermal characteristics²⁾						
Thermal resistance, junction - case	R_{thJC}	-	-	-	2.7	K/W
Thermal resistance, junction - ambient ⁴⁾	R_{thJA}	-	-	28.5	-	
Electrical characteristics, at $T_j=25^\circ\text{C}$, unless otherwise specified						
Static characteristics						
Drain-source breakdown voltage	$V_{(BR)DSS}$	$V_{GS}=0V, I_D=1mA$	80	-	-	V
Gate threshold voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=15\mu A$	1.2	1.6	2.0	
Zero gate voltage drain current	I_{DSS}	$V_{DS}=80V, V_{GS}=0V, T_j=25^\circ\text{C}$	-	-	1	μA
		$V_{DS}=80V, V_{GS}=0V, T_j=85^\circ\text{C}^{2)}$	-	-	20	
Gate-source leakage current	I_{GSS}	$V_{GS}=20V, V_{DS}=0V$	-	-	100	nA
Drain-source on-state resistance	$R_{DS(on)}$	$V_{GS}=4.5V, I_D=20A$	-	16.5	20	m Ω
		$V_{GS}=10V, I_D=20A$	-	12.5	14	
Gate resistance ²⁾	R_G	-	-	1.2	-	Ω

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	

Dynamic characteristics²⁾

Input capacitance	C_{iss}	$V_{GS}=0V, V_{DS}=40V,$ $f=1MHz$	-	829	1078	pF
Output capacitance	C_{oss}		-	146	190	
Reverse transfer capacitance	C_{rss}		-	11	17	
Turn-on delay time	$t_{d(on)}$	$V_{DD}=40V, V_{GS}=10V,$ $I_D=20A, R_{G,ext}=3.5\Omega$	-	2	-	ns
Turn-off delay time	$t_{d(off)}$		-	9	-	
Rise time	t_r		-	1	-	
Fall time	t_f		-	4	-	

Gate Charge Characteristics²⁾

Gate to source charge	Q_{gs}	$V_{DD}=40V, I_D=20A,$ $V_{GS}=0$ to 10V	-	2.7	3.5	nC
Gate to drain charge	Q_{gd}		-	3.2	4.8	
Gate charge total	Q_g		-	14.3	18.6	
Gate plateau voltage	$V_{plateau}$		-	3.2	-	V

Reverse Diode

Diode continuous forward current ²⁾	I_S	$T_C=25^\circ C$	-	-	40	A
Diode pulse current ²⁾	$I_{S,pulse}$	$T_C=25^\circ C$	-	-	160	
Diode forward voltage	V_{SD}	$V_{GS}=0V, I_F=20A,$ $T_j=25^\circ C$	-	0.9	1.2	V
Reverse recovery time ²⁾	t_{rr}	$V_R=40V, I_F=40A,$ $di_F/dt=100A/\mu s$	-	31	-	ns
Reverse recovery charge ²⁾	Q_{rr}		-	25	-	nC

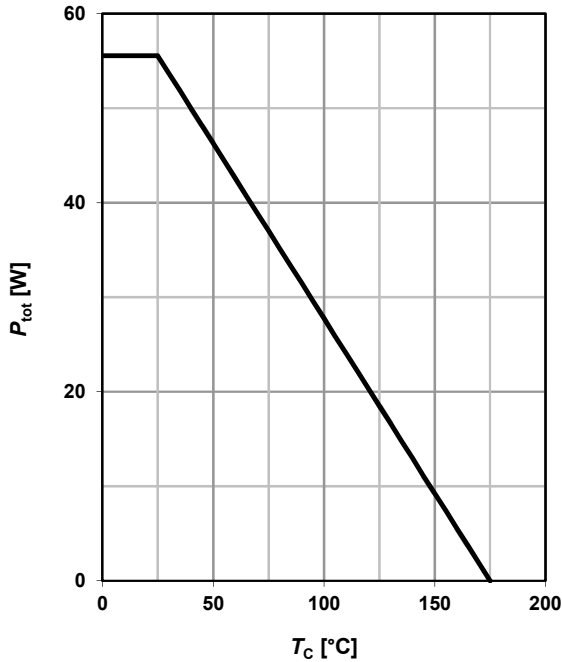
¹⁾ Practically the current is limited by the overall system design including the customer-specific PCB.

²⁾ The parameter is not subject to production test - verified by design/characterization.

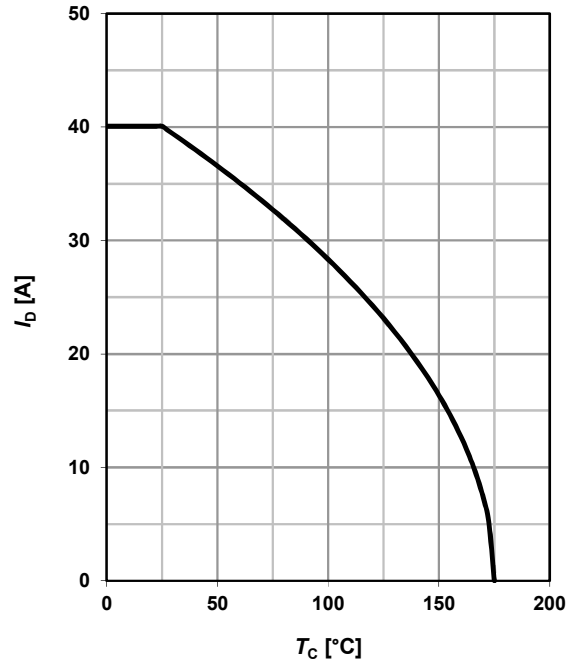
³⁾ Device on a 2s2p FR4 PCB defined in accordance with JEDEC standards (JESD51-5-7). PCB is vertical in still air.

1 Power dissipation

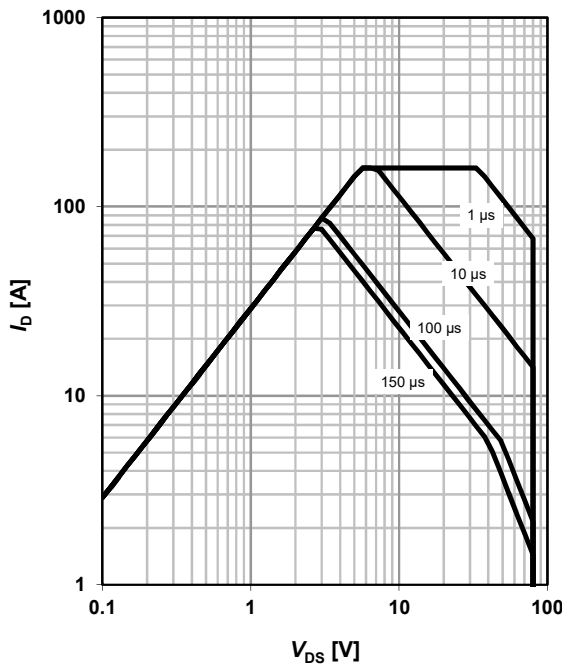
$$P_{\text{tot}} = f(T_C); V_{\text{GS}} = 10 \text{ V}$$


2 Drain current

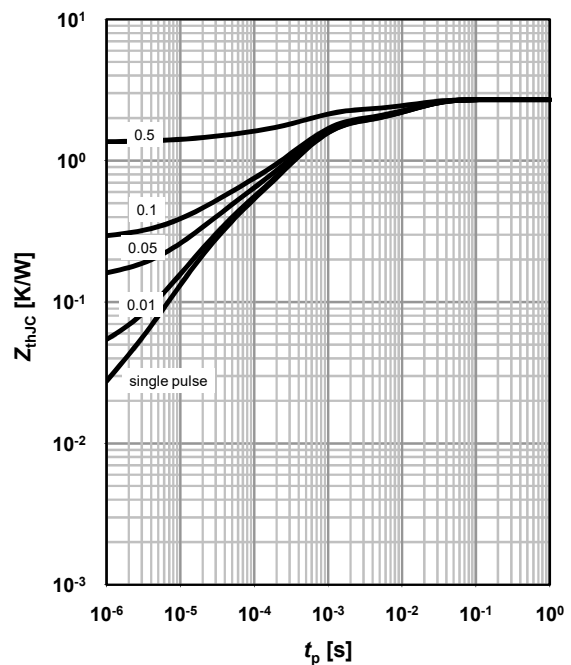
$$I_D = f(T_C); V_{\text{GS}} = 10 \text{ V}$$


3 Safe operating area

$$I_D = f(V_{\text{DS}}); T_C = 25 \text{ °C}; D = 0$$

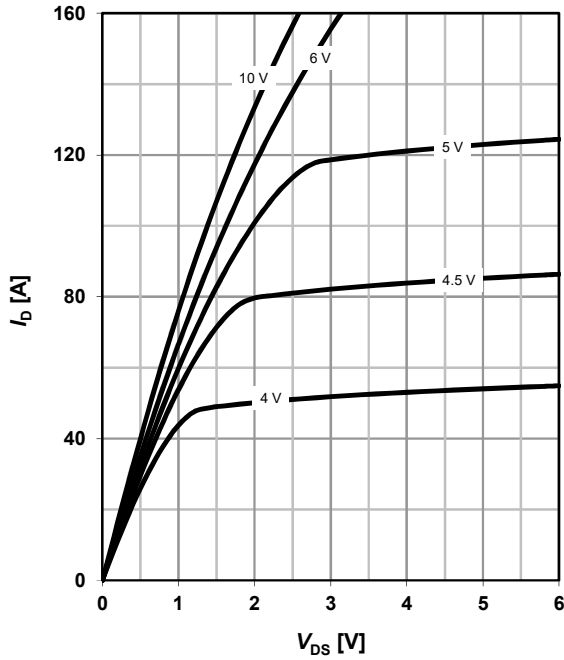
 parameter: t_p

4 Max. transient thermal impedance

$$Z_{\text{thJC}} = f(t_p)$$

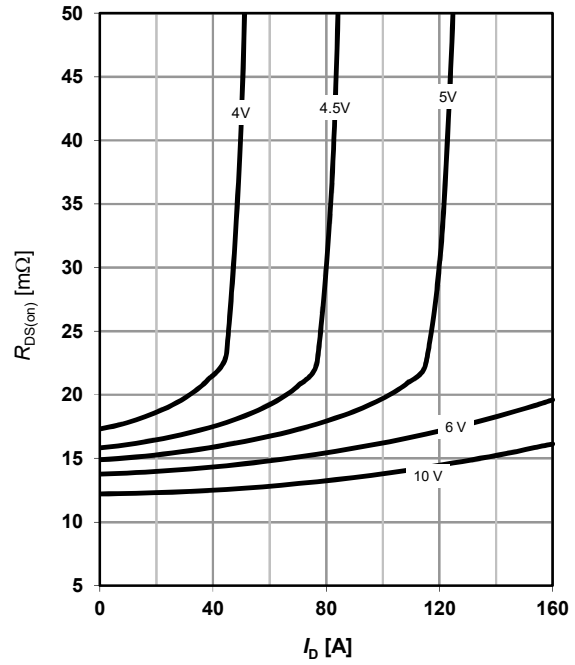
 parameter: $D = t_p/T$


5 Typ. output characteristics

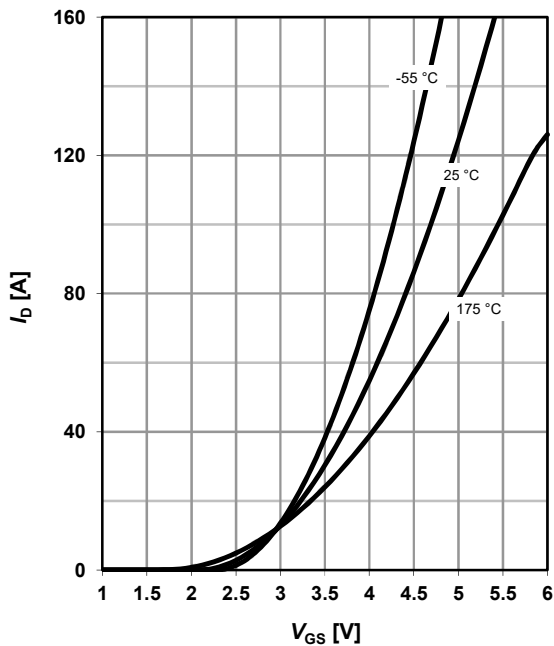
$$I_D = f(V_{DS}); T_j = 25\text{ °C}$$

 parameter: V_{GS}

6 Typ. drain-source on-state resistance

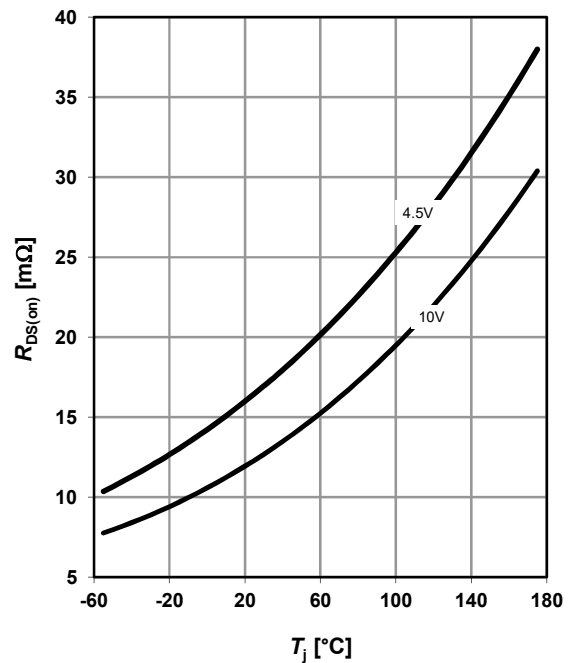
$$R_{DS(on)} = f(I_D); T_j = 25\text{ °C}$$

 parameter: V_{GS}

7 Typ. transfer characteristics

$$I_D = f(V_{GS}); V_{DS} = 6V$$

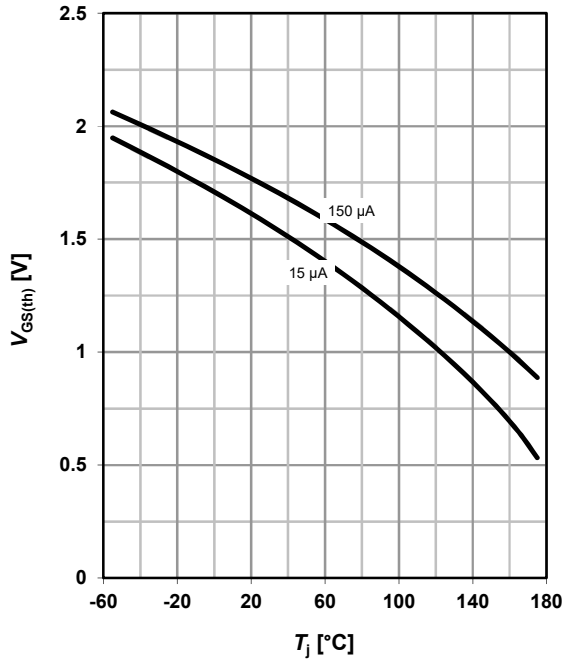
 parameter: T_j

8 Typ. drain-source on-state resistance

$$R_{DS(on)} = f(T_j); I_D = 20A$$

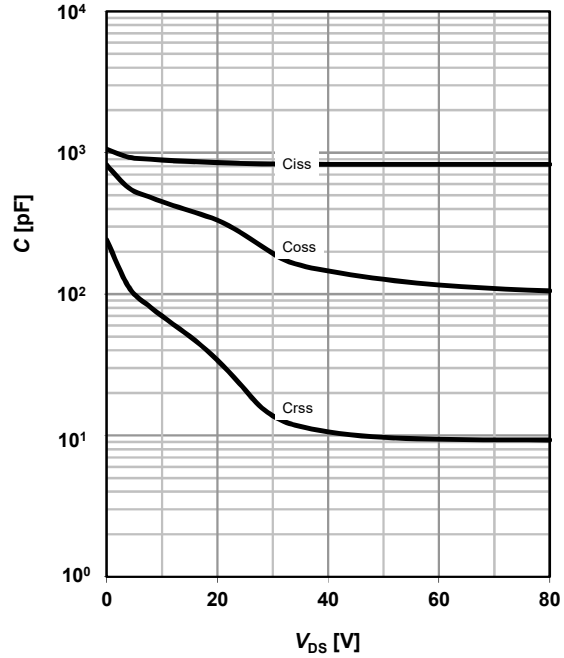
 parameter: V_{GS}


9 Typ. gate threshold voltage

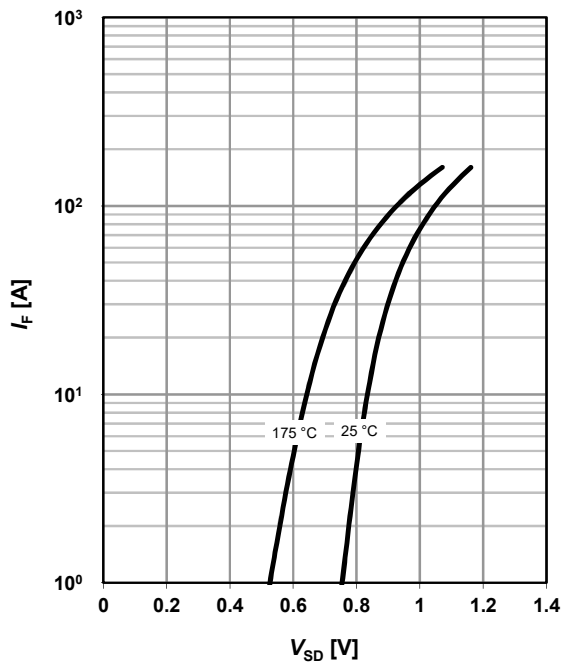
$$V_{GS(th)} = f(T_j); V_{GS} = V_{DS}$$

 parameter: I_D

10 Typ. capacitances

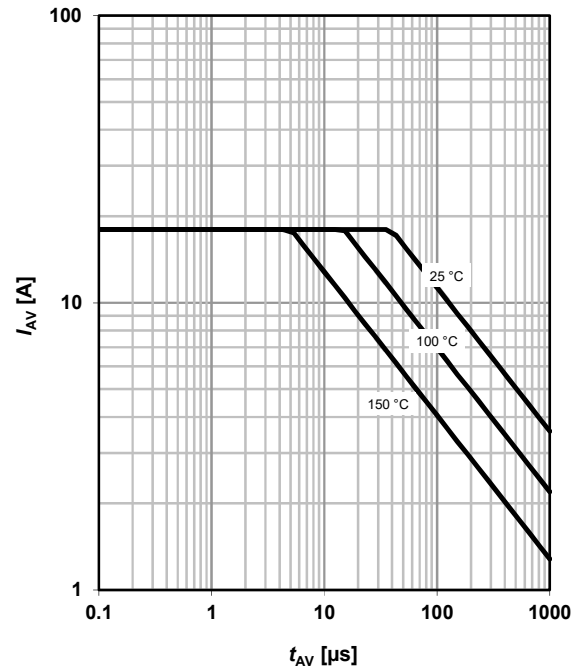
$$C = f(V_{DS}); V_{GS} = 0 \text{ V}; f = 1 \text{ MHz}$$


11 Typical forward diode characteristics

$$I_F = f(V_{SD})$$

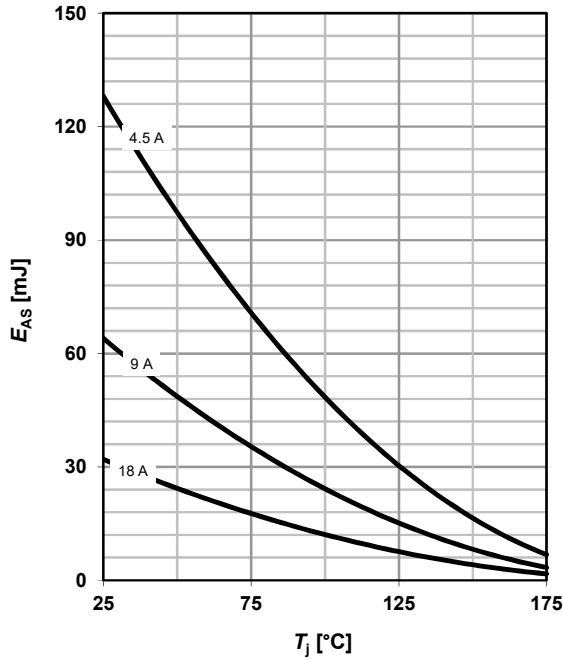
 parameter: T_j

12 Avalanche characteristics

$$I_{AS} = f(t_{AV})$$

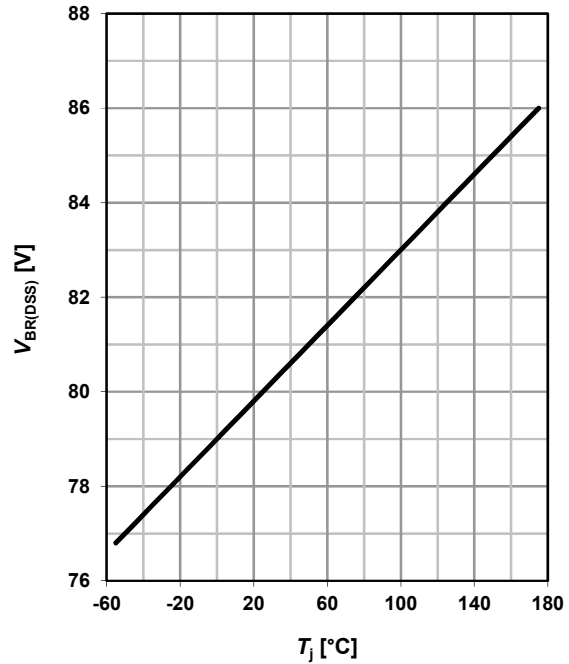
 parameter: $T_{j(start)}$


13 Avalanche energy

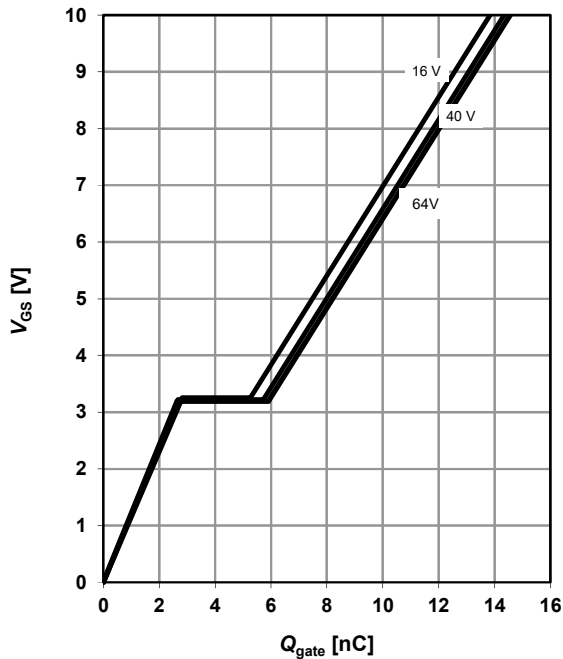
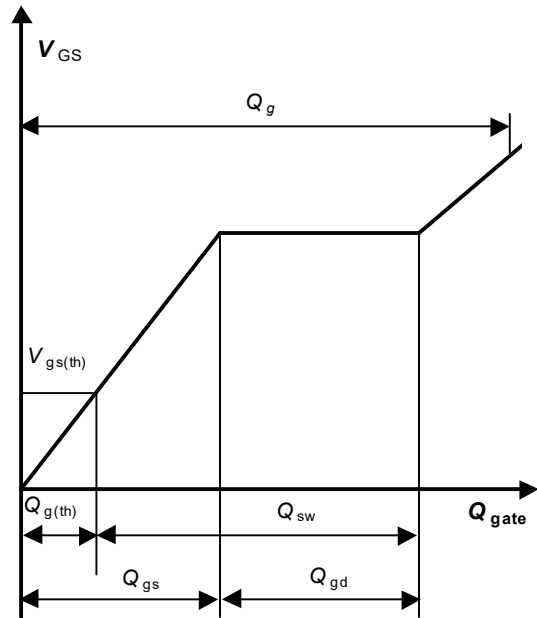
$$E_{AS} = f(T_j)$$

 parameter: I_D

14 Drain-source breakdown voltage

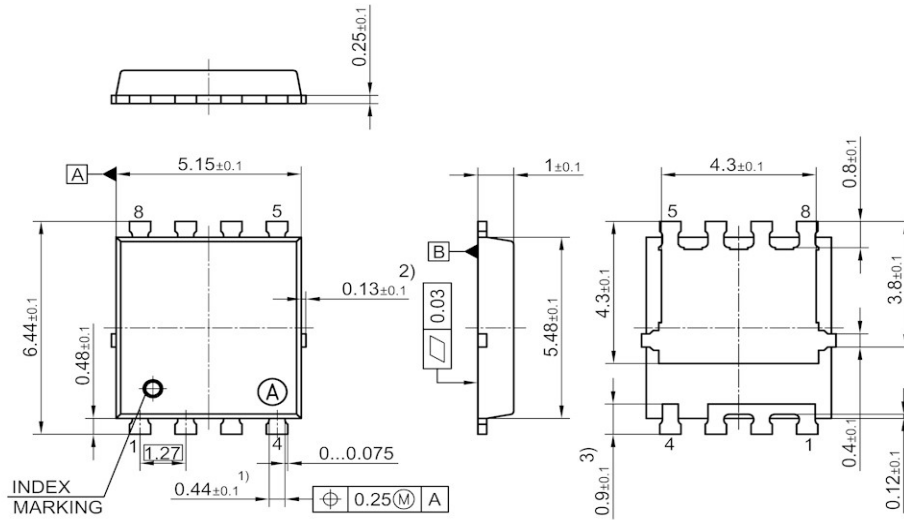
$$V_{BR(DSS)} = f(T_j); I_D = 1 \text{ mA}$$


15 Typ. gate charge

$$V_{GS} = f(Q_{gate}); I_D = 20 \text{ A pulsed}$$

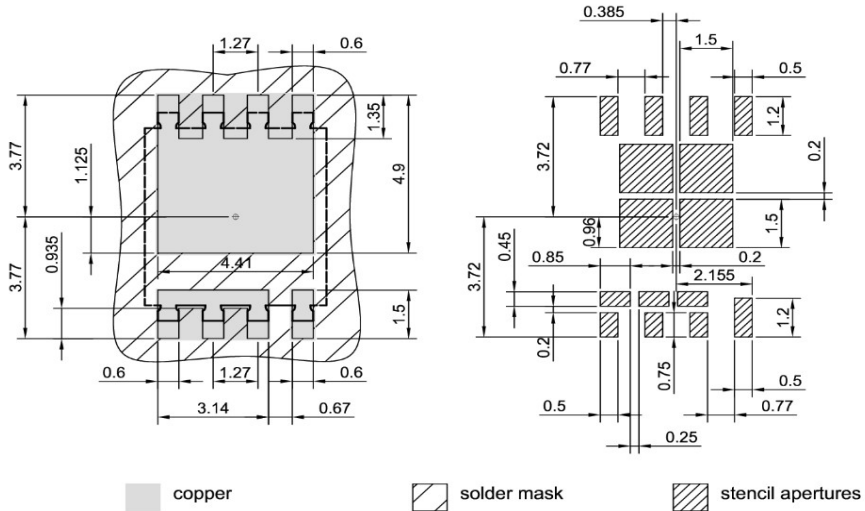
 parameter: V_{DD}

16 Gate charge waveforms


Package Outline



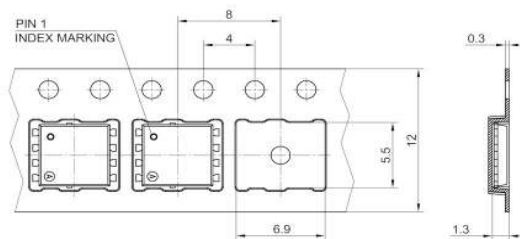
- 1) EXCLUDE MOLD FLASH
 - 2) REMOVAL ON MOLD GATE, INTRUSION 0.1MM AND PROTRUSION 0.1MM
 - 3) LEAD LENGTH UP TO ANTI FLASH LINE
 - 4) ALL METAL SURFACE ARE PLATED, EXCEPT AREA OF CUT
- ALL DIMENSIONS ARE IN UNITS MM
 THE DRAWING IS IN COMPLIANCE WITH ISO 128 & PROJECTION METHOD 1 []

Footprint



All dimensions are in units mm

Packaging



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If they fail, it is reasonable to assume that the health of the user or other persons may be endangered.

Revision History

Version	Date	Changes
Revision 1.0	2021-01-19	Final Data Sheet