Description

The IDT8S89871I is a high speed Differential-to-LVPECL Buffer/Divider. The IDT8S89871I has a selectable ÷2, ÷4, ÷8, ÷16 output dividers. The clock input has internal termination resistors, allowing it to interface with several differential signal types while minimizing the number of required external components.

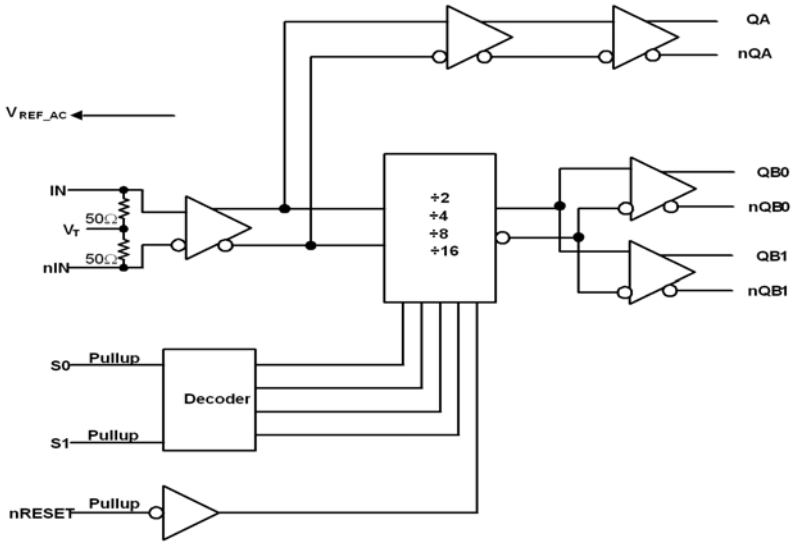
The QA output provides an extra copy of the input frequency, while QB is a divided down output of the input frequency. Both output banks are phase matched and maintain a matched delay independent of the divider setting.

The device is packaged in a small, 3 x 3 mm VFQFN package, making it ideal for use on space-constrained boards.

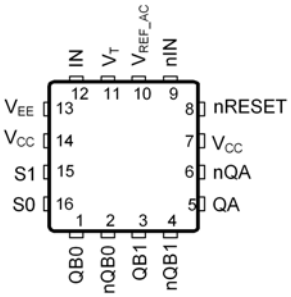
Features

- Three LVPECL output pairs
- Frequency divide select options: ÷2, ÷4, ÷8, ÷16 (Bank B)
- Pass-through output (Bank A)
- IN, nIN input can accept the following differential input levels: LVPECL, LVDS, CML
- Output frequency: 2.5GHz
- Bank skew: 40ps (maximum), Bank B
- Part-to-part skew: 230ps (maximum)
- Additive phase jitter, RMS: 0.15ps (typical)
- Voltage supply range: 2.375V to 3.6V
- -40°C to 85°C ambient operating temperature
- Available in lead-free (RoHS 6) package

Block Diagram



Pin Assignment



IDT8S89871I

16-Lead VFQFN
3mm x 3mm x 0.925mm package body
NL Package
Top View

Table 1. Pin Descriptions

Number	Name	Type		Description
1, 2	QB0, nQB0	Output		Differential output pair. LVPECL interface levels.
3, 4	QB1, nQB1	Output		Differential output pair. LVPECL interface levels.
5, 6	QA, nQA	Output		Differential output pair. LVPECL interface levels.
7, 14	V_{CC}	Power		Power supply pins.
8	nRESET	Input	Pullup	QB [1:0] output reset. Input threshold is $V_{CC}/2$. Includes a 37kΩ pull-up resistor. LVTTL/LVCMOS interface levels. See Table 3.
9	nIN	Input		Inverting differential LVPECL clock input. R_{IN} = 50Ω termination to V_T.
10	V_{REF_AC}	Output		Reference voltage for AC-coupled applications.
11	V_T	Input		Termination input.
12	IN	Input		Non-inverting LVPECL differential clock input. R_{IN} = 50Ω termination to V_T.
13	V_{EE}	Power		Negative supply pin.
15, 16	S1, S0	Input	Pullup	Select pins. LVCMOS/LVTTL interface levels. See Table 3.

NOTE: *Pullup* refers to internal input resistors. See Table 2, *Pin Characteristics,* for typical values.

Table 2. Pin Characteristics

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
R_{PULLUP}	Input Pullup Resistor			37		kΩ

Function Table

Table 3. Control Input and Divider Truth Table

Inputs			Outputs	
nRESET	**S1**	**S0**	**QA Output**	**QB Output**
1 (default)	0	0	Reference Clock	Reference Clock ÷2
1	0	1	Reference Clock	Reference Clock ÷4
1	1	0	Reference Clock	Reference Clock ÷8
1	1 (default)	1 (default)	Reference Clock	Reference Clock ÷16
0	X	X	Reference Clock	Q = LOW, nQ = HIGH; Clock Disabled

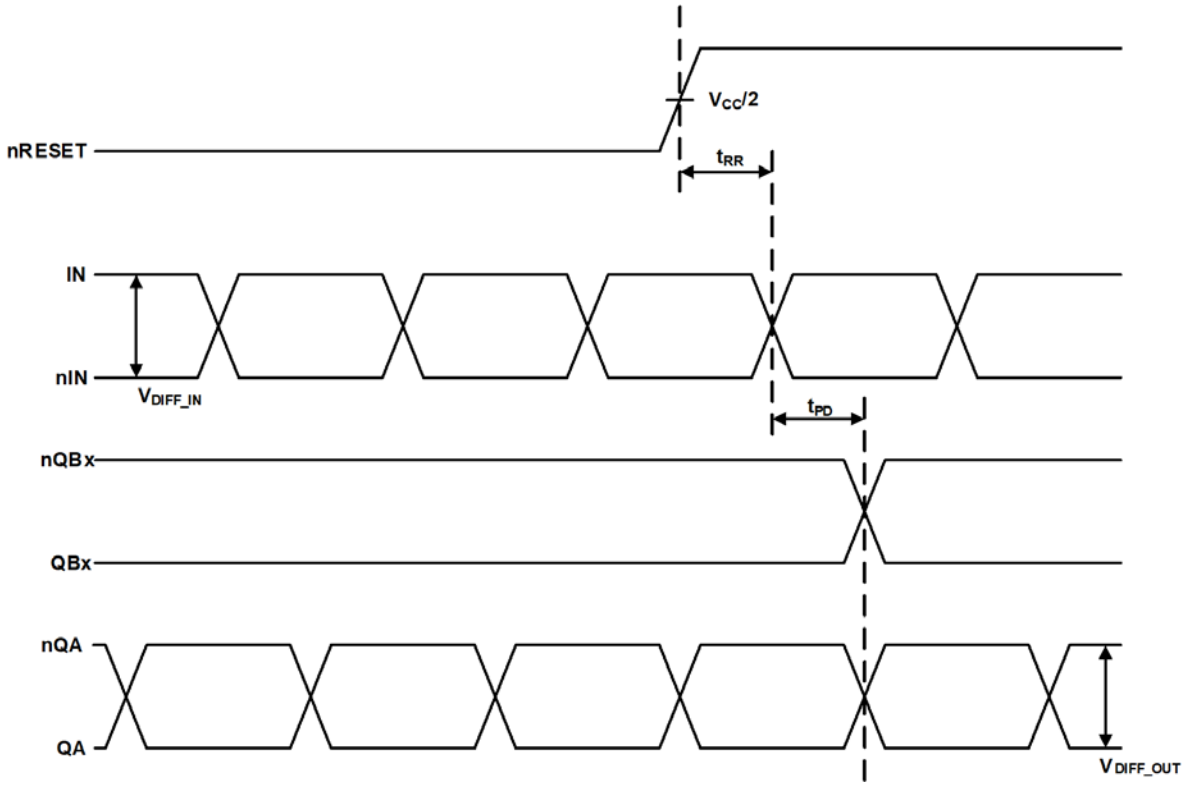


Figure 1. nRESET Timing Diagram

Absolute Maximum Ratings

Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics or AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Item	Rating
Supply Voltage, V_{CC}	4.6V
Inputs, V_I	-0.5V to V_{CC} + 0.5V
Outputs, I_O Continuous Current Surge Current	 50mA 100mA
Input Current, IN, nIN	±50mA
V_T Current, I_{VT}	±100mA
V_{REF_AC} Input Sink/Source, I_{REF_AC}	±2mA
Operating Temperature Range, T_A	-40°C to +85°C
Package Thermal Impedance, θ_{JA}, (Junction-to-Ambient)	74.7°C/W (0 mps)
Storage Temperature, T_{STG}	-65°C to 150°C

DC Electrical Characteristics

Table 4A. Power Supply DC Characteristics, V_{CC} = 3.3V ± 0.3V or 2.5V ± 5%, V_{EE} = 0V, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{CC}	Power Supply Voltage		2.375	3.3	3.6	V
I_{CC}	Power Supply Current	Outputs Unterminated			57	mA

Table 4B. LVCMOS/LVTTL DC Characteristics, V_{CC} = 3.3V ± 0.3V or 2.5V ± 5%, V_{EE} = 0V, T_A = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage			2.2		V_{CC} + 0.3	V
V_{IL}	Input Low Voltage			0		0.8	V
I_{IH}	Input High Current	S[1:0], nRESET	V_{CC} = V_{IN} = 3.6V or 2.625V			10	µA
I_{IL}	Input Low Current	S[1:0], nRESET	V_{CC} = 3.6V or 2.625V, V_{IN} = 0V	-150			µA

Table 4C. Differential DC Characteristics, V_{CC} = 3.3V ± 0.3V or 2.5V ± 5%, V_{EE} = 0V, T_A = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
R_{IN}	Input Resistance	IN, nIN	IN to V_T	40	50	60	Ω
V_{IH}	Input High Voltage	IN, nIN		0.15		V_{CC} + 0.3	V
V_{IL}	Input Low Voltage	IN, nIN		0		V_{IH} – 0.15	V
V_{IN}	Input Voltage Swing; NOTE 1			0.15		V_{CC}	V
V_{DIFF_IN}	Differential Input Voltage Swing			0.3			V
I_{IN}	Input Current; NOTE 2, 3	IN, nIN				45	mA
V_{REF_AC}	Bias Voltage			V_{CC} – 1.46	V_{CC} – 1.38	V_{CC} – 1.31	V

NOTE 1: Refer to Parameter Measurement Information, *Input Voltage Swing* diagram.
NOTE 2: Guaranteed by design.
NOTE 3: Because of the internal termination R_{IN}, the input current I_{IN} will be determined by the voltages applied at IN, nIN and V_T. Observe the voltages applied to those pins so the input current does not exceed the maximum limit.

Table 4D. LVPECL DC Characteristics, V_{CC} = 3.3V ± 0.3V or 2.5V ± 5%, V_{EE} = 0V, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OH}	Output High Voltage; NOTE 1		V_{CC} – 1.175		V_{CC} – 0.82	V
V_{OL}	Output Low Voltage; NOTE 1		V_{CC} – 2.0		V_{CC} – 1.575	V
V_{OUT}	Output Voltage Swing		0.6		1.0	V
V_{DIFF_OUT}	Differential Output Voltage Swing		1.2		2.0	V

NOTE: Input and output parameters vary 1:1 with V_{CC}.
NOTE 1: Outputs terminated with 50Ω to V_{CC} – 2V.

AC Electrical Characteristics

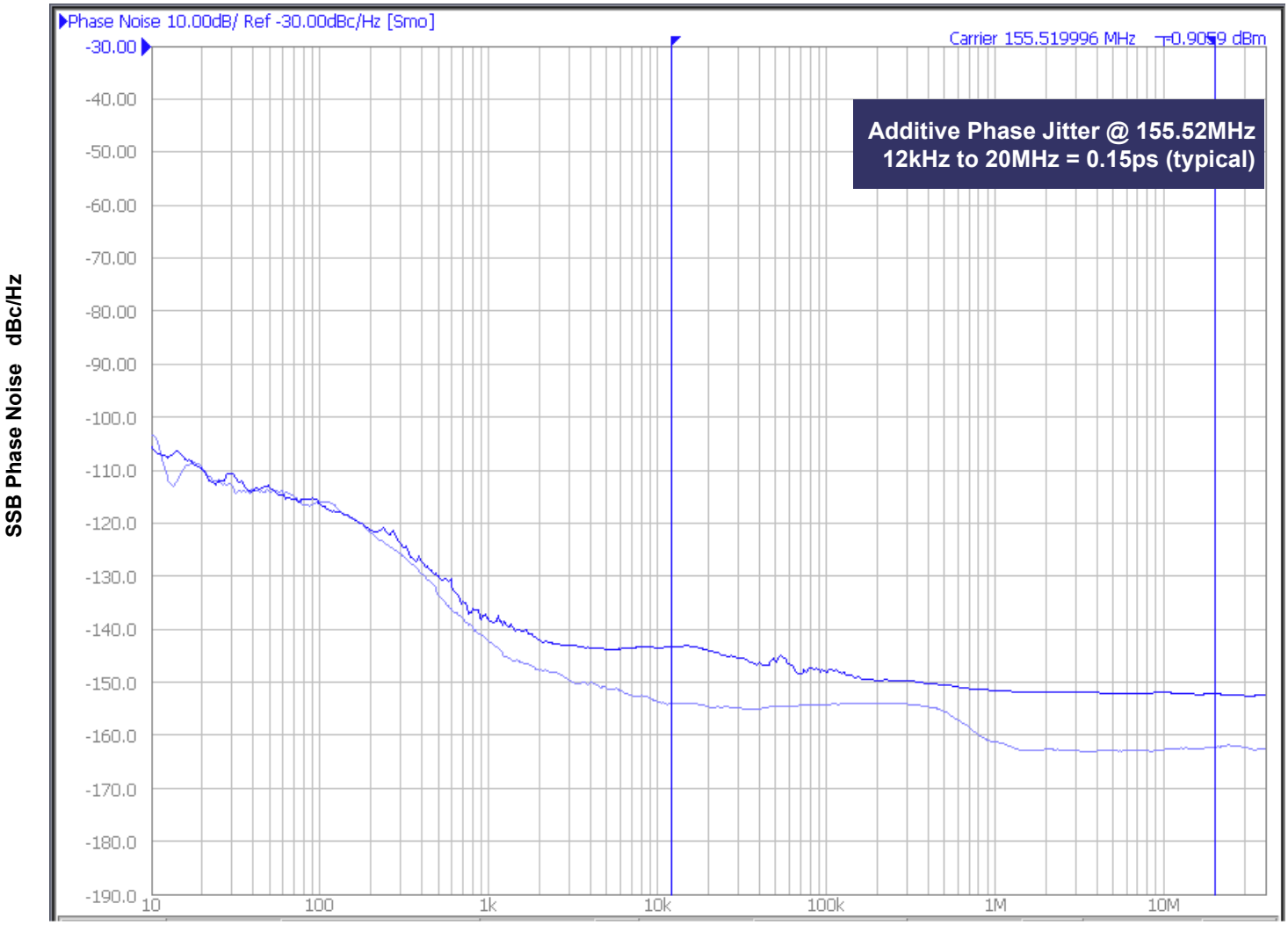
Table 5. AC Characteristics, V_{CC} = 3.3V ± 0.3V or 2.5V ± 5%, V_{EE} = 0V, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency	Output Swing ≥ 450mV			2.5	GHz
f_{IN}	Input Frequency	÷2, ÷4, ÷8			3.2	GHz
		÷1, ÷16			2.5	GHz
t_{PD}	Propagation Delay; (Differential); NOTE 1	Input Swing: <400mV	520	665	805	ps
		Input Swing: ≥ 400mV	510	650	790	ps
*t*sk(o)	Output Skew; NOTE 2, 5			15	55	ps
*t*sk(b)	Bank Skew; NOTE 3, 5	Bank B		13	40	ps
*t*sk(pp)	Part-to-Part Skew; NOTE 4, 5				230	ps
*t*jit	Buffer Additive Jitter; RMS; refer to Additive Phase Jitter Section;	Bank A. 155.52MHz, Integration Range: 12kHz - 20MHz		0.15	0.18	ps
t_{RR}	Reset Recovery Time		600			ps
t_R / t_F	Output Rise/Fall Time	20% to 80%	40		250	ps

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
NOTE: All parameters characterized at ≤ 2.5GHz, 800mV input signal, unless otherwise noted.
NOTE 1: Measured from the differential input crossing point to the differential output crossing point.
NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at the output differential cross points.
NOTE 3: Defined as skew within a bank of outputs at the same supply voltage and with equal load conditions.
NOTE 4: Defined as skew between outputs on different devices operating at the same supply voltage, same temperature, same frequency and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at the differential cross points.
NOTE 5: This parameter is defined in accordance with JEDEC Standard 65.

Additive Phase Jitter

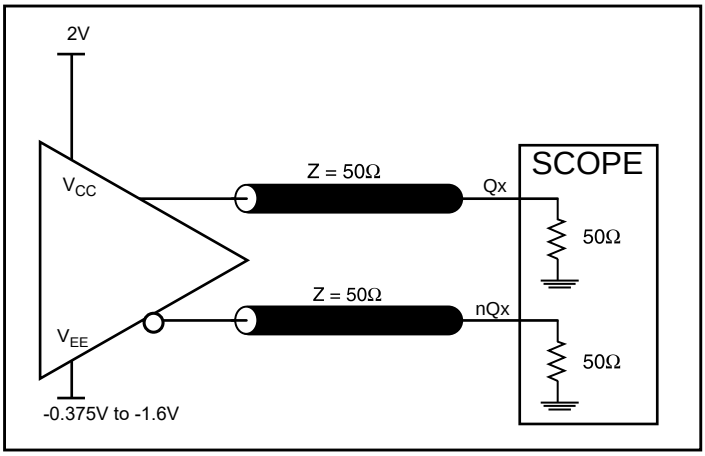
The spectral purity in a band at a specific offset from the fundamental compared to the power of the fundamental is called the ***dBc Phase Noise.*** This value is normally expressed using a Phase Noise plot and is most often the specified plot in many applications. Phase noise is defined as the ratio of the noise power present in a 1Hz band at a specified offset from the fundamental frequency to the power value of the fundamental. This ratio is expressed in decibels (dBm) or a ratio of the power in the 1Hz band to the power in the fundamental. When the required offset is specified, the phase noise is called a ***dBc*** value, which simply means dBm at a specified offset from the fundamental. By investigating jitter in the frequency domain, we get a better understanding of its effects on the desired application over the entire time record of the signal. It is mathematically possible to calculate an expected bit error rate given a phase noise plot.



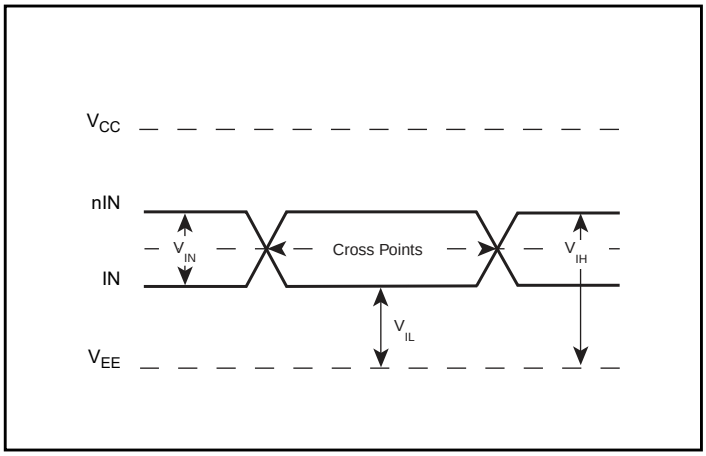
As with most timing specifications, phase noise measurements has issues relating to the limitations of the equipment. Often the noise floor of the equipment is higher than the noise floor of the device. This is illustrated above. The device meets the noise floor of what is shown, but can actually be lower. The phase noise is dependent on the input source and measurement equipment.

Measured using a Rohde & Schwarz SMA100A as the input source.

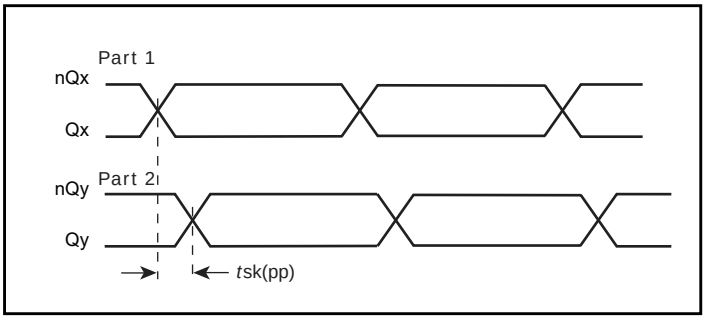
Parameter Measurement Information



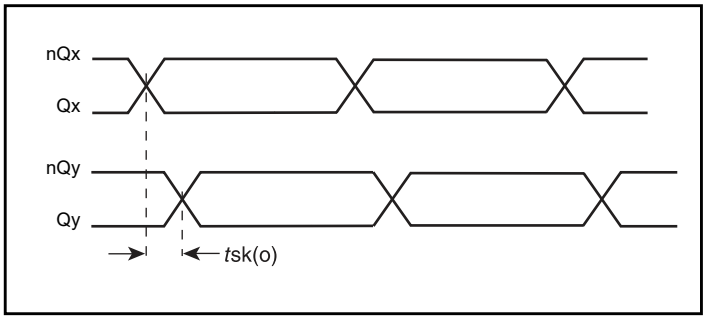
Output Load AC Test Circuit



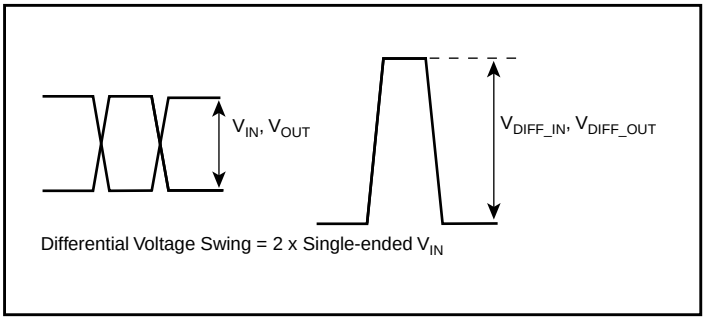
Differential Input Level



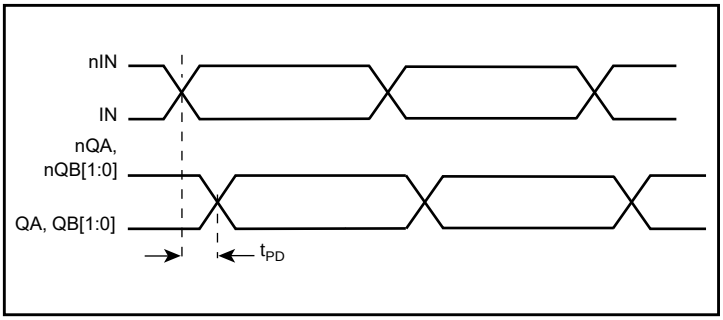
Part-to-Part Skew



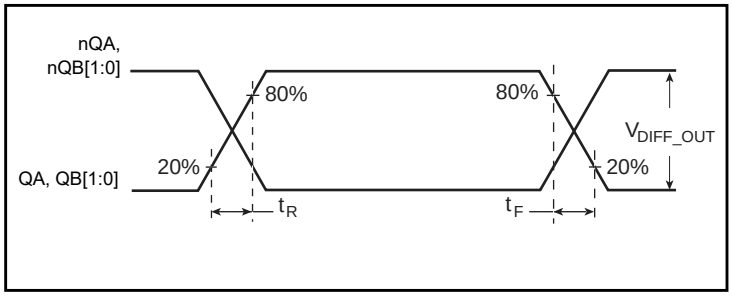
Output Skew



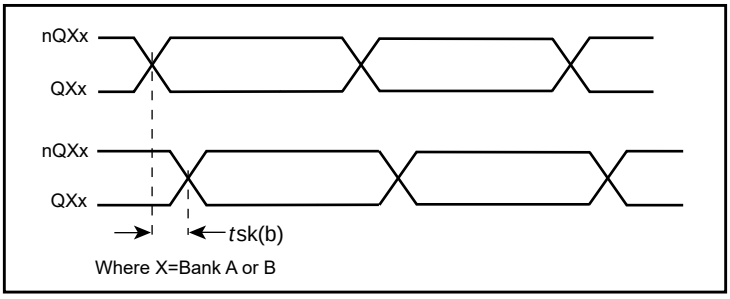
Single-ended & Differential Input Voltage Swing



Propagation Delay



Output Rise/Fall Time



Bank Skew

Applications Information

3.3V Differential Input with Built-In 50Ω Termination Interface

The IN /nIN with built-in 50Ω terminations accept LVDS, LVPECL, CML and other differential signals. Both signals must meet the V_{IN} and V_{IH} input requirements. *Figures 2A to 2D* show interface examples for the IN/nIN input with built-in 50Ω terminations driven by the most common driver types. The input interfaces suggested here are examples only. If the driver is from another vendor, use their termination recommendation. Please consult with the vendor of the driver component to confirm the driver termination requirements.

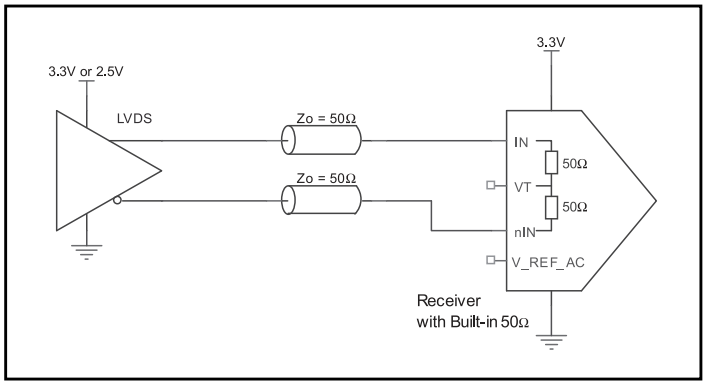


Figure 2A. N/nIN Input with Built-In 50Ω Driven by an LVDS Driver

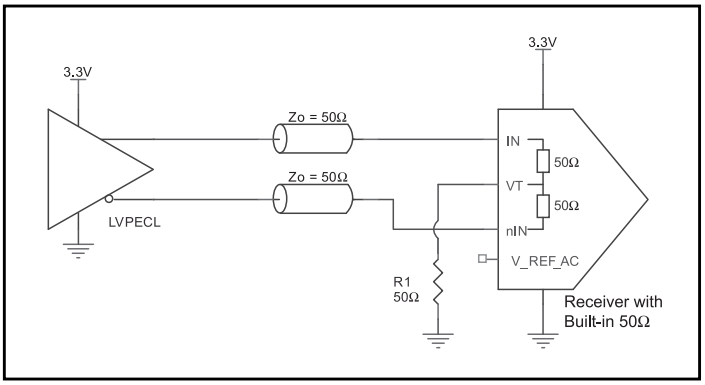


Figure 2B. IN/nIN Input with Built-In 50Ω Driven by an LVPECL Driver

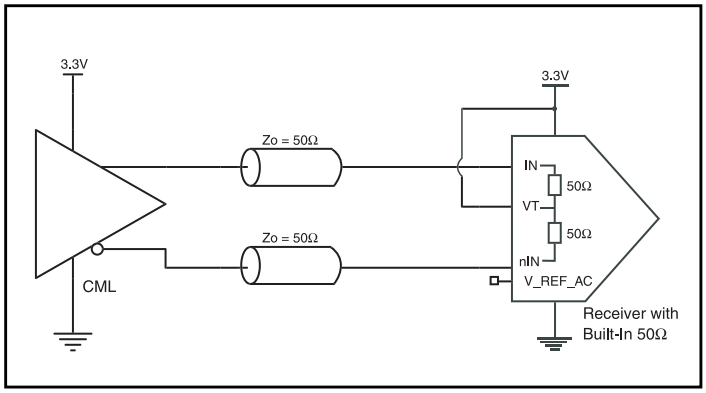


Figure 2C. IN/nIN Input with Built-In 50Ω Driven by a CML Driver

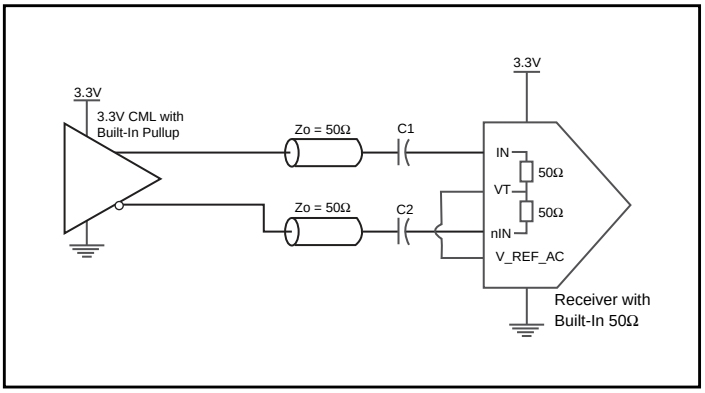


Figure 2D. IN/nIN Input with Built-In 50Ω Driven by a CML Driver with Built-In 50Ω Pullup

2.5V LVPECL Input with Built-In 50Ω Termination Interface

The IN /nIN with built-in 50Ω terminations accept LVDS, LVPECL, CML and other differential signals. Both signals must meet the V_{IN} and V_{IH} input requirements. *Figures 3A to 3D* show interface examples for the IN/nIN with built-in 50Ω termination input driven by the most common driver types. The input interfaces suggested here are examples only. If the driver is from another vendor, use their termination recommendation. Please consult with the vendor of the driver component to confirm the driver termination requirements.

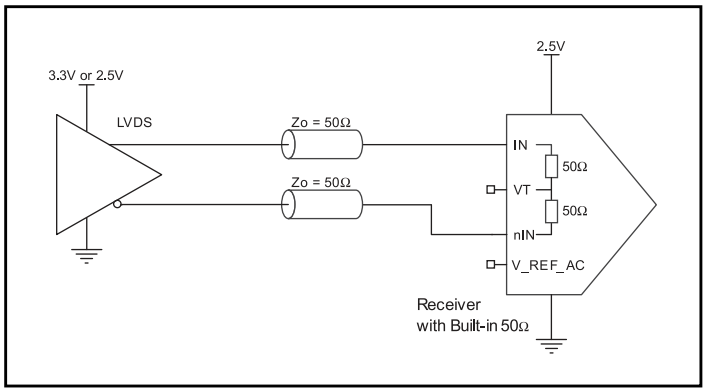


Figure 3A. IN/nIN Input with Built-In 50Ω Driven by an LVDS Driver

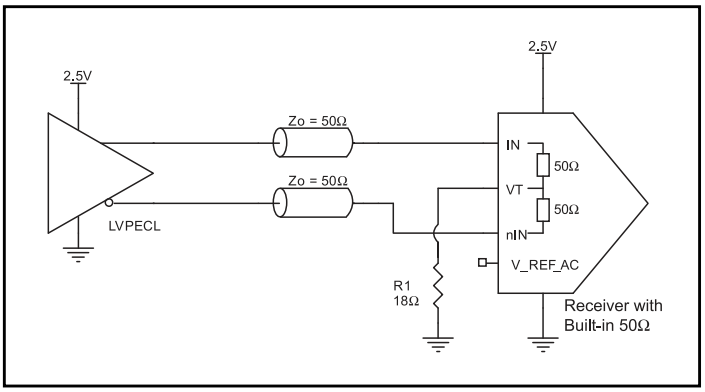


Figure 3B. IN/nIN Input with Built-In 50Ω Driven by an LVPECL Driver

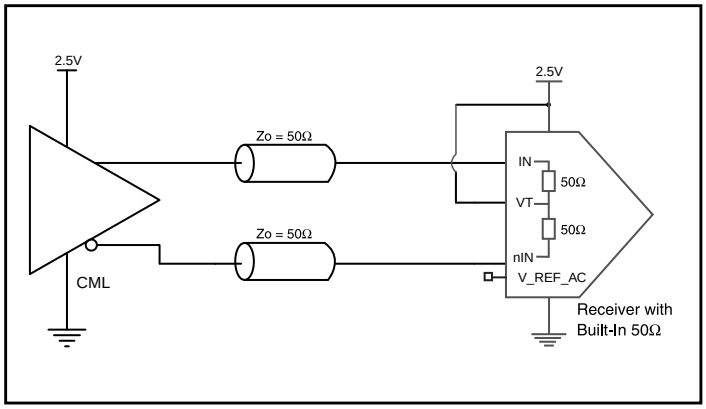


Figure 3C. IN/nIN Input with Built-In 50Ω Driven by a CML Driver

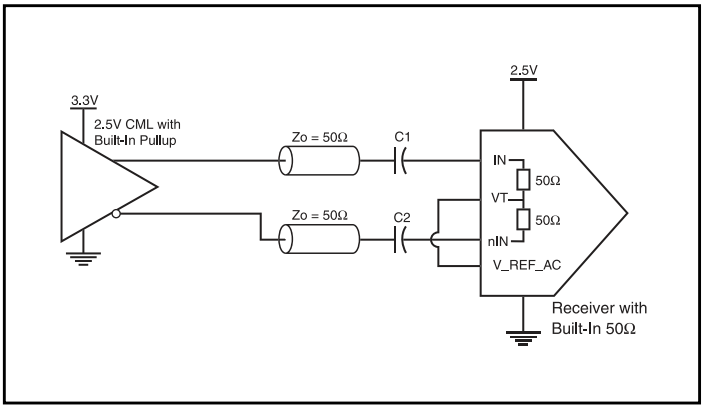


Figure 3D. IN/nIN Input with Built-In 50Ω Driven by a CML Driver with Built-In 50Ω Pullup

Recommendations for Unused Input and Output Pins

Inputs:

LVCMOS Control Pins

All control pins have internal pullups; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

Outputs:

LVPECL Outputs

All unused LVPECL outputs can be left floating. We recommend that there is no trace attached. Both sides of the differential output pair should either be left floating or terminated.

Termination for 3.3V LVPECL Outputs

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines.

The differential outputs are low impedance follower outputs that generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive 50Ω transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion. *Figures 4A and 4B* show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.

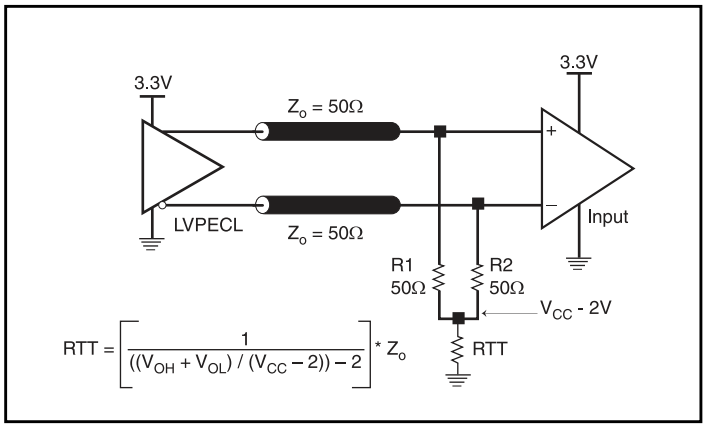


Figure 4A. 3.3V LVPECL Output Termination

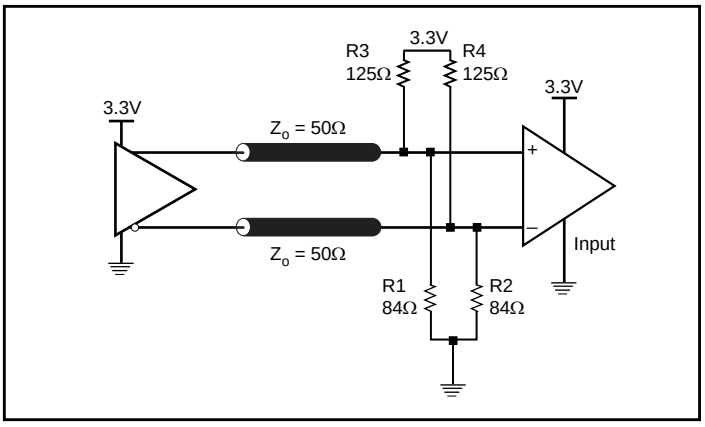


Figure 4B. 3.3V LVPECL Output Termination

Termination for 2.5V LVPECL Outputs

Figure 5A and *Figure 5B* show examples of termination for 2.5V LVPECL driver. These terminations are equivalent to terminating 50Ω to V_{CC} – 2V. For V_{CC} = 2.5V, the V_{CC} – 2V is very close to ground level. The R3 in Figure 5B can be eliminated and the termination is shown in *Figure 5C.*

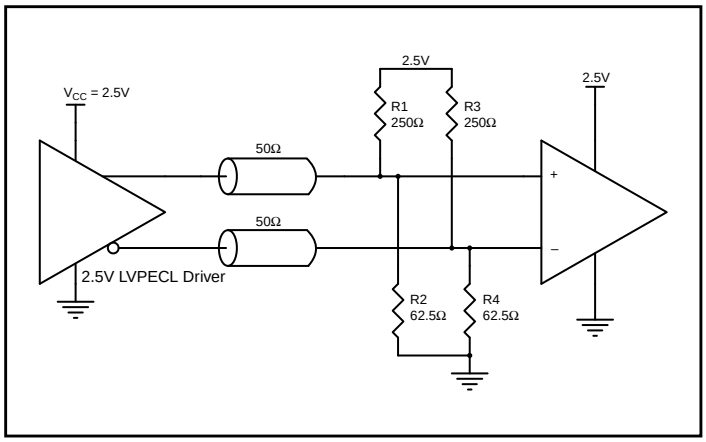


Figure 5A. 2.5V LVPECL Driver Termination Example

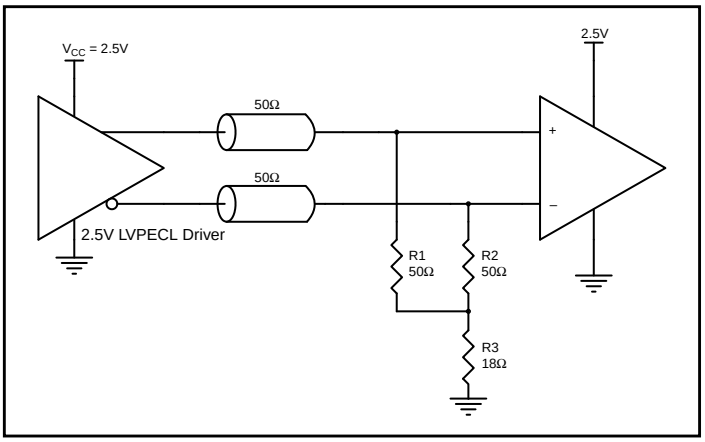


Figure 5B. 2.5V LVPECL Driver Termination Example

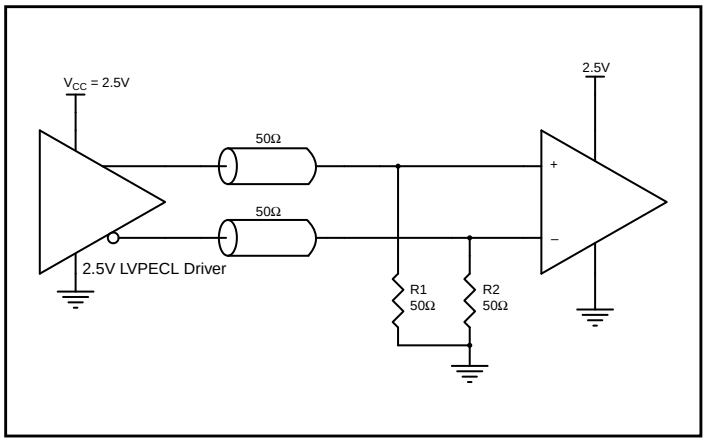


Figure 5C. 2.5V LVPECL Driver Termination Example

VFQFN EPAD Thermal Release Path

In order to maximize both the removal of heat from the package and the electrical performance, a land pattern must be incorporated on the Printed Circuit Board (PCB) within the footprint of the package corresponding to the exposed metal pad or exposed heat slug on the package, as shown in *Figure 6.* The solderable area on the PCB, as defined by the solder mask, should be at least the same size/shape as the exposed pad/slug area on the package to maximize the thermal/electrical performance. Sufficient clearance should be designed on the PCB between the outer edges of the land pattern and the inner edges of pad pattern for the leads to avoid any shorts.

While the land pattern on the PCB provides a means of heat transfer and electrical grounding from the package to the board through a solder joint, thermal vias are necessary to effectively conduct from the surface of the PCB to the ground plane(s). The land pattern must be connected to ground through these vias. The vias act as “heat pipes”. The number of vias (i.e. “heat pipes”) are application specific and dependent upon the package power dissipation as well as electrical conductivity requirements. Thus, thermal and electrical analysis and/or testing are recommended to determine the minimum number needed. Maximum thermal and electrical performance is achieved when an array of vias is incorporated in the land pattern. It is recommended to use as many vias connected to ground as possible. It is also recommended that the via diameter should be 12 to 13mils (0.30 to 0.33mm) with 1oz copper via barrel plating. This is desirable to avoid any solder wicking inside the via during the soldering process which may result in voids in solder between the exposed pad/slug and the thermal land. Precautions should be taken to eliminate any solder voids between the exposed heat slug and the land pattern. Note: These recommendations are to be used as a guideline only. For further information, please refer to the Application Note on the Surface Mount Assembly of Amkor’s Thermally/ Electrically Enhance Leadframe Base Package, Amkor Technology.

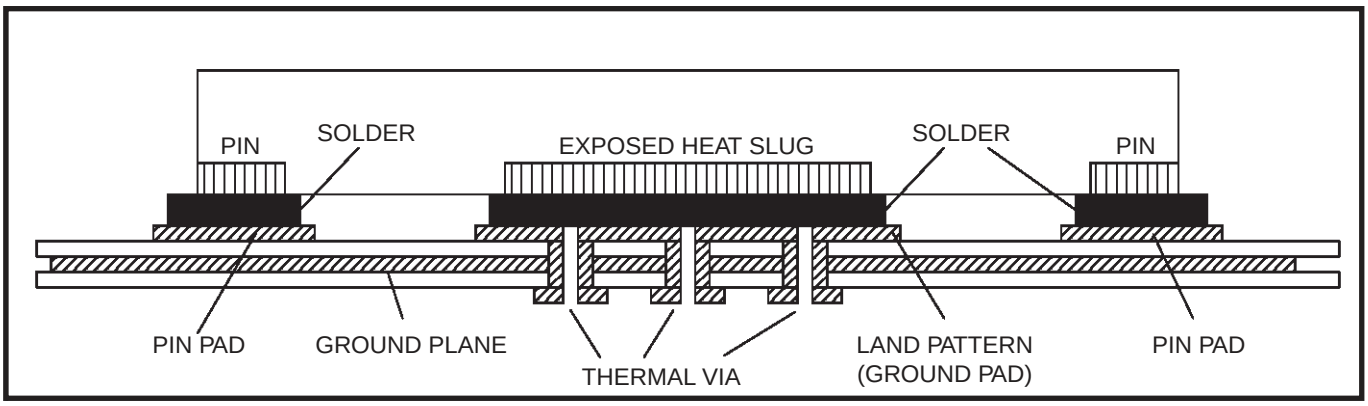


Figure 6. P.C. Assembly for Exposed Pad Thermal Release Path – Side View (drawing not to scale)

Power Considerations

This section provides information on power dissipation and junction temperature for the IDT8S89871I.
Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the IDT8S89871I is the sum of the core power plus the power dissipated at the ouput(s).
The following is the power dissipation for V_{CC} = 3.6V, which gives worst case results.

NOTE: Please refer to Section 3 for details on calculating power dissipated at the output(s).

- Power $(core)_{MAX}$ = V_{CC_MAX} * I_{EE_MAX} = 3.6V * 57mA = **205.2mW**
- Power $(outputs)_{MAX}$ = **32.62mW/Loaded Output pair**
  If all outputs are loaded, the total power is 3 * 32.62mW = **97.86mW**
- Power Dissipation for internal termination R_{IN}
  Power $(R_T)_{MAX}$ = $(V_{IN\_MAX})^2$ / R_{T_MIN}* 2) = $(3.6V)^2$ / 80Ω = **162mW**

Total Power$_{MAX}$ = (3.6V, with all outputs switching) = 205.2mW + 97.86mW + 162mW = **465.06mW**

2. Junction Temperature.

Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad, and directly affects the reliability of the device. The maximum recommended junction temperature is 125°C. Limiting the internal transistor junction temperature, Tj, to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

The equation for Tj is as follows: Tj = θ_{JA} * Pd_total + T_A

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming no air flow and a multi-layer board, the appropriate value is 74.7°C/W per Table 6 below.

Therefore, Tj for an ambient temperature of 85°C with all outputs switching is:

85°C + 0.465W * 74.7°C/W = 119.7°C. This is below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

Table 6. Thermal Resistance θ_{JA} for 16 Lead VFQFN, Forced Convection

θ_{JA} vs. Air Flow			
Meters per Second	**0**	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	74.7°C/W	65.3°C/W	58.5°C/W

3. Calculations and Equations.

The purpose of this section is to calculate the power dissipation for the LVPECL output pairs.

LVPECL output driver circuit and termination are shown in *Figure 7.*

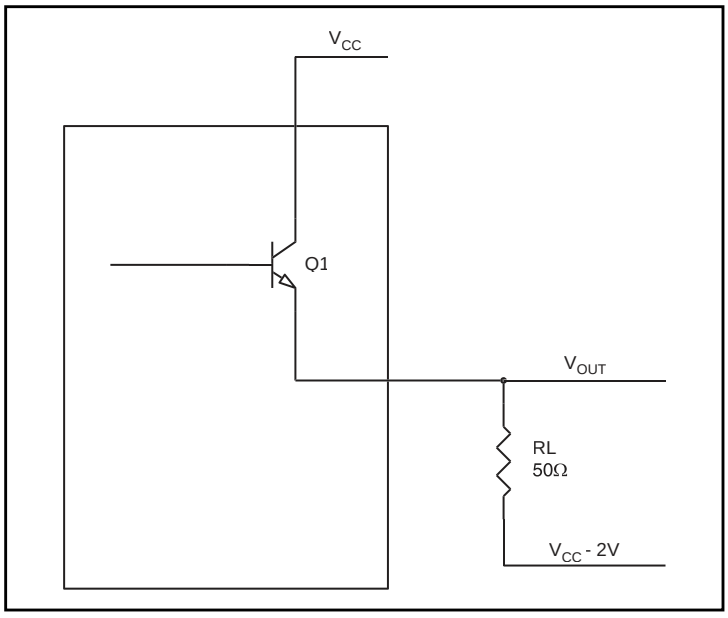


Figure 7. LVPECL Driver Circuit and Termination

To calculate worst case power dissipation at the output(s), use the following equations which assume a 50Ω load, and a termination voltage of V_{CC} – 2V.

- For logic high, $V_{OUT} = V_{OH\_MAX} = \mathbf{V_{CC\_MAX} - 0.82V}$
  $(V_{CC\_MAX} - V_{OH\_MAX}) = \mathbf{0.82V}$
- For logic low, $V_{OUT} = V_{OL\_MAX} = \mathbf{V_{CC\_MAX} - 1.58V}$
  $(V_{CC\_MAX} - V_{OL\_MAX}) = \mathbf{1.58V}$

Pd_H is the power dissipation when the output drives high.

Pd_L is the power dissipation when the output drives low.

$Pd\_H = [(V_{OH\_MAX} – (V_{CC\_MAX} – 2V))/R_L] * (V_{CC\_MAX} – V_{OH\_MAX}) = [(2V – (V_{CC\_MAX} – V_{OH\_MAX}))/R_L] * (V_{CC\_MAX} – V_{OH\_MAX}) =$
$[(2V – 0.82V)/50Ω] * 0.82V =$ **19.35mW**

$Pd\_L = [(V_{OL\_MAX} – (V_{CC\_MAX} – 2V))/R_L] * (V_{CC\_MAX} – V_{OL\_MAX}) = [(2V – (V_{CC\_MAX} – V_{OL\_MAX}))/R_L] * (V_{CO\_MAX} – V_{OL\_MAX}) =$
$[(2V – 1.58V)/50Ω] * 1.58V =$ **13.27mW**

Total Power Dissipation per output pair = Pd_H + Pd_L = **32.62mW**

Reliability Information

Table 7. θ_{JA} vs. Air Flow Table for a 16 Lead VFQFN

θ_{JA} by Velocity			
Meters per Second	**0**	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	74.7°C/W	65.3°C/W	58.5°C/W

Transistor Count

The transistor count for IDT8S89871I is: 239
Pin compatible with ICS889871

Package Outline Drawings

The package outline drawings are located at the end of this document. The package information is the most current data available and is subject to change without notice or revision of this document.

Ordering Information

Table 8. Ordering Information

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
8S89871ANLGI	871AI	“Lead-Free” 16 Lead VFQFN	Tube	-40°C to 85°C
8S89871ANLGI8	871AI	“Lead-Free” 16 Lead VFQFN	2500 Tape & Reel	-40°C to 85°C

NOTE: Parts that are ordered with an “G” suffix to the part number are the Pb-Free configuration and are RoHS compliant.

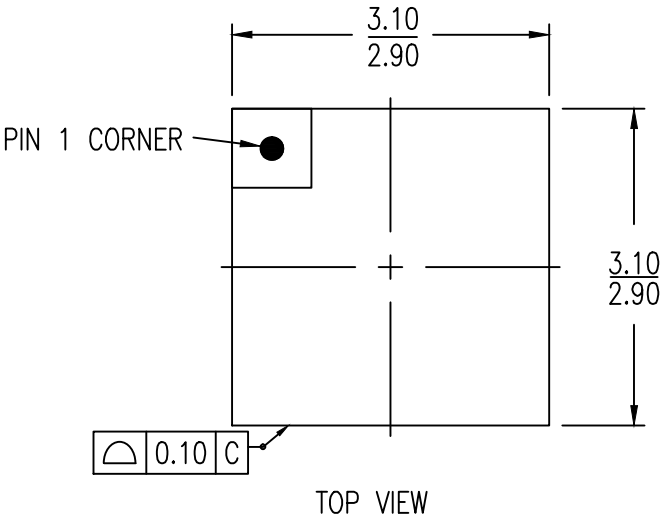
Revision History

Revision Date	Description of Change
November 28, 2017	Updated the package outline drawings; however, no technical changes Completed other minor changes
April 20, 2012	Initial release.

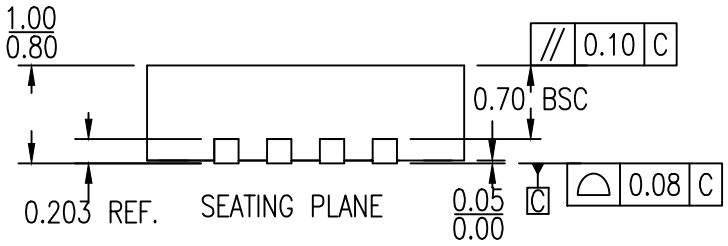
Corporate Headquarters
6024 Silver Creek Valley Road
San Jose, CA 95138 USA
www.IDT.com

Sales
1-800-345-7015 or 408-284-8200
Fax: 408-284-2775
www.IDT.com/go/sales

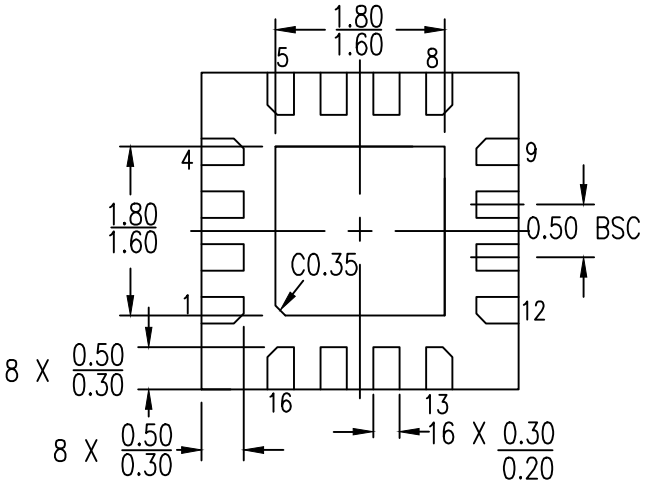
Tech Support
www.idt.com/go/support



TOP VIEW

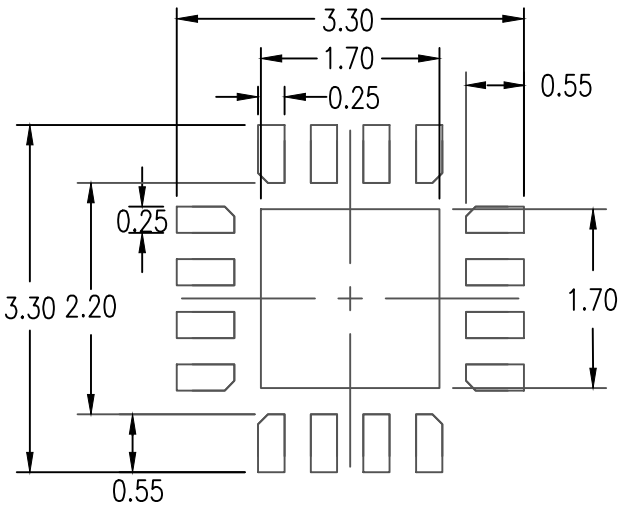


SIDE VIEW



BOTTOM VIEW

NOTES:
1. ALL DIMENSIONS ARE IN mm. ANGLES IN DEGREES



RECOMMENDED LAND PATTERN DIMENSION

NOTES:
1. ALL DIMENSIONS ARE IN mm. ANGLES IN DEGREES
2. TOP DOWN VIEW–AS VIEWED ON PCB
3. LAND PATTERN RECOMMENDATION IS PER IPC–7351B GENERIC REQUIREMENT FOR SURFACE MOUNT DESIGN AND LAND PATTERN

Package Revision History		
Date Created	Rev No.	Description
Oct 25, 2017	Rev 04	Remove Bookmak at Pdf Format & Update Thickness Tolerance
Aug 15, 2017	Rev 03	Update Epad Range